Futaba®

REV.–

VACUUM FLUORESCENT DISPLAY MODULE

ENGINEERING PROPOSAL

M162SD13AA

EVALUATION
☐ ACCEPTED WITHOUT ANY CHANGE
☐ THE FOLLOWING CHANGE IS REQUIRED

2 February 2006

VFD MODULE GROUP

Futaba Corporation

ISSUED BY	Syoichi Nakashima
CHECKED BY	Koji Tajima
CHECKED BY	Katsunori Kase
APPROVED BY	Toshihiro Yamaguchi

⚠ Important Safety Notice

Please read this note carefully before using the product.

Warning

- The module should be disconnected from the power supply before handling.
- The power supply should be switched off before connecting or disconnecting the power or interface cables.
- The module contains electronic components that generate high voltages which may cause an electrical shock when touched.
- Do not touch the electronic components of the module with any metal objects.
- The VFD used on the module is made of glass and should be handled with care. When handling the VFD, it is recommended that cotton gloves be used.
- The module is equipped with a circuit protection.
- Under no circumstances should the module be modified or repaired.
  Any unauthorized modifications or repairs will invalidate the product warranty.
- The module should be abolished as the factory waste.

1. FEATURES

This vacuum fluorescent display (VFD) module consists of a 16 character by 2 line 5×7 dot matrix display, DC-DC/AC converter, and controller/driver circuitry.
The luminance level of the VFD can be varied by setting eight bits in the function set instruction.
Two hundred and forty eight character fonts consisting of a alphabets, European font, numerals and other symbols can be displayed.

2. SPECIFICATIONS

2-1. GENERAL SPECIFICATIONS

Table-1

Item	Value	
Number of characters	16 characters × 2 lines	
Character configuration	5×7 dot matrix	
Display Area	86.7 × 12.0 mm	
Character Size	3.45 × 5.45 mm	
Character Pitch	5.55 × 6.55 mm	
Dot Size	0.57 × 0.65 mm	
Dot Pitch	0.72 × 0.80 mm	
Peak Wavelength of Illumination	Green (λp=505nm)	
Luminance	Minimum 350 cd/m^2	Typical 700 cd/m^2

2-2. ENVIRONMENTAL SPECIFICATIONS

Table-2

Item	Symbol	Min.	Max.	Unit	Comment
Operating Temperature	*T*opr	-40	+85	°C	
Storage Temperature	*T*stg	-40	+85	°C	
Operating Humidity	*H*opr	20	85	%RH	Without condensation
Storage Humidity	*H*stg	20	90	%RH	Without condensation
Vibration	–	–	4	G	Total amplitude: 1.5mm Freq: 10-55 Hz sine wave Sweep time: 1 min./cycle Duration: 2hrs./axis (X,Y,Z)
Shock	–	–	40	G	Duration: 11ms Wave form: half sine wave 3 times/axis (X,Y,Z,-X,-Y,-Z)

2-3. ABSOLUTE MAXIMUM SPECIFICATIONS

Table-3

Item	Symbol	Min.	Max.	Unit
Supply Voltage	*V*cc	-0.3	6.5	V
Input signal Voltage	V_{IN}	-0.3	*V*cc+0.3	V

2-4. DC ELECTRICAL SPECIFICATIONS

Table-4

Item	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	*V*cc	4.5	5.0	5.5	V
Supply Current	*I*cc	–	200	300	mA
Power Consumption	–	–	1.0	1.5	W
High - Level Input Voltage	V_{IH}	0.8*V*cc	–	–	V
Low - Level Input Voltage	V_{IL}	–	–	0.2*V*cc	V
High - Level Input Current	I_{IH}	–	–	5.0	μA
Low - Level Input Current	I_{IL}	–	–	-5.0	μA

3. FUNCTIONAL DESCRIPTION

The following are the list of commands.

Teble-5 INSTRUCTIONS TABLE

INSTRUCTION	MSB 1st Byte							LSB	MSB 2nd Byte							LSB	
	B7	B6	B5	B4	B3	B2	B1	B0	B7	B6	B5	B4	B3	B2	B1	B0	
DCRAM_A DATA WRITE	0	0	0	X4	X3	X2	X1	X0	C7	C6	C5	C4	C3	C2	C1	C0	
DCRAM_B DATA WRITE	0	0	1	X4	X3	X2	X1	X0	C7	C6	C5	C4	C3	C2	C1	C0	
CGRAM DATA WRITE	0	1	0	*	*	Y2	Y1	Y0	*	D30	D25	D20	D15	D10	D5	D0	2nd Byte
									*	D31	D26	D21	D16	D11	D6	D1	3rd Byte
									*	D32	D27	D22	D17	D12	D7	D2	4th Byte
									*	D33	D28	D23	D18	D13	D8	D3	5th Byte
									*	D34	D29	D24	D19	D14	D9	D4	6th Byte
NUMBER OF DIGIT SET	1	1	1	0	0	0	*	*	0	*	*	*	F3	F2	F1	F0	
DIMMING SET	1	1	1	0	0	1	*	*	H7	H6	H5	H4	H3	H2	H1	H0	
GRAY-LEVEL SET	1	0	1	*	*	J2	J1	J0	I7	I6	I5	I4	I3	I2	I1	I0	
GRAY-LEVEL ON/OFF SET	1	1	0	X4	X3	X2	X1	X0	*	*	0	0	0	0	K1	K0	
DISPLAY LIGHT SET	1	1	1	0	1	0	LS	HS	*	*	*	*	*	*	*	*	

*: Not Relevant
Xn: Duty Timing (Digit) Address Set, n = 0 to 4
Cn: CGRAM/CGROM Character Code Bit, n = 0 to 7
Yn: CGRAM Address Bit, n = 0 to 2
Dn: CGRAM Character Code Setting, n = 0 to 34
Fn: Number of Digits Set, n = 0 to 3
Hn: Dimming Quantity Setting, n = 0 to 7
Jn: Gray-Level Register Setting, n = 0 to 2
In: Gray-Level Quantity Setting, n = 0 to 7
Kn: Each Gray-Level Enable/Disable Setting, n = 0 to 1
HS: "1": All Output (Anode, Segment) Data = "H" "0": Normal Mode
LS: "1": All Output (Anode, Segment) Data = "L" "0": Normal Mode

When data is written into the RAM (DCRAM,CGRAM or ADRAM) in a continuous manner, the addresses are automatically incremented internally.
It is therefore not necessary to specify the first byte.

3-1. RESET FUNCTION

When initialized, the internal status after power supply has been reset as follows.

Teble- 6 RESET FUNCTION

Instruction	At Reset Condition
DCRAM_A	DCRAM_A Address=00H ALL DCRAM_A Data=20H
DCRAM_B	DCRAM_B Address=00H ALL DCRAM_B Data=20H
CGRAM	CGRAM Address=00H ALL CGRAM Data=00H
Number of Digit Set	F3 ~ F0="1111"F6 ~ F4="000"
Dimming Set	0/255
Gray Level Set	J2 ~ J0="000" 0/255
Gray Level On / Off Set	GLRAM Address=00H K5 ~ K0="000000"(Gray Level Disable)
Display Light Set	LS="1" HS="0" (Display all off)

3-2. COMMAND FUNCTION

3-2-1. DATA CONTROL RAM (DCRAM) DATA WRITE COMMAND

The DCRAM (Include: DCRAM_A and DCRAM_B) Data Write Command is used to specify the address
of the DCRAM and writes the character code of the CGROM and CGRAM (C0 to C7 bits). The DCRAM consists of 5 address bits which are used to store the CGRAM & CGROM character codes. The character codes specified by the DCRAM are converted to a 5 x 7 dot matrix character pattern via the CGROM and CGRAM. The DCRAM (Include: DCRAM_A, DCRAM_B) can each store up to 24 characters (DCRAM_A = 24 characters, DCRAM_B = 24 characters). The DCRAM Data Write Command Format is shown below.

	MSB							LSB	
1st Byte (1st)	B7	B6	B5	B4	B3	B2	B1	B0	DCRAM_A Data Write Mode is selected and the DCRAM_A Address is specified. (i.e. DCRAM_A Address = 0H)
	0	0	0	X4	X3	X2	X1	X0	

or

	MSB							LSB	
1st Byte (1st)	B7	B6	B5	B4	B3	B2	B1	B0	DCRAM_B Data Write Mode is selected and the DCRAM_B Address is specified. (i.e. DCRAM_B Address = 0H)
	0	0	1	X4	X3	X2	X1	X0	

	MSB							LSB	
2nd Byte (2nd)	B7	B6	B5	B4	B3	B2	B1	B0	CGROM & CGRAM Character Codes are specified. (They are written into the DCRAM Address 0H) Please refer to Table-20
	C7	C6	C5	C4	C3	C2	C1	C0	

3-2-2. CGRAM DATA WRITE COMMAND

The Character Generator RAM (CGRAM) Data Write Command is used to specify the CGRAM address (00H to 07H) and write the character pattern data. It consists of 3 address bits which is used to store the 5 x 7 dot matrix character patterns. The CGRAM can store up to 8 types of character patterns which may be displayed by specifying the Character Code (DCRAM Address). The CGRAM Data Write Command Format is given below.

	MSB							LSB	
1st Byte (1st)	B7	B6	B5	B4	B3	B2	B1	B0	CGRAM Data Write Mode is selected and the CGRAM Address is specified (i.e. CGRAM Address = 00H).
	0	1	0	*	*	Y2	Y1	Y0	

	MSB							LSB	
2nd Byte (2nd)	B7	B6	B5	B4	B3	B2	B1	B0	1st Column Data is specified and rewritten into the CGRAM Address 00H.
	*	D30	D25	D20	D15	D10	D5	D0	

	MSB							LSB	
3rd Byte (3rd)	B7	B6	B5	B4	B3	B2	B1	B0	2nd Column Data is specified and rewritten into the CGRAM Address 00H.
	*	D31	D26	D21	D16	D11	D6	D1	

	MSB							LSB	
4th Byte (4th)	B7	B6	B5	B4	B3	B2	B1	B0	3rd Column Data is specified and rewritten into the CGRAM Address 00H.
	*	D32	D27	D22	D17	D12	D7	D2	

	MSB							LSB	
5th Byte (5th)	B7	B6	B5	B4	B3	B2	B1	B0	4th Column Data is specified and rewritten into the CGRAM Address 00H.
	*	D33	D28	D23	D18	D13	D8	D3	

	MSB							LSB	
6th Byte (6th)	B7	B6	B5	B4	B3	B2	B1	B0	5th Column Data is specified and rewritten into the CGRAM Address 00H.
	*	D34	D29	D24	D19	D14	D9	D4	

During a continuous data write operation from one CGRAM Address to the next, it is not necessary to specify the CGRAM address since they are automatically incremented; however, the character pattern data must be specified. The 2nd to the 6th character pattern data byte are considered as one data item, **therefore 1µs is sufficient value for parameter tDOFF between bytes**. Please refer to the information below.

	MSB							LSB	
2nd Byte (7th)	B7	B6	B5	B4	B3	B2	B1	B0	1st Column Data is specified and rewritten into the CGRAM Address 01H.
	*	D30	D25	D20	D15	D10	D5	D0	

:
:

	MSB							LSB	
6th Byte (11th)	B7	B6	B5	B4	B3	B2	B1	B0	5th Column Data is specified and rewritten into the CGRAM Address 01H.
	*	D34	D29	D24	D19	D14	D9	D4	

where: Y2 (MSB) to Y0 (LSB): CGRAM Address Bits (8 Characters)
D34 (MSB) to D0 (LSB): Character Pattern Data Bits (35 outputs)

Please refer below for the CGROM Address and CGRAM Address Setting relationship.

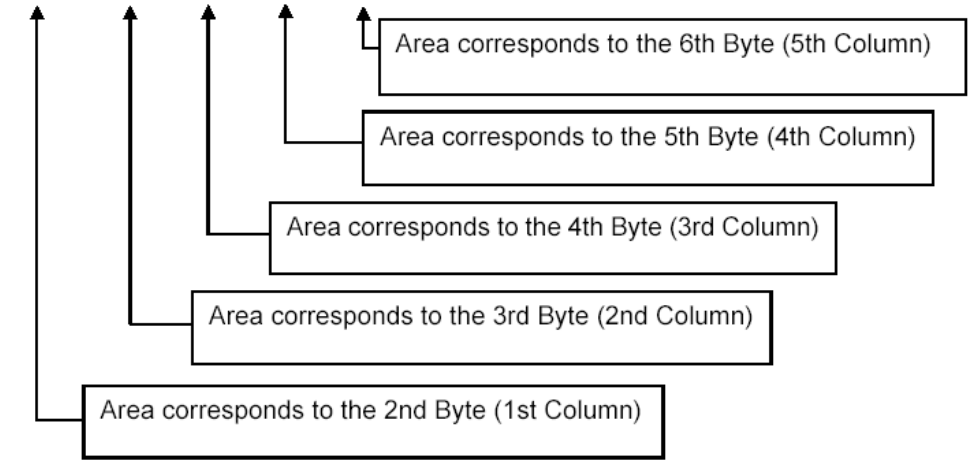
Teble-7

Y2	Y1	Y0	CGROM Address
0	0	0	RAM00(01000000B)
0	0	1	RAM01(01000001B)
0	1	0	RAM02(01000010B)
0	1	1	RAM03(01000011B)
1	0	0	RAM04(01000100B)
1	0	1	RAM05(01000101B)
1	1	0	RAM06(01000110B)
1	1	1	RAM07(01000111B)

The CGROM and CGRAM output area placement is given in the table below.

Teble-8

D0	D1	D2	D3	D4
D5	D6	D7	D8	D9
D10	D11	D12	D13	D14
D15	D16	D17	D18	D19
D20	D21	D22	D23	D24
D25	D26	D27	D28	D29
D30	D31	D32	D33	D34



The Character Generator ROM (CGROM) consists of 8 CGROM Address bits generating 5 x 7 dot matrix character patterns. It can store up to a maximum of 248 types of character patterns.

3-2-3. NUMBER OF DIGITS SET COMMAND

The Number of Digits Set Command is used to write the number of display into the display digit register.

	MSB							LSB
1st Byte	B7	B6	B5	B4	B3	B2	B1	B0
	1	1	1	0	0	0	*	*

	MSB							LSB
2nd Byte	B7	B6	B5	B4	B3	B2	B1	B0
	0	*	*	*	F3	F2	F1	F0

The Number of Digits Set Mode is selected and the number of digit value is specified, Universal Function set to ON/OFF.

where: F3 (MSB) to F0 (LSB): Display Duty Data Bits (16 stages)

Teble-9

F3	F2	F1	F0	Digits
0	0	0	0	T1 (G1)
0	0	0	1	T1 (G1)~T2 (G2)
0	0	1	0	T1 (G1)~T3 (G3)
0	0	1	1	T1 (G1)~T4 (G4)
0	1	0	0	T1 (G1)~T5 (G5)
0	1	0	1	T1 (G1)~T6 (G6)
0	1	1	0	T1 (G1)~T7 (G7)
0	1	1	1	T1 (G1)~T8 (G8)
1	0	0	0	T1 (G1)~T9 (G9)
1	0	0	1	T1 (G1)~T10 (G10)
1	0	1	0	T1 (G1)~T11 (G11)
1	0	1	1	T1 (G1)~T12 (G12)
1	1	0	0	T1 (G1)~T13 (G13)
1	1	0	1	T1 (G1)~T14 (G14)
1	1	1	0	T1 (G1)~T15 (G15)
1	1	1	1	T1 (G1)~T16 (G16)

3-2-4. DIMMING SET COMMAND

The Dimming Set Command is used to write the display duty value to the duty cycle register. Using a 8-bit data, the display duty adjusts the contrast in 240 stages. When the power is turned ON or when the /RESET signal is inputted, the duty cycle register value is set to "0". It's advisable to always execute this command before turning on the display, after which the desired duty value may be set. The command format is given below.

	MSB							LSB
1st Byte	B7	B6	B5	B4	B3	B2	B1	B0
	1	1	1	0	0	1	*	*

	MSB							LSB
2nd Byte	B7	B6	B5	B4	B3	B2	B1	B0
	H7	H6	H5	H4	H3	H2	H1	H0

Display Duty Set Mode is selected and the duty value is specified.

The relationship between the Setup Data, Controlled Grid Duty and the Synchronous Signal Quantity are given in the table below.

Teble-10

H7	H6	H5	H4	H3	H2	H1	H0	Dimming Quantity (Grid pin)
0	0	0	0	0	0	0	0	0/255 x T
0	0	0	0	0	0	0	1	1/255 x T
0	0	0	0	0	0	1	0	2/255 x T
0	0	0	0	0	0	1	1	3/255 x T
0	0	0	0	0	1	0	0	4/255 x T
:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:
1	1	1	0	1	1	1	1	239/255 x T
1	1	1	1	0	0	0	0	240/255 x T
1	1	1	1	0	0	0	1	240/255 x T
:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	0	240/255 x T
1	1	1	1	1	1	1	1	240/255 x T

*default

3-2-5. GRAY-LEVEL SET COMMAND

The Gray-Level Set Command is used to write the register setting value and gray level duty value to the register. Using a 3-bit data 1st byte and 8-bit data 2nd byte, the set register adjusts the contrast in 240 stages. When the power is turned ON or when the /RESET signal is inputted, both the register are set to "0".
The data sets the "1" (enable state) or "0" (disable state). The command format is given below.

	MSB							LSB
1st Byte	B7	B6	B5	B4	B3	B2	B1	B0
	1	0	1	*	*	J2	J1	J0

J2	J1	J0	Register Setting
0	0	0	Anode (D0A～D34A)
0	0	1	Anode (D0B～D34B)
0	1	0	Don't Care
0	1	1	Don't Care
1	0	0	Don't Care
1	0	1	Don't Care
1	1	0	Don't Care
1	1	1	Don't Care

	MSB							LSB
2nd Byte	B7	B6	B5	B4	B3	B2	B1	B0
	I7	I6	I5	I4	I3	I2	I1	I0

Teble-12

I7	I6	I5	I4	I3	I2	I1	I0	Dimming Data
0	0	0	0	0	0	0	0	0/255
0	0	0	0	0	0	0	1	1/255
0	0	0	0	0	0	1	0	2/255
0	0	0	0	0	0	1	1	3/255
:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:
1	1	1	0	1	1	1	1	239/255
1	1	1	1	0	0	0	0	240/255
1	1	1	1	0	0	0	1	240/255
:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	1	240/255

*default

3-2-6. GRAY-LEVEL ON/OFF SET COMMAND

The Gray-Level ON/OFF Set consists of 2 address bits used to store the symbol data. The symbol data specified by the GLRAM is directly outputted. The command format is given below.

	MSB							LSB
1st Byte	B7	B6	B5	B4	B3	B2	B1	B0
	1	1	0	X4	X3	X2	X1	X0

	MSB							LSB
2nd Byte	*	*	0	0	0	0	K1	K0

K1 = "0": Anode (D0B～D34B) are turned "OFF"
K1 = "1": Anode (D0B～D34B) are turned "ON"

K0 = "0": Anode (D0A～D34A) are turned "OFF"
K0 = "1": Anode (D0A～D34A) are turned "ON"

Please refer to the table below for Anode/Segment (K0~K2) position and GLRAM (X0~X4) Duty Timing (Digit) Address setting relationship.

Teble-13

Duty Timing (Digit) Address	Anode (D0A～D34A)	Anode (D0B～D34B)
T1 (11000000B)	ON/OFF	ON/OFF
T2 (11000001B)	ON/OFF	ON/OFF
T3 (11000010B)	ON/OFF	ON/OFF
T4 (11000011B)	ON/OFF	ON/OFF
T5 (11000100B)	ON/OFF	ON/OFF
T6 (11000101B)	ON/OFF	ON/OFF
T7 (11000110B)	ON/OFF	ON/OFF
T8 (11000111B)	ON/OFF	ON/OFF
T9 (11001000B)	ON/OFF	ON/OFF
T10 (11001001B)	ON/OFF	ON/OFF
T11 (11001010B)	ON/OFF	ON/OFF
T12 (11001011B)	ON/OFF	ON/OFF
T13 (11001100B)	ON/OFF	ON/OFF
T14 (11001101B)	ON/OFF	ON/OFF
T15 (11001110B)	ON/OFF	ON/OFF
T16 (11001111B)	ON/OFF	ON/OFF

3-2-7. DISPLAY LIGHT SET COMMAND

The Display Light Set Command is used to turn all display lights ON or OFF. All Display Lights On Mode is primarily used for testing the display. The All Display Light OFF Mode is used for the blinking display and to prevent any malfunction when the power is turned on. The command format is given below.

	MSB							LSB
1st Byte	B7	B6	B5	B4	B3	B2	B1	B0
	1	1	1	0	1	0	LS	HS

where: HS: All Display Lights are turned ON
LS: All Display Lights are turned OFF

The table below shows Segment and Anode Display Status in relation to the Display Light Set Command data.

Teble-14

Bit Name	Segment and Anode Display Status
HS	"0": Normal Display Mode "1": All outputs (Anode, Segment) = "High" The duty of Grid will be follow Dimming Setting. The duty of Anode/Segment will be follow Gray-Level Setting.
LS	"0": Normal Display Mode "1": All outputs (Anode, Segment) = "Low"

4. CONNECTION

Connector : 2213R-06G-F1 (NELTRON)
Applicable mating Connector : HIF3BA-6D-2.54R (HIROSE)

Connector Pin Assignment

Table-15

Pin No.	Description
1	Vcc(5V)
2	CS
3	CP
4	DA
5	RESET
6	GND

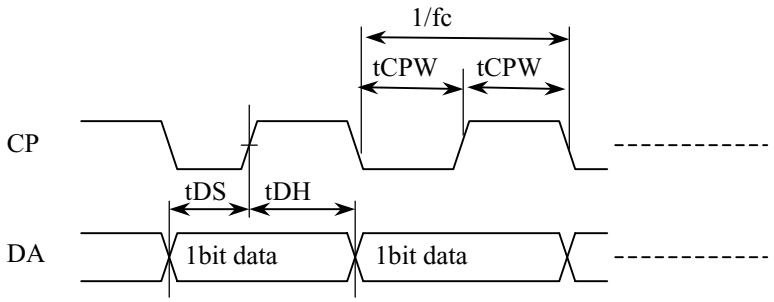
Connector Pin Specifications

Teble-16

Function	Symbol	Input／Output	Description
Shift Clock Input	CP	Input	Serial data is shifted on the rising edge of CP
Serial Data Input	DA	Input	Input from LSB.
Chip Select Input	$\overline{CS}$	Input	Serial data transfer is disabled when CS pin is "H" level.
Reset Input	$\overline{RESET}$	Input	"Low" initializes all the functions. For an initial status, see Reset Function
GND Pin	GND	Input	GND

5. TIMING CHARACTERISTICS

5-1. WRITING WAVEFORM



Teble-17

Parameter	Symbol	Min	Typ	Max	Unit
CP Frequency	fc	-	-	0.5	MHz
CP Pulse Width	tCPW	700	-	-	ns
CP Hold Time	tCS-CP	1000	-	-	ns
CS Hold Time	tCP-CS	1000	-	-	ns
CS Pulse Width	tCSW	1000	-	-	ns
Data Processing Time	tDOFF	2000	-	-	ns
Data Setup Time	tDS	300	-	-	ns
Deta Hold Time	tDH	300	-	-	ns

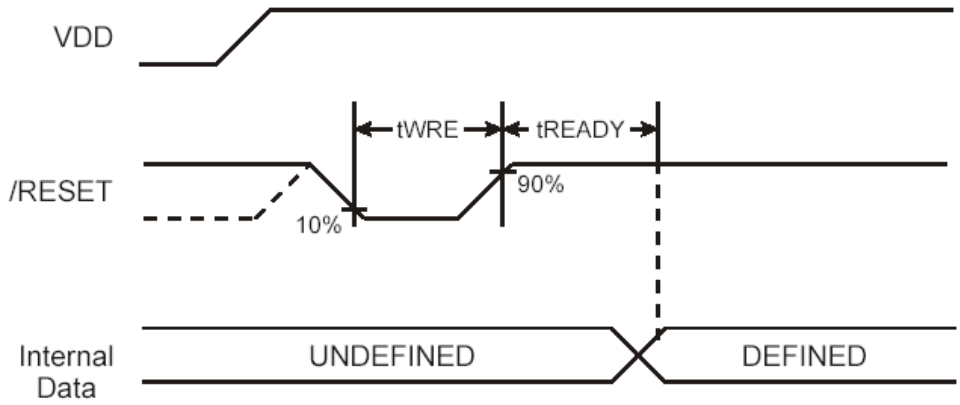
5-2. GRID SCAN TIMING

Teble-18

Grid Scan Timing	DCRAM Address Gray-Level ON/OFF Set Address	ON/OFF timing of Grid																Selection of code	
		1G	2G	3G	4G	5G	6G	7G	8G	9G	10G	11G	12G	13G	14G	15G	16G	DCRAM_A	DCRAM_B
T1	00H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	Note	Note
T2	01H	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	Note	Note
T3	02H	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	Note	Note
T4	03H	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	Note	Note
T5	04H	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	Note	Note
T6	05H	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	Note	Note
T7	06H	L	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	Note	Note
T8	07H	L	L	L	L	L	L	L	H	L	L	L	L	L	L	L	L	Note	Note
T9	08H	L	L	L	L	L	L	L	L	H	L	L	L	L	L	L	L	Note	Note
T10	09H	L	L	L	L	L	L	L	L	L	H	L	L	L	L	L	L	Note	Note
T11	0AH	L	L	L	L	L	L	L	L	L	L	H	L	L	L	L	L	Note	Note
T12	0BH	L	L	L	L	L	L	L	L	L	L	L	H	L	L	L	L	Note	Note
T13	0CH	L	L	L	L	L	L	L	L	L	L	L	L	H	L	L	L	Note	Note
T14	0DH	L	L	L	L	L	L	L	L	L	L	L	L	L	H	L	L	Note	Note
T15	0EH	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	L	Note	Note
T16	0FH	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	Note	Note
T17	10H	don't use																	
T18	11H																		
T19	12H																		
T20	13H																		
T21	14H																		
T22	15H																		
T23	16H																		
T24	17H																		

Note) Please specify an arbitrary code from the CGROM code.

5-3. RESET CONTROL WAVE



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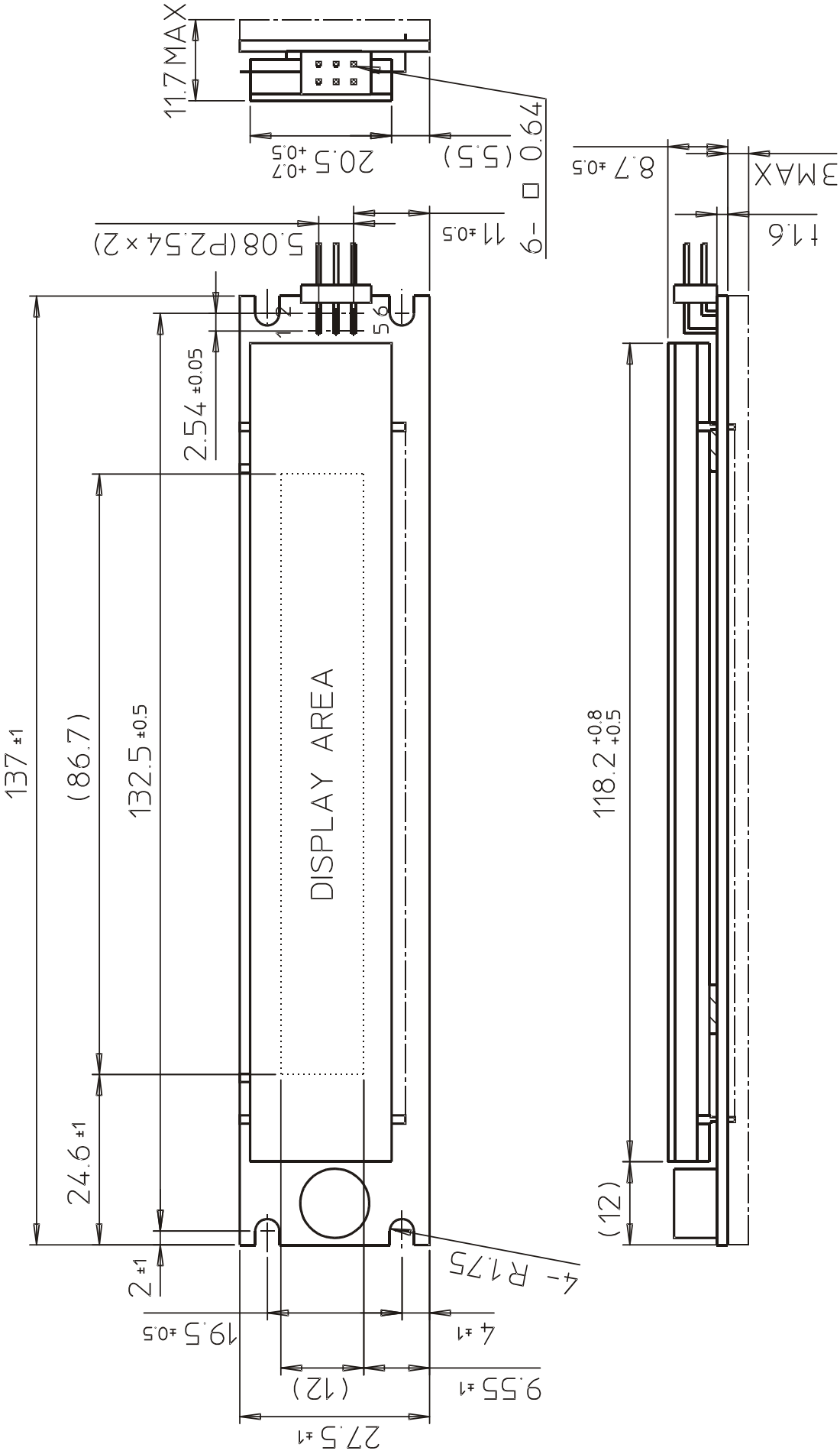
Item	Symbol	Min	Typ	Max	Unit
Reset Pulse Width	tWRE	2	-	-	μ s
Ready Time after Reset	tREADY	3	-	-	ms

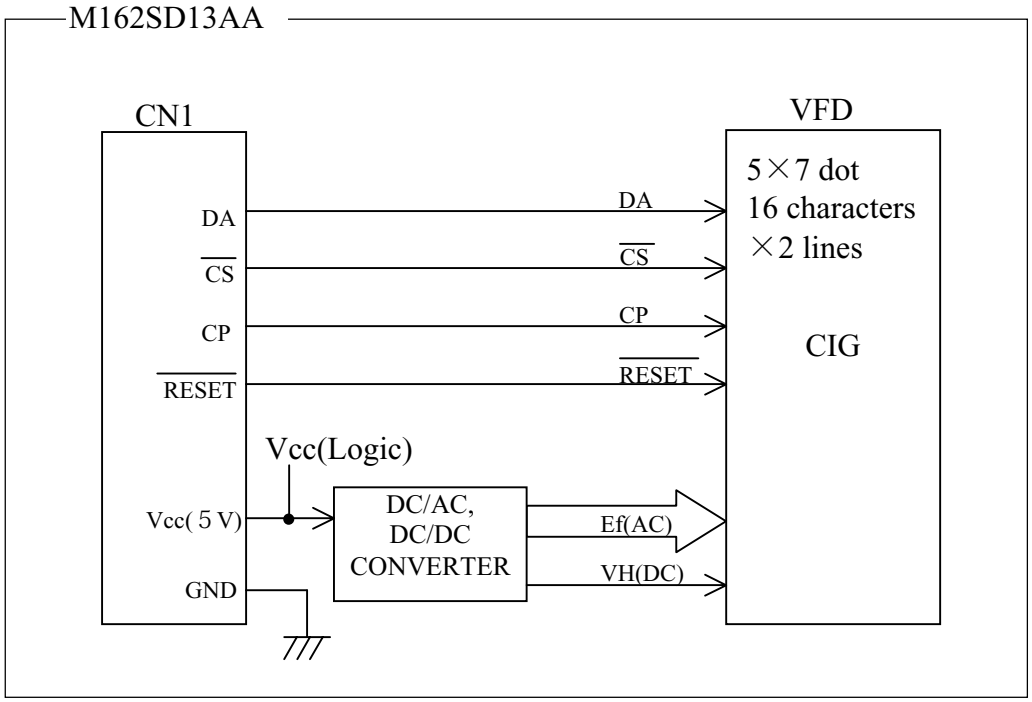
6. OUTER DIMENSION

FIGURE-1



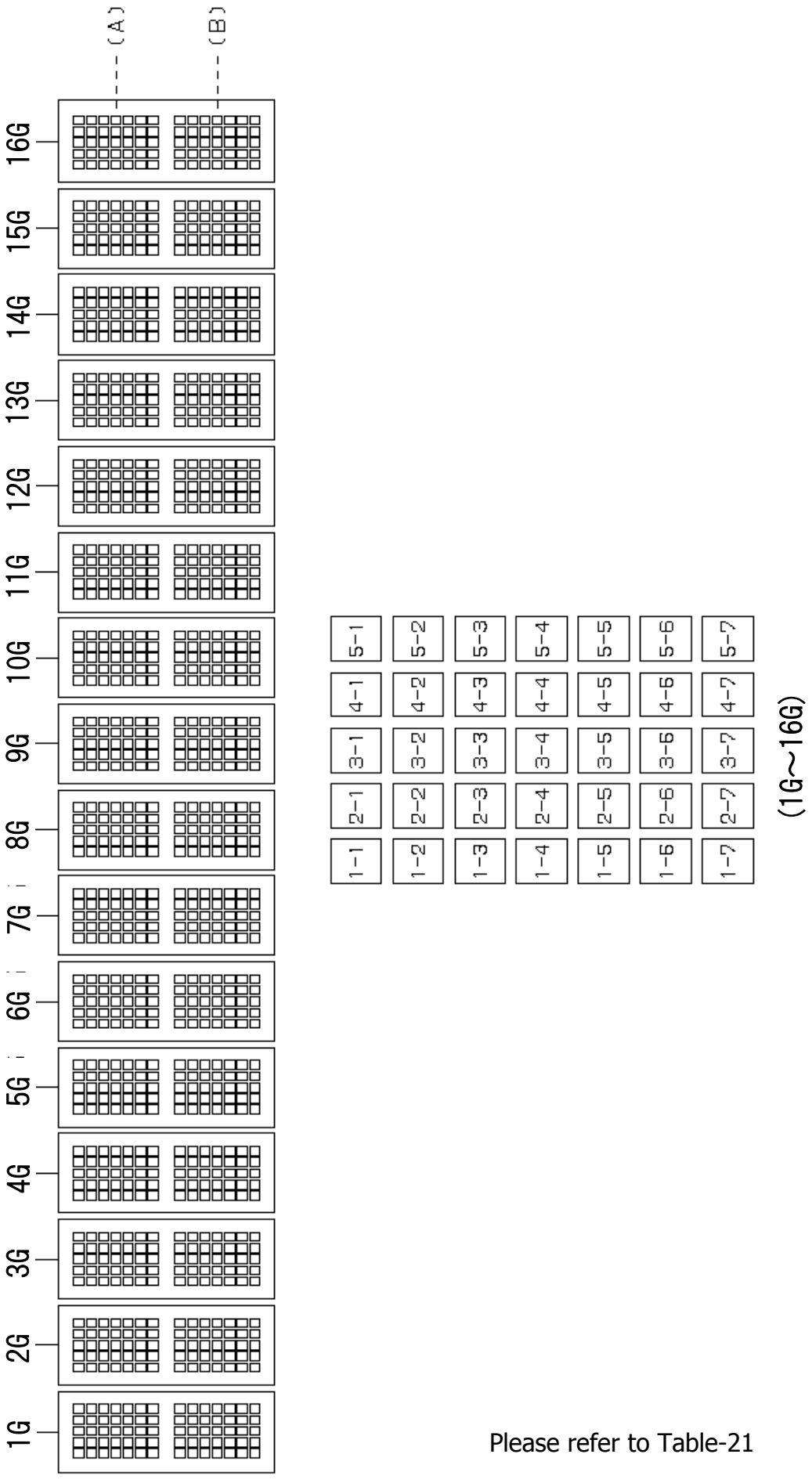
7. CIRCUIT BLOCK DIAGRAM

FIGURE-2



8. GRID ASSIGNMENT

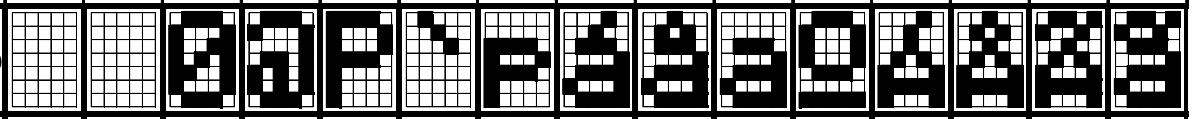
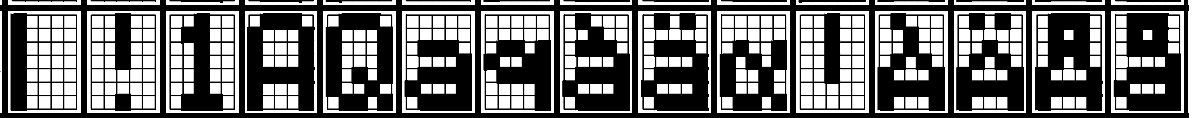
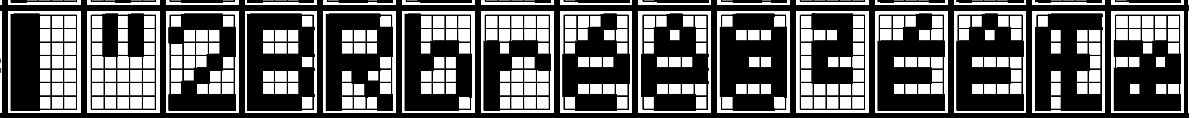
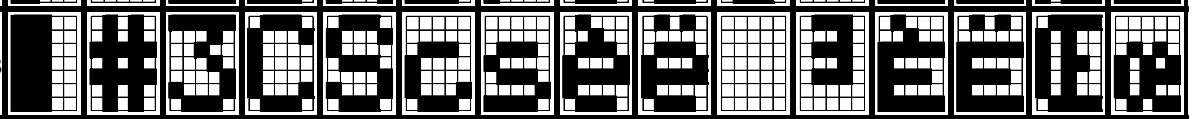
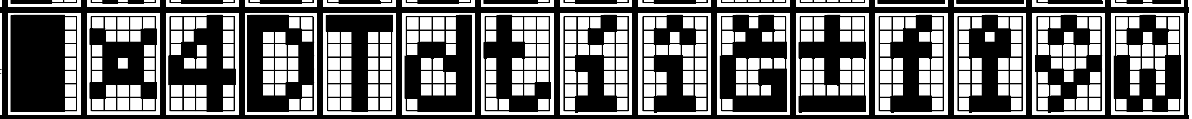
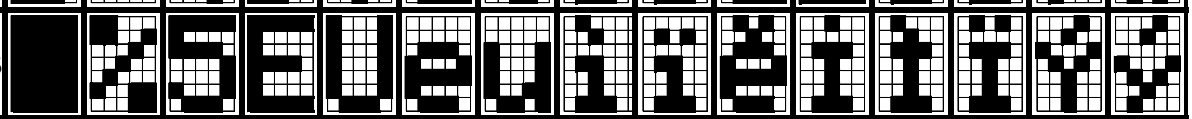
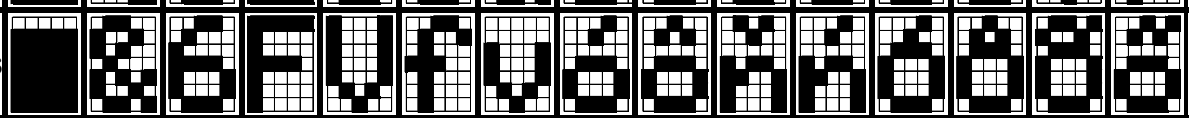
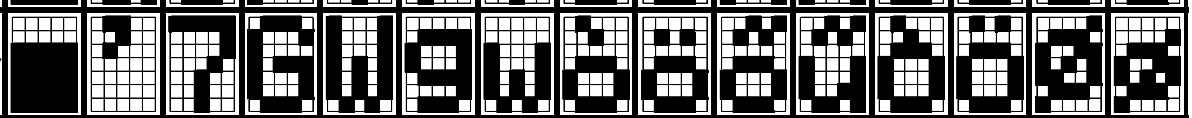
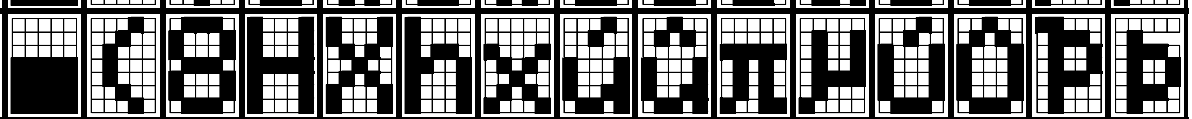
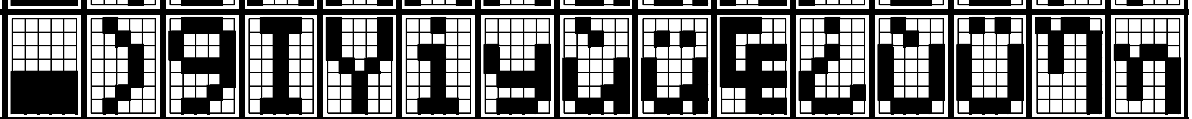
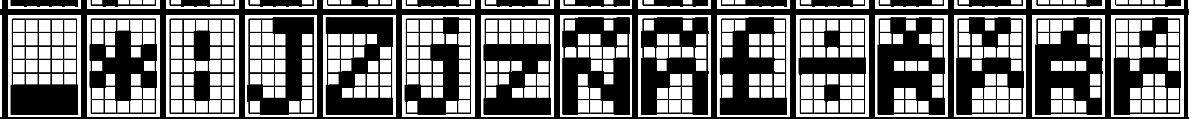
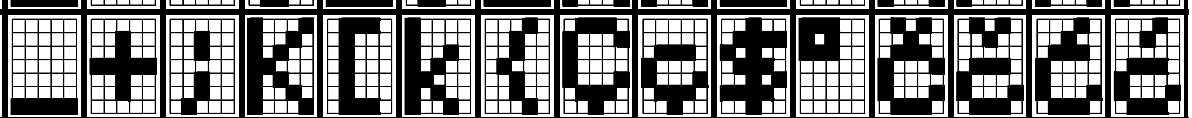
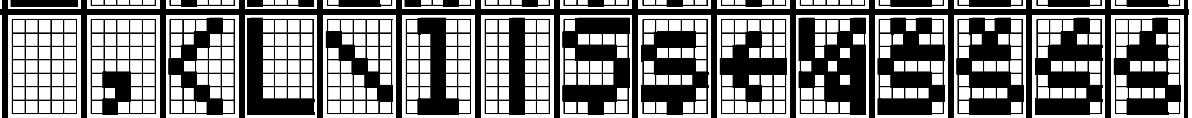
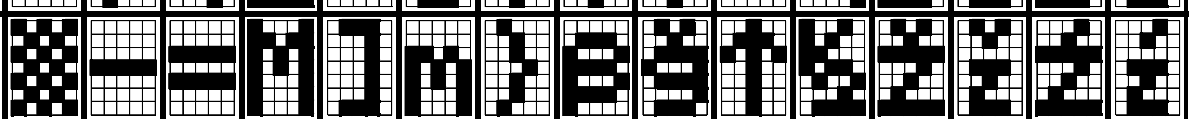
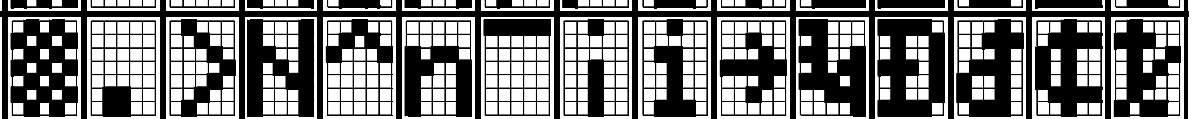
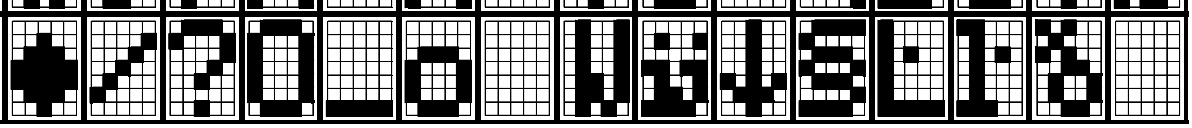
FIGURE-3



9. Please refer to Table-21

CHARACTER FONT TABLES (European Font)

Teble-20

MSB / LSB	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
0000	RAM0															
0001	RAM1															
0010	RAM2															
0011	RAM3															
0100	RAM4															
0101	RAM5															
0110	RAM6															
0111	RAM7															
1000																
1001																
1010																
1011																
1100																
1101																
1110																
1111																

10. ANODE CONNECTION

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	16G~1G
D0A	1-1 A
D1A	2-1 A
D2A	3-1 A
D3A	4-1 A
D4A	5-1 A
D5A	1-2 A
D6A	2-2 A
D7A	3-2 A
D8A	4-2 A
D9A	5-2 A
D10A	1-3 A
D11A	2-3 A
D12A	3-3 A
D13A	4-3 A
D14A	5-3 A
D15A	1-4 A
D16A	2-4 A
D17A	3-4 A
D18A	4-4 A
D19A	5-4 A
D20A	1-5 A
D21A	2-5 A
D22A	3-5 A
D23A	4-5 A
D24A	5-5 A
D25A	1-6 A
D26A	2-6 A
D27A	3-6 A
D28A	4-6 A
D29A	5-6 A
D30A	1-7 A
D31A	2-7 A
D32A	3-7 A
D33A	4-7 A
D34A	5-7 A

	16G~1G
D0B	1-1 B
D1B	2-1 B
D2B	3-1 B
D3B	4-1 B
D4B	5-1 B
D5B	1-2 B
D6B	2-2 B
D7B	3-2 B
D8B	4-2 B
D9B	5-2 B
D10B	1-3 B
D11B	2-3 B
D12B	3-3 B
D13B	4-3 B
D14B	5-3 B
D15B	1-4 B
D16B	2-4 B
D17B	3-4 B
D18B	4-4 B
D19B	5-4 B
D20B	1-5 B
D21B	2-5 B
D22B	3-5 B
D23B	4-5 B
D24B	5-5 B
D25B	1-6 B
D26B	2-6 B
D27B	3-6 B
D28B	4-6 B
D29B	5-6 B
D30B	1-7 B
D31B	2-7 B
D32B	3-7 B
D33B	4-7 B
D34B	5-7 B

11. WARRANTY

This display module is guaranteed for 1 year after a shipment from FUTABA.

12. OPERATING RECOMMENDATION

12-1. Since VFDs are made of glass material.
Avoid applying excessive shock or vibration beyond the specification for the module.
Careful handing is essential.

12-2. Applying lower voltage than the specified may cause non activation for selected pixels.
Conversely, higher voltage may cause may non-selected pixel to be activated.
If such a phenomenon is observed, check the voltage level of the power supply.

12-3. Avoid plugging or unplugging the interface connection with the power on.

12-4. If the start up time of the supply voltage is slow, the controller may not be reset.
The supply voltage must be risen up to the specified voltage level within 30msec.

12-5. Avoid using the module where excessive noise interference is expected. Noise affects the interface signal and causes improper operation.
Keep the length of the interface cable less than 50cm (When the longer cable is required, please contact FUTABA engineering.).

12-6. When power supply is turned off, the capacitor does not discharge immediately.
The high voltage applied to the VFD must not contact the controller IC.
(The shorting of the mounted components within 30 seconds after power off may cause damage.)

12-7. When fixed pattern is displayed for long time, you may see uneven luminance.
It is recommended to change the display patterns sometimes in order to keep best display quality.

REMARKS

This specification is subject to change without prior in order improve the design and quality. Your consultation with FUTABA sales office is recommended for the use of this module.