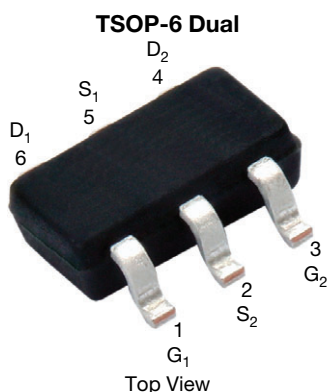


Automotive N- and P-Channel 20 V (D-S) MOSFET



Marking Code: 9V

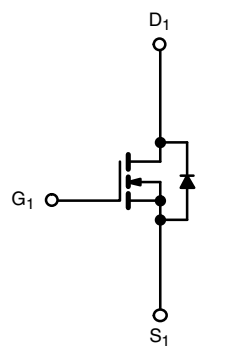
PRODUCT SUMMARY		
	N-CHANNEL	P-CHANNEL
V_{DS} (V)	20	-20
$R_{DS(on)}$ (Ω) at $V_{GS} = \pm 4.5$ V	0.052	0.077
$R_{DS(on)}$ (Ω) at $V_{GS} = \pm 2.5$ V	0.070	0.119
I_D (A)	4.7	-4.1
Configuration	N- and p-pair	

FEATURES

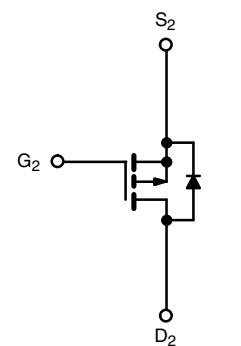
- TrenchFET® power MOSFET
- AEC-Q101 qualified
- 100 % R_g and UIS tested
- Material categorization:
for definitions of compliance please see
www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE



N-Channel MOSFET



P-Channel MOSFET

ORDERING INFORMATION	
Package	TSOP-6 Dual
Lead (Pb)-free and halogen-free	SQ3583CEV (for detailed order number please see www.vishay.com/doc?79771)

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$, unless otherwise noted)				
PARAMETER	SYMBOL	N-CHANNEL	P-CHANNEL	UNIT
Drain-source voltage	V_{DS}	20	-20	V
Gate-source voltage	V_{GS}	± 12	± 12	
Continuous drain current	I_D	4.7	-4.1	A
		2.7	-2.4	
Pulsed drain current	I_{DM}	22	-20	
Continuous source current (diode conduction)	I_S	4.7	-4.1	W
Maximum power dissipation	P_D	1.67	1.67	
		0.56	0.56	
Unclamped inductive surge UIS	I_{AV}	9.0	7.5	A
Operating junction and storage temperature range	T_J, T_{stg}	-55 to +175		$^\circ\text{C}$

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	N-CHANNEL MAX.	P-CHANNEL MAX.	UNIT
Maximum junction-to-ambient ^a	Steady state	R_{thJA}	150	$^\circ\text{C}/\text{W}$
Maximum junction-to-foot (drain)	Steady state	R_{thJF}	90	

Note

a. Surface mounted on 1" x 1" FR4 board



SPECIFICATIONS (T _J = 25°C, unless otherwise noted)										
PARAMETER	SYMBOL	TEST CONDITIONS			MIN.	TYP.	MAX.	UNIT		
Static										
Gate threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA		N-Ch	0.6	-	1.3	V		
		V _{DS} = V _{GS} , I _D = -250 μA		P-Ch	-0.6	-	-1.3			
Gate-body leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 12 V		N-Ch	-	-	± 100	nA		
				P-Ch	-	-	± 100			
Zero gate voltage drain current	I _{DSS}	V _{GS} = 0 V	V _{DS} = 20 V	N-Ch	-	-	1	μA		
		V _{GS} = 0 V	V _{DS} = -20 V	P-Ch	-	-	-1			
		V _{GS} = 0 V	V _{DS} = 20 V, T _J = 55 °C	N-Ch	-	-	5			
		V _{GS} = 0 V	V _{DS} = -20 V, T _J = 55 °C	P-Ch	-	-	-5			
On-state drain current ^a	I _{D(on)}	V _{GS} = 4.5 V	V _{DS} ≥ 5 V	N-Ch	5	-	-	A		
		V _{GS} = -4.5 V	V _{DS} ≤ -5 V	P-Ch	-5	-	-			
Drain-source on-state resistance ^a	R _{DS(on)}	V _{GS} = 4.5 V	I _D = 1 A	N-Ch	-	0.043	0.052	Ω		
		V _{GS} = -4.5 V	I _D = -1 A	P-Ch	-	0.061	0.077			
		V _{GS} = 2.5 V	I _D = 1 A	N-Ch	-	0.056	0.070			
		V _{GS} = -2.5 V	I _D = -1 A	P-Ch	-	0.091	0.119			
Forward transconductance ^a	g _{fs}	V _{DS} = 5 V, I _D = 1 A		N-Ch	-	9	-	S		
		V _{DS} = -5 V, I _D = -1 A		P-Ch	-	6	-			
Diode forward voltage ^a	V _{SD}	I _S = 1.05 A, V _{GS} = 0 V		N-Ch	-	0.80	1.10	V		
		I _S = -1.05 A, V _{GS} = 0 V		P-Ch	-	-0.83	-1.10			
Dynamic ^b										
Total gate charge	Q _g	V _{GS} = 4.5 V	V _{DS} = 10 V, I _D = 1 A	N-Ch	-	3.0	5.0	nC		
		V _{GS} = -4.5 V	V _{DS} = -10 V, I _D = -1 A	P-Ch	-	6.0	9.0			
Gate-source charge	Q _{gs}	V _{GS} = 4.5 V	V _{DS} = 10 V, I _D = 1 A	N-Ch	-	1.0	-			
		V _{GS} = -4.5 V	V _{DS} = -10 V, I _D = -1 A	P-Ch	-	1.0	-			
Gate-drain charge	Q _{gd}	V _{GS} = 4.5 V	V _{DS} = 10 V, I _D = 1 A	N-Ch	-	1.0	-			
		V _{GS} = -4.5 V	V _{DS} = -10 V, I _D = -1 A	P-Ch	-	1.5	-			
Gate resistance	R _g	f = 1 MHz		N-Ch	2.5	-	7.6	Ω		
				P-Ch	4.7	-	14.2			
Turn-on delay time	t _{d(on)}	N-Channel V _{DD} = 10 V, R _L = 10 Ω I _D ≡ 1 A, V _{GEN} = 10 V, R _g = 1 Ω		N-Ch	-	10	15	ns		
Rise time	t _r			P-Ch	-	11	17			
				N-Ch	-	16	24			
				P-Ch	-	18	27			
Turn-off delay time	t _{d(off)}			N-Ch	-	19	29			
				P-Ch	-	30	45			
Fall time	t _f	P-Channel V _{DD} = -10 V, R _L = 10 Ω I _D ≡ -1 A, V _{GEN} = -10 V, R _g = 1 Ω		N-Ch	-	8	12			
				P-Ch	-	20	30			

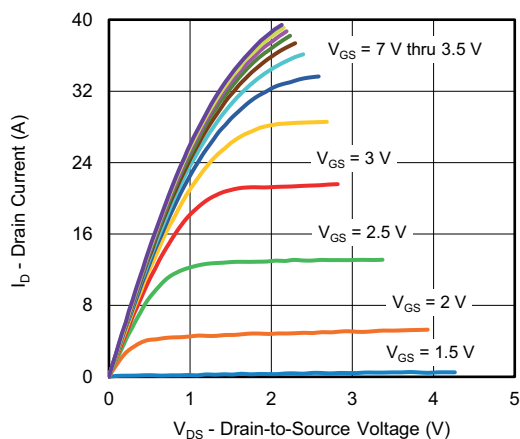
Notes

- a. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$
b. Guaranteed by design, not subject to production testing

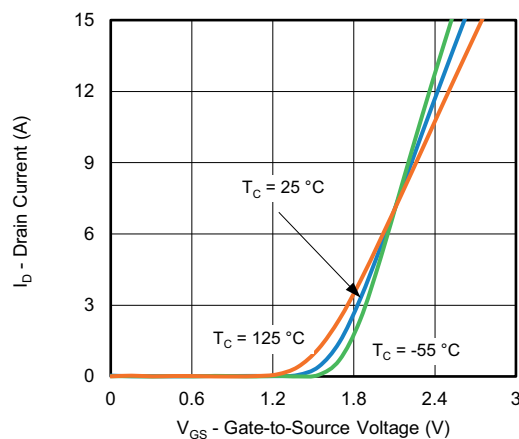
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



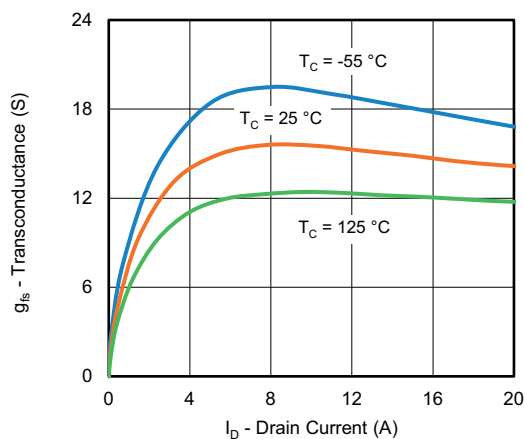
N-CHANNEL TYPICAL CHARACTERISTICS (25 °C unless otherwise noted)



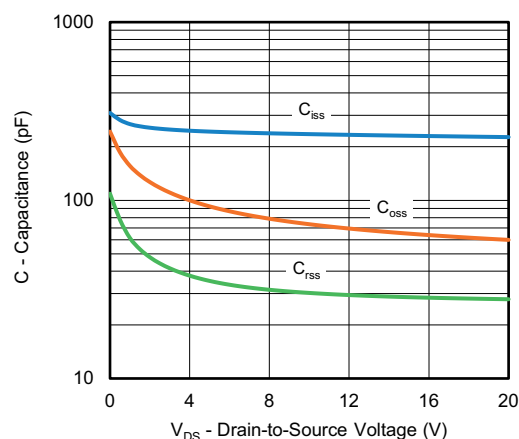
Output Characteristics



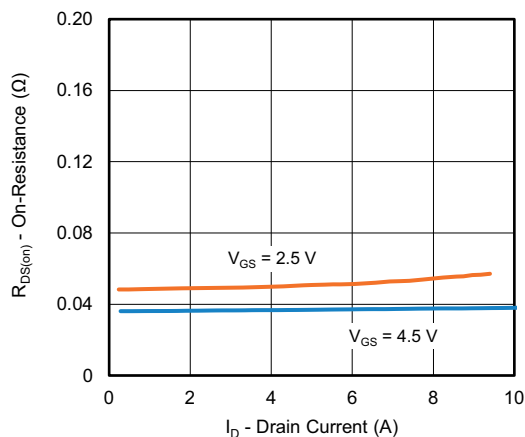
Transfer Characteristics



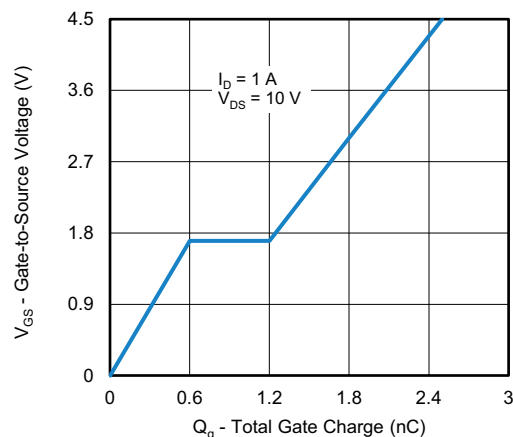
Transconductance



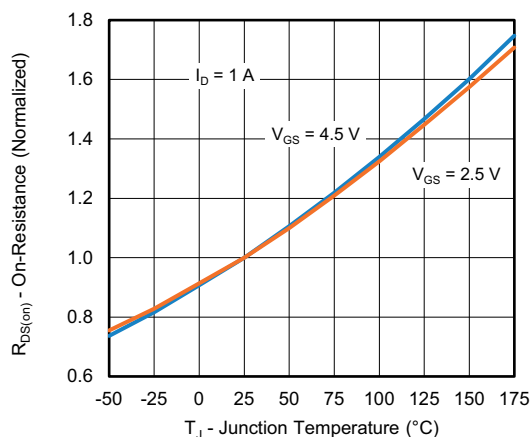
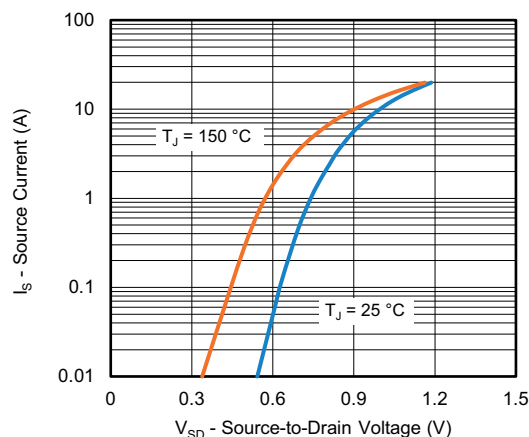
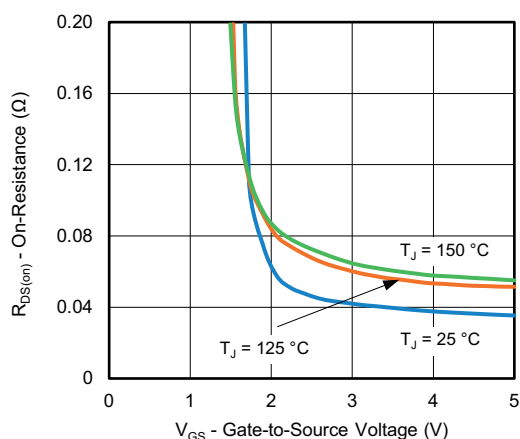
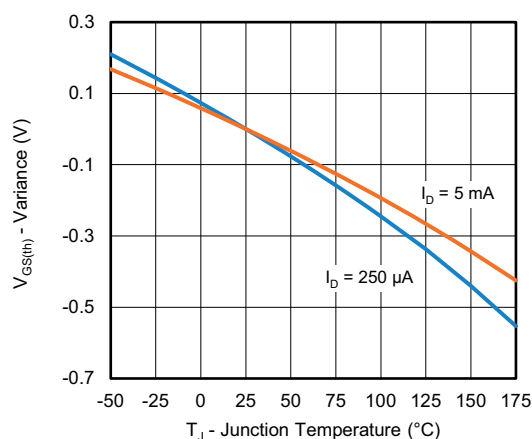
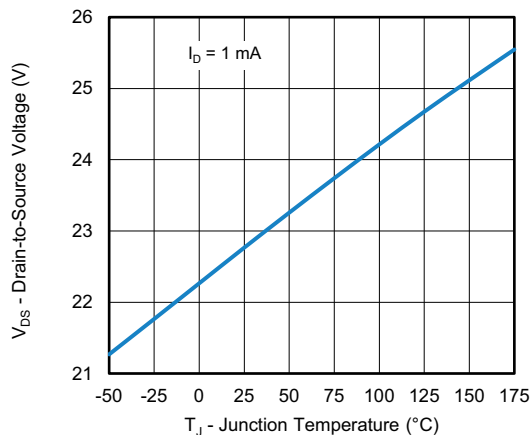
Capacitance

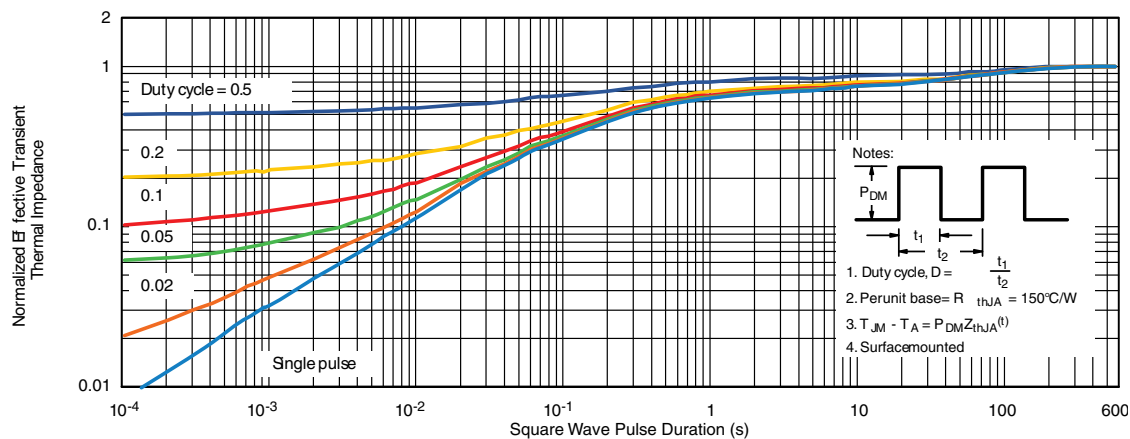
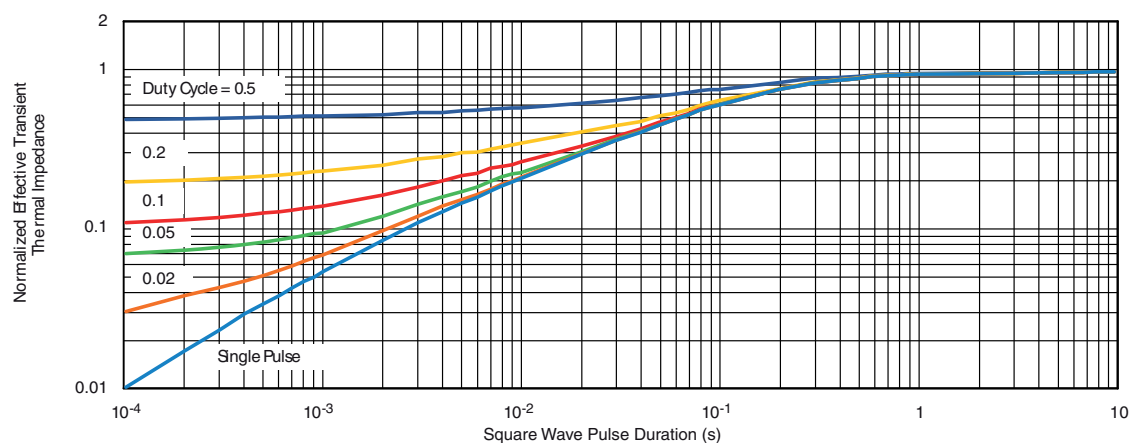


On-Resistance vs. Drain Current



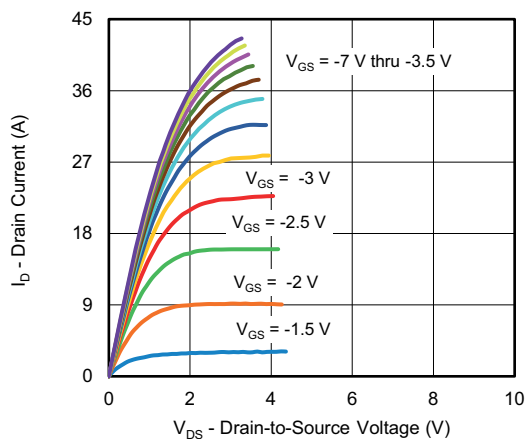
Gate Charge

N-CHANNEL TYPICAL CHARACTERISTICS (25 °C unless otherwise noted)

On-Resistance vs. Junction Temperature

Source-Drain Diode Forward Voltage

On-Resistance vs. Gate-to-Source Voltage

Threshold Voltage

Drain Source Breakdown vs. Junction Temperature

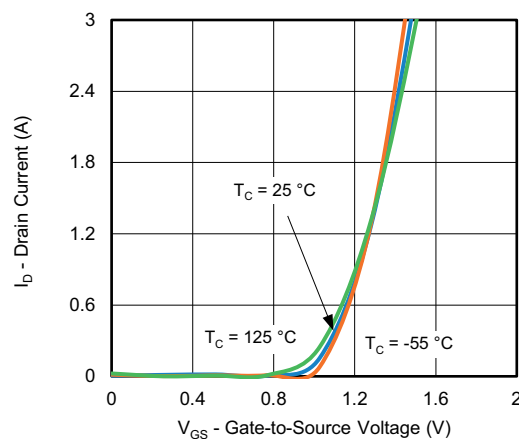
N-CHANNEL TYPICAL CHARACTERISTICS (25 °C unless otherwise noted)

Normalized Thermal Transient Impedance, Junction-to-Ambient

Normalized Thermal Transient Impedance, Junction-to-Foot



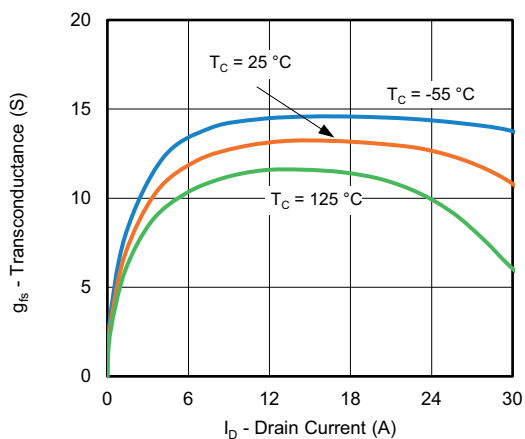
P-CHANNEL TYPICAL CHARACTERISTICS (25 °C unless otherwise noted)



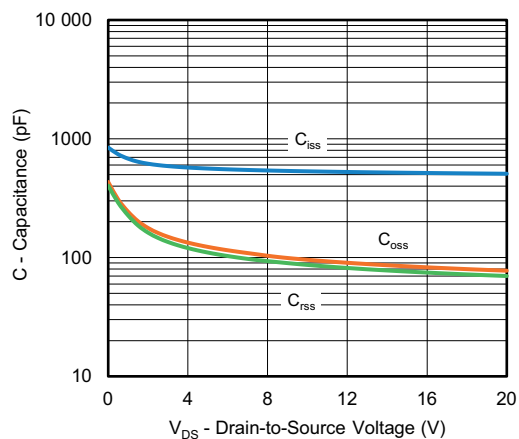
Output Characteristics



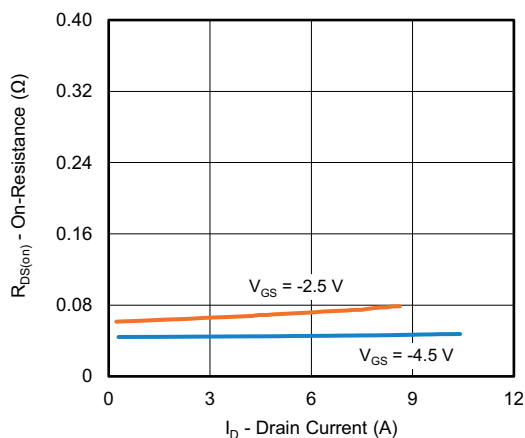
Transfer Characteristics



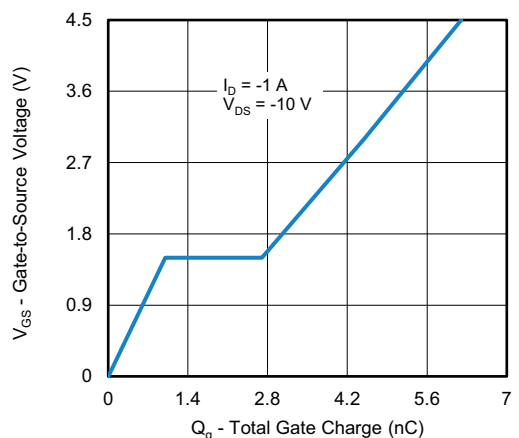
Transconductance



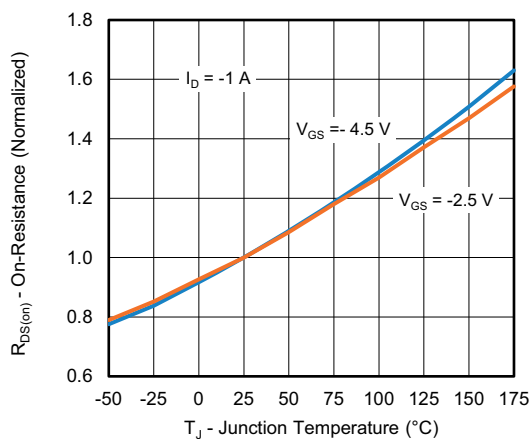
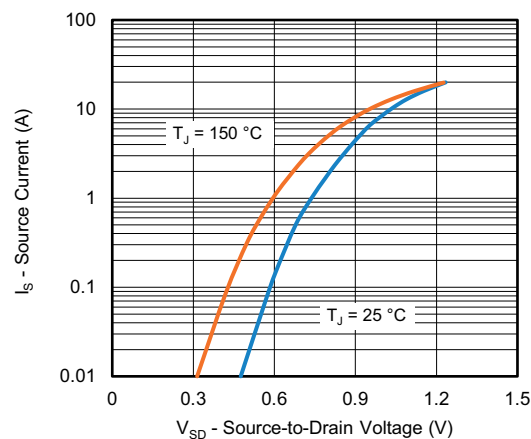
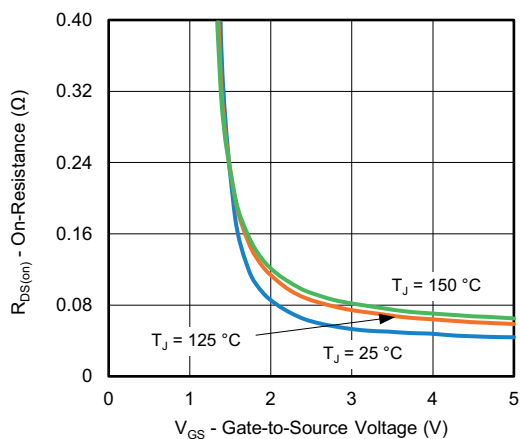
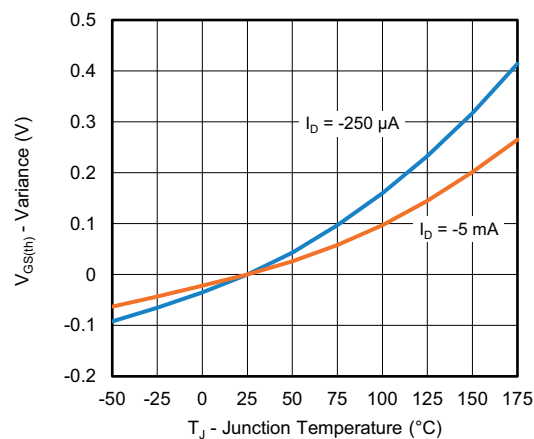
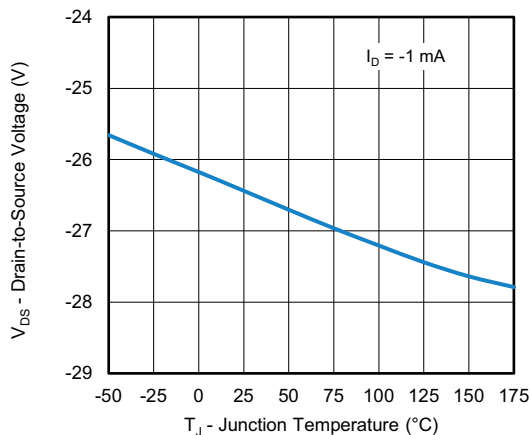
Capacitance



On-Resistance vs. Drain Current

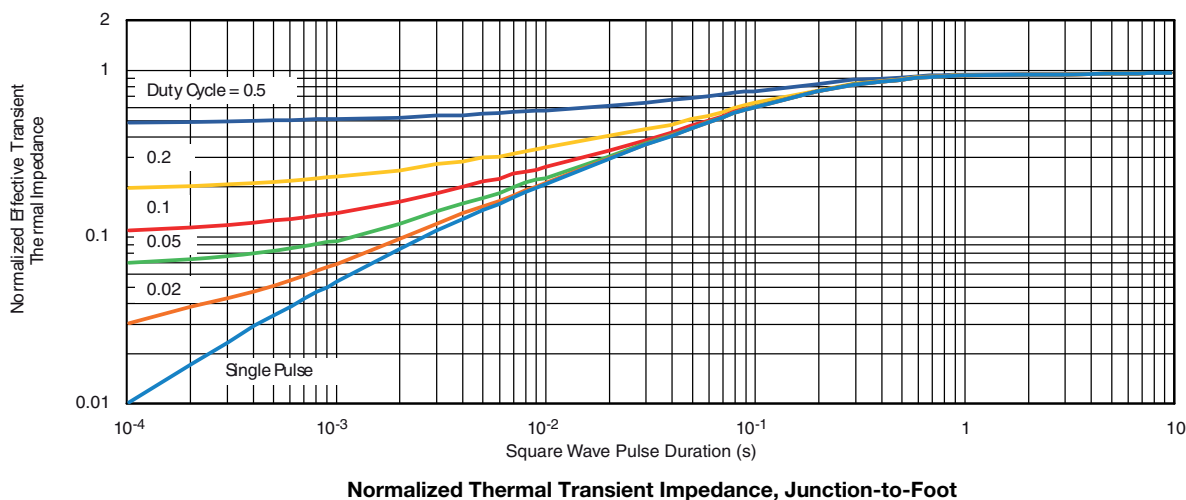
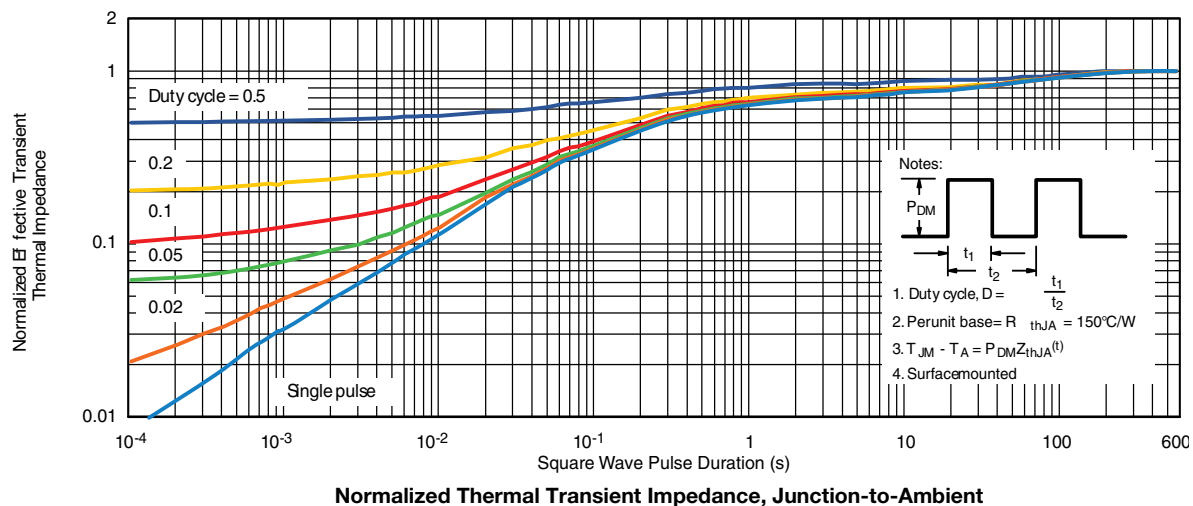


Gate Charge

P-CHANNEL TYPICAL CHARACTERISTICS (25 °C unless otherwise noted)

On-Resistance vs. Junction Temperature

Source-Drain Diode Forward Voltage

On-Resistance vs. Gate-to-Source Voltage

Threshold Voltage

Drain Source Breakdown vs. Junction Temperature



P-CHANNEL TYPICAL CHARACTERISTICS (25 °C unless otherwise noted)



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