# Voltage Regulator - Low Dropout

## 400 mA

## NCV4274C

### Description

The NCV4274C is a precision micro−power voltage regulator with an output current capability of 400 mA available in the DPAK, D2PAK and SOT−223 packages.

The output voltage is accurate within ±2.0% with a maximum dropout voltage of 0.5 V with an input up to 40 V. Low quiescent current is a feature drawing only 125 μA with a 1 mA load. This part is ideal for automotive and all battery operated microprocessor equipment.

The regulator is protected against reverse battery, short circuit, and thermal overload conditions. The device can withstand load dump transients making it suitable for use in automotive environments.

### Features

- 3.3 V, 5.0 V, ±2.0% Output Options
- Low 125 μA Quiescent Current at 1 mA load current
- 400 mA Output Current Capability
- Fault Protection
- +60 V Peak Transient Voltage with Respect to GND
  - −42 V Reverse Voltage
  - Short Circuit
  - Thermal Overload
- Very Low Dropout Voltage
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
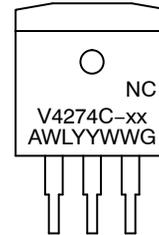- These are Pb−Free Devices

**MARKING DIAGRAMS**

**DPAK**
**DT SUFFIX**
**CASE 369C**

```
74C−xxG
ALYWW
```
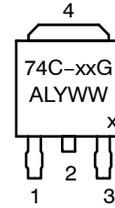
| 1 | Input |
|---|---|
| 2, 4 | Ground |
| 3 | Output |

**D2PAK**
**DS SUFFIX**
**CASE 418AF**

```
NC
V4274C−xx
AWLYYWWG
```

| 1 | Input |
|---|---|
| 2, 4 | Ground |
| 3 | Output |

**SOT−223**
**ST SUFFIX**
**CASE 318E**

```
AYW
74Cxx■
```
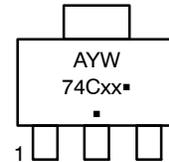
| xx | = 33 (3.3 V) |
|---|---|
| | = 50 (5.0 V) |
| A | = Assembly Location |
| L, WL | = Wafer Lot |
| Y, YY | = Year |
| W, WW | = Work Week |
| G or ■ | = Pb−Free Package |

(Note: Microdot may be in either location)

### ORDERING INFORMATION

NOTE: Some of the devices on this data sheet have been **DISCONTINUED**.

# NCV4274C
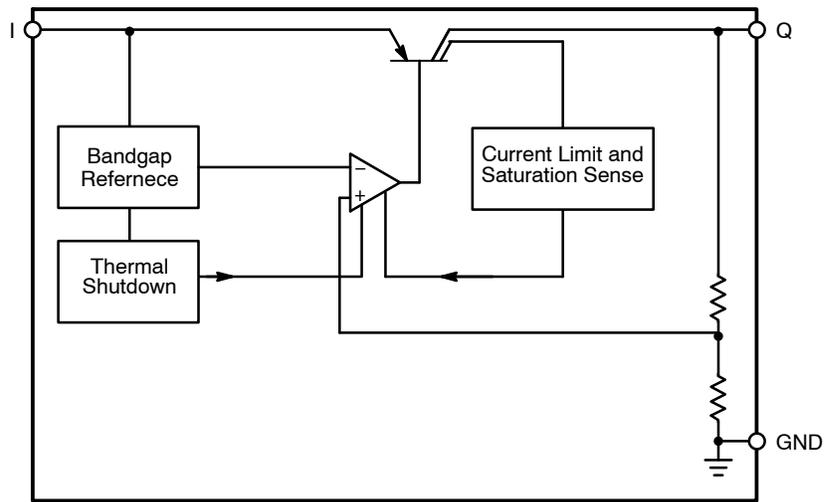


**Figure 1. Block Diagram**

## Pin Definitions and Functions

| Pin No. | Symbol | Function |
|---------|--------|----------|
| 1 | I | Input; Bypass directly at the IC with a ceramic capacitor to GND. |
| 2,4 | GND | Ground |
| 3 | Q | Output; Bypass with a capacitor to GND. |

## ABSOLUTE MAXIMUM RATINGS

| Pin Symbol, Parameter | | Symbol | Condition | Min | Max | Unit |
|---|---|---|---|---|---|---|
| **I**, Input−to−Regulator | Voltage | $V_I$ | | −42 | 45 | V |
| | Current | $I_I$ | | Internally Limited | Internally Limited | |
| **I**, Input peak Transient Voltage to Regulator with Respect to GND (Note 1) | | $V_I$ | | | 60 | V |
| **Q,** Regulated Output | Voltage | $V_Q$ | $V_Q = V_I$ | −1.0 | 40 | V |
| | Current | $I_Q$ | | Internally Limited | Internally Limited | |
| **GND,** Ground Current | | $I_{GND}$ | | − | 100 | mA |
| Junction Temperature<br>Storage Temperature | | $T_J$<br>$T_{Stg}$ | | −40<br>−50 | 150<br>150 | °C<br>°C |
| ESD Capability, Human Body Model (Note 2) | | $ESD_{HB}$ | | 4 | | kV |
| ESD Capability, Machine Model (Note 2) | | $ESD_{MM}$ | | 200 | | V |
| ESD Capability, Charged Device Model (Note 2) | | $ESD_{CDM}$ | | 1 | | kV |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. Load Dump Test B (with centralized load dump suppression) according to ISO16750-2 standard. Guaranteed by design. Not tested in production. Passed Class C.
2. This device series incorporates ESD protection and is tested by the following methods:
   ESD HBM tested per AEC−Q100−002 (EIA/JESD22−A114)
   ESD MM tested per AEC−Q100−003 (EIA/JESD22−A115)
   Field Induced Charge Device Model ESD characterization is not performed on plastic molded packages with body sizes <50mm$^2$ due to the inability of a small package body to acquire and retain enough charge to meet the minimum CDM discharge current waveform characteristic defined in JEDEC JS−002−2014.

# NCV4274C

## OPERATING RANGE

| Parameter | Symbol | Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| Input Voltage (5.0 V Version) | $V_I$ | | 5.5 | 40 | V |
| Input Voltage (3.3 V Version) | $V_I$ | | 4.5 | 40 | V |
| Junction Temperature | $T_J$ | | −40 | 150 | °C |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

## THERMAL RESISTANCE

| Parameter | | Symbol | Condition | Min | Max | Unit |
|---|---|---|---|---|---|---|
| Junction−to−Ambient | DPAK | $R_{thja}$ | | – | 72.5 (Note 3) | °C/W |
| Junction−to−Ambient | D2PAK | $R_{thja}$ | | – | 56.7 (Note 3) | °C/W |
| Junction−to−Case | DPAK | $R_{thjc}$ | | – | 5.8 | °C/W |
| Junction−to−Case | D2PAK | $R_{thjc}$ | | – | 5.8 | °C/W |
| Junction−to−Tab | SOT−223 | $\Psi_{-JLX}, \Psi_{LX}$ | | – | 15.6 (Note 3) | °C/W |
| Junction−to−Ambient | SOT−223 | $R_{\theta JA}, \theta_{JA}$ | | – | 87 (Note 3) | °C/W |

3. 1 oz copper, 300 mm$^2$ copper area, single−sided FR4 PCB.

## MOISTURE SENSITIVITY LEVEL (Note 4)

| Parameter | Symbol | Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| Moisture Sensitivity Level | MSL | DPAK and D2PAK<br>SOT−223 | 1<br>3 | –<br>– | |

4. For more information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## ELECTRICAL CHARACTERISTICS

$-40°C < T_J < 150°C$; $V_I = 13.5$ V unless otherwise noted.

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **REGULATOR** | | | | | | |
| Output Voltage (5.0 V Version) | $V_Q$ | 5 mA < $I_Q$ < 400 mA<br>6 V < $V_I$ < 28 V | 4.9 | 5.0 | 5.1 | V |
| Output Voltage (5.0 V Version) | $V_Q$ | 5 mA < $I_Q$ < 200 mA<br>6 V < $V_I$ < 40 V | 4.9 | 5.0 | 5.1 | V |
| Output Voltage (3.3 V Version) | $V_Q$ | 5 mA < $I_Q$ < 400 mA<br>4.5 V < $V_I$ < 28 V | 3.23 | 3.3 | 3.37 | V |
| Output Voltage (3.3 V Version) | $V_Q$ | 5 mA < $I_Q$ < 200 mA<br>4.5 V < $V_I$ < 40 V | 3.23 | 3.3 | 3.37 | V |
| Current Limit (All Versions) | $I_Q$ | $V_Q$ = 90% $V_{QTYP}$ | 400 | 600 | – | mA |
| Quiescent Current | $I_q$ | $I_Q$ = 1 mA<br>  $V_Q$ = 5.0 V<br>  $V_Q$ = 3.3 V<br>$I_Q$ = 250 mA<br>  $V_Q$ = 5.0 V<br>  $V_Q$ = 3.3 V<br>$I_Q$ = 400 mA<br>  $V_Q$ = 5.0 V<br>  $V_Q$ = 3.3 V | <br>–<br>–<br><br>–<br>–<br><br>–<br>– | <br>125<br>125<br><br>5<br>5<br><br>10<br>10 | <br>250<br>250<br><br>15<br>15<br><br>35<br>35 | <br>μA<br>μA<br><br>mA<br>mA<br><br>mA<br>mA |
| Dropout Voltage<br><br>5.0 V Version | $V_{DR}$ | $I_Q$ = 250 mA,<br>$V_{DR} = V_I - V_Q$<br>$V_I$ = 5.0 V | – | 250 | 500 | mV |
| Load Regulation (3.3 V and 5 V Versions) | $\Delta V_Q$ | $I_Q$ = 5 mA to 400 mA | – | 3 | 20 | mV |
| Line Regulation (3.3 V and 5 V Versions) | $\Delta V_Q$ | $\Delta V_I$ = 12 to 32 V<br>$I_Q$ = 5 mA | – | 4 | 25 | mV |
| Power Supply Ripple Rejection | PSRR | $fr$ = 100 Hz,<br>$V_r$ = 0.5 $V_{PP}$ | – | 60 | – | dB |
| Thermal Shutdown Temperature* | $T_{SD}$ | $I_Q$ = 5 mA | 150 | – | 210 | °C |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
*Guaranteed by design, not tested in production
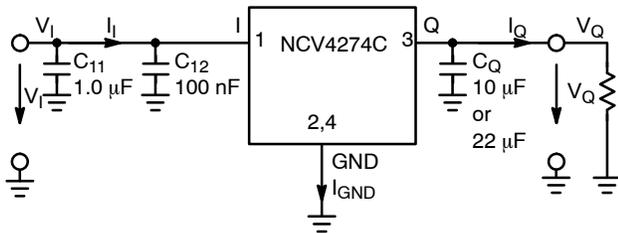


**Figure 2. Measuring Circuit**
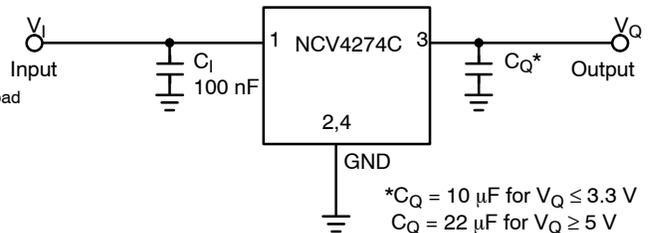


**Figure 3. Application Circuit**

## TYPICAL CHARACTERISTIC CURVES − 5 V VERSION
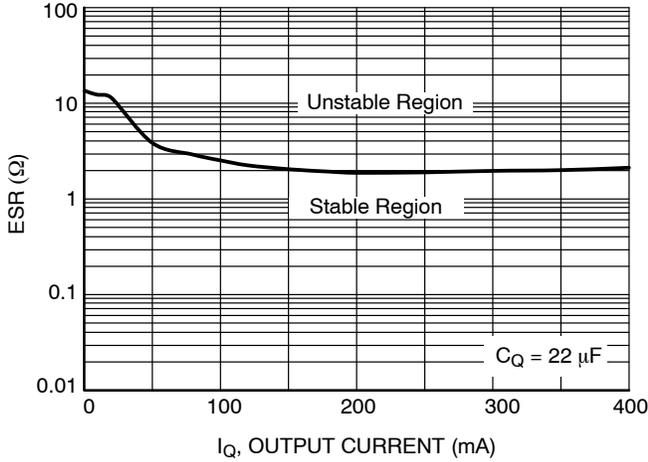


**Figure 4. Output Stability with Output Capacitor ESR**
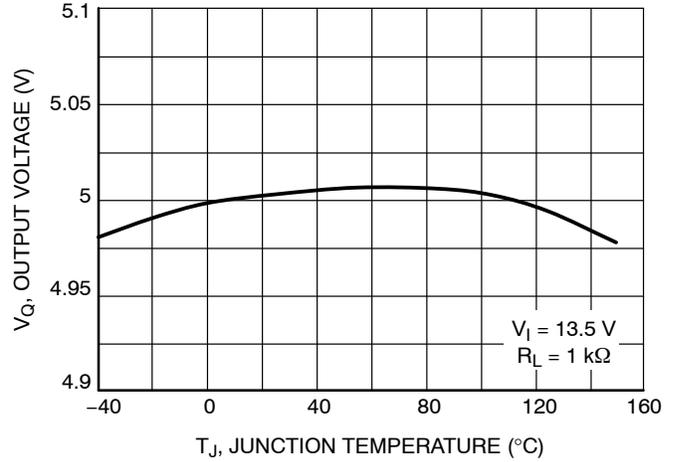


**Figure 5. Output Voltage vs. Junction Temperature**
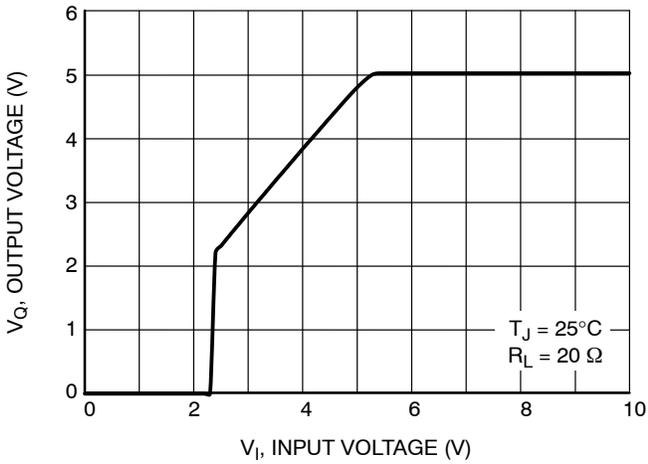


**Figure 6. Output Voltage vs. Input Voltage**
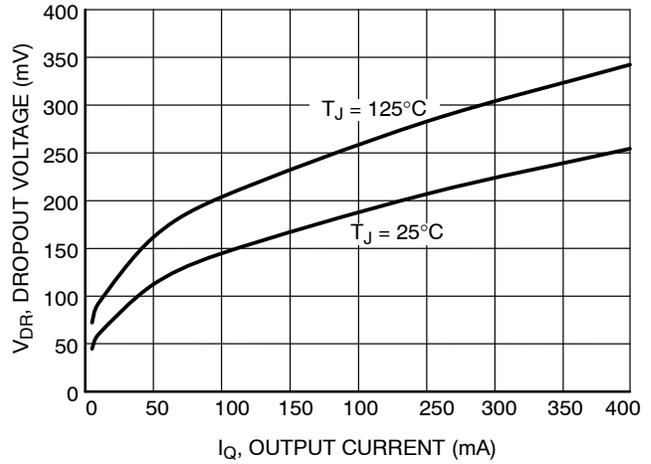


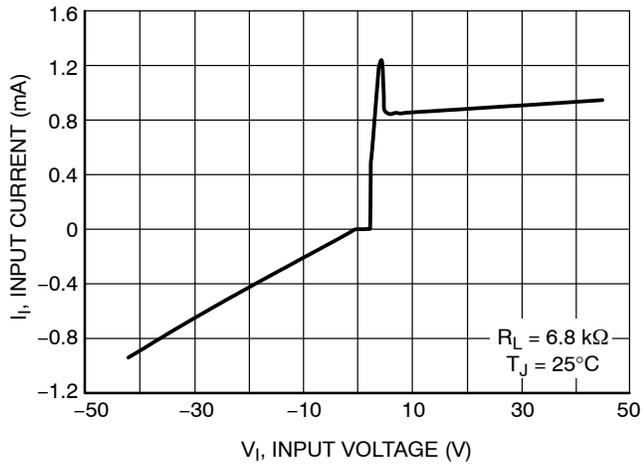**Figure 7. Dropout Voltage vs. Output Current**
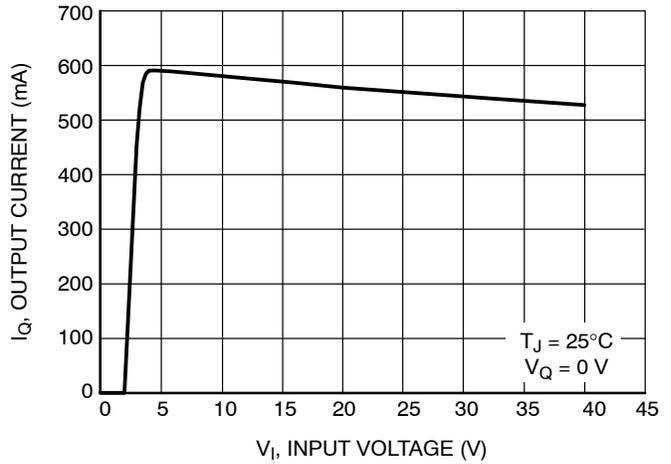


**Figure 8. Input Current vs. Input Voltage**



**Figure 9. Maximum Output Current vs. Input Voltage**
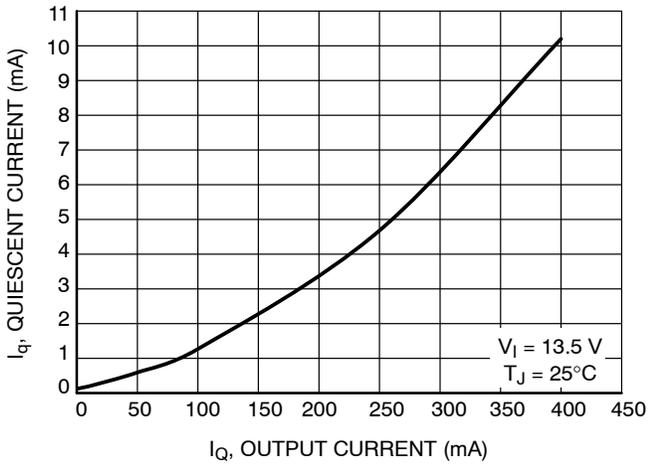
## TYPICAL CHARACTERISTIC CURVES – 5 V VERSION
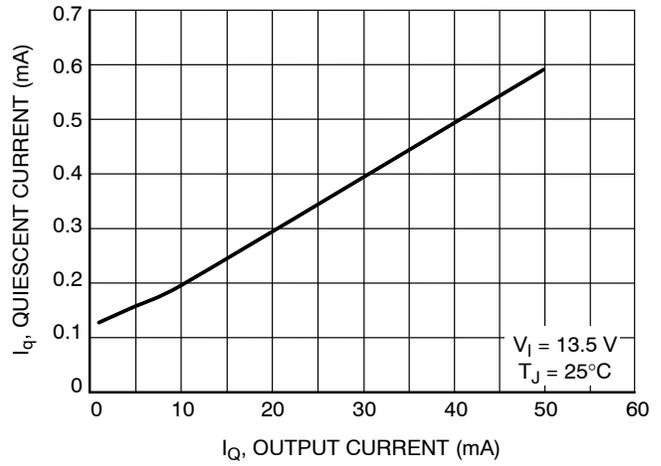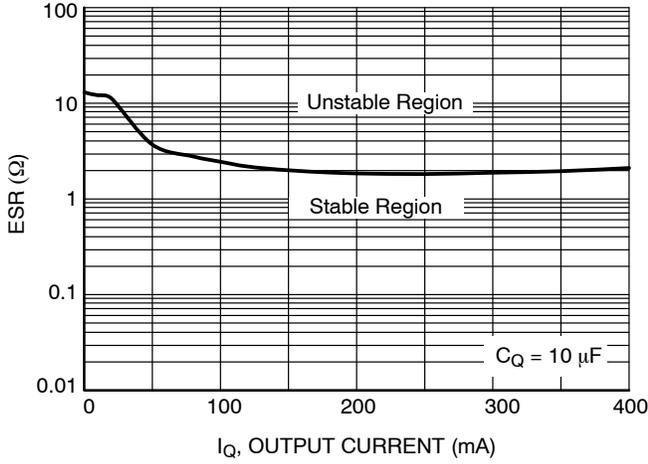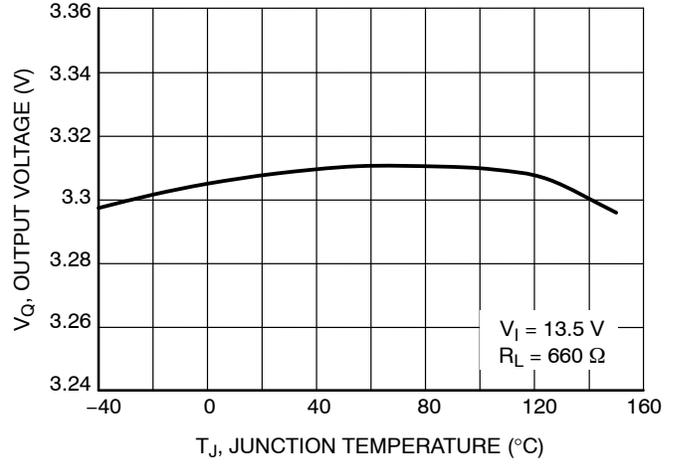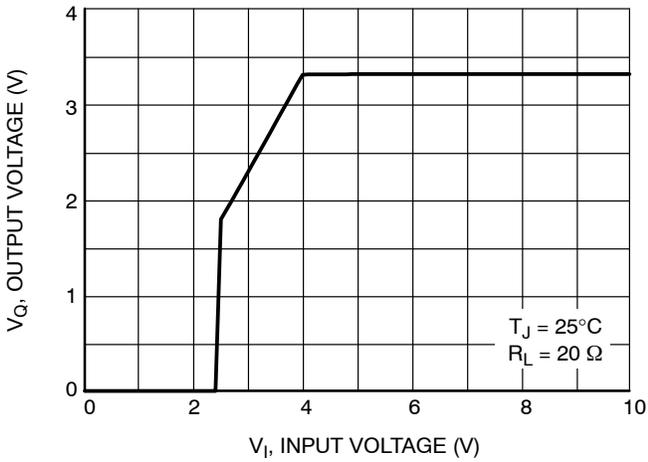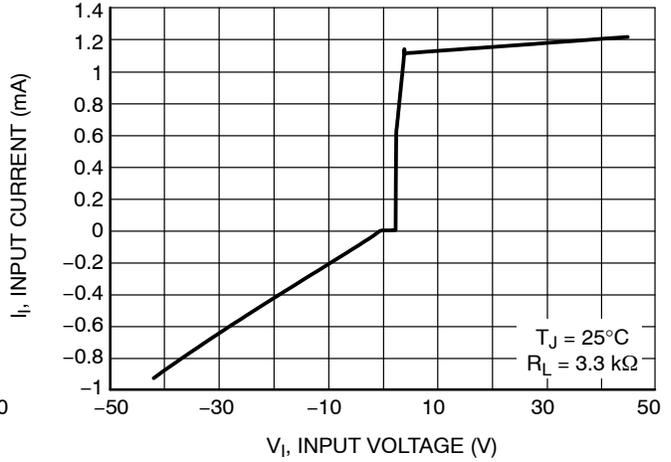
Figure 10. Quiescent Current vs.
Output Current (High Load)

Figure 11. Quiescent Current vs. Output
Current (Low Load)
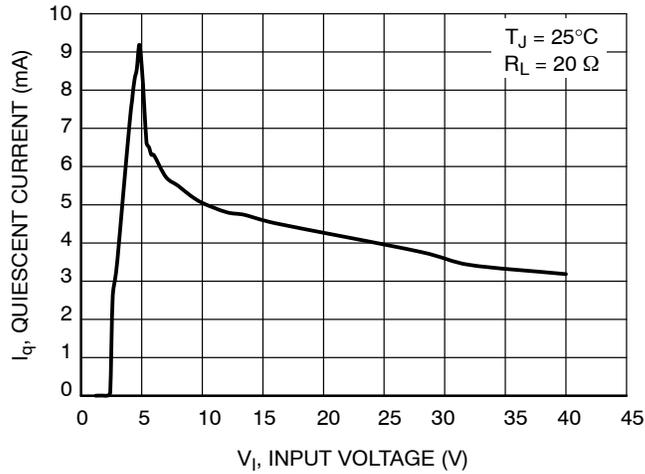
Figure 12. Quiescent Current vs. Input Voltage

## TYPICAL CHARACTERISTIC CURVES – 3.3 V VERSION



**Figure 13. Output Stability with Output Capacitor ESR**



**Figure 14. Output Voltage vs. Junction Temperature**



**Figure 15. Output Voltage vs. Input Voltage**



**Figure 16. Input Current vs. Input Voltage**
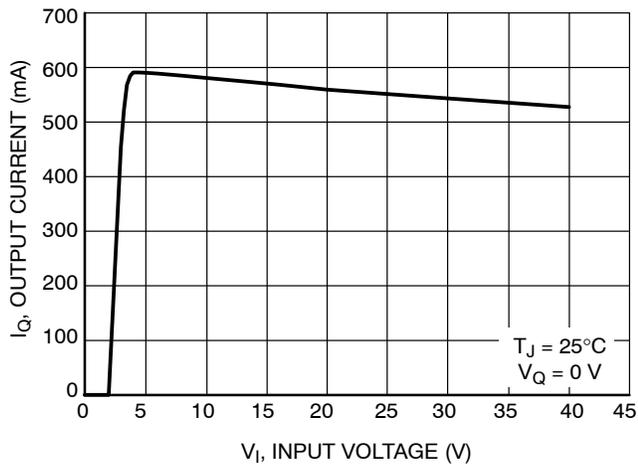


**Figure 17. Maximum Output Current vs. Input Voltage**
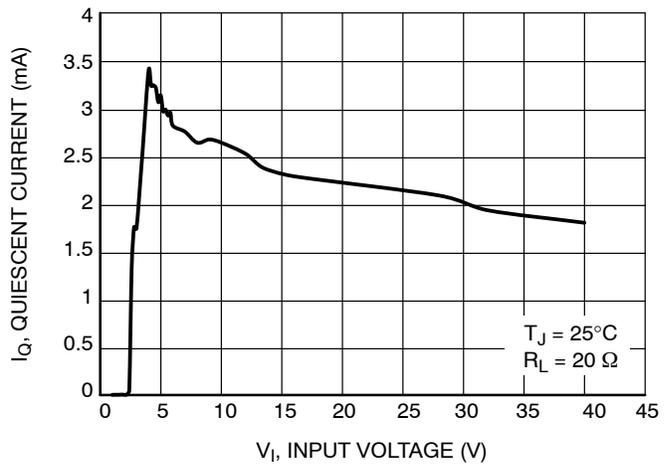


**Figure 18. Quiescent Current vs. Input Voltage**

## TYPICAL CHARACTERISTIC CURVES – 3.3 V VERSION
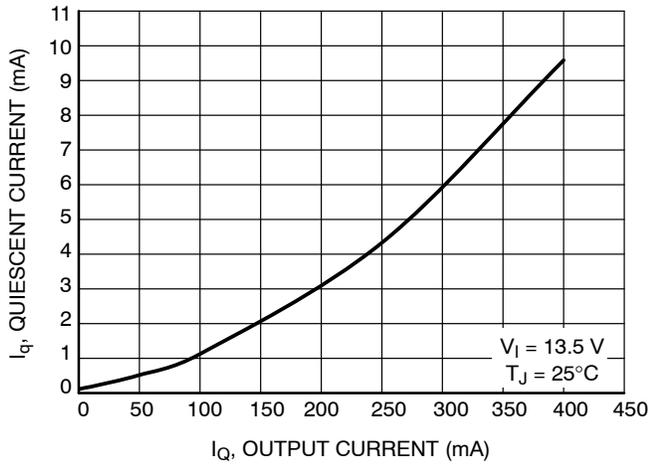


**Figure 19. Quiescent Current vs.
Output Current (High Load)**
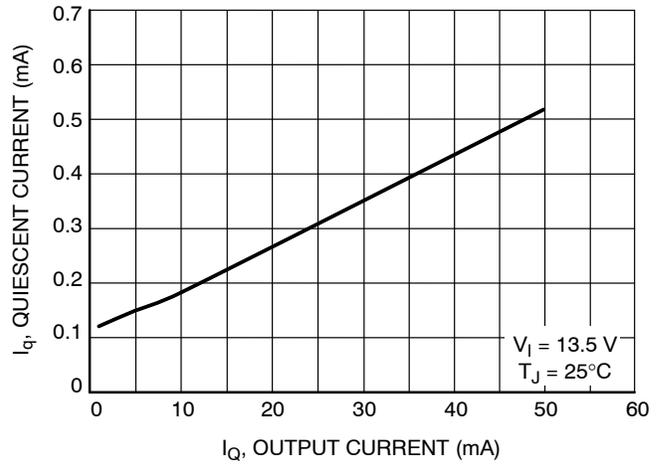


**Figure 20. Quiescent Current vs.
Output Current (Low Load)**

# NCV4274C

## APPLICATION DESCRIPTION

### Output Regulator

The output is controlled by a precision trimmed reference and error amplifier. The PNP output has saturation control for regulation while the input voltage is low, preventing over saturation. Current limit and voltage monitors complement the regulator design to give safe operating signals to the processor and control circuits.

### Stability Considerations

The input capacitor $C_{I1}$ in Figure 2 is necessary for compensating input line reactance. Possible oscillations caused by input inductance and input capacitance can be damped by using a resistor of approximately 1 Ω in series with $C_{I2.}$

The output or compensation capacitor helps determine three main characteristics of a linear regulator: startup delay, load transient response and loop stability.

The capacitor value and type should be based on cost, availability, size and temperature constraints. The aluminum electrolytic capacitor is the least expensive solution, but, if the circuit operates at low temperatures (−25°C to −40°C), both the value and ESR of the capacitor will vary considerably. The capacitor manufacturer's data sheet usually provides this information.

The value for the output capacitor $C_Q$ shown in Figure 2 should work for most applications; however, it is not necessarily the optimized solution. Actual Stability Regions are shown in a graphs in the Typical Performance Characteristics section.

### Calculating Power Dissipation in a Single Output Linear Regulator

The maximum power dissipation for a single output regulator (Figure 3) is:

$$P_{D(max)} = [V_{I(max)} - V_{Q(min)}]I_{Q(max)} + V_{I(max)}I_q \quad \text{(eq. 1)}$$

Where:
$V_{I(max)}$ is the maximum input voltage,
$V_{Q(min)}$ is the minimum output voltage,
$I_{Q(max)}$ is the maximum output current for the application, and
$I_q$ is the quiescent current the regulator consumes at $I_{Q(max)}$.

Once the value of $P_{D(max)}$ is known, the maximum permissible value of $R_{\theta JA}$ can be calculated:

$$P_{\theta_{JA}} = \frac{(150\,C - T_A)}{P_D} \quad \text{(eq. 2)}$$

The value of $R_{\theta JA}$ can then be compared with those in the package section of the data sheet. Those packages with $R_{\theta JA}$'s less than the calculated value in Equation 2 will keep the die temperature below 150°C. In some cases, none of the packages will be sufficient to dissipate the heat generated by the IC, and an external heat sink will be required. The current flow and voltages are shown in the Measurement Circuit Diagram.

### Heat Sinks

A heat sink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air.

Each material in the heat flow path between the IC and the outside environment will have a thermal resistance. Like series electrical resistances, these resistances are summed to determine the value of $R_{\theta JA}$:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CS} + R_{\theta SA} \quad \text{(eq. 3)}$$

Where:
$R_{\theta JC}$ = the junction−to−case thermal resistance,
$R_{\theta CS}$ = the case−to−heat sink thermal resistance, and
$R_{\theta SA}$ = the heat sink−to−ambient thermal resistance.

$R_{\theta JC}$ appears in the package section of the data sheet. Like $R_{\theta JA}$, it too is a function of package type. $R_{\theta CS}$ and $R_{\theta SA}$ are functions of the package type, heat sink and the interface between them. These values appear in data sheets of heat sink manufacturers.

Thermal, mounting, and heat sinking are discussed in the **onsemi** application note AN1040/D, available on the **onsemi** Website.
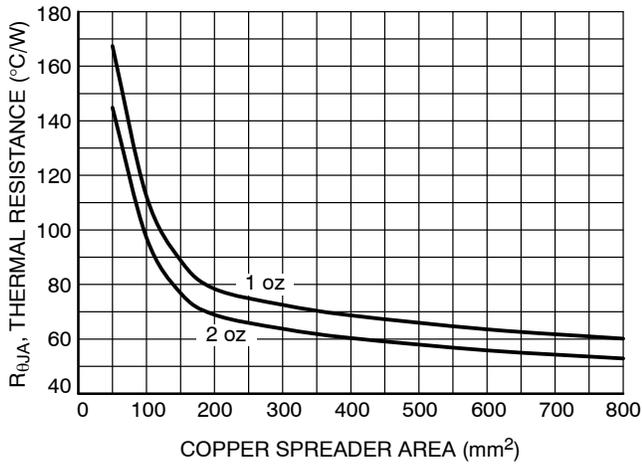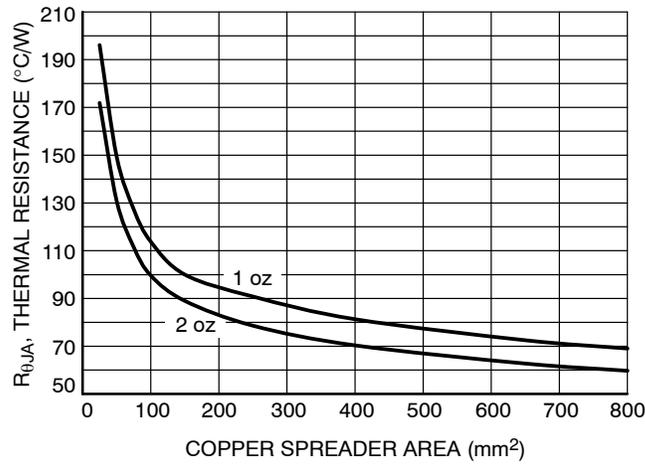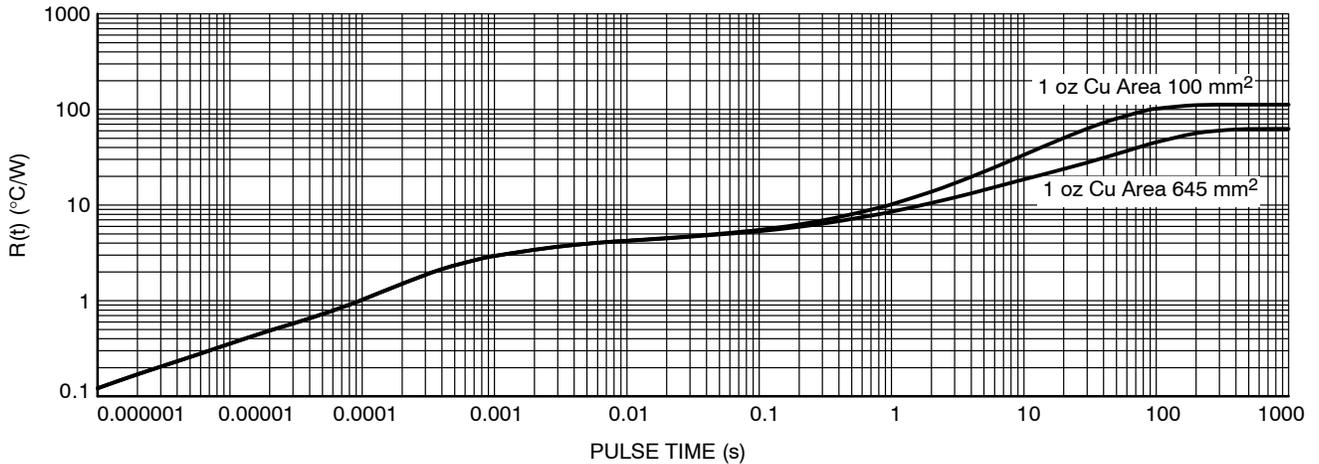
**Figure 21. R$_{\theta JA}$ vs. Copper Spreader Area,
DPAK 3−Lead**
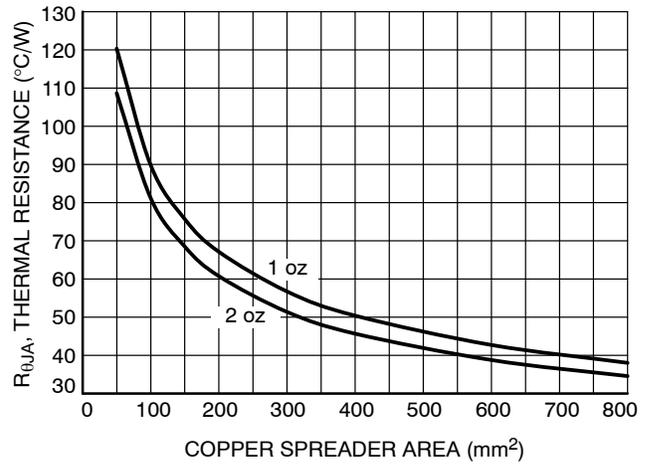


**Figure 22. R$_{\theta JA}$ vs. Copper Spreader Area,
D$^2$PAK 3−Lead**



**Figure 23. R$_{\theta JA}$ vs. Copper Spreader Area,
SOT 223−Lead**


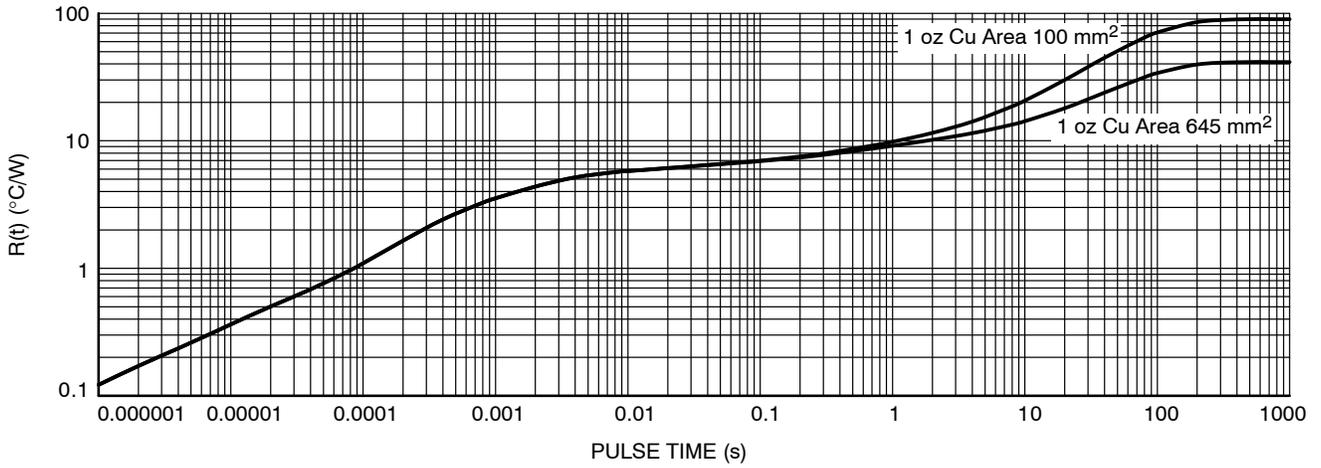
**Figure 24. Single−Pulse Heating Curves, DPAK 3−Lead**
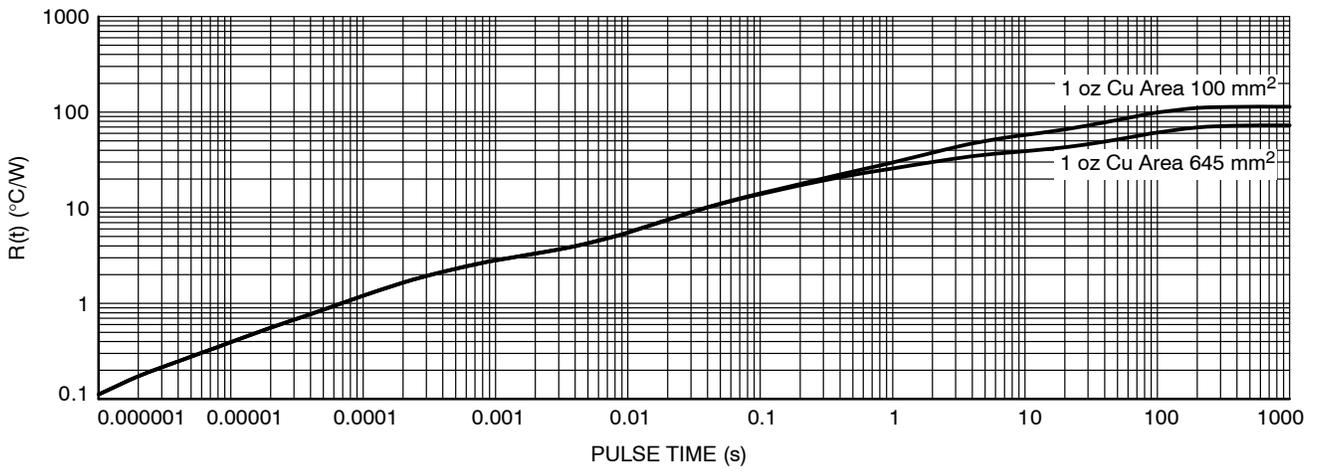
**Figure 25. Single−Pulse Heating Curves, D²PAK 3−Lead**
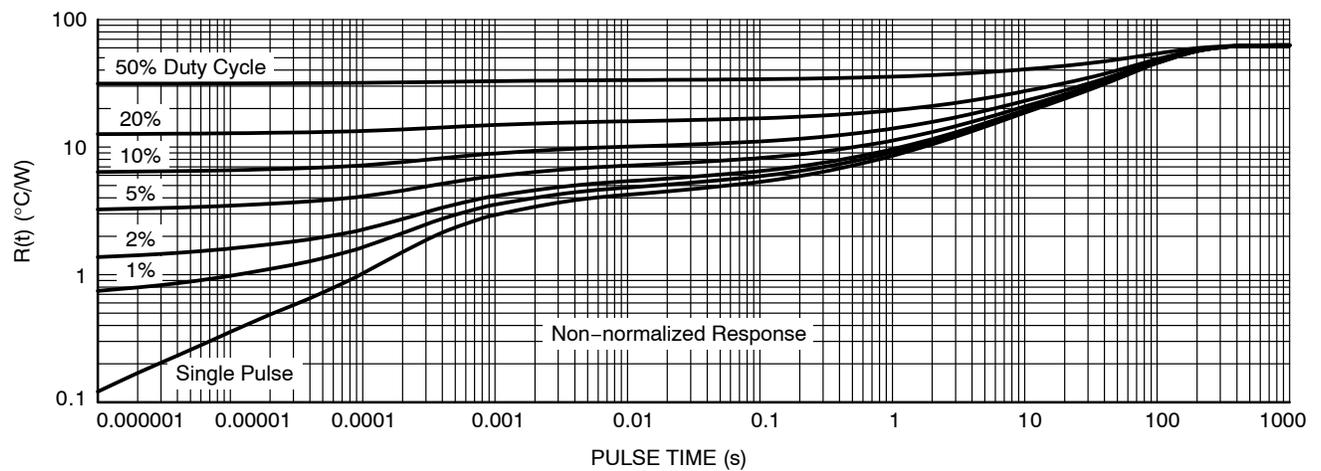


**Figure 26. Single−Pulse Heating Curves, SOT 223−Lead**



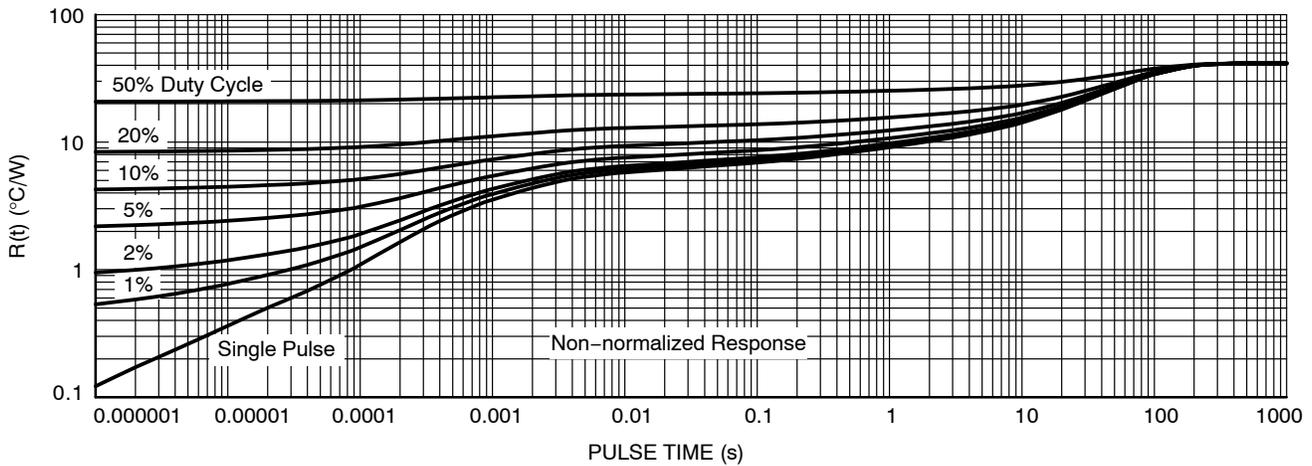**Figure 27. Duty Cycle for 1 inch² (645 mm²) Spreader Board, DPAK 3−Lead**

**Figure 28. Duty Cycle for 1 inch$^2$ (645 mm$^2$) Spreader Board, D$^2$PAK 3−Lead**
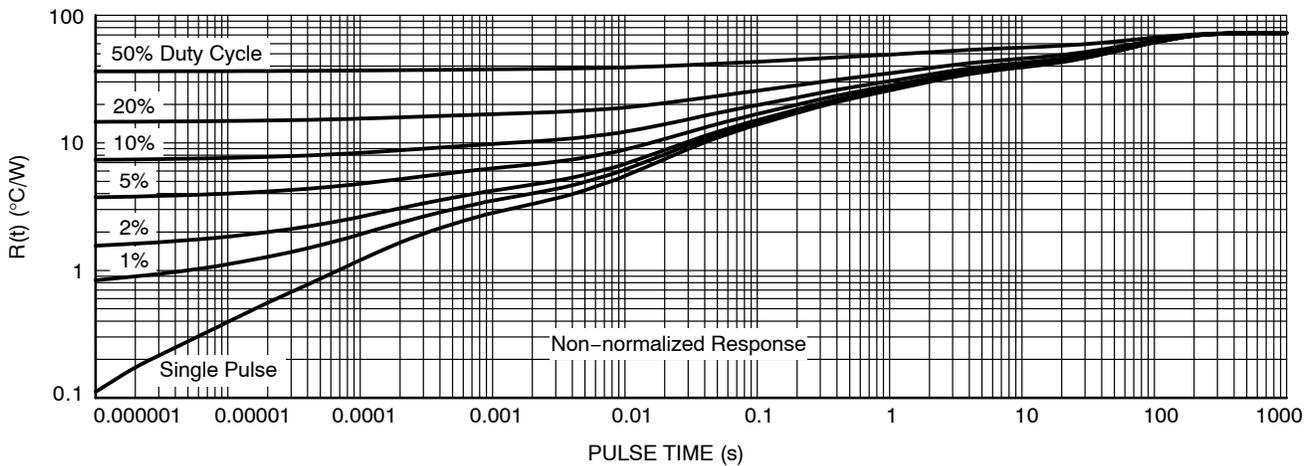


**Figure 29. Duty Cycle for 1 inch$^2$ (645 mm$^2$) Spreader Board, SOT 223−Lead**

## ORDERING INFORMATION

| Device* | Output Voltage Accuracy | Output Voltage | Package | Shipping[†] |
|---|---|---|---|---|
| NCV4274CDT33RKG | 2% | 3.3 V | DPAK (Pb−Free) | 2500 / Tape & Reel |
| NCV4274CDT50RKG | 2% | 5.0 V | DPAK (Pb−Free) | 2500 / Tape & Reel |
| NCV4274CST33T3G | 2% | 3.3 V | SOT−223 (Pb−Free) | 4000 / Tape & Reel |
| NCV4274CST50T3G | 2% | 5.0 V | SOT−223 (Pb−Free) | 4000 / Tape & Reel |

**DISCONTINUED** (Note 5)

| | | | | |
|---|---|---|---|---|
| NCV4274CDS33R4G | 2% | 3.3 V | D2PAK (Pb−Free) | 800 / Tape & Reel |
| NCV4274CDS50R4G | 2% | 5.0 V | D2PAK (Pb−Free) | 800 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.

5. **DISCONTINUED:** These devices are not recommended for new design. Please contact your **onsemi** representative for information. The most current information on these devices may be available on www.onsemi.com.

**SOT−223 (TO−261)**
CASE 318E−04
ISSUE R

DATE 02 OCT 2018

SCALE 1:1
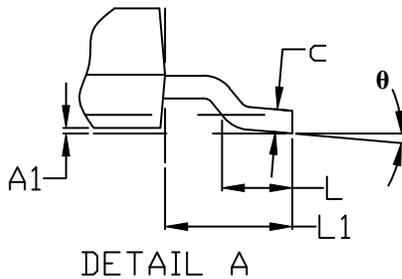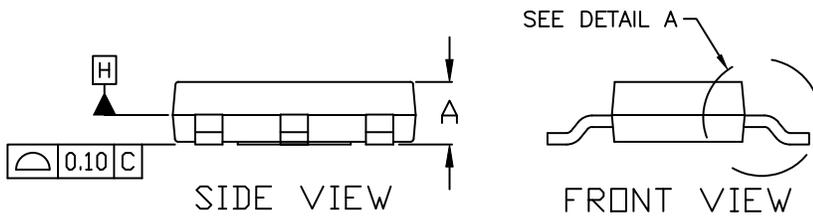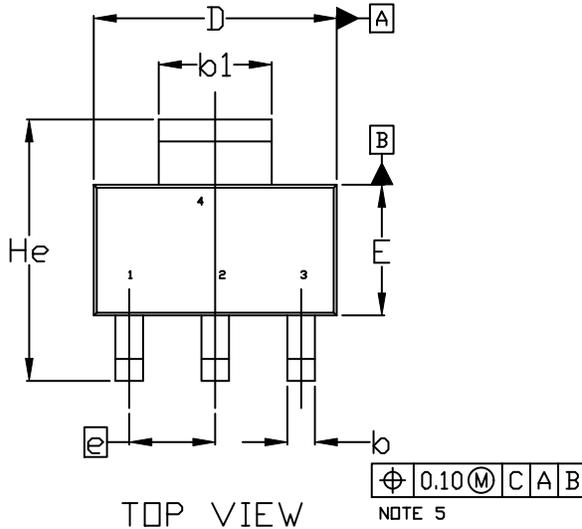
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D & E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.200MM PER SIDE.
4. DATUMS A AND B ARE DETERMINED AT DATUM H.
5. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
6. POSITIONAL TOLERANCE APPLIES TO DIMENSIONS b AND b1.

TOP VIEW

NOTE 5

SIDE VIEW

FRONT VIEW

SEE DETAIL A

DETAIL A

| DIM | MILLIMETERS | | |
|-----|------|------|------|
|     | MIN. | NOM. | MAX. |
| A   | 1.50 | 1.63 | 1.75 |
| A1  | 0.02 | 0.06 | 0.10 |
| b   | 0.60 | 0.75 | 0.89 |
| b1  | 2.90 | 3.06 | 3.20 |
| c   | 0.24 | 0.29 | 0.35 |
| D   | 6.30 | 6.50 | 6.70 |
| E   | 3.30 | 3.50 | 3.70 |
| e   | 2.30 BSC | | |
| L   | 0.20 | --- | --- |
| L1  | 1.50 | 1.75 | 2.00 |
| He  | 6.70 | 7.00 | 7.30 |
| θ   | 0° | --- | 10° |

3.80

2.00

6.30

3× 2.00

2.30 PITCH

3× 1.50

RECOMMENDED MOUNTING FOOTPRINT

| DOCUMENT NUMBER: | 98ASB42680B | | |
|---|---|---|---|
| DESCRIPTION: | SOT−223 (TO−261) | | PAGE 1 OF 2 |

## SOT−223 (TO−261)
### CASE 318E−04
### ISSUE R

DATE 02 OCT 2018

STYLE 1:
PIN 1. BASE
    2. COLLECTOR
    3. EMITTER
    4. COLLECTOR

STYLE 2:
PIN 1. ANODE
    2. CATHODE
    3. NC
    4. CATHODE

STYLE 3:
PIN 1. GATE
    2. DRAIN
    3. SOURCE
    4. DRAIN

STYLE 4:
PIN 1. SOURCE
    2. DRAIN
    3. GATE
    4. DRAIN

STYLE 5:
PIN 1. DRAIN
    2. GATE
    3. SOURCE
    4. GATE

STYLE 6:
PIN 1. RETURN
    2. INPUT
    3. OUTPUT
    4. INPUT

STYLE 7:
PIN 1. ANODE 1
    2. CATHODE
    3. ANODE 2
    4. CATHODE

STYLE 8:
    CANCELLED

STYLE 9:
PIN 1. INPUT
    2. GROUND
    3. LOGIC
    4. GROUND

STYLE 10:
PIN 1. CATHODE
    2. ANODE
    3. GATE
    4. ANODE

STYLE 11:
PIN 1. MT 1
    2. MT 2
    3. GATE
    4. MT 2

STYLE 12:
PIN 1. INPUT
    2. OUTPUT
    3. NC
    4. OUTPUT

STYLE 13:
PIN 1. GATE
    2. COLLECTOR
    3. EMITTER
    4. COLLECTOR

### GENERIC
### MARKING DIAGRAM*

```
      ┌────┐
   ┌──┴────┴──┐
   │  AYW     │
   │  XXXXX■  │
   │    ■     │
   └─┬──┬──┬──┘
  1  └┘ └┘ └┘
```
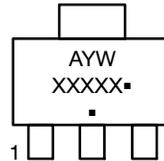
A     = Assembly Location
Y     = Year
W     = Work Week
XXXXX = Specific Device Code
■     = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to
device data sheet for actual part marking.
Pb−Free indicator, "G" or microdot "■", may
or may not be present. Some products may
not follow the Generic Marking.

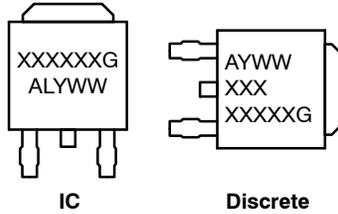| DOCUMENT NUMBER: | 98ASB42680B | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. | |
|---|---|---|---|
| DESCRIPTION: | SOT−223 (TO−261) | | PAGE 2 OF 2 |

**DPAK3 6.10x6.54x2.28, 2.29P**
CASE 369C
ISSUE H

DATE 15 JUL 2025

SCALE 1:1

TOP VIEW

SIDE VIEW

DETAIL A
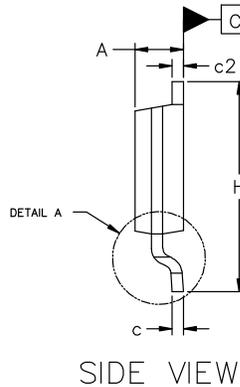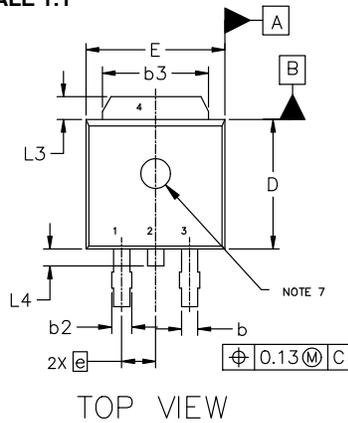
| MILLIMETERS | | | |
|------|------|------|------|
| DIM | MIN | NOM | MAX |
| A | 2.18 | 2.28 | 2.38 |
| A1 | 0.00 | ――― | 0.13 |
| b | 0.63 | 0.76 | 0.89 |
| b2 | 0.72 | 0.93 | 1.14 |
| b3 | 4.57 | 5.02 | 5.46 |
| c | 0.46 | 0.54 | 0.61 |
| c2 | 0.46 | 0.54 | 0.61 |
| D | 5.97 | 6.10 | 6.22 |
| E | 6.35 | 6.54 | 6.73 |
| e | 2.29 BSC | | |
| H | 9.40 | 9.91 | 10.41 |
| L | 1.40 | 10.10 | 1.78 |
| L1 | 2.90 REF | | |
| L2 | 0.51 BSC | | |
| L3 | 0.89 | ――― | 1.27 |
| L4 | ――― | ――― | 1.01 |
| Z | 3.93 | ――― | ――― |

BOTTOM VIEW
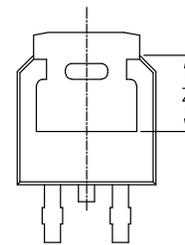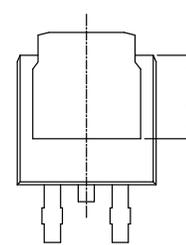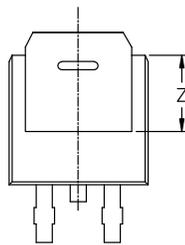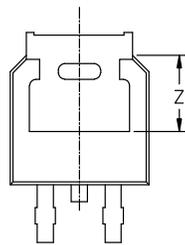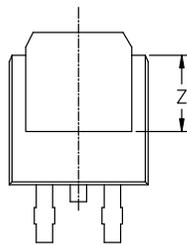
ALTERNATE CONSTRUCTIONS

NOTES:

1. DIMENSIONING AND TOLERANCING ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3, AND Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15mm PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. OPTIONAL MOLD FEATURE.

DETAIL A
ROTATED 90° CW

GAUGE PLANE

SEATING PLANE

RECOMMENDED MOUNTING FOOTPRINT*

5.80
6.20
2.58
1.60
3.00
6.17

*FOR ADDITIONAL INFORMATION ON OUR PB−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

| DOCUMENT NUMBER: | 98AON10527D | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. | |
|---|---|---|---|
| DESCRIPTION: | DPAK3 6.10x6.54x2.28, 2.29P | | PAGE 1 OF 2 |

**DPAK3 6.10x6.54x2.28, 2.29P**
CASE 369C
ISSUE H

**GENERIC
MARKING DIAGRAM\***



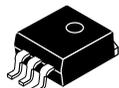| | |
|---|---|
| **IC** | **Discrete** |

XXXXXX = Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

\*This information is generic. Please refer to
device data sheet for actual part marking.
Pb−Free indicator, "G" or microdot "▪", may
or may not be present. Some products may
not follow the Generic Marking.

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

STYLE 4:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 5:
PIN 1. GATE
2. ANODE
3. CATHODE
4. ANODE

STYLE 6:
PIN 1. MT1
2. MT2
3. GATE
4. MT2

STYLE 7:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 8:
PIN 1. N/C
2. CATHODE
3. ANODE
4. CATHODE

STYLE 9:
PIN 1. ANODE
2. CATHODE
3. RESISTOR ADJUST
4. CATHODE

STYLE 10:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. ANODE

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|---|---|---|---|
| DESCRIPTION: | DPAK3 6.10x6.54x2.28, 2.29P | | PAGE 2 OF 2 |

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**onsemi**

**D2PAK**
CASE 418AF
ISSUE E

DATE 15 SEP 2015

SCALE 1:1
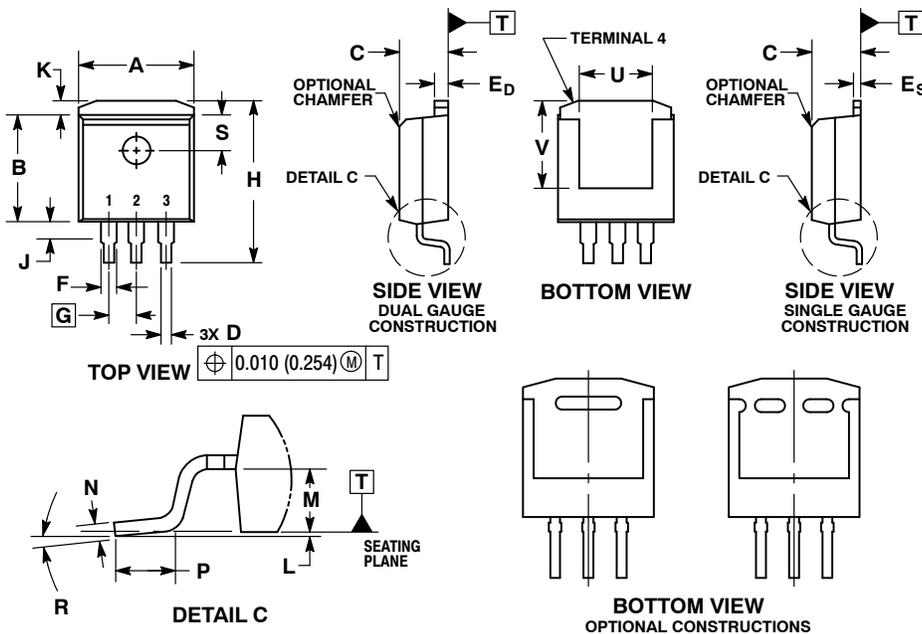
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCHES.
3. TAB CONTOUR OPTIONAL WITHIN DIMENSIONS A AND K.
4. DIMENSIONS U AND V ESTABLISH A MINIMUM MOUNTING SURFACE FOR TERMINAL 4.
5. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH OR GATE PROTRUSIONS. MOLD FLASH AND GATE PROTRUSIONS NOT TO EXCEED 0.025 (0.635) MAXIMUM.
6. SINGLE GAUGE DESIGN WILL BE SHIPPED AFTER FPCN EXPIRATION IN OCTOBER 2011.

TOP VIEW

SIDE VIEW
DUAL GAUGE CONSTRUCTION

BOTTOM VIEW

SIDE VIEW
SINGLE GAUGE CONSTRUCTION

DETAIL C

SEATING PLANE

BOTTOM VIEW
OPTIONAL CONSTRUCTIONS

| DIM | INCHES | | MILLIMETERS | |
|-----|--------|--------|-------------|--------|
|     | MIN | MAX | MIN | MAX |
| A | 0.386 | 0.403 | 9.804 | 10.236 |
| B | 0.356 | 0.368 | 9.042 | 9.347 |
| C | 0.170 | 0.180 | 4.318 | 4.572 |
| D | 0.026 | 0.036 | 0.660 | 0.914 |
| E_D | 0.045 | 0.055 | 1.143 | 1.397 |
| E_S | 0.018 | 0.026 | 0.457 | 0.660 |
| F | 0.051 REF | | 1.295 REF | |
| G | 0.100 BSC | | 2.540 BSC | |
| H | 0.539 | 0.579 | 13.691 | 14.707 |
| J | 0.125 MAX | | 3.175 MAX | |
| K | 0.050 REF | | 1.270 REF | |
| L | 0.000 | 0.010 | 0.000 | 0.254 |
| M | 0.088 | 0.102 | 2.235 | 2.591 |
| N | 0.018 | 0.026 | 0.457 | 0.660 |
| P | 0.058 | 0.078 | 1.473 | 1.981 |
| R | 0° | 8° | 0° | 8° |
| S | 0.116 REF | | 2.946 REF | |
| U | 0.200 MIN | | 5.080 MIN | |
| V | 0.250 MIN | | 6.350 MIN | |

## SOLDERING FOOTPRINT*
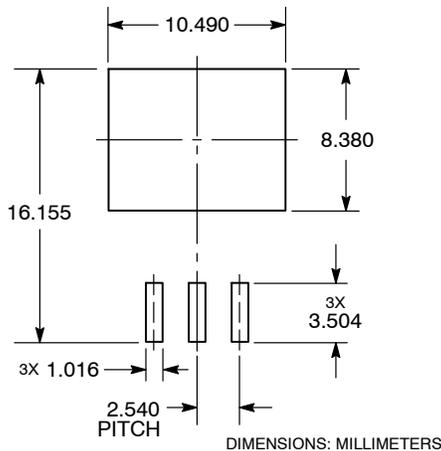
10.490

8.380

16.155

3X 3.504

3X 1.016

2.540 PITCH

DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## GENERIC
## MARKING DIAGRAM*

XX
XXXXXXXXX
AWLYYWWG
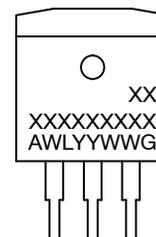
XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G", may or not be present.

| DOCUMENT NUMBER: | 98AON21981D | | |
|---|---|---|---|
| DESCRIPTION: | D2PAK | | PAGE 1 OF 1 |

## ADDITIONAL INFORMATION

**TECHNICAL PUBLICATIONS**:
**Technical Library:** www.onsemi.com/design/resources/technical–documentation
**onsemi Website:** www.onsemi.com

**ONLINE SUPPORT**: www.onsemi.com/support
**For additional information, please contact your local Sales Representative at**
www.onsemi.com/support/sales

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