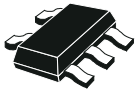
TS3121P

Datasheet

Rail-to-rail, open-drain comparator with embedded Power-on Reset (PoR)



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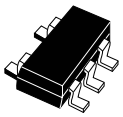


SOT23-5

Maturity status link
TS3121P

Related products	
TS880	For lower supply current
TS3011	For higher speed
TS3021	For push-pull output

Features

- AEC-Q100 qualified
- Low power consumption: 90 µA typ.
- Wide supply voltage: 1.7 to 5.5 V
- Propagation delay: 60 ns
- Rail-to-rail input
- Open-drain output
- Power-on Reset (PoR) allows sequential on/off cycles of V_{CC}
- High ESD tolerance: 4 kV HBM
- Extended temperature range: -40 to 125 °C
- Safety capable: Documentation available to aid functional safety system design

Applications

- Industrial
- Automotive
- Power tools
- Overcurrent protection
- Controllers, sensors

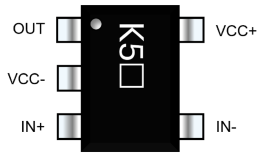
Description

The TS3121P single comparator permits high-speed response time at low power consumption over a supply voltage specified from 1.7 to 5.5 V. This device operates over a wide temperature range from -40 °C to +125 °C making it ideal for industrial and automotive applications with the associated qualification.

An embedded power-on reset circuit ensures a known output condition while activating the supply rail. Thanks to the small package size, the TS3121P can be used in applications where space on the board is limited. It can thus reduce the overall cost of the PCB.

1 Pin configuration

Figure 1. Pin connection (top view)



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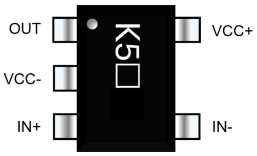
Dot or letter K denotes pin 1 position



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Dot or letter K denotes pin 1 position

Table 1. Pin description

Pin n°	Pin name	Description
1	OUT	Output
2	V_{CC-}	Negative supply voltage
3	IN +	Positive input voltage
4	IN -	Negative input voltage
5	V_{CC+}	Positive supply voltage

2 Maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter		Value	Unit
V_{CC}	Supply voltage (1)		6	V
V_{in}	Input voltage from V_{CC-}		-0.3 to V_{CC+} + 0.3	V
I_{in}	Input current (2)		10	mA
V_{out}	Output voltage		6	V
T_{stg}	Storage temperature		-65 to 150	°C
T_j	Junction temperature		150	°C
R_{th-ja}	Thermal resistance junction to ambient (3) (4)	SOT23-5	250	°C/W
		SC70-5	205	
ESD	Human Body Model (HBM) (5)		4000	V
	Charged Device Model (CDM) (6)		1500	

1. *All voltage values, except differential voltage, are with respect to network ground terminal.*
2. *Input current must be limited by a resistor in series with the inputs.*
3. *R_{th} are typical values.*
4. *Short-circuits can cause excessive heating and destructive dissipation.*
5. *According to JEDEC standard JESD22-A114F.*
6. *According to ANSI/ESD STM5.3.1.*

Table 3. Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	1.7 to 5.5	V
V_{in}	Common mode input voltage range	-0.2 to V_{CC+} + 0.2	V
V_{out}	Output voltage	0 to 5.5	V
T	Operating free-air temperature range	-40 to +125	°C

3 Electrical characteristics

Table 4. Electrical characteristics - V_{CC} = 5 V, V_{icm} = V_{CC}/2, T = 25 °C (unless otherwise specified).

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC performance						
V_{IO}	Input offset voltage	T = 25 °C Tmin < T < Tmax	-6 -8	0.5	6 8	mV
$\|\Delta V_{IO}/\Delta T\|$	Input offset voltage drift	Tmin < T < Tmax		3	20	µV/°C
V_{HYST}	Input hysteresis voltage (1)			1		mV
$\|I_{IB}\|$	Input bias current	T = 25 °C Tmin < T < Tmax		5	50 200	pA
$\|I_{IO}\|$	Input offset current	T = 25 °C Tmin < T < Tmax		1	20 100	
CMRR	Common mode rejection ratio: 20 log ($\Delta V_{icm}/\Delta V_{io}$)	0 < V_{icm} < V_{CC} Tmin < T < Tmax	 55	70		dB
SVR	Supply voltage rejection: 20 log ($\Delta V_{cc}/\Delta V_{io}$)	V_{icm} = 0 V, T = 25 °C V_{icm} = 0 V, Tmin < T < Tmax	 58	80		
I_{sink}	Output sink current	V_{OUT} = V_{CC+},V_{ID} = - 0.1 V Tmin < T < Tmax	100 70	140		mA
I_{OH}	High-level output leakage current, V_{OUT} = V_{CC} (2)	V_{OUT} = V_{CC}, V_{ID} = +0.1 V		460	800	pA
		Tmin < T < Tmax			250	nA
V_{OL}	Low-level output voltage I_{sink} = 1 mA	T = 25 °C Tmin< T < Tmax		18	30 45	mV
I_{CC}	Supply current	Output low, V_{ID} = - 0.1 V Tmin < T < Tmax		100	148 155	µA
		Output high, V_{ID} = +0.1 V Tmin < T < Tmax		80	148 155	
t_{PoR}	Power-on Reset	V_{CC} > 1.5 V		10	15	µs
t_{PLH} (3)	Propagation delay (low to high), C_L = 15 pF, overdrive = 20 mV, V_{PU} = V_{CC}	R_{PU} = 2.5 kΩ, T = 25 °C Tmin < T < Tmax		170	235 250	ns
	C_L = 15 pF, overdrive = 100 mV, V_{PU} = V_{CC}	R_{PU} = 2.5 kΩ, T = 25 °C Tmin < T < Tmax		130	160 185	
t_{PHL} (4)	Propagation delay (high to low), C_L = 15 pF, overdrive = 20 mV,V_{PU} = V_{CC}	R_{PU} = 2.5 kΩ, T = 25 °C Tmin < T < Tmax		100	135 185	
	C_L = 15 pF, overdrive = 100 mV, V_{PU} = V_{CC}	R_{PU} = 2.5 kΩ, T = 25 °C Tmin < T < Tmax		60	85 125	
t_F	Fall time (90% to 10%)	C_L = 15 pF, R_{PU} = 2.5 kΩ, overdrive = 100 mV		2.5		

1. *Hysteresis is a built-in feature. It is defined as the voltage difference between the trip points.*
2. *Maximum high-level output leakage current at T = 25 °C is guaranteed by design.*
3. *t_{PLH} is measured when the output signal crosses a voltage level at 50% of V_{CC} with the following conditions: inverting inputvoltage (IN-) = V_{ICM} and non-inverting input voltage (IN+) moving from V_{ICM} - 100 mV to V_{ICM} + overdrive.*

4. *t_{PHL} is measured when the output signal crosses a voltage level at 50% of V_{CC} with the following conditions: inverting inputvoltage (IN-) = V_{ICM} and non-inverting input voltage (IN+) moving from V_{ICM} + 100 mV to V_{ICM} - overdrive.*

Table 5. Electrical characteristics - V_{CC} = 3.3 V, V_{icm} = V_{CC}/2, T = 25 °C (unless otherwise specified).

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC performance						
V_{IO}	Input offset voltage	T = 25 °C Tmin < T < Tmax	-6 -8	0.5	6 8	mV
$\|\Delta V_{IO}/\Delta T\|$	Input offset voltage drift	Tmin < T < Tmax		3	20	µV/°C
V_{HYST}	Input hysteresis voltage (1)			1		mV
$\|I_{IB}\|$	Input bias current	T = 25 °C Tmin < T < Tmax		5	50 200	pA
$\|I_{IO}\|$	Input offset current	T = 25 °C Tmin < T < Tmax		1	20 100	pA
CMRR	Common mode rejection ratio: 20 log ($\Delta V_{icm}/\Delta V_{io}$)	0 < V_{icm} < V_{CC} Tmin < T < Tmax	50	70		dB
I_{sink}	Output sink current	V_{OUT} = V_{CC+},V_{ID} = - 0.1 V Tmin < T < Tmax	45 35	70		mA
I_{OH}	High-level output leakage current, V_{OUT} = V_{CC} (2)	V_{OUT} = V_{CC}, V_{ID} = +0.1 V		425	700	pA
		Tmin < T < Tmax			200	nA
V_{OL}	Low-level output voltage I_{sink} = 1 mA	T = 25 °C Tmin< T < Tmax		20	35 50	mV
I_{CC}	Supply current	Output low, V_{ID} = - 0.1 V Tmin < T < Tmax		85	148 155	µA
		Output high, V_{ID} = +0.1 V Tmin < T < Tmax		65	148 155	µA
t_{PoR}	Power-on Reset	V_{CC} > 1.5 V		10	15	µs
t_{PLH} (3)	Propagation delay (low to high), f = 1 kHz, C_L = 15 pF, overdrive = 20 mV, V_{PU} = V_{CC}	R_{PU} = 2.5 kΩ, T = 25 °C Tmin < T < Tmax		160	220 240	ns
	C_L = 15 pF, overdrive = 100 mV, V_{PU} = V_{CC}	R_{PU} = 2.5 kΩ, T = 25 °C Tmin < T < Tmax		130	160 175	ns
t_{PHL} (4)	Propagation delay (high to low), f = 1 kHz, C_L = 15 pF, overdrive = 20 mV,V_{PU} = V_{CC}	R_{PU} = 2.5 kΩ, T = 25 °C Tmin < T < Tmax		90	115 160	ns
	C_L = 15 pF, overdrive = 100 mV, V_{PU} = V_{CC}	R_{PU} = 2.5 kΩ, T = 25 °C Tmin < T < Tmax		60	85 125	ns
t_F	Fall time (90% to 10%)	C_L = 15 pF, R_{PU} = 2.5 kΩ, overdrive = 100 mV		3.5		ns

1. *Hysteresis is a built-in feature of the TS3121. It is defined as the voltage difference between the trip points.*
2. *Maximum high-level output leakage current at T = 25 °C is guaranteed by design.*
3. *t_{PLH} is measured when the output signal crosses a voltage level at 50% of V_{CC} with the following conditions: inverting inputvoltage (IN-) = V_{ICM} and non-inverting input voltage (IN+) moving from V_{ICM} - 100 mV to V_{ICM} + overdrive.*
4. *t_{PHL} is measured when the output signal crosses a voltage level at 50% of V_{CC} with the following conditions: inverting inputvoltage (IN-) = V_{ICM} and non-inverting input voltage (IN+) moving from V_{ICM} + 100 mV to V_{ICM} - overdrive*

Table 6. Electrical characteristics - V_{CC} = 1.8 V, V_{icm} = V_{CC}/2, T = 25 °C (unless otherwise specified).

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC performance						
V_{IO}	Input offset voltage	T = 25 °C Tmin < T < Tmax	-6 -8	0.5	6 8	mV
$\|\Delta V_{IO}/\Delta T\|$	Input offset voltage drift	Tmin < T < Tmax		3	20	µV/°C
V_{HYST}	Input hysteresis voltage (1)			1		mV
$\|I_{IB}\|$	Input bias current	T = 25 °C Tmin < T < Tmax		5	50 200	pA
$\|I_{IO}\|$	Input offset current	T = 25 °C Tmin < T < Tmax		1	20 100	pA
CMRR	Common mode rejection ratio: 20 log ($\Delta V_{icm}/\Delta V_{io}$)	0 < V_{icm} < V_{CC} Tmin < T < Tmax	50	70		dB
I_{sink}	Output sink current	V_{OUT} = V_{CC+}, V_{ID} = - 0.1 V Tmin < T < Tmax	11 9	18		mA
I_{OH}	High-level output leakage current, V_{OUT} = V_{CC} (2)	V_{OUT} = V_{CC}, V_{ID} = +0.1 V		193	700	pA
		Tmin < T < Tmax			200	nA
V_{OL}	Low-level output voltage I_{sink} = 1 mA	T = 25 °C Tmin< T < Tmax		36	60 80	mV
I_{CC}	Supply current	Output low, V_{ID} = - 0.1 V, V_{ICM} = 0 V Tmin < T < Tmax		75	148 155	µA
		Output high, V_{ID} = +0.1 V , V_{ICM} = 0 V Tmin < T < Tmax		55	148 155	µA
t_{PoR}	Power-on Reset	V_{CC} > 1.5 V		10	15	µs
t_{PLH} (3)	Propagation delay (low to high), C_L = 15 pF, overdrive = 20 mV, V_{PU} = V_{CC}	R_{PU} = 2.5 kΩ, T = 25 °C Tmin < T < Tmax		160	220 225	ns
	C_L = 15 pF, overdrive = 100 mV, V_{PU} = V_{CC}	R_{PU} = 2.5 kΩ, T = 25 °C Tmin < T < Tmax		130	160 175	ns
t_{PHL} (4)	Propagation delay (high to low), C_L = 15 pF, overdrive = 20 mV, V_{PU} = V_{CC}	R_{PU} = 2.5 kΩ, T = 25 °C Tmin < T < Tmax		90	115 165	ns
	C_L = 15 pF, overdrive = 100 mV, V_{PU} = V_{CC}	R_{PU} = 2.5 kΩ, T = 25 °C Tmin < T < Tmax		60	85 125	ns
t_F	Fall time (90% to 10%)	C_L = 15 pF, R_{PU} = 2.5 kΩ, overdrive = 100 mV		3.5		ns

1. *Hysteresis is a built-in feature of the TS3121. It is defined as the voltage difference between the trip points.*
2. *Maximum high-level output leakage current at T = 25 °C is guaranteed by design.*
3. *t_{PLH} is measured when the output signal crosses a voltage level at 50% of V_{CC} with the following conditions: inverting inputvoltage (IN-) = V_{ICM} and non-inverting input voltage (IN+) moving from V_{ICM} - 100 mV to V_{ICM} + overdrive.*
4. *t_{PHL} is measured when the output signal crosses a voltage level at 50% of V_{CC} with the following conditions: inverting inputvoltage (IN-) = V_{ICM} and non-inverting input voltage (IN+) moving from V_{ICM} + 100 mV to V_{ICM} - overdrive.*

4 Typical performance characteristics

Figure 2. Supply current vs. supply voltage at $V_{icm} = V_{CC}$, output high

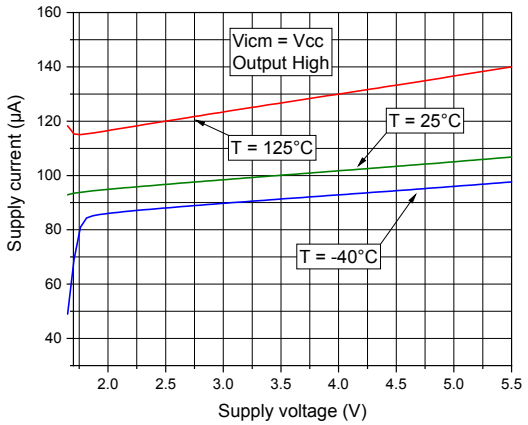


Figure 3. Supply current vs. supply voltage at $V_{icm} = V_{CC}/2$, output high

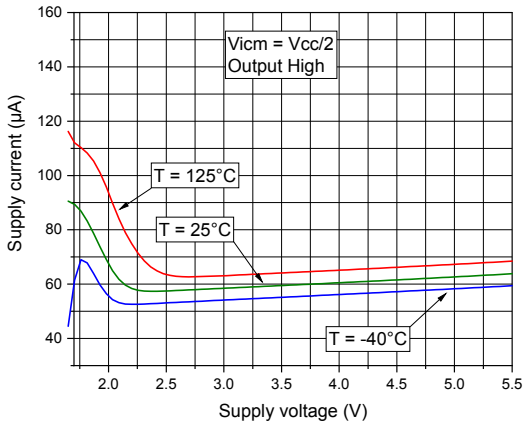


Figure 4. Supply current vs. supply voltage at $V_{icm} = V_{CC}$-, output high

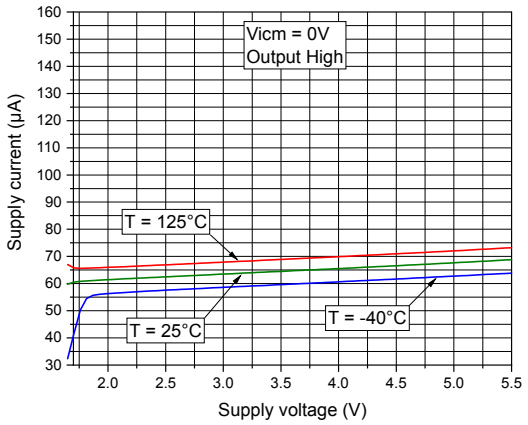


Figure 5. Supply current vs. supply voltage at $V_{icm} = V_{CC}$, output high

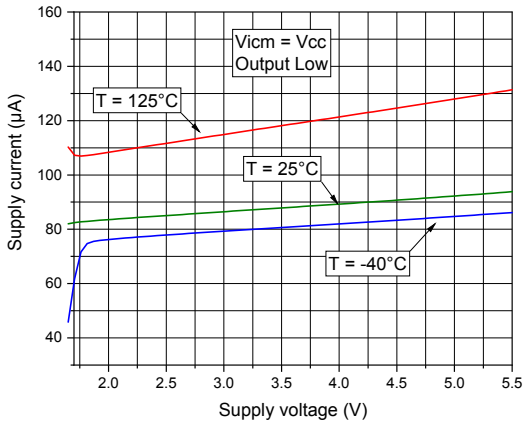


Figure 6. Supply current vs. supply voltage at $V_{icm} = V_{CC}/2$, output low

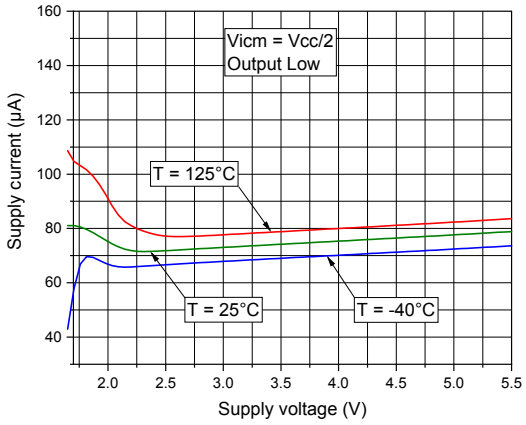


Figure 7. Supply current vs. supply voltage at $V_{icm} = V_{CC}$-, output low

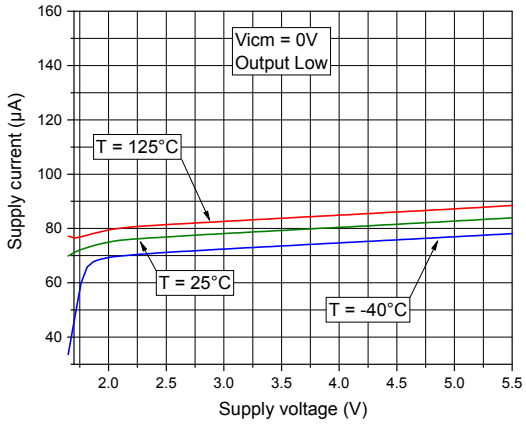


Figure 8. Supply current vs. input common-mode voltage at V_{CC} = 1.8 V, output high

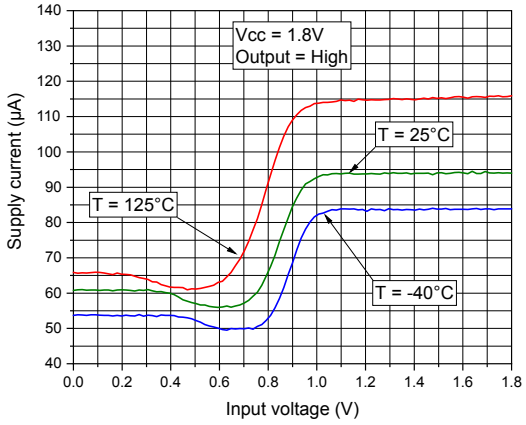


Figure 9. Supply current vs. input common-mode voltage at V_{CC} = 3.3 V, output high

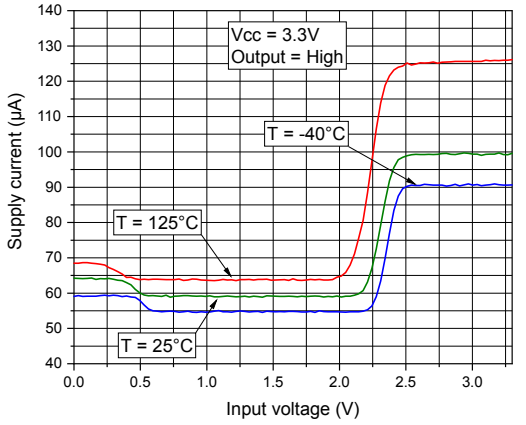


Figure 10. Supply current vs. input common-mode voltage at V_{CC} = 5.0 V, output high

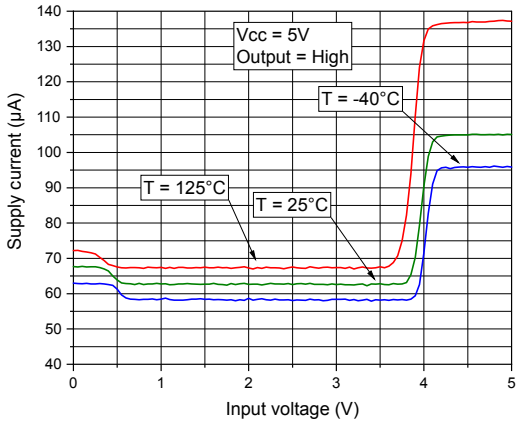


Figure 11. Input bias current vs. input common-mode voltage at V_{CC} = 1.8 V

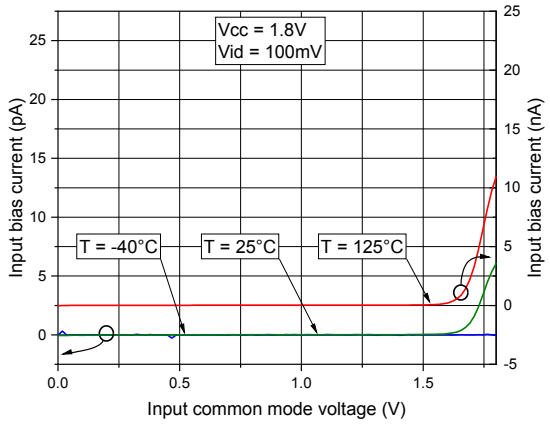


Figure 12. Input bias current vs. input common-mode voltage at V_{CC} = 3.3 V

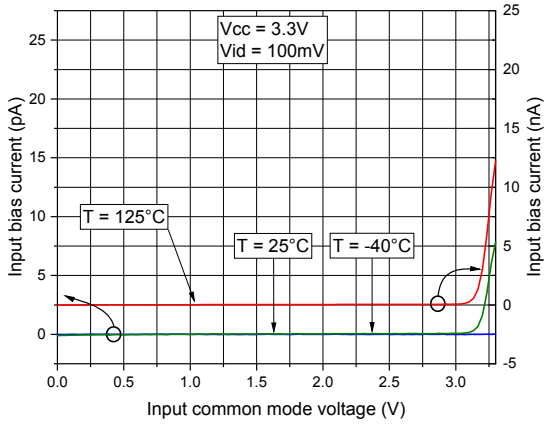


Figure 13. Input bias current vs. input common-mode voltage at V_{CC} = 5.0 V

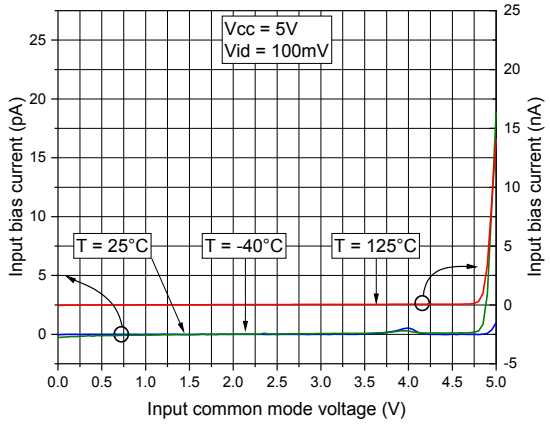


Figure 14. Input bias current vs. supply voltage at $V_{icm} = V_{CC}/2$

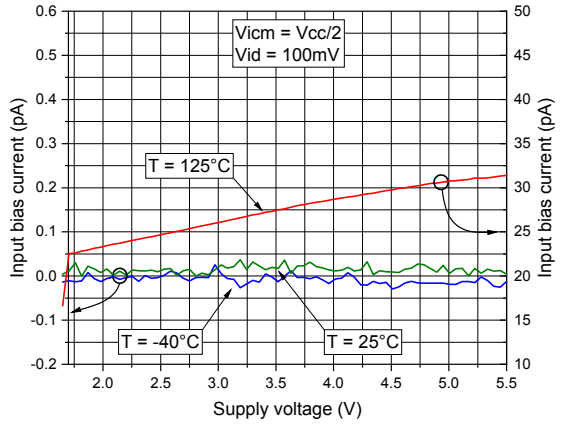


Figure 15. Input offset voltage vs. input common-mode voltage at V_{CC} = 1.8 V

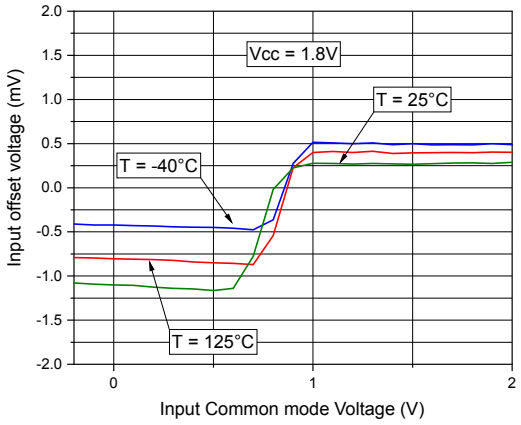


Figure 16. Input offset voltage vs. input common-mode voltage at V_{CC} = 3.3 V

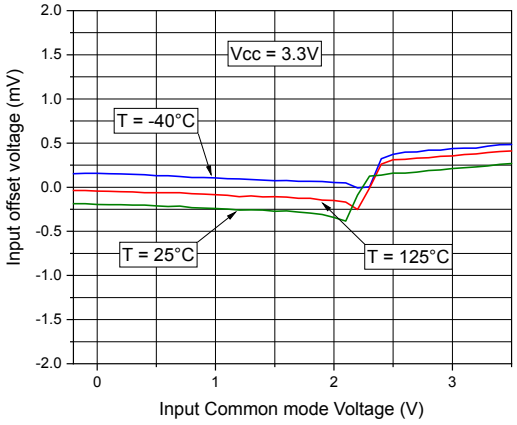


Figure 17. Input offset voltage vs. input common-mode voltage at V_{CC} = 5.0 V

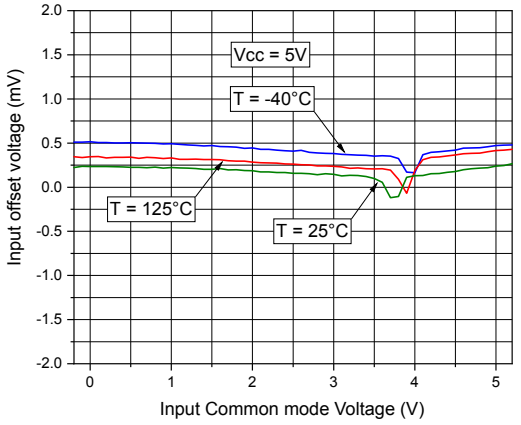


Figure 18. Input offset voltage vs. supply voltage at $V_{icm} = V_{CC}$-

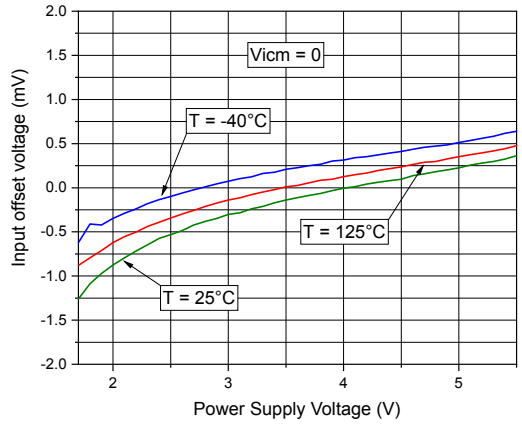


Figure 19. Input offset voltage vs. supply voltage at $V_{icm} = V_{CC}/2$

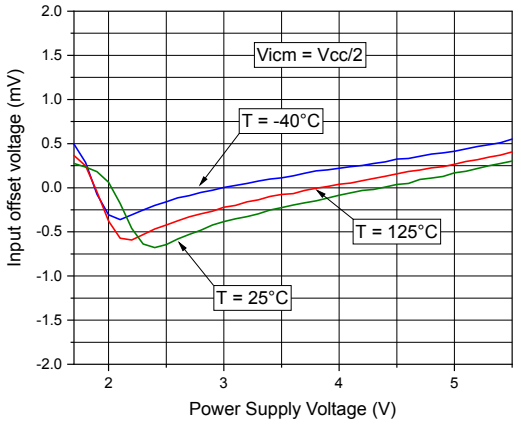


Figure 20. Input offset voltage vs. supply voltage at $V_{icm} = V_{CC}$

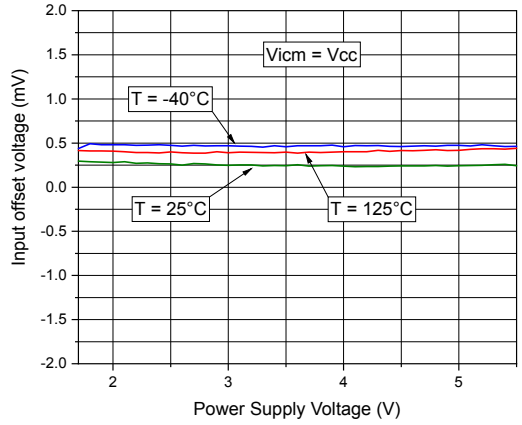


Figure 21. Input offset voltage drift vs. temperature from -40 °C to +25 °C

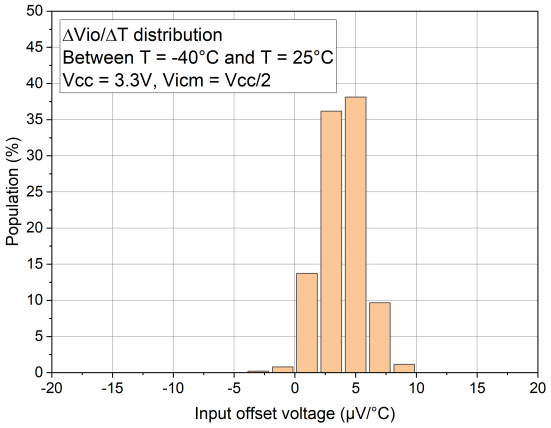


Figure 22. Input offset voltage drift vs. temperature from -25 °C to +125 °C

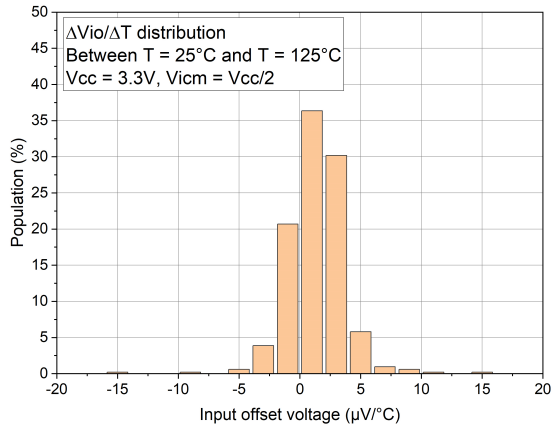


Figure 23. Input offset voltage vs. temperature at V_{CC} = 1.8 V

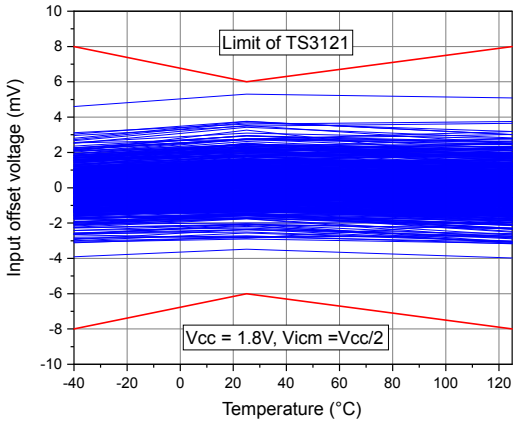


Figure 24. Input offset voltage vs. temperature at V_{CC} = 5.0 V

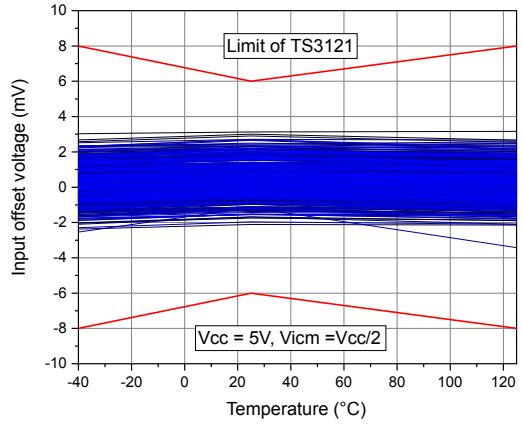


Figure 25. Input offset voltage distribution at V_{CC} = 1.8 V

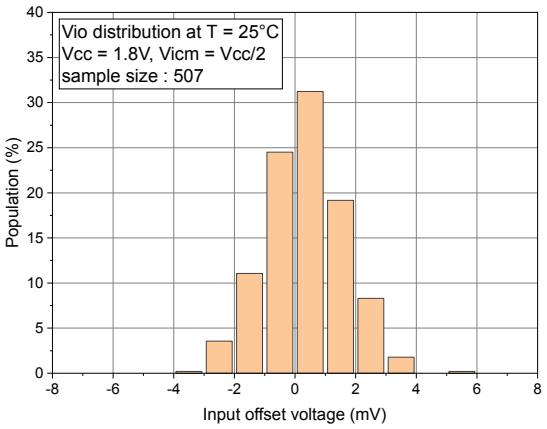


Figure 26. Input offset voltage distribution at V_{CC} = 3.3 V

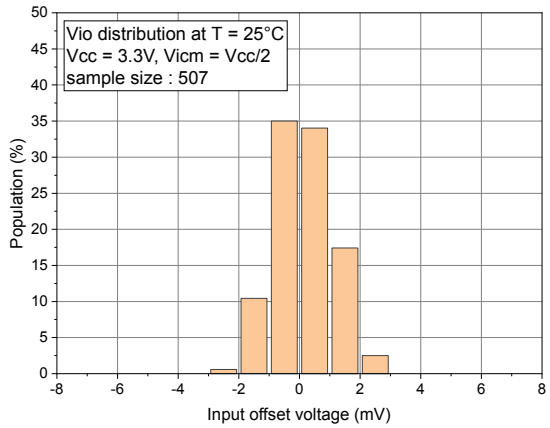


Figure 27. Input offset voltage distribution at V_{CC} = 5.0 V

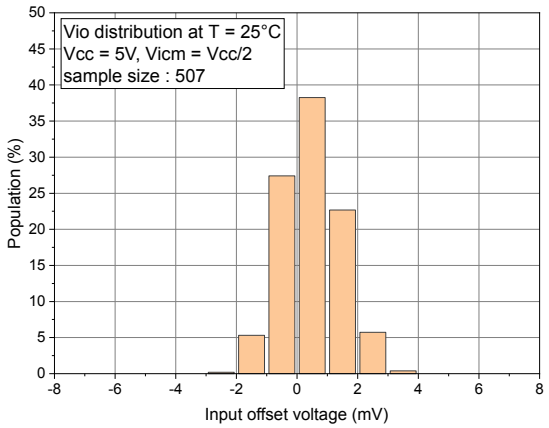


Figure 28. Output drop voltage vs. output sink current at V_{CC} = 1.8 V

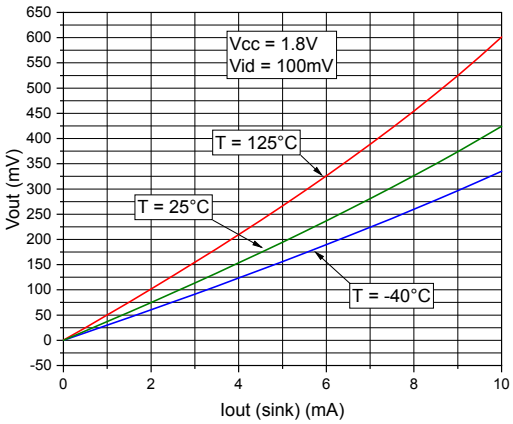


Figure 29. Output drop voltage vs. output sink current at V_{CC} = 3.3 V

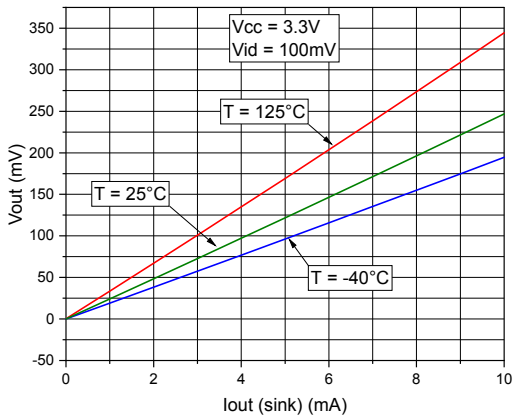


Figure 30. Output drop voltage vs. output sink current at V_{CC} = 5.0 V

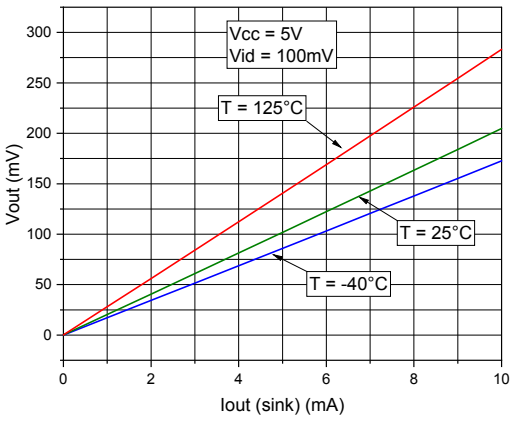


Figure 31. High-level output leakage current vs. output voltage at V_{CC} = 1.8 V

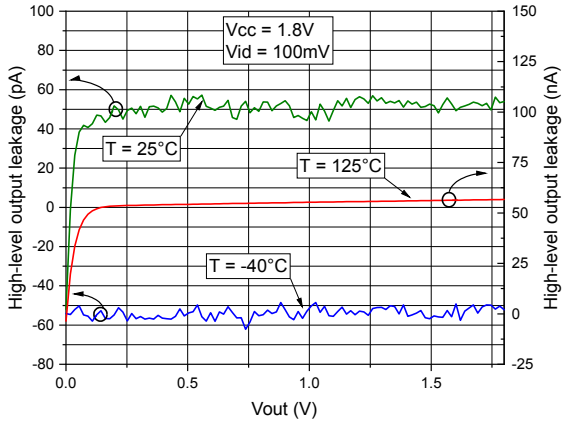


Figure 32. High-level output leakage current vs. output voltage at V_{CC} = 5.0 V

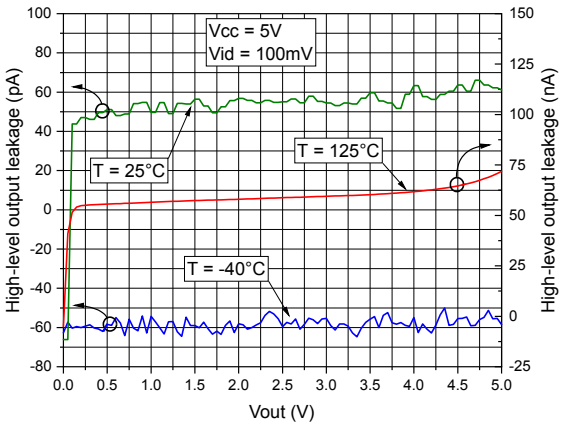


Figure 33. High-to-low propagation delay vs. overdrive at V_{CC} = 1.8 V, C_L = 15 pF, R_{PU} = 2.5 kΩ, V_{PU} = V_{CC}

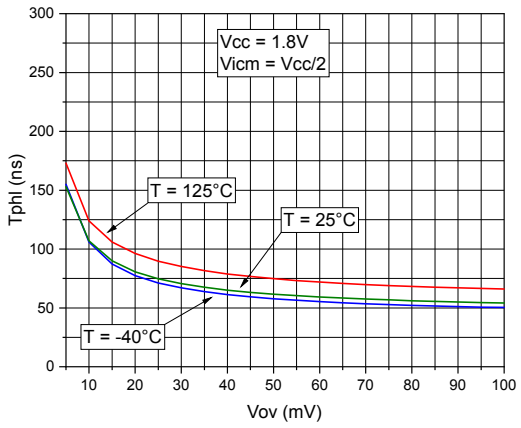


Figure 34. High-to-low propagation delay vs. overdrive at V_{CC} = 3.3 V, C_L = 15 pF, R_{PU} = 2.5 kΩ, V_{PU} = V_{CC}

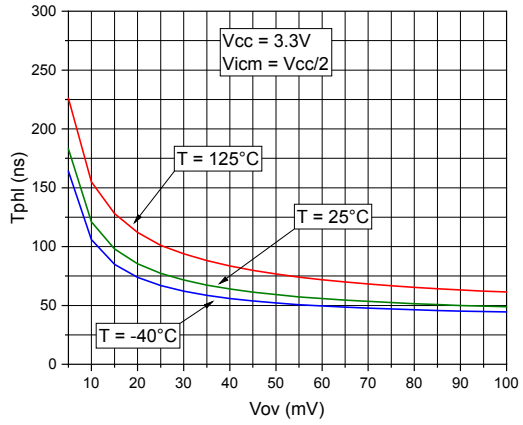


Figure 35. High-to-low propagation delay vs. overdrive at V_{CC} = 5.0 V, C_L = 15 pF, R_{PU} = 2.5 kΩ, V_{PU} = V_{CC}

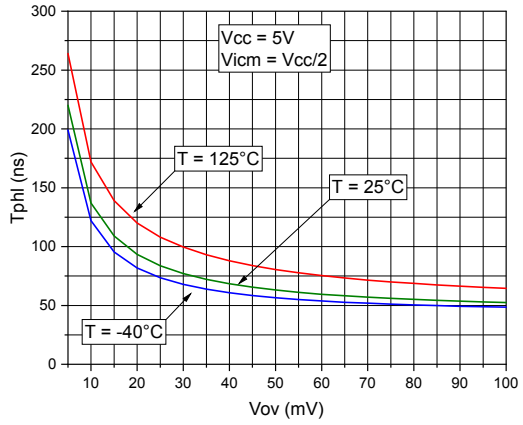


Figure 36. Low-to-high propagation delay vs. overdrive at V_{CC} = 1.8 V, C_L = 15 pF, R_{PU} = 2.5 kΩ, V_{PU} = V_{CC}

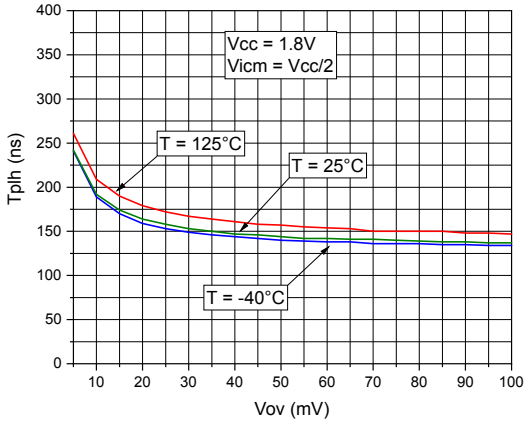


Figure 37. Low-to-high propagation delay vs. overdrive at V_{CC} = 3.3 V, C_L = 15 pF, R_{PU} = 2.5 kΩ, V_{PU} = V_{CC}

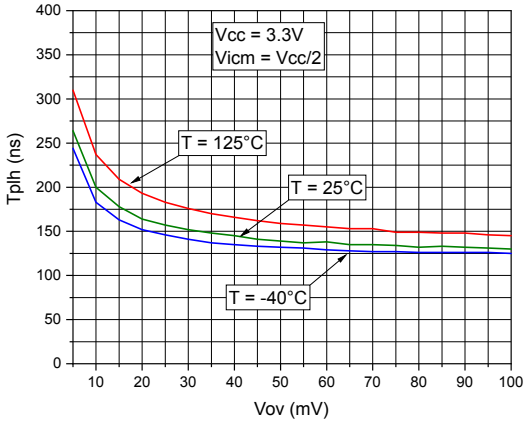


Figure 38. Low-to-high propagation delay vs. overdrive at V_{CC} = 5.0 V, C_L = 15 pF, R_{PU} = 2.5 kΩ, V_{PU} = V_{CC}

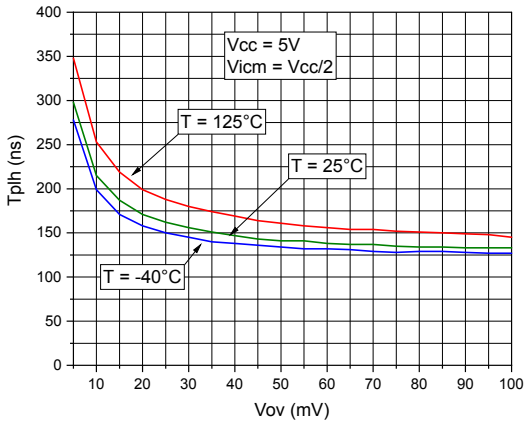


Figure 39. Low-to-high propagation delay vs. input common-mode voltage at V_{CC} = 1.8 V, C_L = 15 pF, R_{PU} = 2.5 kΩ, V_{PU} = V_{CC}

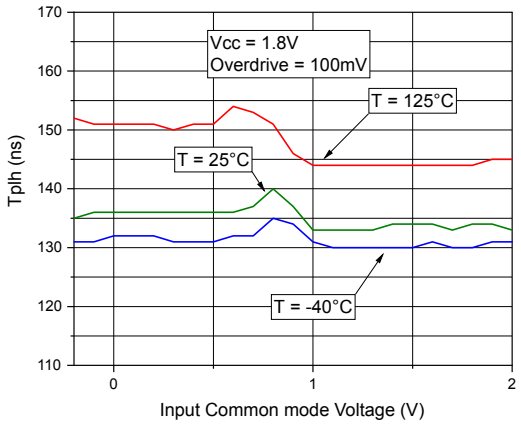


Figure 40. Low-to-high propagation delay vs. input common-mode voltage at V_{CC} = 3.3 V, C_L = 15 pF, R_{PU} = 2.5 kΩ, V_{PU} = V_{CC}

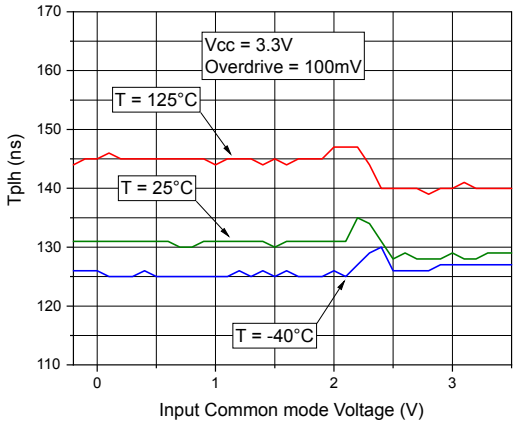


Figure 41. Low-to-high propagation delay vs. input common-mode voltage at V_{CC} = 5.0 V, C_L = 15 pF, R_{PU} = 2.5 kΩ, V_{PU} = V_{CC}

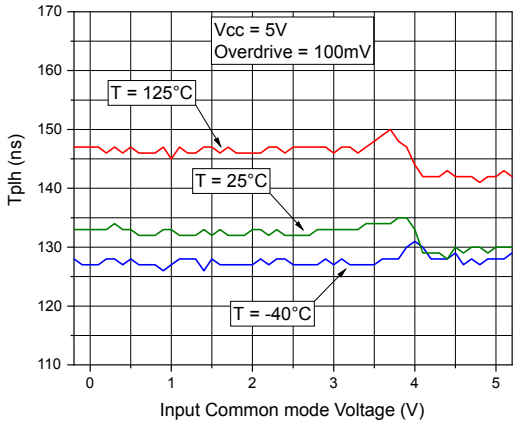


Figure 42. Low-to-high propagation delay vs. supply voltage at V_{icm} = V_{CC}/2, C_L = 15 pF, R_{PU} = 2.5 kΩ, V_{PU} = V_{CC}

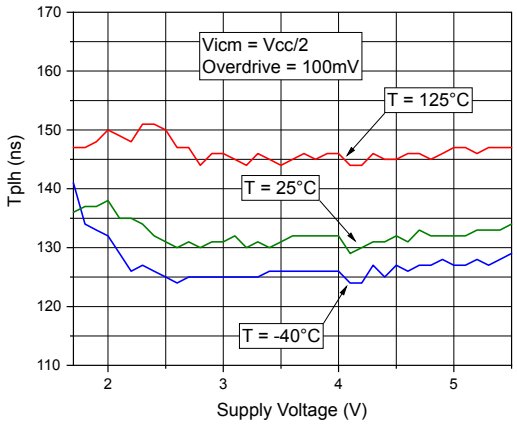


Figure 43. High-to-low propagation delay vs. input common-mode voltage at V_{CC} = 1.8 V, C_L = 15 pF, R_{PU} = 2.5 kΩ, V_{PU} = V_{CC}

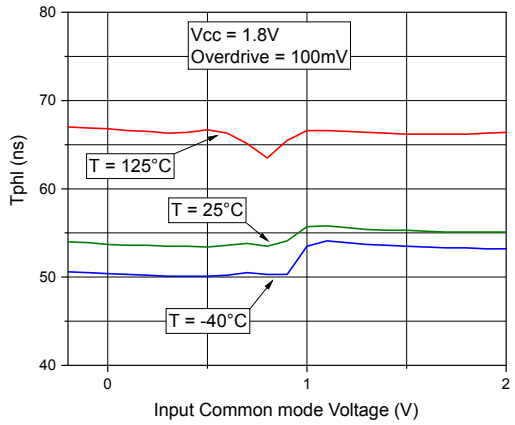


Figure 44. High-to-low propagation delay vs. input common-mode voltage at V_{CC} = 3.3 V, C_L = 15 pF, R_{PU} = 2.5 kΩ, V_{PU} = V_{CC}

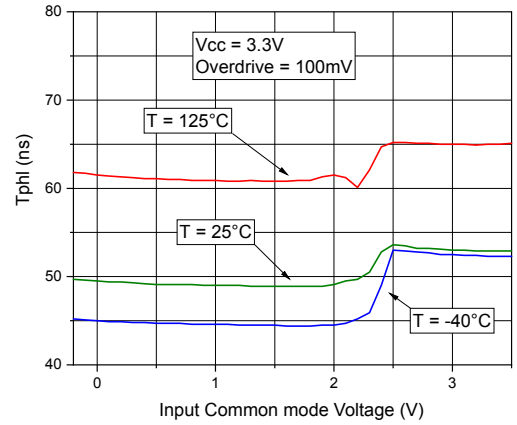


Figure 45. High-to-low propagation delay vs. input common-mode voltage at V_{CC} = 5.0 V, C_L = 15 pF, R_{PU} = 2.5 kΩ, V_{PU} = V_{CC}

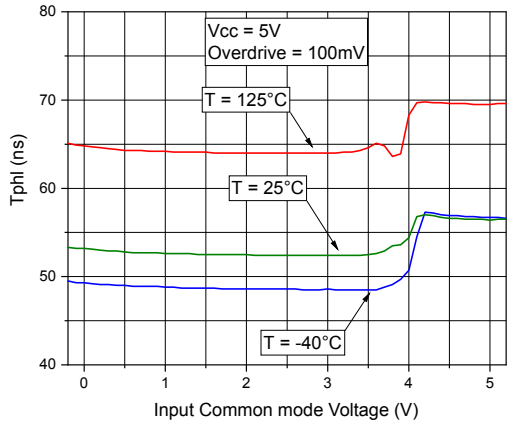


Figure 46. High-to-low propagation delay vs. supply voltage at V_{icm} = V_{CC}/2, C_L = 15 pF, R_{PU} = 2.5 kΩ, V_{PU} = V_{CC}

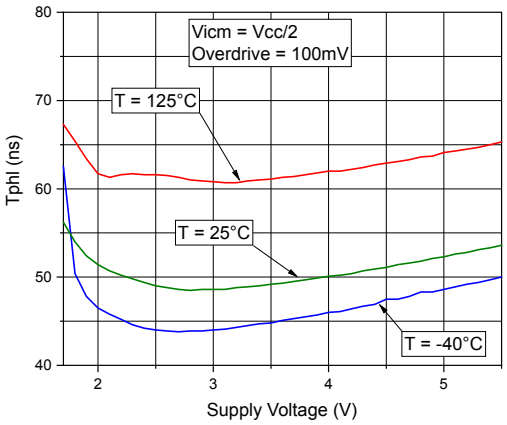


Figure 47. Power-on Reset output sequence V_{CC} = 1.8 V, R_{PU} = 2.5 kΩ, V_{PU} = V_{CC}

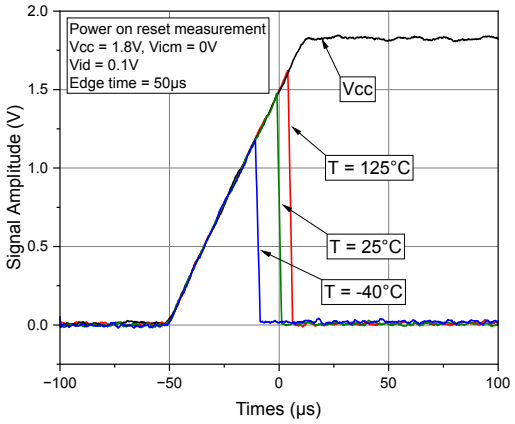


Figure 48. Power-on Reset output sequence V_{CC} = 3.3 V, R_{PU} = 2.5 kΩ, V_{PU} = V_{CC}

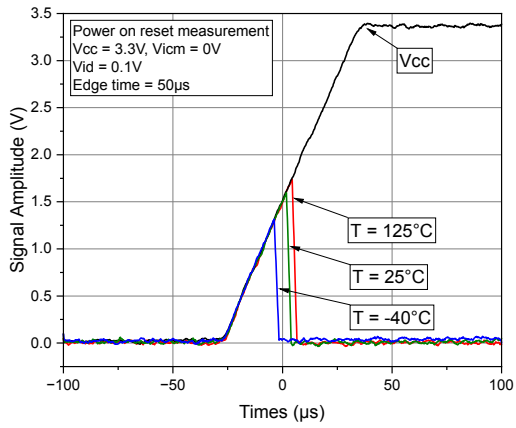
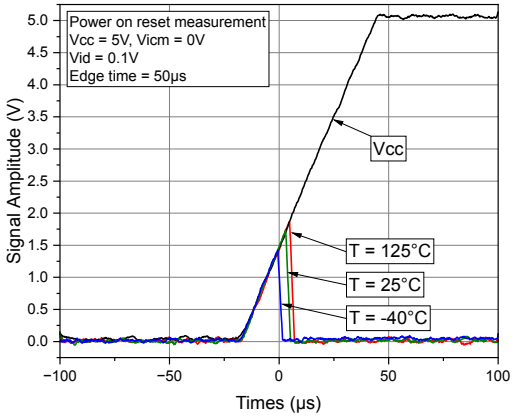


Figure 49. Power-on Reset output sequence V_{CC} = 5.0 V, R_{PU} = 2.5 kΩ, V_{PU} = V_{CC}



5 Application information

Operating voltages

The TS3121P can operate from 1.7 V to 5.5 V and parameters are fully specified at 1.8 V, 3.3 V, and 5 V. The specifications are guaranteed in the extended temperature range of -40 to 125 °C. The TS3121P features an open-drain output stage that is decoupled from V_{CC}. This allows output voltages from 0 V to 5.5 V, independent of V_{CC}.

Input offset voltage drift versus temperature

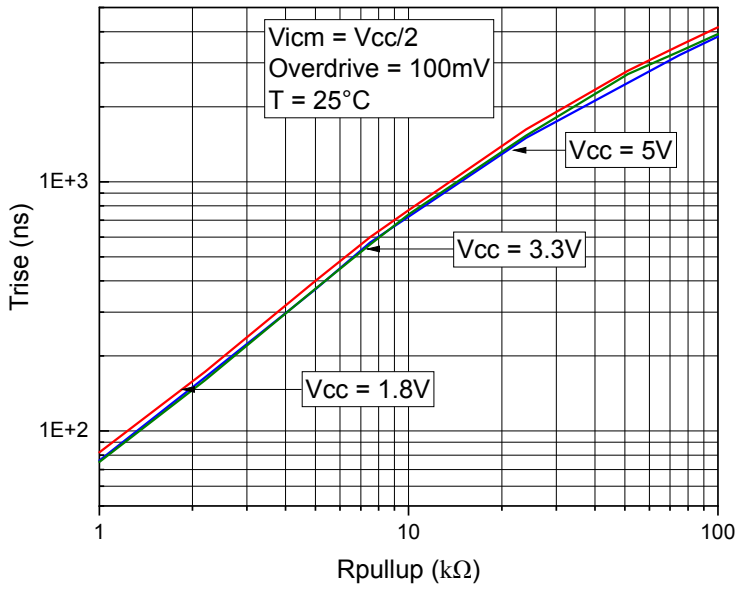
The input voltage drift variation versus temperature is defined as the offset variation related to the offset value measured at 25 °C. The signal chain accuracy at 25 °C can be compensated during the production at the application level. The maximum input voltage drift over the temperature enables the system designer to anticipate the effect of temperature variations.

$$\frac{\Delta V_{io}}{\Delta V} = \max\left|\frac{V_{io}(T) - V_{io}(25°C)}{T - 25°C}\right| \quad (1)$$

Where T = -40 °C and +125 °C. The datasheet maximum value is guaranteed by a measurement on a representative sample size ensuring a Cpk (process capability index) greater than 1.3. The datasheet reports the absolute worst-case value between -40 °C and +125 °C.

Resistor values for high-speed design

Figure 50. Rise time vs. pull-up resistor

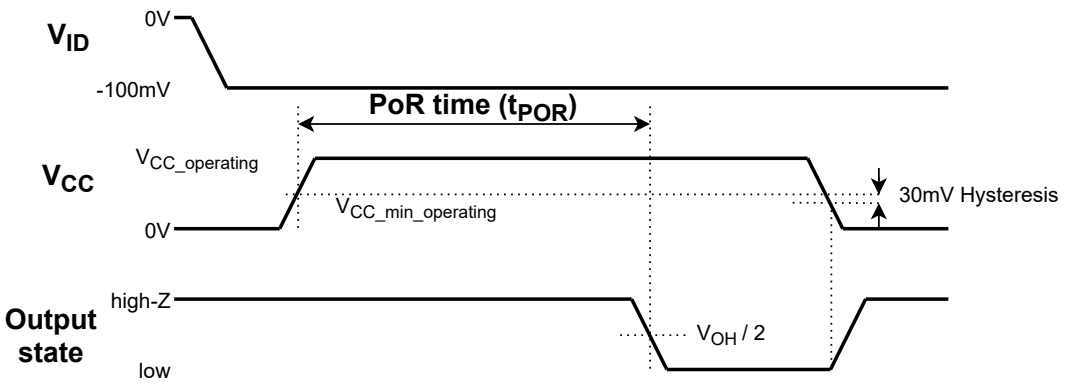


Power-on Reset (PoR) time

The TS3121P has an embedded Power-On Reset (PoR) circuit for known start-up and power-down conditions. While the power supply (V_{CC}) is ramping up, the PoR circuitry will be activated for 10 µs (t_{POR}) after the minimum supply voltage ($V_{CC\_min\_operating}$) threshold is crossed, or immediately when the supply voltage drops below approximately $V_{CC\_min\_operating}$ - 30 mV. When the supply voltage is equal or greater than the minimum supply voltage for a minimum delay period, the comparator output reflects the state of the differential input (VID).

The PoR circuit keeps the output in high impedance (HI-Z) during the PoR period (t_{PoR}). For low power applications, the supply voltage of the TS3121P can be disconnected when the device is not in use. The PoR controller by design allows high reliability even for short on/off cycles below 1 ms. Note that it the nature of an open drain output that the output rises with the pull-up voltage during the PoR period.

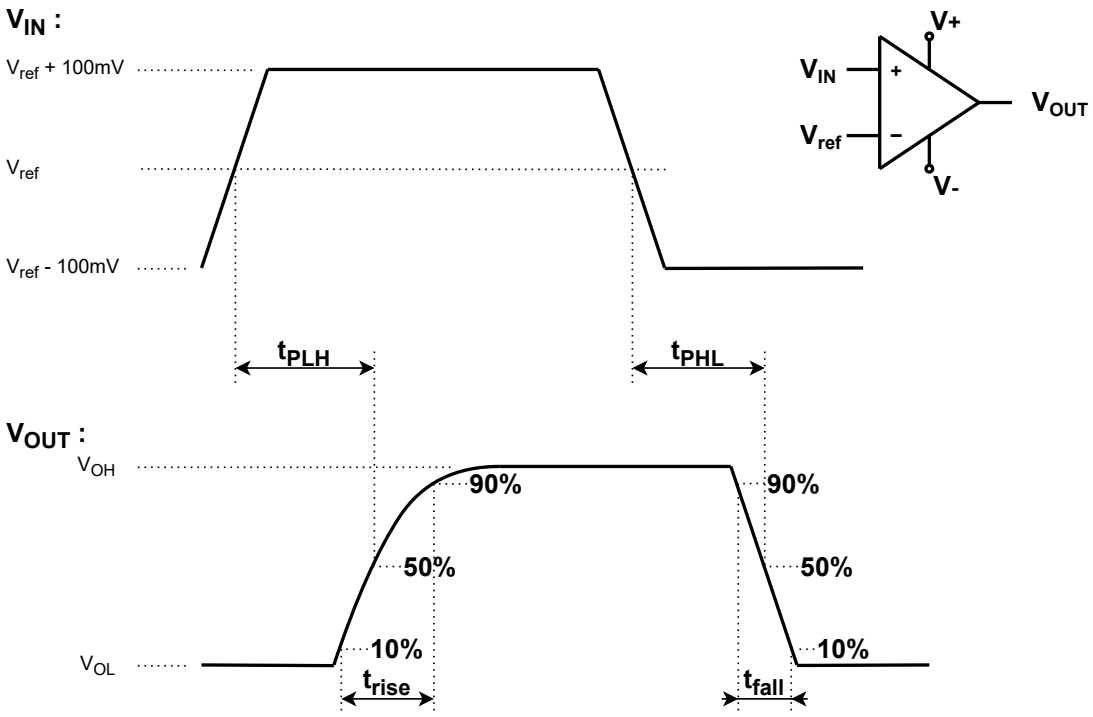
Figure 51. **Power-on Reset timing diagram**



Propagation delay

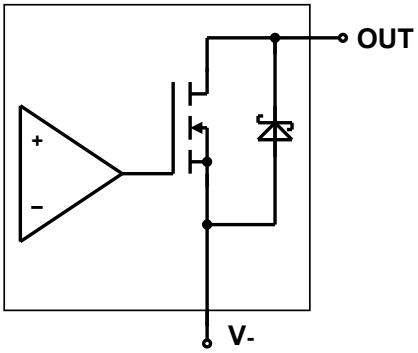
There is a delay between when the input crosses the reference voltage and the output responds. This is called the propagation delay. Propagation delay can be different between high-to-low and low-to-high input transitions. This is shown as t_{PLH} and t_{PHL} in Figure below and is measured from the mid-point of the input to the midpoint of the output. Note that for open-drain comparators, the output rise time trise and t_{PLH} strongly depend on the pull-up circuit connected to the output pin.

Figure 52. **Propagation delay**



Output stage

Figure 53. **Output stage**



With a dedicated ESD clamp in the open-drain output stage, voltage levels higher than V_{CC} can be applied to the comparator output. The TS3121P can thus be used for level shifter applications where the output voltage is independent of the comparator supply voltage.

PCB layout recommendations

Particular attention must be paid to the layout of the PCB tracks connected to the comparator, load, and power supply. The power and ground traces are critical as they must provide adequate energy and grounding for all circuits. The best practice is to use short and wide PCB traces to minimize voltage drops and parasitic inductance. In addition to minimizing parasitic impedance over the entire surface, a multi-via technique that connects the bottom and top layer ground planes together in many locations is often used. The copper traces that connect the output pins to the load and supply pins should be as wide as possible to minimize trace impedance.

Decoupling capacitor

To ensure op amp full functionality, it is recommended to place two decoupling capacitors of 100 nF and 10 nF as close as possible to the comparator supply pins. A good decoupling helps to reduce electromagnetic interference impact.

6 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

6.1 SC70-5 (or SOT323-5) package information

Figure 54. SC70-5 (or SOT323-5) package outline

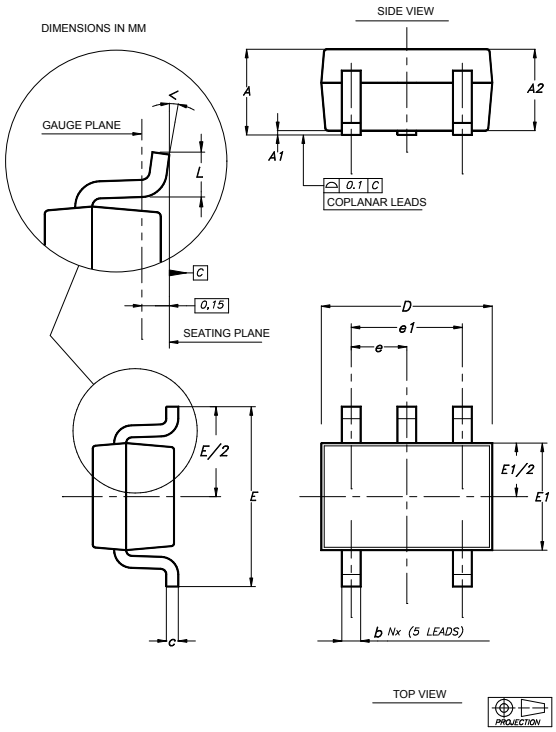


Table 7. SC70-5 (or SOT323-5) package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.80		1.10	0.032		0.043
A1			0.10			0.004
A2	0.80	0.90	1.00	0.032	0.035	0.039
b	0.15		0.30	0.006		0.012
c	0.10		0.22	0.004		0.009
D	1.80	2.00	2.20	0.071	0.079	0.087
E	1.80	2.10	2.40	0.071	0.083	0.094
E1	1.15	1.25	1.35	0.045	0.049	0.053
e		0.65			0.025	
e1		1.30			0.051	
L	0.26	0.36	0.46	0.010	0.014	0.018
<	0°		8°	0°		8°

6.2 SOT23-5 package information

Figure 55. **SOT23-5 package outline**

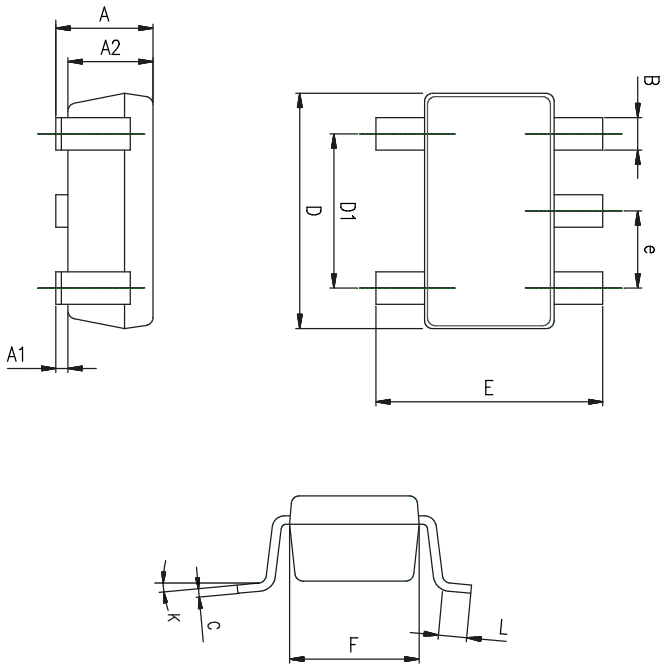


Table 8. **SOT23-5 mechanical data**

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.90	1.20	1.45	0.035	0.047	0.057
A1			0.15			0.006
A2	0.90	1.05	1.30	0.035	0.041	0.051
B	0.35	0.40	0.50	0.014	0.016	0.020
C	0.09	0.15	0.20	0.004	0.006	0.008
D	2.80	2.90	3.00	0.110	0.114	0.118
D1		1.90			0.075	
e		0.95			0.037	
E	2.60	2.80	3.00	0.102	0.110	0.118
F	1.50	1.60	1.75	0.059	0.063	0.069
L	0.10	0.35	0.60	0.004	0.014	0.024
K	0 degrees		10 degrees	0 degrees		10 degrees

7 Ordering information

Table 9. Order code

Order code	Package	Packaging	Marking
TS3121PICT	SC70-5	Tape and reel	K5X
TS3121PIYCT (1)			K5Y
TS3121PILT	SOT23-5		K5X
TS3121PIYLT (1)			K5Y

1. *Qualifiedand characterized according to AEC Q100 and Q003 or equivalent, advanced screening according to AEC Q001 & Q002 or equivalent.*

Revision history

Table 10. **Document revision history**

Date	Revision	Changes
13-Jan-2026	1	Initial release.

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