

Am29F010 (Known Good Die)

1 Megabit (131,072 x 8-Bit)

CMOS 5.0 Volt-only, Sectored Flash Memory—Die Revision 1

DISTINCTIVE CHARACTERISTICS

- **5.0 V \pm 10% for read and write operations**
 - Minimizes system-level power requirements
- **Compatible with JEDEC-standard commands**
 - Software compatible with single-power-supply flash standards
 - Superior inadvertent write protection
- **Minimum 100,000 write erase cycles guaranteed**
- **High performance**
 - Access times as fast as 90 ns
- **Sector architecture**
 - Eight uniform sectors of 16 Kbytes each
 - Any combination of sectors can be erased. Also supports full chip erase.
- **Sector protection**
 - Hardware method that disables any combination of sectors from write or erase operations.
- **Embedded Erase Algorithm**
 - Automatically pre-programs and erases the chip or any sector
- **Embedded Program Algorithm**
 - Automatically programs and verifies data at a specified address
- **Data Polling and Toggle Bit feature**
 - Detects program or erase cycle completion
- **Low power consumption**
 - 30 mA typical active read current
 - 50 mA typical program/erase current
- **Enhanced power management for standby mode**
 - < 25 μ A typical standby current
- **Low V_{CC} write inhibit \leq 3.2 V**
- **Tested to datasheet specifications at temperature**
- **Quality and reliability levels equivalent to standard packaged components**

GENERAL DESCRIPTION

The Am29F010 in Known Good Die (KGD) form is a 1 Mbit, 5.0 Volt-only Flash memory. AMD defines KGD as standard product in die form, tested for functionality and speed. AMD KGD products have the same reliability and quality as AMD products in packaged form.

Am29F010 Features

The Am29F010 device is organized as eight uniform sectors of 16 Kbytes each for flexible erase capability. This device is designed to be programmed in-system with the standard system 5.0 Volt V_{CC} supply. A power supply providing 12.0 Volt V_{PP} is not required for program or erase operations.

The Am29F010 in KGD form offers access times of 90 ns and 120 ns, allowing high speed microprocessors to operate without wait states. To eliminate bus contention, the device has separate chip enable (\overline{CE}), write enable (\overline{WE}), and output enable (\overline{OE}) controls.

The Am29F010 is entirely command set compatible with the JEDEC single-power-supply Flash standard.

Commands are written to the command register using standard microprocessor write timings. Register contents serve as input to an internal state-machine, which controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from 12.0 Volt Flash or EPROM devices.

The Am29F010 is programmed by executing the program command sequence, which invokes the Embedded Program Algorithm. This internal algorithm automatically times the program pulse widths and verifies proper cell margin. The Am29F010 is erased by executing the erase command sequence, which invokes the Embedded Erase Algorithm. Before executing the erase operation, this internal algorithm automatically preprograms the array if it is not already programmed. During erase, the device automatically times the erase pulse widths and verifies proper cell margin.

This device also features a sector erase architecture, which allows sectors of memory to be erased and

reprogrammed without affecting the data contents of other sectors. A sector is typically erased and verified within 1.0 second if already pre-programmed. The Am29F010 is erased when shipped from the factory.

The Am29F010 also features hardware sector protection. This feature disables both program and erase operations in any combination of the eight sectors of memory.

The device features single 5.0 Volt power supply operation for both read and write functions.

Internally generated and regulated voltages are provided for the program and erase operations. A low V_{CC} detector automatically inhibits write operations when a loss of device power occurs. The end of program or erase is detected by $\overline{\text{Data}}$ Polling (DQ7), or by the Toggle Bit (DQ6). Once the end of a program or erase cycle has been completed, the device automatically resets to the read mode.

The Am29F010 memory electrically erases all bits within a sector simultaneously via Fowler-Nordheim tunneling. The bytes are programmed one byte at a time using the EPROM programming mechanism of hot electron injection. AMD's Flash technology combines years of Flash memory manufacturing experience to produce the highest levels of quality, reliability and cost effectiveness.

ELECTRICAL SPECIFICATIONS

Refer to the Am29F010 data sheet, PID 16736, for full electrical specifications for the Am29F010 in KGD form.

FLEXIBLE SECTOR ARCHITECTURE

- Eight 16 Kbyte sectors
- Individual-sector or multiple-sector erase capability
- Sector protection is user definable

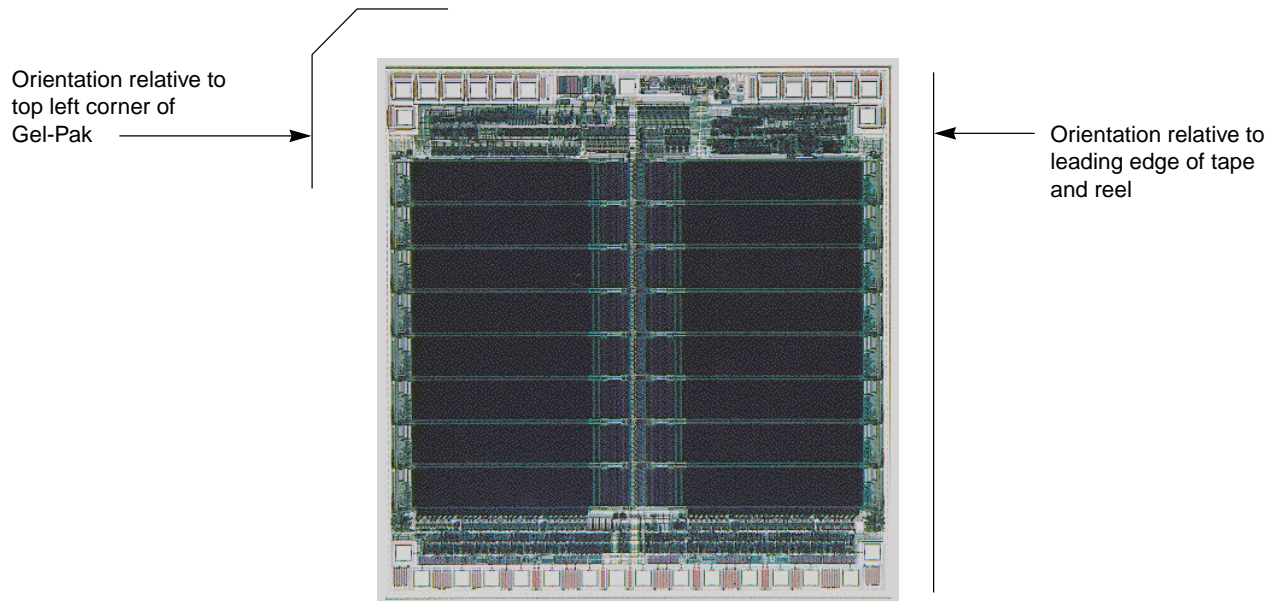
Sector	Sector Size	Address Range
SA7	16 Kbytes	1C000h–1FFFFh
SA6	16 Kbytes	18000h–1BFFFh
SA5	16 Kbytes	14000h–17FFFh
SA4	16 Kbytes	10000h–13FFFh
SA3	16 Kbytes	0C000h–0FFFFh
SA2	16 Kbytes	08000h–0BFFFh
SA1	16 Kbytes	04000h–07FFFh
SA0	16 Kbytes	00000h–03FFFh

Am29F010 Sector Architecture

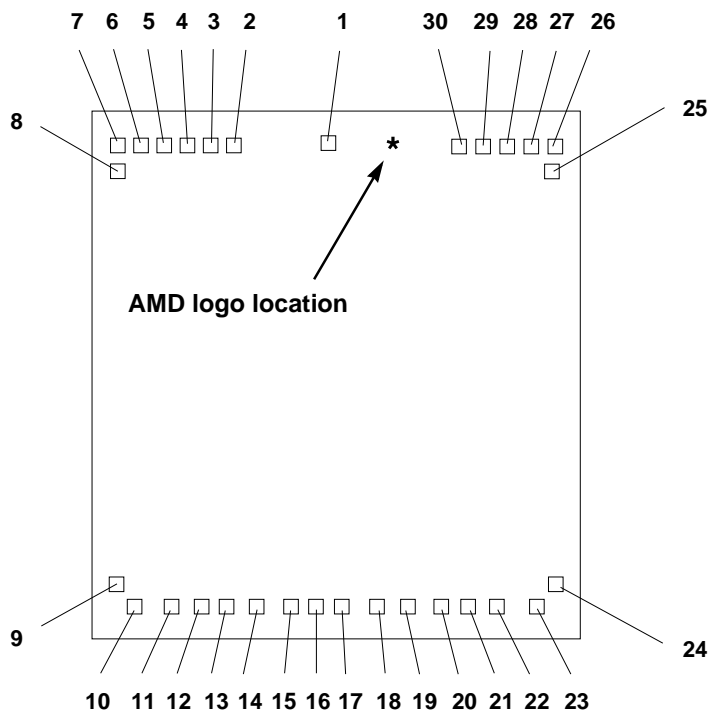
PRODUCT SELECTOR GUIDE

Family Part No:	Am29F010 (KGD)	
	-90	-120
Ordering Part No: $V_{CC} = 5.0\text{ V} \pm 10\%$		
Max Access Time (ns)	90	120
\overline{CE} (\overline{E}) Access (ns)	90	120
\overline{OE} (\overline{G}) Access (ns)	35	50

DIE PHOTOGRAPH



DIE PAD LOCATIONS



PAD DESCRIPTION

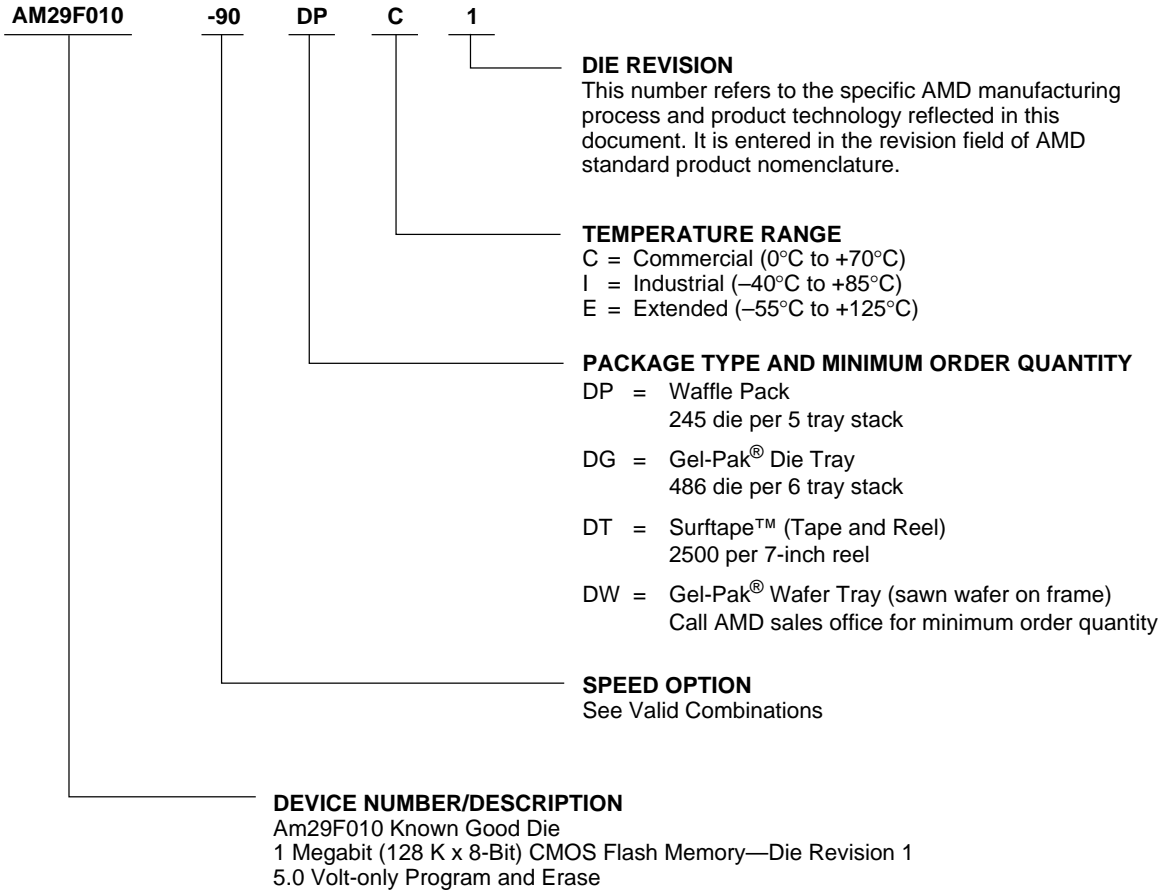
Pad	Signal	Pad Center (mils)		Pad Center (millimeters)	
		X	Y	X	Y
1	V _{CC}	0.00	0.00	0.00	0.00
2	A16	-33.20	-1.30	-0.84	-0.03
3	A15	-41.60	-1.30	-1.06	-0.03
4	A12	-49.90	-1.30	-1.27	-0.03
5	A7	-58.30	-1.30	-1.48	-0.03
6	A6	-66.60	-1.30	-1.69	-0.03
7	A5	-75.00	-1.30	-1.91	-0.03
8	A4	-74.40	-10.50	-1.89	-0.27
9	A3	-75.60	-158.20	-1.92	-4.02
10	A2	-69.40	-166.80	-1.76	-4.24
11	A1	-56.10	-166.80	-1.42	-4.24
12	A0	-46.10	-166.80	-1.17	-4.24
13	D0	-36.30	-166.90	-0.92	-4.24
14	D1	-25.90	-166.90	-0.66	-4.24
15	D2	-13.30	-166.90	-0.34	-4.24
16	V _{SS}	-4.30	-166.90	-0.11	-4.24
17	D3	4.70	-166.90	0.12	-4.24
18	D4	17.30	-166.90	0.44	-4.24
19	D5	27.60	-166.90	0.70	-4.24
20	D6	40.20	-166.90	1.02	-4.24
21	D7	50.60	-166.90	1.29	-4.24
22	\overline{CE}	60.60	-166.80	1.54	-4.24
23	A10	74.00	-166.80	1.88	-4.24
24	\overline{OE}	81.40	-158.20	2.07	-4.02
25	A11	80.20	-10.40	2.04	-0.26
26	A9	80.80	-1.30	2.05	-0.03
27	A8	72.40	-1.30	1.84	-0.03
28	A13	64.10	-1.30	1.63	-0.03
29	A14	55.70	-1.30	1.41	-0.03
30	\overline{WE}	47.40	-1.30	1.20	-0.03

Note: The coordinates above are relative to the center of pad 1 and can be used to operate wire bonding equipment.

ORDERING INFORMATION

Standard Products

AMD KGD products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the following:



Valid Combinations	
AM29F010-90	DPC 1, DPI 1, DPE 1, DGC 1, DGI 1, DGE 1,
AM29F010-120	DTC 1, DTI 1, DTE 1, DWC 1, DWI 1, DWE 1

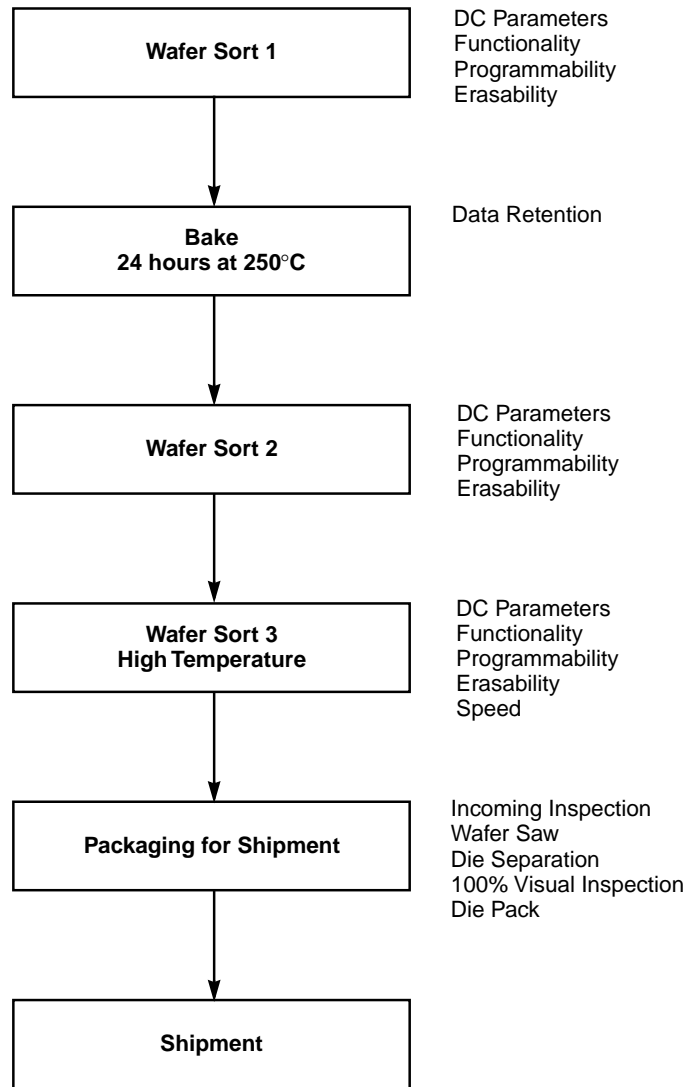
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

PRODUCT TEST FLOW

The following chart provides an overview of AMD's Known Good Die test flow. For more detailed information, refer to the Am29F010 product qualification database supplement for KGD. AMD implements quality assurance procedures throughout the product test

flow. In addition, an off-line quality monitoring program (QMP) further guarantees AMD quality standards are met on Known Good Die products. These QA procedures also allow AMD to produce KGD products without requiring or implementing burn-in.



AMD KGD Product Test Flow

PHYSICAL SPECIFICATIONS

Die dimensions	174 mils x 189 mils 4.42 mm x 4.80 mm
Die Thickness	~20 mils or ~0.51 mm
Bond Pad Size	4.47 mils x 4.47 mils 113.48 μm x 113.48 μm
Pad Area Free of Passivation	19.98 mils ² 12,878 μm^2
Pads Per Die	30
Bond Pad Metalization	Al/Si/Cu
Die Backside	No metal, may be grounded (optional)
Passivation	Nitride/SOG/Nitride

DC OPERATING CONDITIONS

V_{CC} (Supply Voltage)	4.5 V to 5.5 V
Junction Temperature Under Bias	T_J (max) = 130°C
For Read-only	T_J (max) = 140°C
Operating Temperature	Commercial 0°C to +70°C Industrial -40°C to +85°C Extended -55°C to +125°C

MANUFACTURING INFORMATION

Manufacturing and Test	Fab 14, Austin, TX
Manufacturing ID	98108AK
Preparation for Shipment	Penang, Malaysia
Fabrication Process	CS19AFDS
Die Revision	1

SPECIAL HANDLING INSTRUCTIONS**Processing**

Do not expose KGD products to ultraviolet light or process them at temperatures greater than 250°C. Failure to adhere to these handling instructions will result in irreparable damage to the devices. For best yield, AMD recommends assembly in a Class 10K clean room with 30% to 60% relative humidity.

Storage

Store at a maximum temperature of 30°C in a nitrogen-purged cabinet or vacuum-sealed bag. Observe all standard ESD handling procedures.

TERMS AND CONDITIONS OF SALE FOR AMD NON-VOLATILE MEMORY DIE

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