MPQ7231

MPSafe™ 42V, 3A Buck or 2.4A Buck-Boost, Synchronous Infrared LED Driver, AEC-Q100 Qualified

DESCRIPTION

The MPQ7231 is a fixed-frequency, constant current, infrared (IR) LED driver with integrated eye safety features. The device operates across a 6V to 42V input voltage (V_{IN}) range. It can be configured to either buck or buck-boost mode, and achieve up to 3A and 2.4A of peak current (I_{LED_PEAK}), respectively. The MPQ7231 is ideal for driving one or two IR LEDs.

The MPQ7231 provides ultra-low on resistance ($R_{DS(ON)}$) MOSFETs, with a 44mΩ high-side MOSFET (HS-FET) and 40mΩ low-side MOSFET (LS-FET), using MPS's advanced BCD FET technology to minimize ohmic losses. This improves the total system loss up to a factor of 10 times compared to the traditional, non-synchronous architecture with a Schottky diode. As a result, the system runs cooler and is significantly more efficient.

The MPQ7231 can support a 10Hz to 2kHz pulse-width modulation (PWM) dimming frequency range, which is compatible with IR LED applications that require 30fps, 60fps, or 120fps dimming. Constant frequency hysteretic control mode provides extremely fast transient response without loop compensation. Frequency spread spectrum (FSS) modulation improves EMC performance.

Eye-safety features include LED current limiting and factory preset dimming on-time limits (1ms, 3ms, or 5ms) to support the system in achieving ASIL requirements. The MPQ7231 provides a dedicated fault pin as well as protection features including LED short to battery (or ground) protection, LED open protection, over-current protection (OCP) with latch, thermal derating, and thermal shutdown.

The MPQ7231 requires a minimal number of readily available, standard external components to ensure a simple, compact, and efficient system design. It is available in a space-saving QFN-19 (3mmx4mm) package.

FEATURES

- Built for Infrared (IR) LED Applications:
  - 10Hz to 2kHz Pulse-Width Modulation (PWM) Dimming Frequency
  - Compatible with 30fps, 60fps, and 120fps Dimming
- Improved Efficiency and Thermals:
  - Integrated Current-Sense Resistor
  - 44mΩ/40mΩ On Resistance ($R_{DS(ON)}$) Internal MOSFETs
- Optimized for EMC/EMI:
  - 2.4MHz (Buck) or 1.25MHz (Buck-Boost) Switching Frequency (f_{SW}) with Frequency Spread Spectrum (FSS)
  - EMI Reduction Techniques
- Functional Safety:
  - Eye Safety Features Include:
    - LED Current Limit
    - Dimming On Time Limit (1ms, 3ms, or 5ms)
  - Functional Safety Documents Available
  - Fault Indication for LED Short (Battery and Ground), LED Open, OVP, and Thermal Shutdown
  - Over-Current Protection (OCP) with Latch
- Additional Features:
  - Wide 6V to 42V Operating V_{IN} Range
  - 3A Buck or 2.4A Buck-Boost I_{L_PEAK}
  - Configurable Thermal Derating via NTC Remote Temperature Sensing
  - Available in a QFN-19 (3mmx4mm) Package with Wettable Flanks
  - Available in AEC-Q100 Grade 1

MPSafe™ QM

APPLICATIONS

- Driver Monitoring Systems (DMS)
- IR Illumination for Automotive Cameras
- Surveillance Systems

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TYPICAL APPLICATION

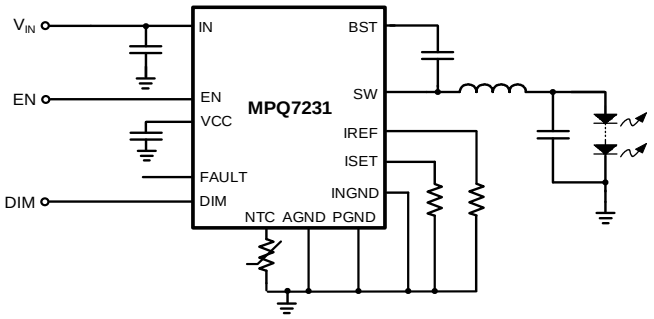
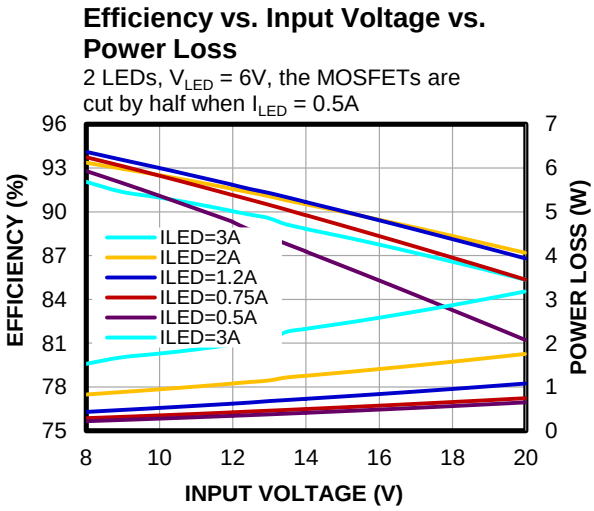


Figure 1: Typical Application Circuit (Buck Topology, ≥14.7kΩ R_{IREF} to Select Mode)



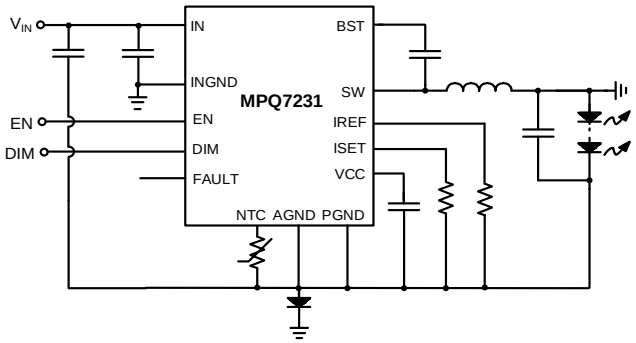
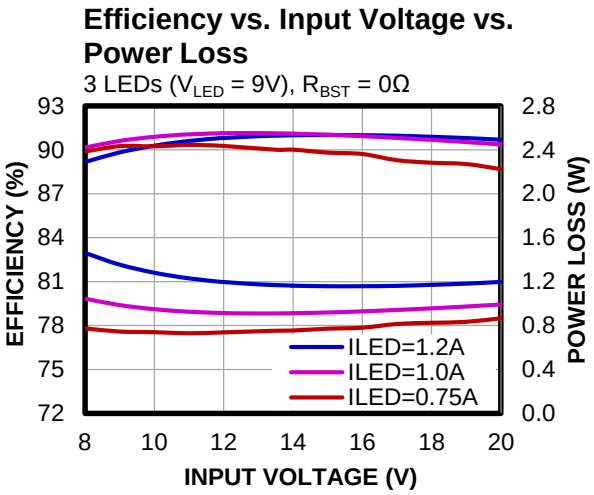


Figure 2: Typical Application Circuit (Buck-Boost Topology, ≤9.09kΩ R_{IREF} to Select Mode)



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ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating**
MPQ7231GLE-D00-AEC1***	QFN-19 (3mmx4mm)	*See Below*	1
MPQ7231GLE-D10-AEC1***			
MPQ7231GLE-D30-AEC1***			
MPQ7231GLE-D50-AEC1***			

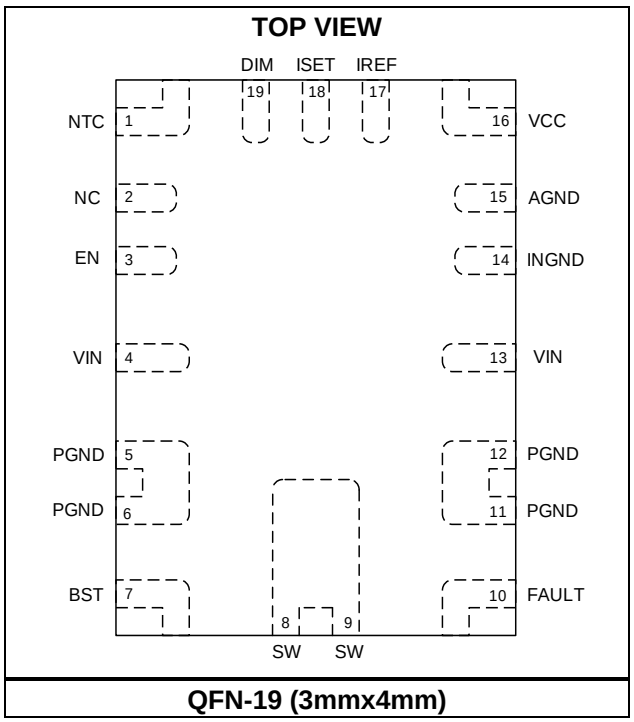
* For Tape & Reel, add suffix -Z (e.g. MPQ7231GLE-D00-AEC1-Z).
** Moisture Sensitivity Level Rating
*** Wettable Flank

TOP MARKING

MPYW
7231
LLL
E

MP: MPS prefix
Y: Year code
W: Week code
7231: Part number
LLL: Lot number
E: Wettable lead flank

PACKAGE REFERENCE



QFN-19 (3mmx4mm)

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PIN FUNCTIONS

Pin #	Name	Description
1	NTC	**Remote temperature sense.** Connect a negative temperature coefficient (NTC) resistor network (R_{NTC}) between the NTC and AGND pins to configure the temperature derating starting point. NTC short to PGND as well as NTC short to AGND are protected.
2	NC	**Not connected.** Connect the NC pin to PGND on the board externally.
3	EN	**Enable.** Pull the EN pin above 1V to enable the chip; pull EN below 0.9V to shut down the chip. Connect EN to the VIN pin via a resistor for automatic start-up once V_{IN} and V_{CC} exceed their respective under-voltage lockout (UVLO) thresholds. EN is pulled low via an internal resistor, meaning the chip is off by default if EN is floating.
4, 13	VIN	**Supply voltage.** The MPQ7231 operates from a 6V to 42V input voltage (V_{IN}) and requires an input capacitor (C_{IN}) to decouple the input rail. Connect the VIN pin to the input rail using a wide PCB trace.
5, 6, 11, 12	PGND	**Power ground.** The PGND pin is the power device's reference ground, including the configuration pins, and requires careful consideration during PCB layout. PGND is also used to dissipate the thermal heat.
7	BST	**Bootstrap.** The BST pin requires a capacitor connected between the SW and BST pins to form a floating supply across the high-side MOSFET (HS-FET) driver. Place a resistor between SW and the BST capacitor (C_{BST}) to reduce the SW spike voltage and improve EMI performance.
8, 9	SW	**Switch output.** The SW pin is the middle point of the HS-FET and low-side MOSFET (LS-FET). It is recommended to use a wide trace and overall small-size SW node for the PCB to reduce noise coupling and improve EMI.
10	FAULT	**Fault indicator.** The FAULT pin is an open-drain output with an internal, 300kΩ pull-up resistor connected to VIN and a 4MΩ pull-down resistor connected to INGND. Pull FAULT low if an LED short, LED open, over-temperature (OT), over-current (OC), or false mode detection condition occurs. Connect FAULT to VIN continuously using a pull-up resistor.
14	INGND	**VIN, EN, DIM, and FAULT ground for buck-boost topology.** For buck topology, connect the INGND pin to PGND or AGND.
15	AGND	**Analog ground.** The AGND pin is the reference ground of the logic circuit. Connect AGND to the PGND pin via an external trace.
16	VCC	**Internal bias supply.** The VCC pin supplies power to the internal control circuit and gate drivers. Place a ≥3µF decoupling capacitor to ground, close to VCC. Considering the capacitance derating, a 10µF/10V or 16V X7R capacitor is strongly recommended.
17	IREF	**Mode selection and NTC reference current setting.** Connect a ≤9.09kΩ resistor at the IREF pin to select buck-boost mode; connect a ≥14.7kΩ at IREF to select buck mode. The IREF pin voltage (V_{IREF}) is set to 0.57V after mode detection finishes. Connect a resistor (R_{IREF}) from IREF to ground to obtain a 0.57V/R_{IREF} reference current. If IREF is shorted to ground or an IREF open fault is detected, the part latches off and FAULT asserts. The NTC pin's current is 50 or 5 times of IREF's reference current (I_{REF}) for buck mode and buck-boost mode, respectively.
18	ISET	**LED current setting.** Connect an external resistor from the ISET pin to ground to set the LED average current. If ISET is shorted to ground or a SET open fault is detected, the part latches off and FAULT asserts.
19	DIM	**Dimming control.** Apply an external pulse-width modulation (PWM) signal to the DIM pin for PWM dimming. Pull the DIM pin above 1V to turn dimming on; pull DIM below 0.9V to turn dimming off. Ensure that the dimming on time is at least 100µs to avoid mistriggering FAULT. A long dimming high signal on DIM does not generate a FAULT. LED on time is limited to 1ms, 3ms, and 5ms, based on different trim options. The dimming off time can last as long as 100ms, allowing the device to support a low to 10Hz dimming frequency for 30Hz IR LED driver applications.

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ABSOLUTE MAXIMUM RATINGS (1)

V_{IN} - V_{PGND}, V_{AGND} .....-0.3V to +50V
V_{IN} - V_{INGND} .....-0.3V to +50V
V_{FAULT} - V_{INGND} .....-0.3V to +50V
V_{EN}, V_{DIM} - V_{INGND}.....-0.3V to +5.5V
V_{DIM} - V_{PGND}, V_{AGND} .....-0.3V to +50V
V_{SW} - V_{PGND}, V_{AGND}.. ……
…….-0.3V to V_{IN} - V_{PGND}, V_{AGND} + 0.3V
V_{BST} ..... V_{SW} + 5.5V
All other pins to V_{PGND}, V_{AGND} .....-0.3V to +5.5V
Continuous power dissipation (T_A = 25°C) (2) (6)
QFN-19 (3mmx4mm) 3.9W
Junction temperature (T_J) .....150°C
Lead temperature .....260°C
Storage temperature..... -65°C to +150°C

ESD Ratings

Human body model (HBM) .....Class 2 (3)
Charged-device model (CDM) ..... Class C2b (4)

Recommended Operating Conditions

Supply voltage (V_{IN} - V_{PGND}).....6V to 42V
LED current (I_{LED}) at buck mode…….
…….Up to 3A
Continuous I_{LED} at buck-boost mode……..…..
……..Up to 1.2A
Peak LED current (I_{LED_PEAK}) at buck-boost mode
……..Up to 2.4A
Operating junction temp (T_J).....-40°C to +150°C

Thermal Resistance θ_{JA} θ_{JC}

QFN-19 (3mmx4mm)
JESD51-7 ..... 48 ..... 11°C/W (5)
EVQ7231-L-00A ..... 32 ..... 6.°C/W (6)

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can produce an excessive die temperature, which causes the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) Per AEC-Q100-002.
4) Per AEC-Q100-011.
5) Measured on a JESD51-7, 4-layer PCB. The values given in this table are only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application. The θ_{JC} value shows the thermal resistance from the junction-to-case bottom.
6) Measured on an MPS standard EVB for the MPQ7231: a 4-layer, 2oz PCB (83.5mmx83.5mm). The θ_{JC} value shows the thermal resistance from the junction-to-case top.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 13.5V, V_{EN} = 2V, T_J = -40°C to +150°C, typical values are at T_J = 25°C, unless otherwise noted.

BUCK MODE

Parameter	Symbol	Condition	Min	Typ	Max	Units
Shutdown supply current	I_{SD}	V_{EN} = 0V		30	80	μA
Quiescent supply current	I_Q	V_{EN} = 2V, no switching, float IREF (exclude I_{REF} and NTC current)		1.2	2	mA
		FAULT latch			2	mA
High-side MOSFET (HS-FET) on resistance	$R_{DS(ON)_HS}$	V_{BST-SW} = 5V, R_{ISET} = 10.5kΩ		44	85	mΩ
		V_{BST-SW} = 5V, R_{ISET} = 40.2kΩ		85	160	mΩ
Low-side MOSFET (LS-FET) on resistance	$R_{DS(ON)_LS}$	V_{CC} = 5.2V, R_{ISET} = 10.5kΩ		40	80	mΩ
		V_{CC} = 5.2V, R_{ISET} = 40.2kΩ		80	150	mΩ
Switch leakage	I_{SW_LKG}	V_{EN} = 0V, V_{SW} =13.5V, T_J = 25°C			1	μA
		V_{EN} = 0V, V_{SW} = 13.5V			5	μA
Peak current limit (7)	I_{LIMIT_PEAK}	R_{ISET} = 40.2kΩ	3.61	4.25	4.89	A
		R_{ISET} = 10.5kΩ	6.85	8	9.15	A
Zero-current detection (ZCD) (7)				50		mA
Switching frequency	f_{SW}	FSS activated	2000	2400	2800	kHz
Minimum on time (7)	t_{ON_MIN}			55	80	ns
Minimum off time (7)	t_{OFF_MIN}			75	100	ns
Maximum duty cycle (7)	D_{MAX}	Low-dropout	95	98		%
Frequency spread spectrum (FSS) (7)				15		kHz
FSS range (7)				±10%		f_{SW}
LED current	I_{LED}	R_{ISET} = 10.5kΩ, T_J = 25°C to 100°C	1.9	2	2.1	A
		R_{ISET} = 10.5kΩ	1.7		2.3	A
LED current threshold for cut MOSFET	I_{LED_CUT}			800	950	mA
ISET voltage	V_{ISET}	I_{ISET} = 45μA	0.573	0.592	0.606	V
ISET current threshold for pin short		$I_{LED} < I_{LED_CUT}$	180	220	260	μA
		$I_{LED} > I_{LED_CUT}$	270	330	390	μA
ISET current threshold for pin open			0.5	1.4	5	μA
EN rising threshold	V_{EN_RISING}	V_{EN} - V_{INGND}		1	1.6	V
EN falling threshold	$V_{EN_FALLING}$	V_{EN} - V_{INGND}	0.7	0.9		V
EN threshold hysteresis	V_{EN_HYS}	V_{EN} - V_{INGND}		100		mV
EN input current	I_{EN}	V_{EN} - V_{INGND} = 2V		2	8	μA
		V_{EN} - V_{INGND} = 0V		0	0.2	μA
DIM rising threshold	V_{DIM_RISING}	V_{DIM} - V_{INGND}		1	1.6	V
DIM falling threshold	$V_{DIM_FALLING}$	V_{DIM} - V_{INGND}	0.7	0.9		V
DIM threshold hysteresis	V_{DIM_HYS}	V_{DIM} - V_{INGND}		100		mV

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 13.5V, V_{EN} = 2V, T_J = -40°C to +150°C, typical values are at T_J = 25°C, unless otherwise noted.

BUCK MODE

Parameter	Symbol	Condition	Min	Typ	Max	Units
DIM on time limit of the MPQ7231GLE-D10	t_{DIM_ON}		0.8	1	1.2	ms
DIM on time limit of the MPQ7231GLE-D30			2.4	3	3.6	ms
DIM on time limit of the MPQ7231GLE-D50			4	5	6	ms
DIM input current	I_{DIM}	V_{DIM} - V_{INGND} = 2V		2	8	µA
		V_{DIM} - V_{INGND} = 0V		0	0.2	µA
DIM turn-off delay (7)	$t_{DIM_D_OFF}$		100			ms
V_{IN} under-voltage lockout (UVLO) rising threshold	$V_{IN_UVLO_VTH_R}$	V_{IN} - V_{INGND}	5.75	6	6.25	V
V_{IN} UVLO falling threshold	$V_{IN_UVLO_VTH_F}$	V_{IN} - V_{INGND}	4.4	4.9	5.2	V
V_{IN} UVLO hysteresis threshold	$V_{IN_UVLO_HYS}$	V_{IN} - V_{INGND}		1.1		V
V_{CC} UVLO rising threshold	$V_{CC_UVLO_VTH_R}$	V_{CC} - V_{AGND}	4.4	4.7	5	V
V_{CC} UVLO falling threshold	$V_{CC_UVLO_VTH_F}$	V_{CC} - V_{AGND}	3.4	4.05	4.7	V
V_{CC} UVLO hysteresis threshold	$V_{CC_UVLO_HYS}$	V_{CC} – V_{AGND}		650		mV
VCC regulator	V_{CC}	I_{CC} = 0mA	4.9	5.1	5.3	V
VCC load regulation		I_{CC} = 20mA	4.7			V
VCC maximum current ability		V_{CC} = V_{CC_UVLO} + 100mV, no switching	50	80	120	mA
VCC source current ability (7)		V_{CC} = V_{CC_UVLO} + 100mV, switching		25		mA
Output under-voltage (UV) threshold	V_{UV_VTH}		0.6	1.2	1.7	V
LED low current threshold		$I_{LED_SETTING}$ < I_{LED_CUT}	85	100	130	mA
		$I_{LED_SETTING}$ > I_{LED_CUT}	180	220	260	mA
FAULT assert delay time at start-up	$t_{FT_D_START}$		3	4	5	ms
FAULT assert deglitch time after start-up (7)	t_{FT_D}			20		µs
FAULT assert low sink current ability	I_{FAULT_SINK}	V_{FAULT} = 12V	10	30	50	mA
		V_{FAULT} = 0.2V	5	12		mA
FAULT pull-up resistor			100	330	500	kΩ
IREF current for mode detection			200	240	280	µA
IREF voltage (V_{IREF}) threshold for mode detection			2.6	2.7	2.8	V

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 13.5V, V_{EN} = 2V, T_J = -40°C to +150°C, typical values are at T_J = 25°C, unless otherwise noted.

BUCK MODE

Parameter	Symbol	Condition	Min	Typ	Max	Units
IREF voltage	V_{IREF}	I_{IREF} = 20μA	0.51	0.57	0.63	V
IREF current threshold for pin short detection			60	85	120	μA
IREF current threshold for pin open detection				3	6	μA
NTC source current	I_{NTC}	V_{NTC} = 1.5V, I_{REF} = 20μA	930	1020	1090	μA
NTC voltage (V_{NTC}) for current derating		I_{LED} = 98% of nominal voltage	-2.5%	1.25	+2.5%	V
		I_{LED} = 74% of nominal voltage	-2.5%	0.89	+2.5%	V
		I_{LED} = 50% of nominal voltage	-2.5%	0.53	+2.5%	V
V_{NTC} threshold for over-temperature protection (OTP)				0.37		V
V_{NTC} deglitch time for OTP		V_{NTC} = 0.3V	180	256	320	μs
V_{NTC} recovery threshold for OTP				0.48		V
Thermal shutdown (7)			155	170	185	°C

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 13.5V, V_{EN} = 2V, T_J = -40°C to +150°C, typical values are at T_J = 25°C, unless otherwise noted.

BUCK-BOOST MODE

Parameter	Symbol	Condition	Min	Typ	Max	Units
Shutdown supply current	I_{SD}	V_{EN} = 0V		30	80	μA
Quiescent supply current	I_Q	V_{EN} = 2V, no switching, float IREF (exclude I_{REF} and NTC current)		1.2	2	mA
		FAULT latch			2	mA
HS-FET on resistance	$R_{DS(ON)_HS}$	V_{BST-SW} = 5V, R_{ISET} = 10.5kΩ		44	85	mΩ
LS-FET on resistance	$R_{DS(ON)_LS}$	V_{CC} = 5.2V, R_{ISET} = 10.5kΩ		40	80	mΩ
Switch leakage	I_{SW_LKG}	V_{EN} = 0V, V_{SW} = 13.5V, T_J = 25°C			1	μA
		V_{EN} = 0V, V_{SW} = 13.5V			5	μA
Peak current limit (7)	I_{LIMIT_PEAK}		6.85	8	9.15	A
ZCD (7)				50		mA
Switching frequency	f_{SW}	FSS activated	1020	1250	1600	kHz
Minimum on time (7)	t_{ON_MIN}			55	80	ns
Minimum off time (7)	t_{OFF_MIN}			75	100	ns
Maximum duty cycle (7)	D_{MAX}	Low dropout	95	98		%
FSS (7)				15		kHz
FSS range (7)				±10%		f_{SW}
LED current	I_{LED}	R_{ISET} = 10.5kΩ, T_J = 25°C to 100°C	1.9	2	2.1	A
		R_{ISET} = 10.5kΩ	1.7		2.3	
ISET voltage	V_{ISET}	I_{ISET} = 45μA	0.573	0.592	0.606	V
Power derating ratio		V_{IN} = 6.6V, V_{ISET} relative to nominal voltage		95		%
		V_{IN} = 5.3V, V_{ISET} relative to nominal voltage		75		%
ISET current threshold for pin short		$I_{LED_SETTING}$ > I_{LED_CUT}	130	160	190	μA
ISET current threshold for pin open			0.5	1.4	5	μA
EN rising threshold	V_{EN_RISING}	V_{EN} - V_{INGND}		1	1.6	V
EN falling threshold	$V_{EN_FALLING}$	V_{EN} - V_{INGND}	0.7	0.9		V
EN threshold hysteresis	V_{EN_HYS}	V_{EN} - V_{INGND}		100		mV
EN input current	I_{EN}	V_{EN} = 2V		2	8	μA
		V_{EN} = 0V		0	0.2	μA
DIM rising threshold	V_{DIM_RISING}	V_{DIM} - V_{INGND}		1	1.6	V
DIM falling threshold	$V_{DIM_FALLING}$	V_{DIM} - V_{INGND}	0.7	0.9		V
DIM threshold hysteresis	V_{DIM_HYS}	V_{DIM} - V_{INGND}		100		mV
DIM on time limit of MPQ7231GLE-D10	t_{DIM_ON}		0.8	1	1.2	ms
DIM on time limit of MPQ7231GLE-D30			2.4	3	3.6	ms
DIM on time limit of MPQ7231GLE-D50			4	5	6	ms

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 13.5V, V_{EN} = 2V, T_J = -40°C to +150°C, typical values are at T_J = 25°C, unless otherwise noted.

BUCK-BOOST MODE

Parameter	Symbol	Condition	Min	Typ	Max	Units
DIM input current	I_{DIM}	V_{DIM} - V_{INGND} = 2V		2	8	µA
		V_{DIM} - V_{INGND} = 0V		0	0.2	µA
DIM turn-off delay (7)	$t_{DIM_D_OFF}$		100			ms
V_{IN} UVLO rising threshold	$V_{IN_UVLO_RISING}$	V_{IN} - V_{INGND}	5.75	6	6.25	V
V_{IN} UVLO falling threshold	$V_{IN_UVLO_FALLING}$	V_{IN} - V_{INGND}	4.4	4.9	5.2	V
V_{IN} UVLO hysteresis threshold	$V_{IN_UVLO_HYS}$	V_{IN} - V_{INGND}		1.1		V
V_{CC} UVLO rising threshold	$V_{CC_UVLO_RISING}$	V_{CC} - V_{AGND}	4.4	4.7	5	V
V_{CC} UVLO falling threshold	$V_{CC_UVLO_FALLING}$	V_{CC} - V_{AGND}	3.4	4.05	4.7	V
V_{CC} UVLO hysteresis threshold	$V_{CC_UVLO_HYS}$	V_{CC} - V_{AGND}		650		mV
VCC regulator	V_{CC}	I_{CC} = 0mA	4.9	5.1	5.3	V
VCC load regulation		I_{CC} = 20mA	4.7			V
VCC maximum current ability		V_{CC} = V_{CC_UVLO} + 100mV, no switching	50	80	120	mA
VCC source current ability (7)		V_{CC} = V_{CC_UVLO} + 100mV, switching		25		mA
Output over-voltage protection (OVP) threshold	V_{OUT_OVP}	V_{INGND} - V_{AGND}	17	18	19	V
Output under-voltage protection (UVP) threshold	V_{OUT_UVP}	V_{INGND} - V_{AGND}	1	1.35	1.7	V
V_{IN} load dump protection threshold			38	40	42	V
V_{IN} load dump protection falling threshold			37	39	41	V
V_{IN} load dump protection hysteresis				1		V
Output discharge current for load dump protection		V_{INGND} - V_{PGND} > 5V	40	100	180	mA
		V_{INGND} - V_{PGND} = 1V	20	45	90	mA
FAULT assert delay time at start-up	$t_{FT_D_START}$		3	4	5	ms
FAULT assert deglitch time after start-up	t_{FT_D}			20		µs
FAULT assert low sink current ability	I_{FAULT_SINK}	V_{FAULT} = 12V	10	30	50	mA
		V_{FAULT} = 0.2V	5	12		mA
FAULT pull-up resistor			100	330	500	kΩ

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 13.5V, V_{EN} = 2V, T_J = -40°C to +150°C, typical values are at T_J = 25°C, unless otherwise noted.

BUCK-BOOST MODE

Parameter	Symbol	Condition	Min	Typ	Max	Units
IREF current for mode detection			200	240	280	µA
V_{IREF} threshold for mode detection			2.6	2.7	2.8	V
IREF voltage	V_{IREF}	I_{REF} = 20µA	0.51	0.57	0.63	V
IREF current threshold for pin short detection			650	800	1000	µA
IREF current threshold for pin open detection				40	55	µA
NTC source current	I_{NTC}	V_{NTC} = 1.5V, I_{REF} = 200µA	930	1020	1090	µA
V_{NTC} for current derating		I_{LED} = 98% of nominal voltage	-2.5%	1.25	+2.5%	V
		I_{LED} = 74% of nominal voltage	-2.5%	0.89	+2.5%	V
		I_{LED} = 50% of nominal voltage	-2.5%	0.53	+2.5%	V
V_{NTC} threshold for OTP				0.37		V
V_{NTC} deglitch time for OTP		V_{NTC} = 0.3V	180	256	320	µs
V_{NTC} recovery threshold for OTP				0.48		V
Thermal shutdown (7)			155	170	185	°C

Note:

7) Not tested in production. Guaranteed by design and characterization.

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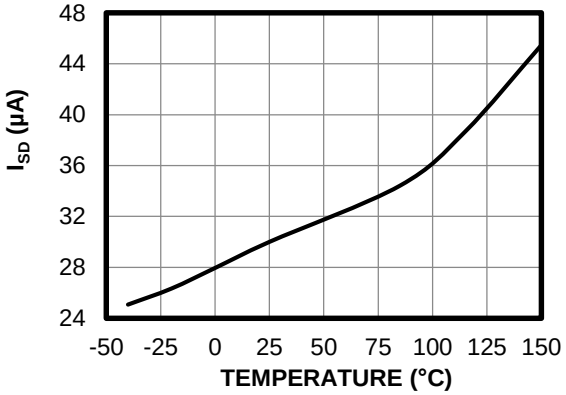
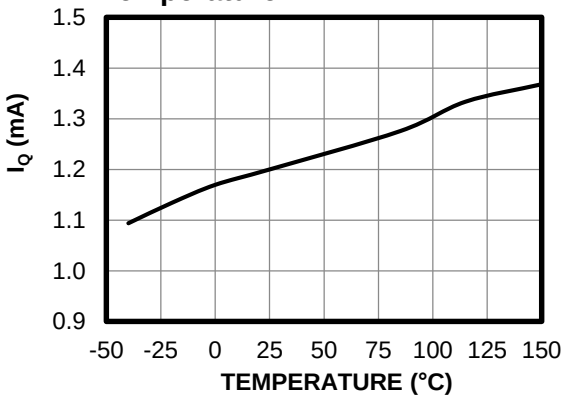
TYPICAL CHARACTERISTICS

V_{IN} = 12V, T_J = -40°C to +150°C, unless otherwise noted.

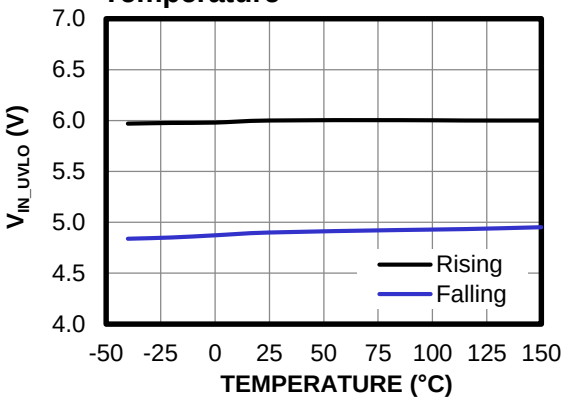
Shutdown Current vs. Temperature



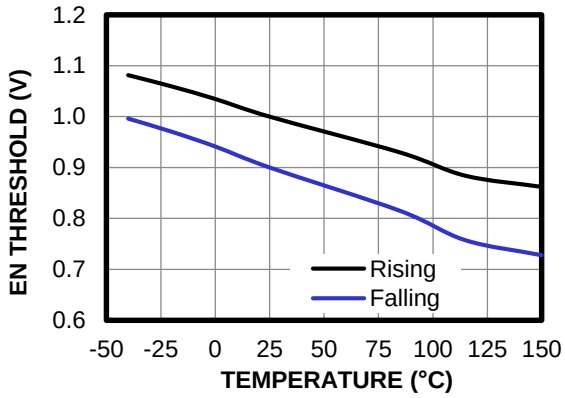
Quiescent Current vs. Temperature



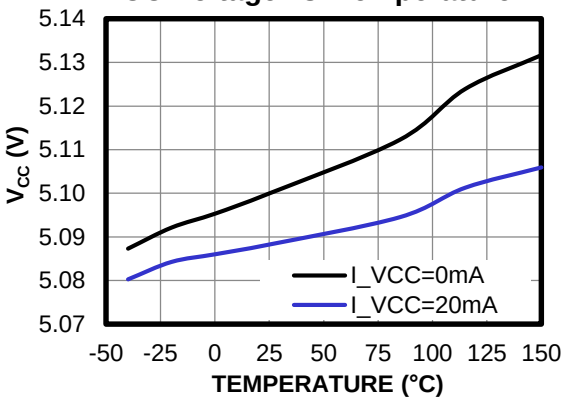
V_{IN} UVLO Threshold vs. Temperature



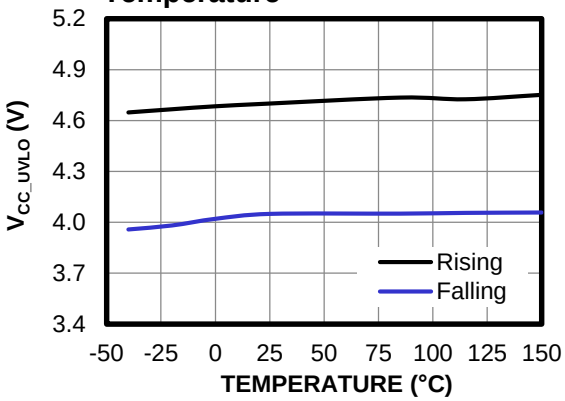
EN Threshold vs. Temperature



VCC Voltage vs. Temperature



V_{CC} UVLO Threshold vs. Temperature



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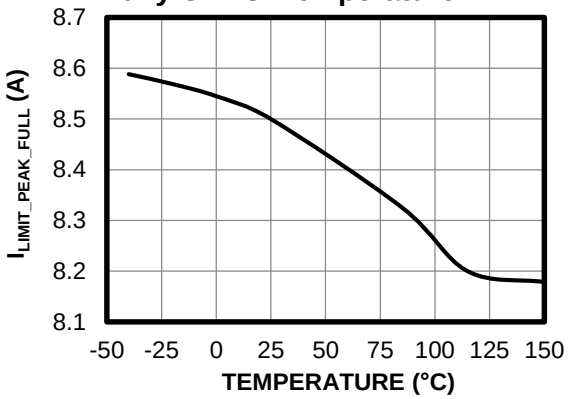
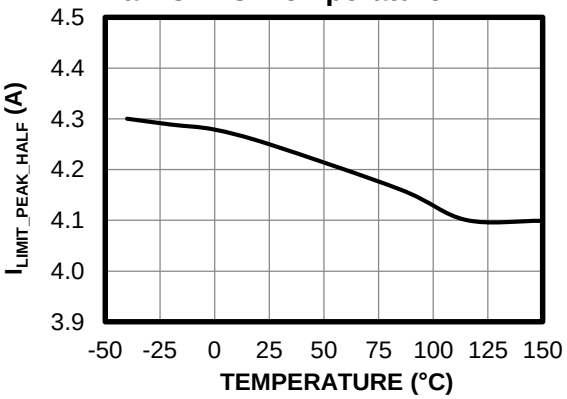
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_J = -40°C to +150°C, unless otherwise noted.

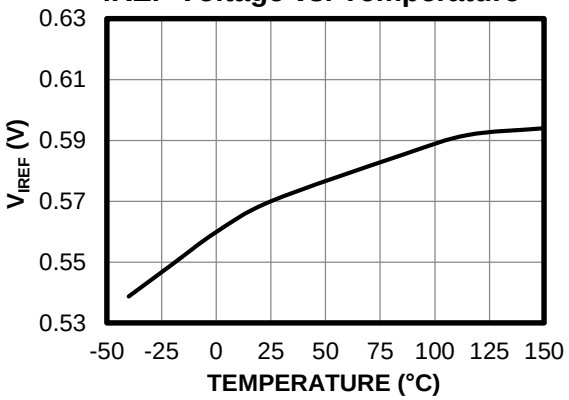
Current Limit with MOSFETs Fully On vs. Temperature



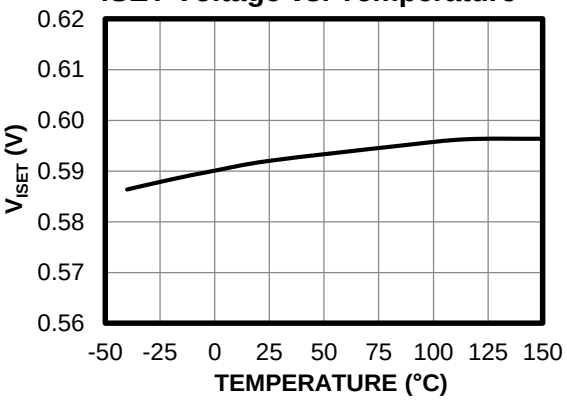
Current Limit with MOSFETs Half-On vs. Temperature



IREF Voltage vs. Temperature

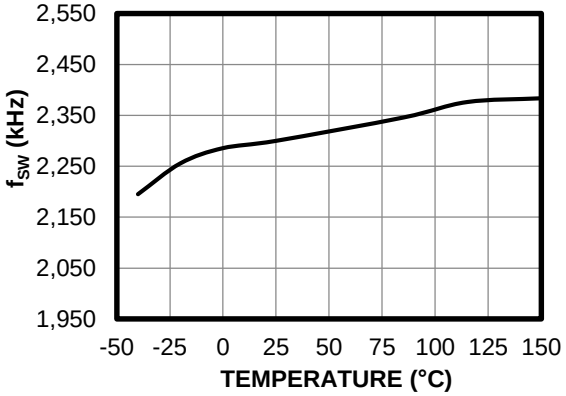


ISET Voltage vs. Temperature



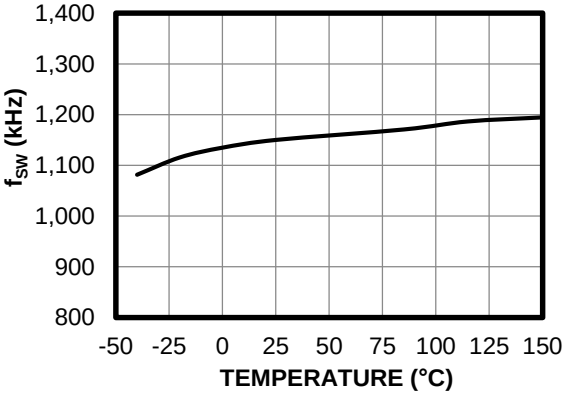
Switching Frequency vs. Temperature

Buck mode



Switching Frequency vs. Temperature

Buck-boost mode



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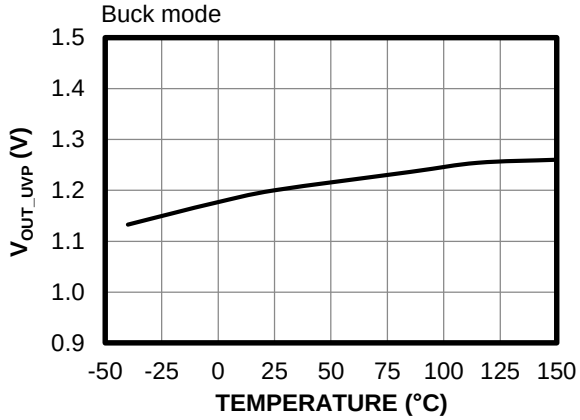
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_J = -40°C to +150°C, unless otherwise noted.

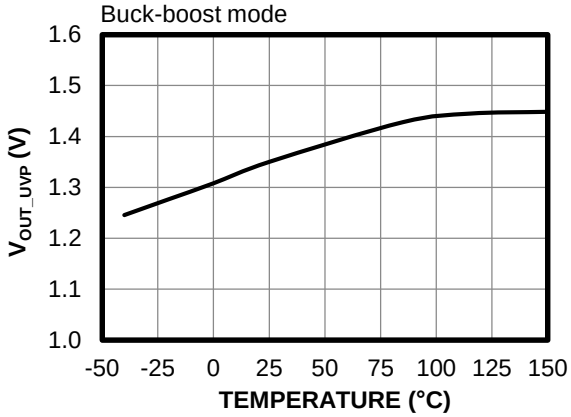
V_{OUT} UVP Threshold vs. Temperature

Buck mode



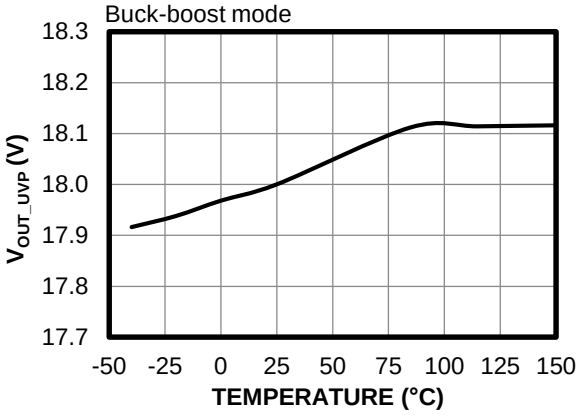
V_{OUT} UVP Threshold vs. Temperature

Buck-boost mode



V_{OUT} UVP Threshold vs. Temperature

Buck-boost mode



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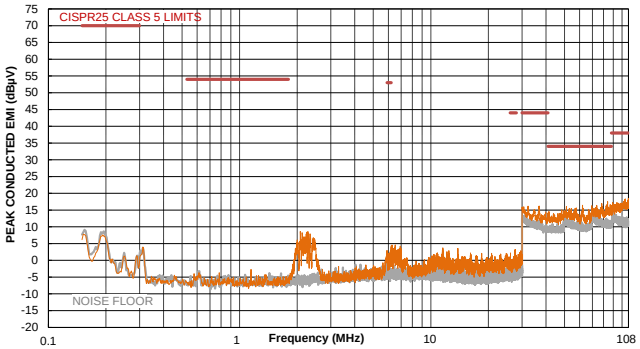
TYPICAL PERFORMANCE CHARACTERISTICS

Buck mode, two LEDs in series (V_{LED} = 6V), V_{IN} = 13.5V, I_{LED} = 3A, f_{SW} = 2.4MHz, L = 3.3µH, with EMI filters, T_A = 25°C, unless otherwise noted. (8)

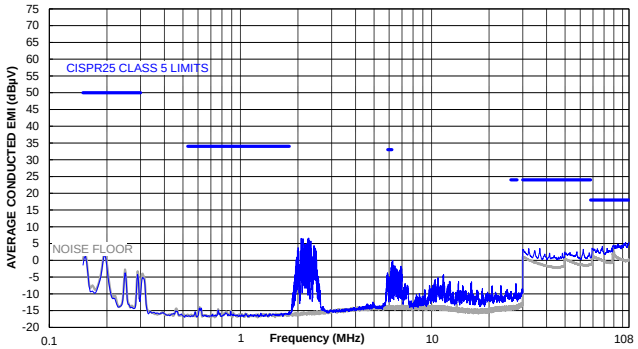
CISPR25 Class 5 Peak Conducted Emissions

150kHz to 108MHz



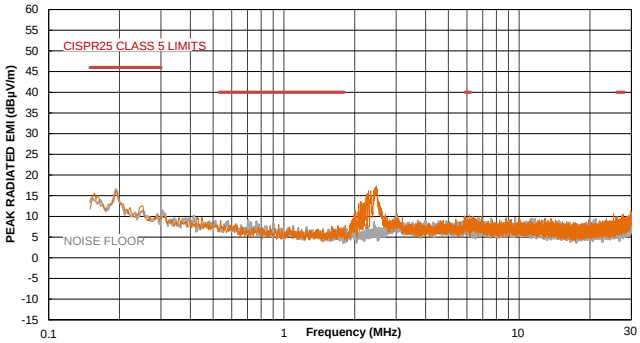
CISPR25 Class 5 Average Conducted Emissions

150kHz to 108MHz



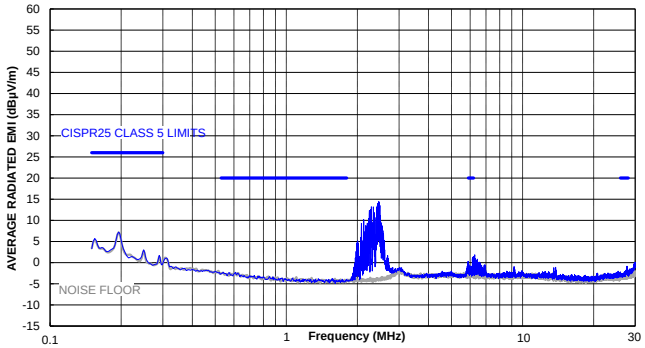
CISPR25 Class 5 Peak Radiated Emissions

150kHz to 30MHz



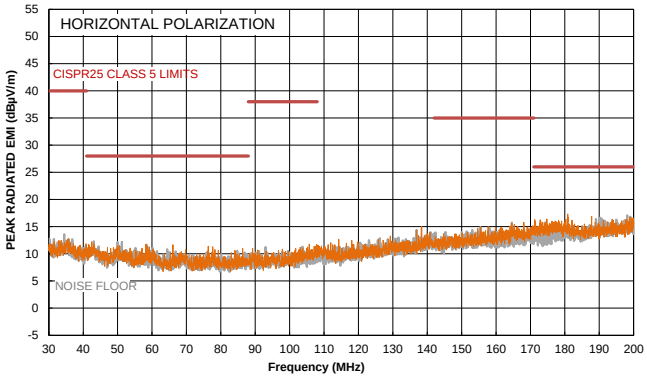
CISPR25 Class 5 Average Radiated Emissions

150kHz to 30MHz



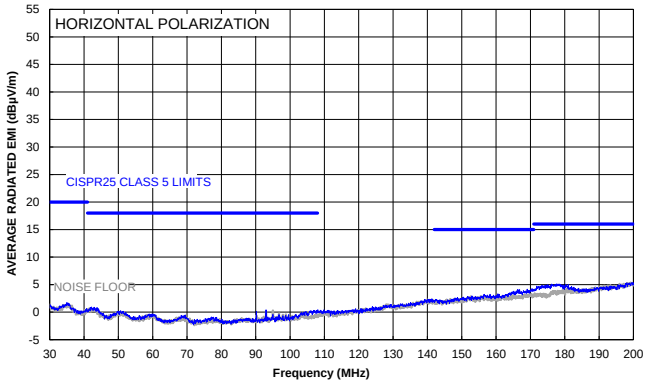
CISPR25 Class 5 Peak Radiated Emissions

Horizontal, 30MHz to 200MHz



CISPR25 Class 5 Average Radiated Emissions

Horizontal, 30MHz to 200MHz



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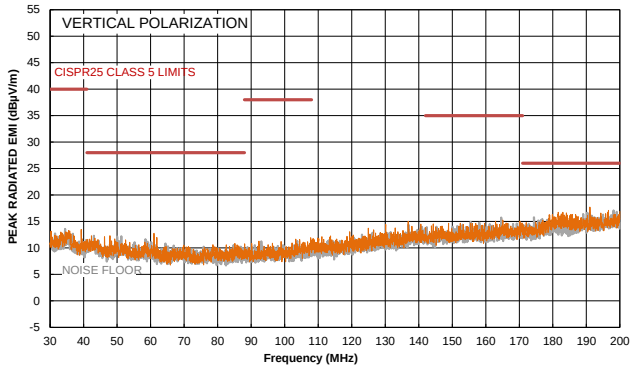
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Buck mode, two LEDs in series (V_{LED} = 6V), V_{IN} = 13.5V, I_{LED} = 3A, f_{SW} = 2.4MHz, L = 3.3µH, with EMI filters, T_A = 25°C, unless otherwise noted. (8)

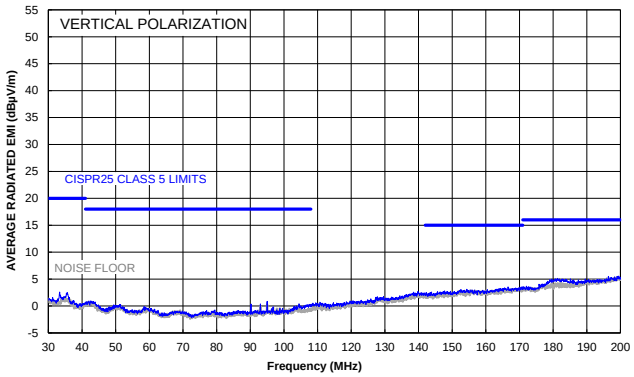
CISPR25 Class 5 Peak Radiated Emissions

Vertical, 30MHz to 200MHz



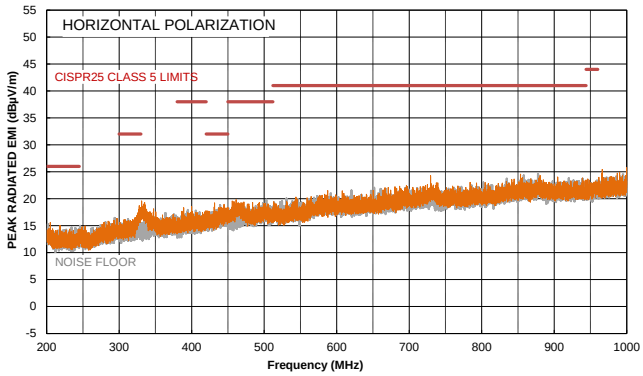
CISPR25 Class 5 Average Radiated Emissions

Vertical, 30MHz to 200MHz



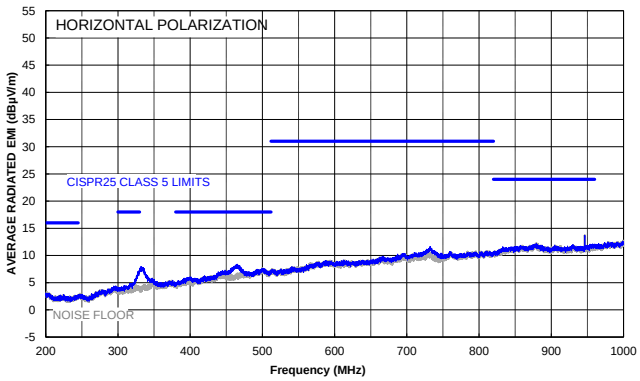
CISPR25 Class 5 Peak Radiated Emissions

Horizontal, 200MHz to 1GHz



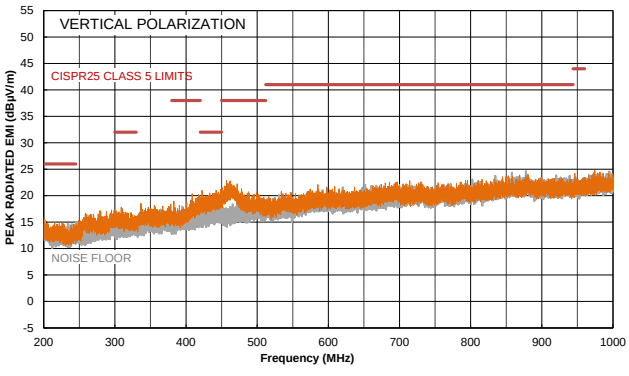
CISPR25 Class 5 Average Radiated Emissions

Horizontal, 200MHz to 1GHz



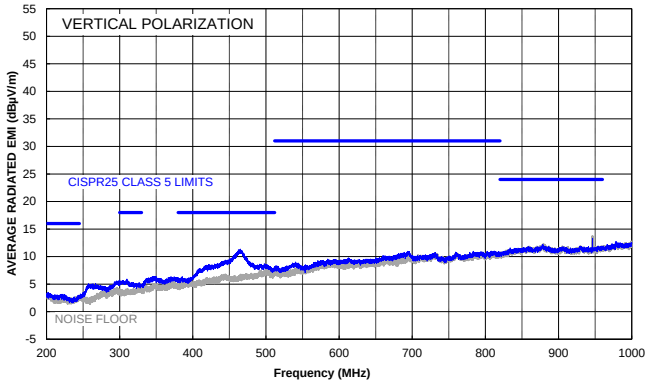
CISPR25 Class 5 Peak Radiated Emissions

Vertical, 200MHz to 1GHz



CISPR25 Class 5 Average Radiated Emissions

Vertical, 200MHz to 1GHz



Note:

8) The MPQ7231's buck mode EMC test results are based on Figure 10 on page 46.

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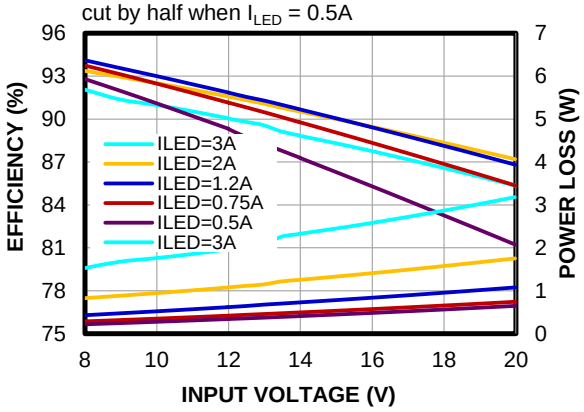
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Buck mode, two LEDs in series (V_{LED} = 6V), V_{IN} = 13.5V, f_{SW} = 2.4MHz, L = 3.3µH, T_A = 25°C, unless otherwise noted. (9)

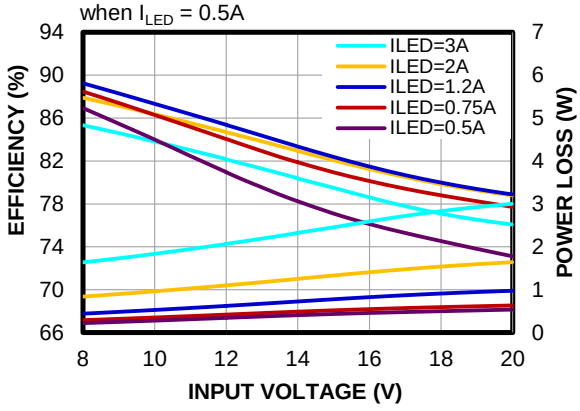
Efficiency vs. Input Voltage vs. Power Loss

2 LEDs, V_{LED} = 6V, the MOSFETs are cut by half when I_{LED} = 0.5A



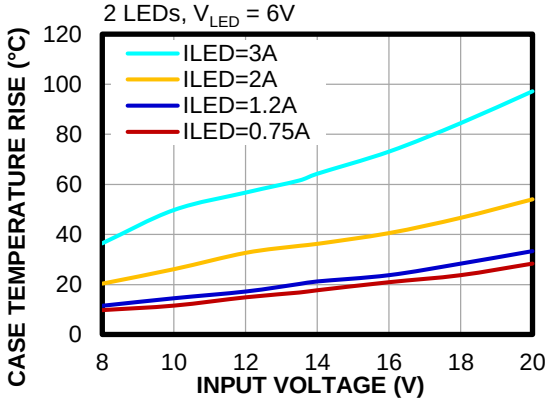
Efficiency vs. Input Voltage vs. Power Loss

V_{LED} = 3V, THE MOSFETs are cut by half when I_{LED} = 0.5A



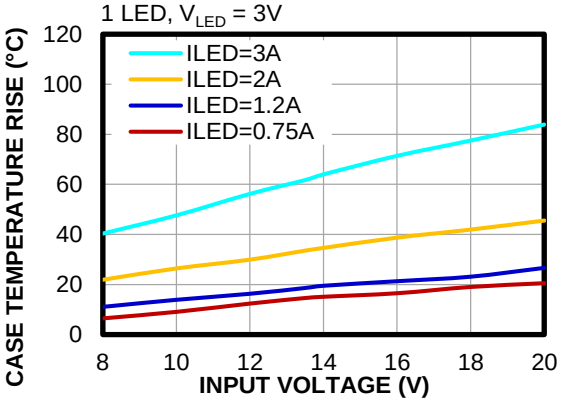
Case Temperature Rise

2 LEDs, V_{LED} = 6V



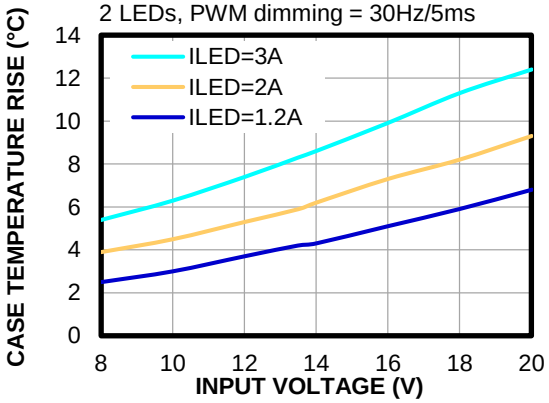
Case Temperature Rise

1 LED, V_{LED} = 3V



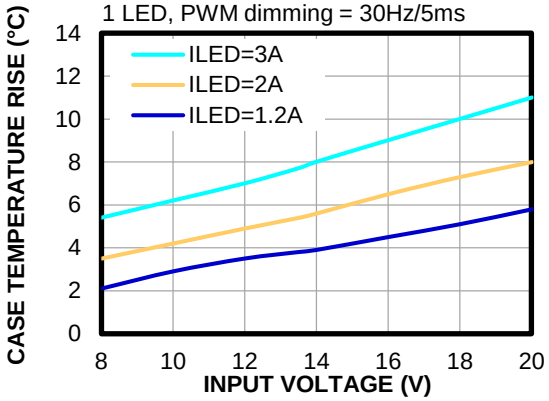
Case Temperature Rise

2 LEDs, PWM dimming = 30Hz/5ms



Case Temperature

1 LED, PWM dimming = 30Hz/5ms



Note:

9) The efficiency and thermal curves are based on Figure 10 on page 46 when R_{BST} = 0Ω, and the output and input filters have been removed. L = 3.3µH (XEL4030-332MEB).

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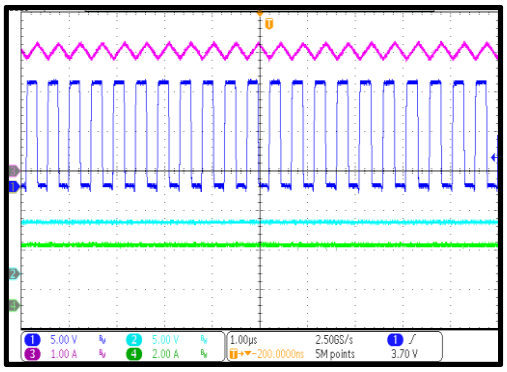
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Buck mode, two LEDs in series (V_{LED} = 6V), V_{IN} = 13.5V, I_{LED} = 3A, f_{SW} = 2.4MHz, L = 3.3µH, T_A = 25°C, unless otherwise noted.

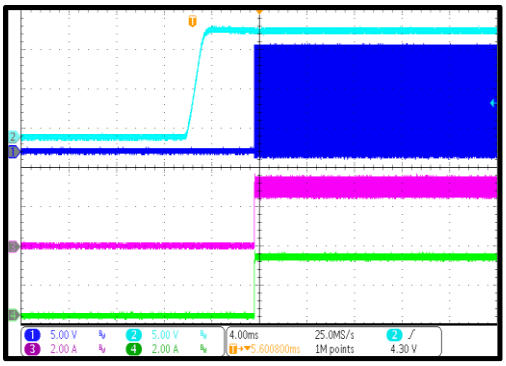
Steady State

I_{LED} = 3A



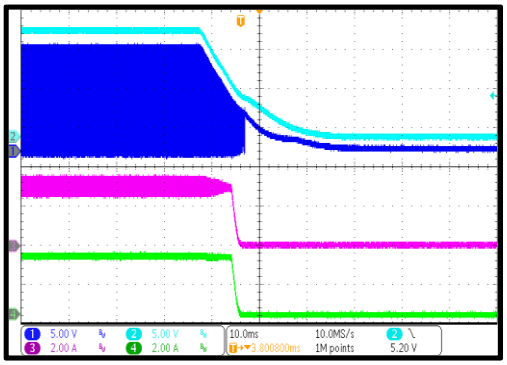
Start-Up through VIN

I_{LED} = 3A



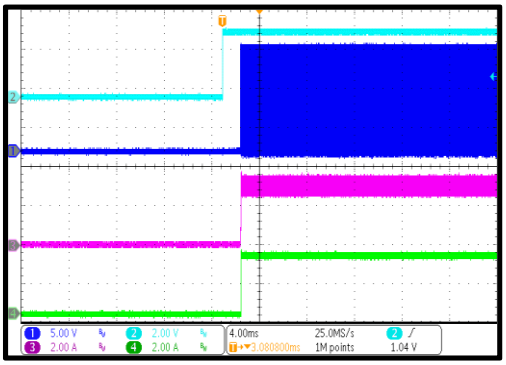
Shutdown through VIN

I_{LED} = 3A



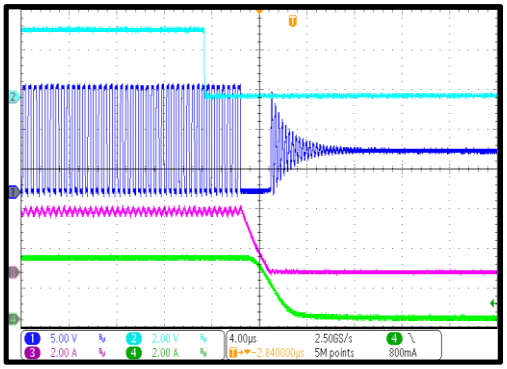
Start-Up through EN

I_{LED} = 3A



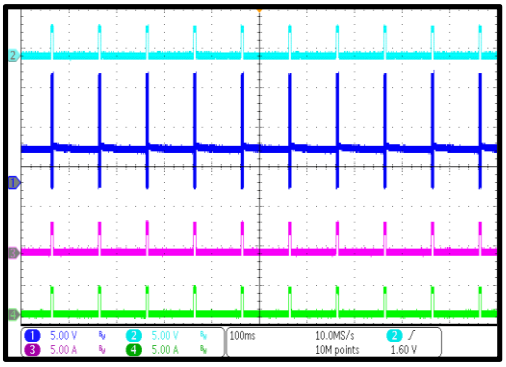
Shutdown through EN

I_{LED} = 3A



PWM Dimming Steady State

Dimming frequency = 10Hz/5ms



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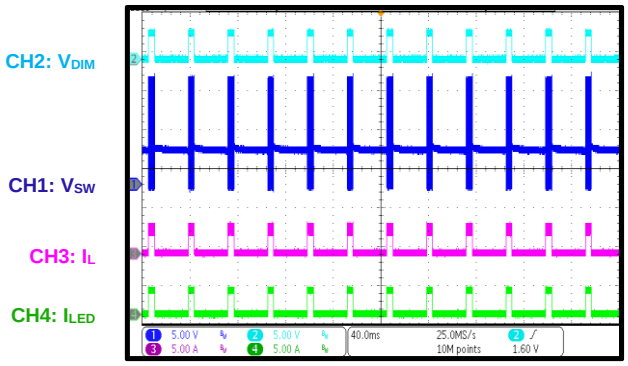
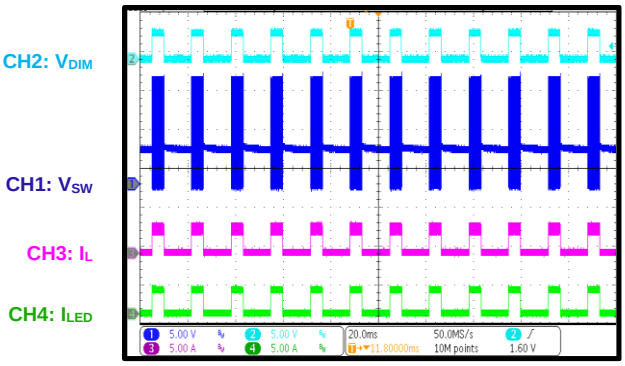
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Buck mode, two LEDs in series (V_{LED} = 6V), V_{IN} = 13.5V, I_{LED} = 3A, f_{SW} = 2.4MHz, L = 3.3µH, T_A = 25°C, unless otherwise noted.

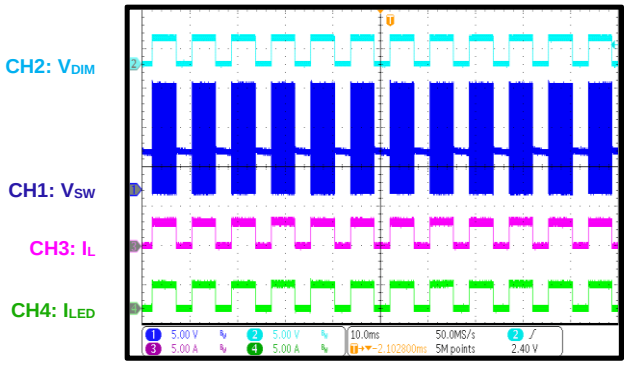
PWM Dimming Steady State
Dimming frequency = 30Hz/5ms



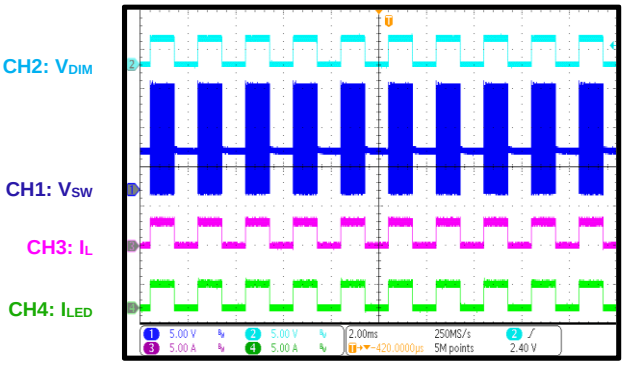
PWM Dimming Steady State
Dimming frequency = 60Hz/5ms



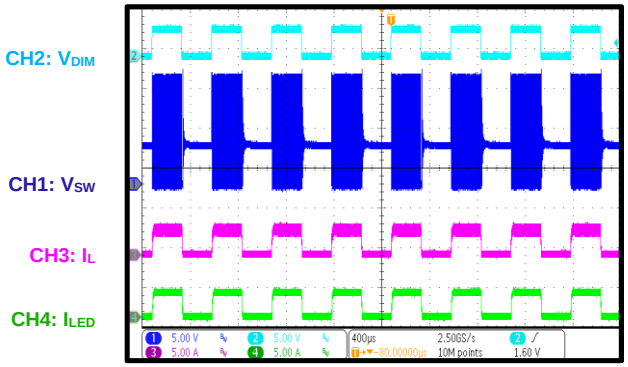
PWM Dimming Steady State
Dimming frequency = 120Hz/5ms



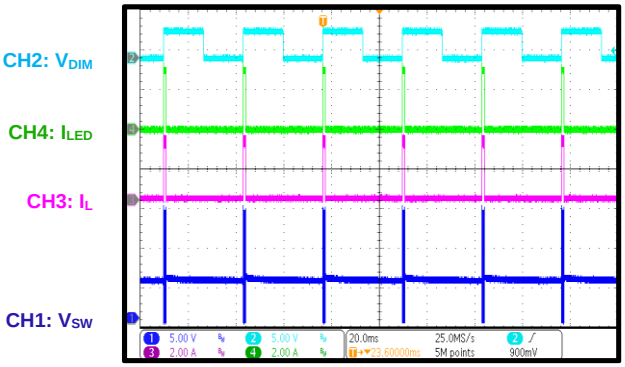
PWM Dimming Steady State
Dimming frequency = 500Hz/50%



PWM Dimming Steady State
Dimming frequency = 2kHz/50%



PWM Dimming Steady State
With 1ms DIM on time limit



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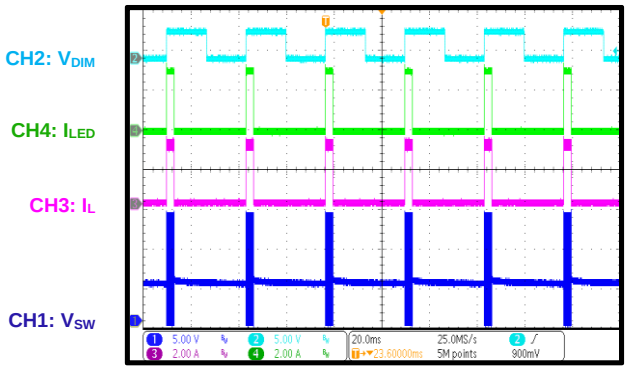
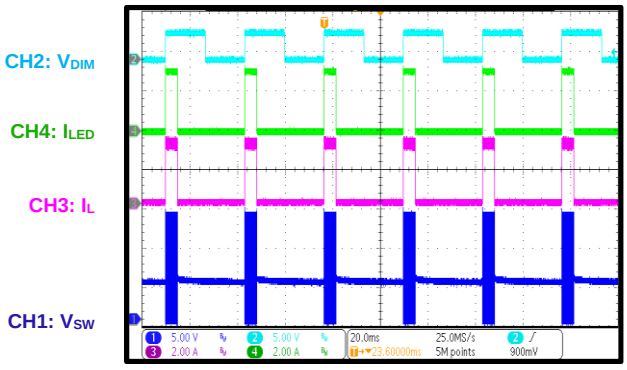
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Buck mode, two LEDs in series (V_{LED} = 6V), V_{IN} = 13.5V, I_{LED} = 3A, f_{SW} = 2.4MHz, L = 3.3µH, T_A = 25°C, unless otherwise noted.

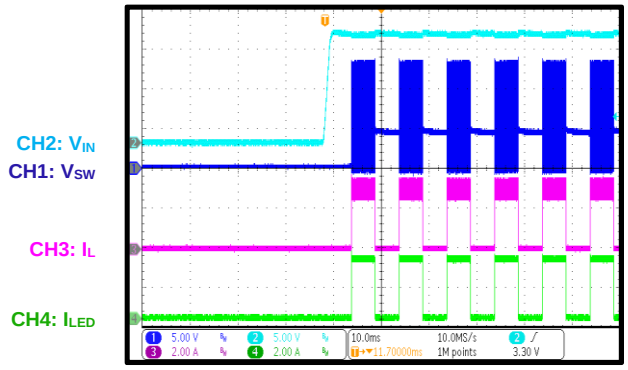
PWM Dimming Steady State
With 3ms DIM on time limit



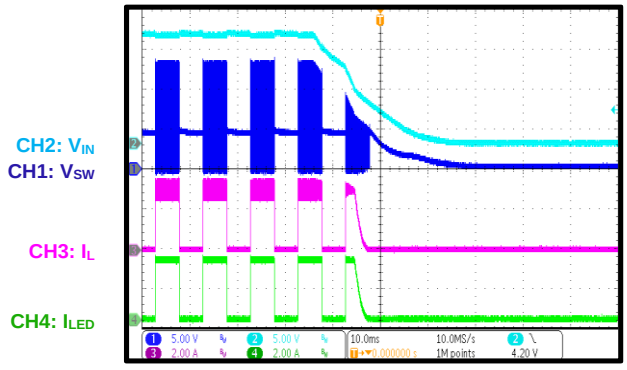
PWM Dimming Steady State
With 5ms DIM on time limit



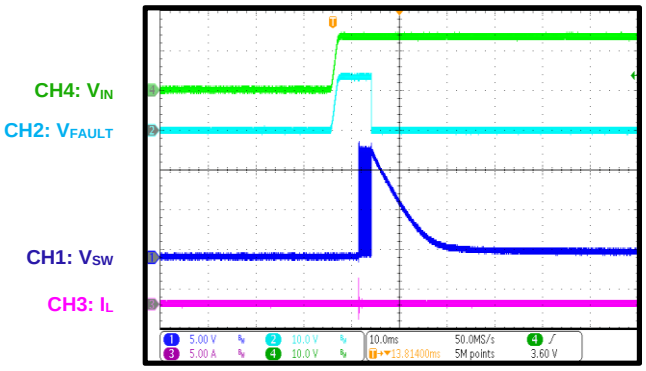
PWM Dimming
Start-up through VIN



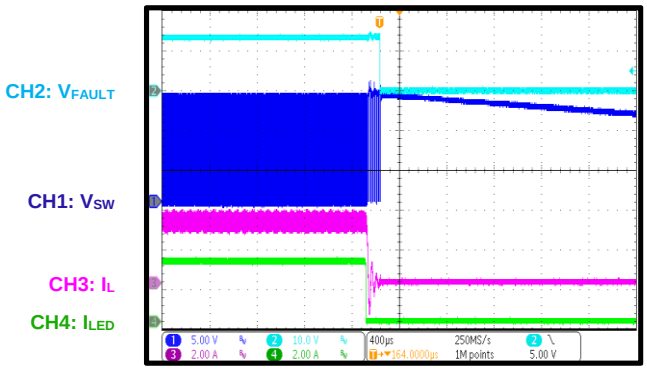
PWM Dimming
Shutdown through VIN



No Dimming
LED open input start-up



No Dimming
LED open entry



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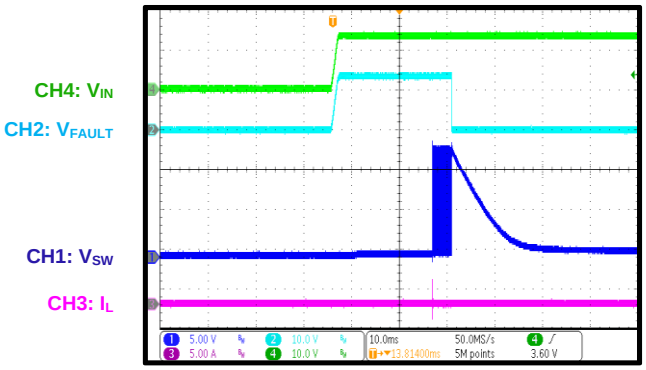
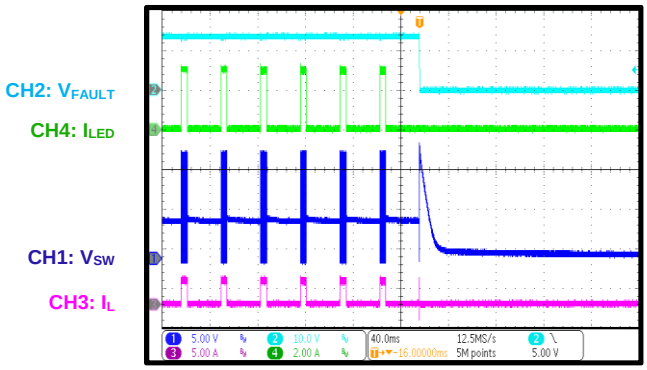
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Buck mode, two LEDs in series (V_{LED} = 6V), V_{IN} = 13.5V, I_{LED} = 3A, f_{SW} = 2.4MHz, L = 3.3µH, T_A = 25°C, unless otherwise noted.

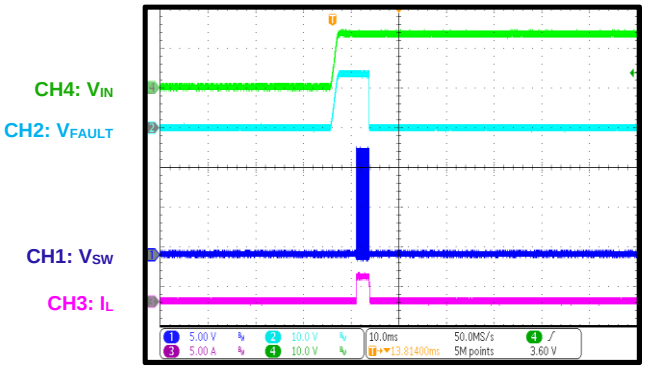
PWM Dimming
LED open input start-up



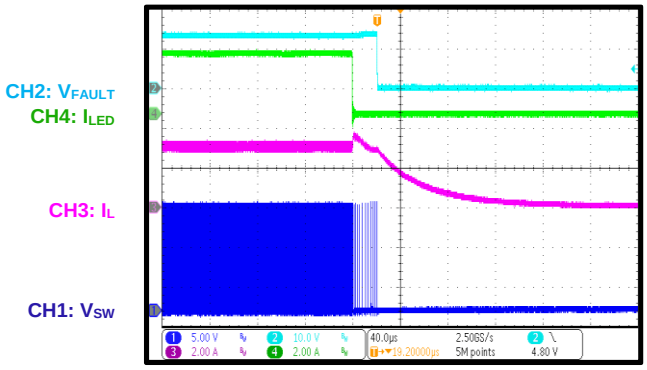
PWM Dimming
LED open entry



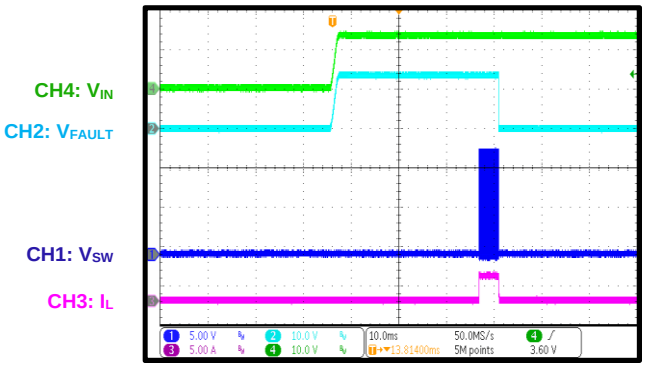
No Dimming
LED+ short to LED- start-up



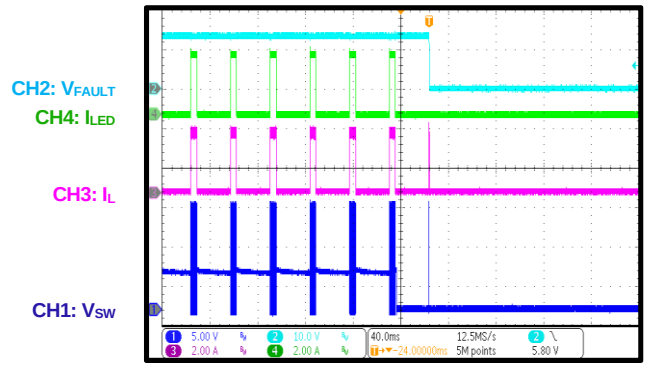
No Dimming
LED+ short to LED- entry



PWM Dimming
LED+ short to LED- start-up



PWM Dimming
LED+ short to LED- entry



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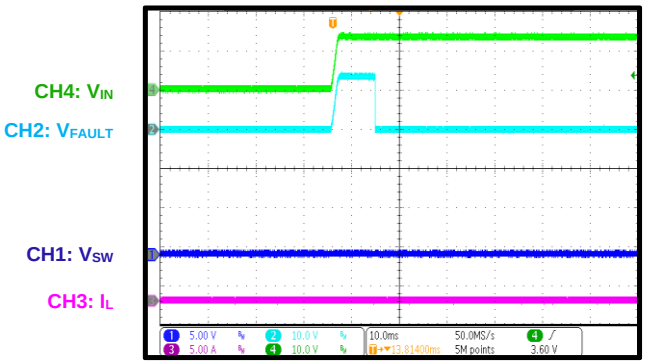
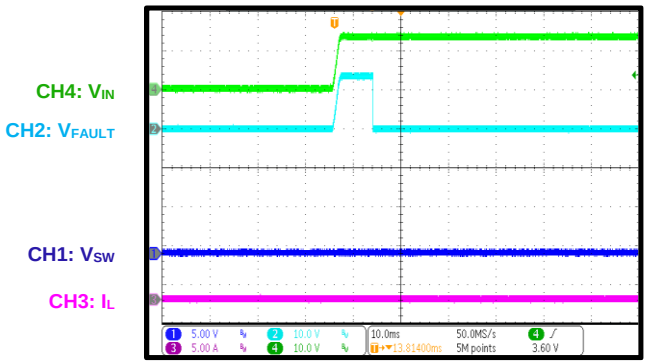
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Buck mode, two LEDs in series (V_{LED} = 6V), V_{IN} = 13.5V, I_{LED} = 3A, f_{SW} = 2.4MHz, L = 3.3µH, T_A = 25°C, unless otherwise noted.

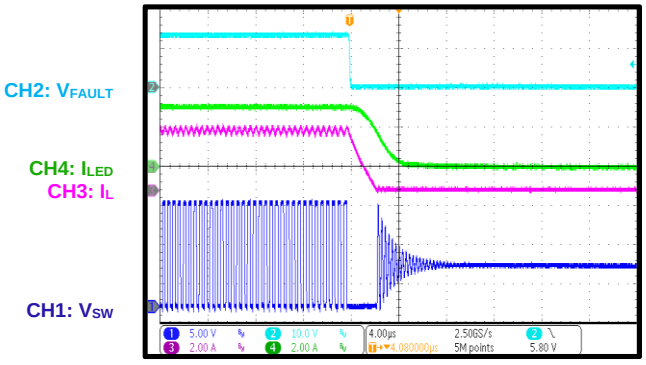
IREF Short Fault before IC Start-Up



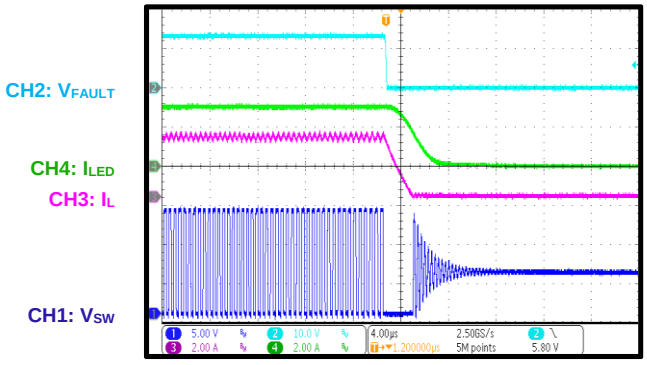
IREF Open Fault before IC Start-Up



IREF Short Fault after IC Start-Up

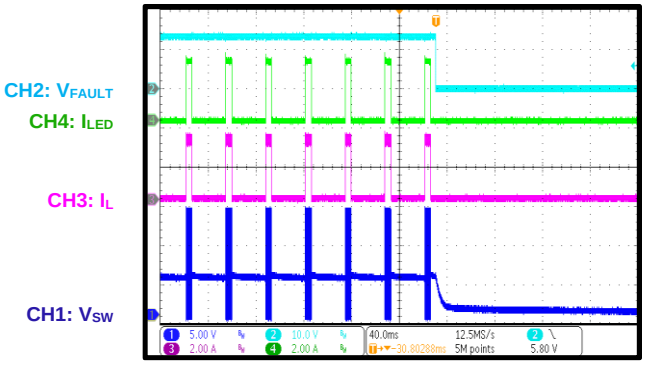


IREF Open Fault after IC Start-Up



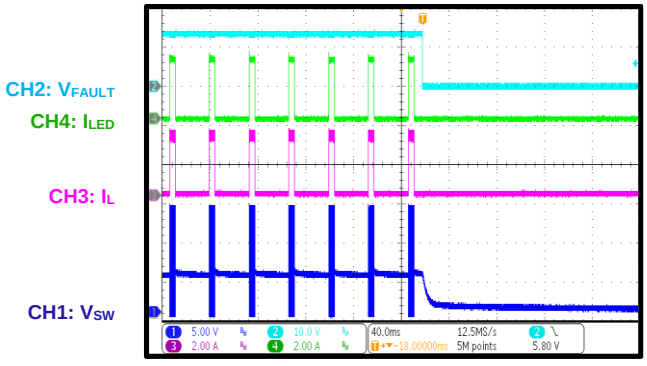
PWM Dimming

IREF short fault after the IC starts up



PWM Dimming

IREF open fault after the IC starts up



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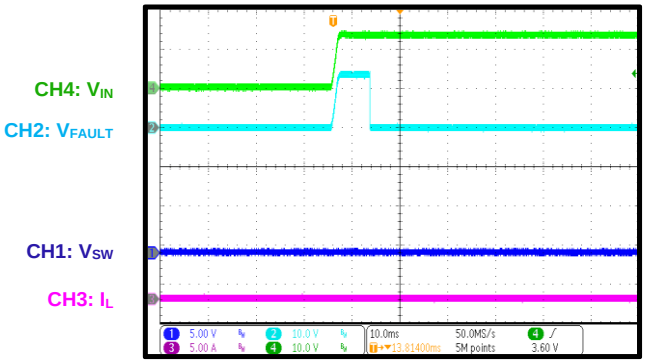
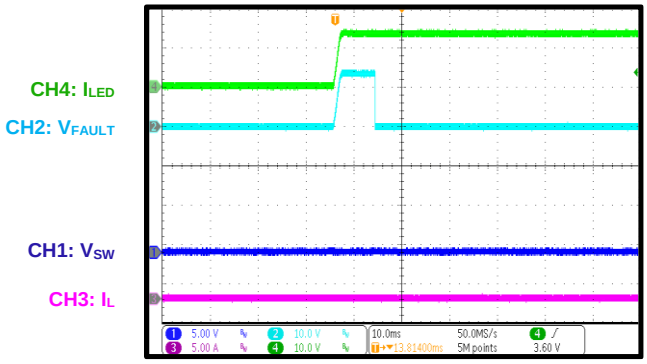
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Buck mode, two LEDs in series (V_{LED} = 6V), V_{IN} = 13.5V, I_{LED} = 3A, f_{SW} = 2.4MHz, L = 3.3µH, T_A = 25°C, unless otherwise noted.

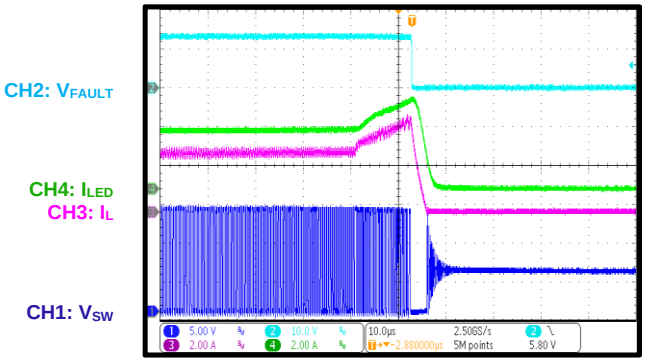
ISET Short Fault before IC Start-Up



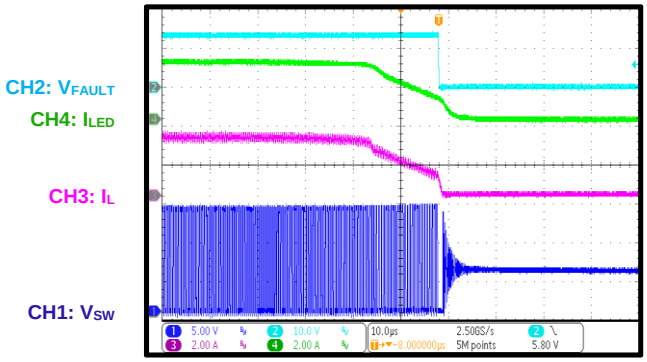
ISET Open Fault before IC Start-Up



ISET Short Fault after IC Start-Up

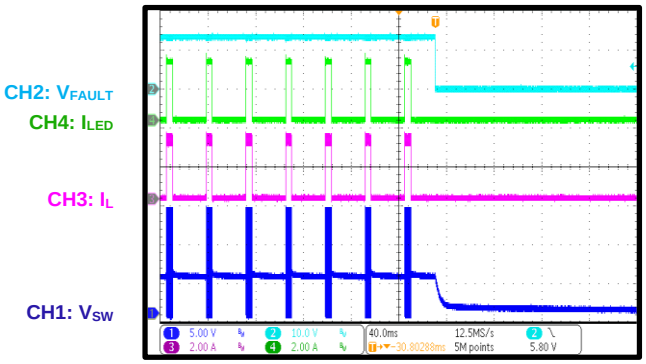


ISET Open Fault after IC Start-Up



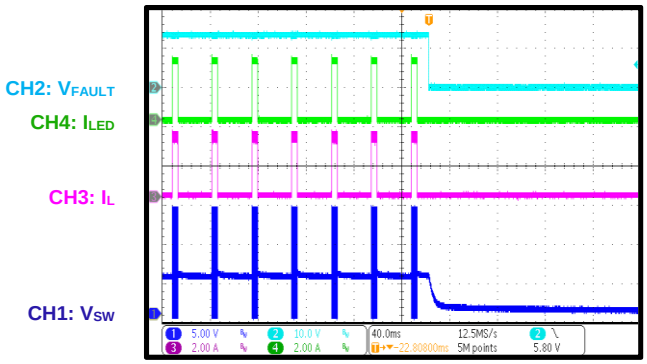
PWM Dimming

ISET short fault after the IC starts up



PWM Dimming

ISET open fault after the IC starts up



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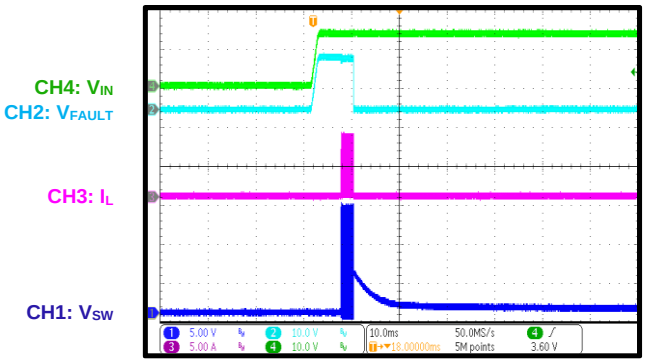
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Buck mode, two LEDs in series (V_{LED} = 6V), V_{IN} = 13.5V, I_{LED} = 3A, f_{SW} = 2.4MHz, L = 3.3µH, T_A = 25°C, unless otherwise noted.

False Mode Detection during Start-Up through VIN



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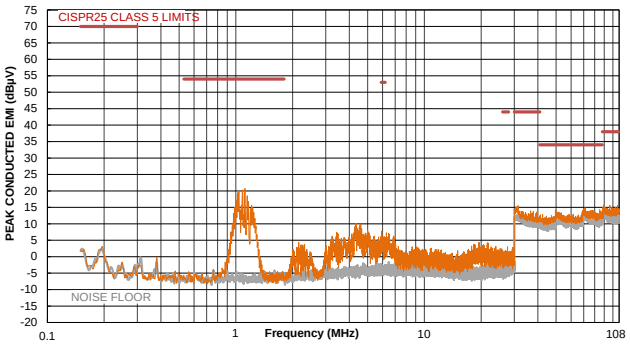
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Buck-boost mode, three LEDs in series (V_{LED} = 9V), V_{IN} = 13.5V, I_{LED} = 1.2A, f_{SW} = 1.25MHz, L = 3.3µH, with EMI filters, T_A = 25°C, unless otherwise noted. (10)

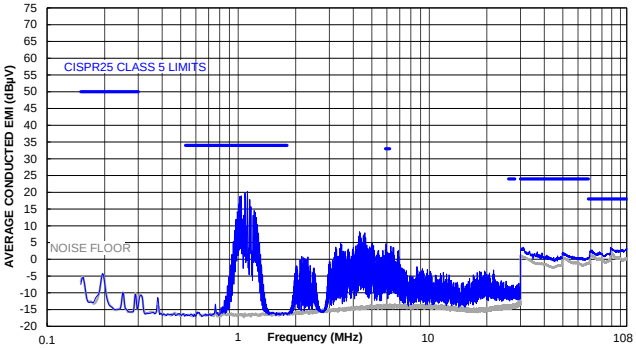
CISPR25 Class 5 Peak Conducted Emissions

150kHz to 108MHz



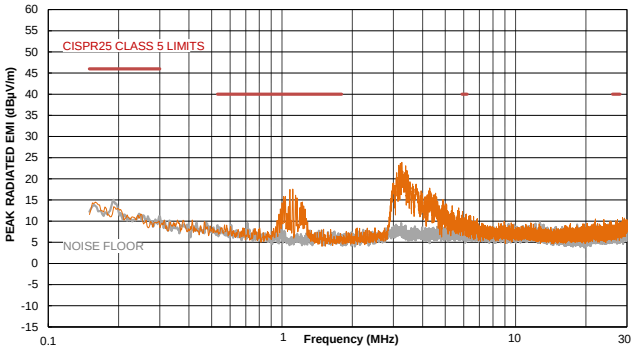
CISPR25 Class 5 Average Conducted Emissions

150kHz to 108MHz



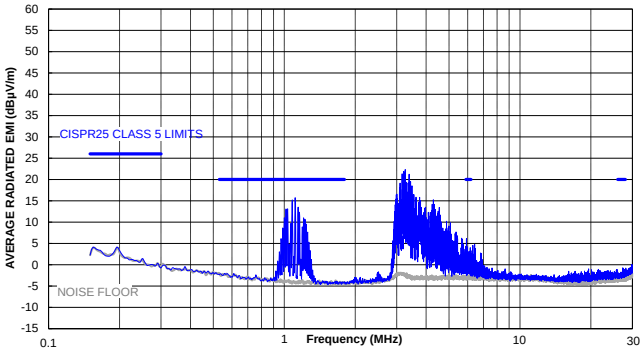
CISPR25 Class 5 Peak Radiated Emissions

150kHz to 30MHz



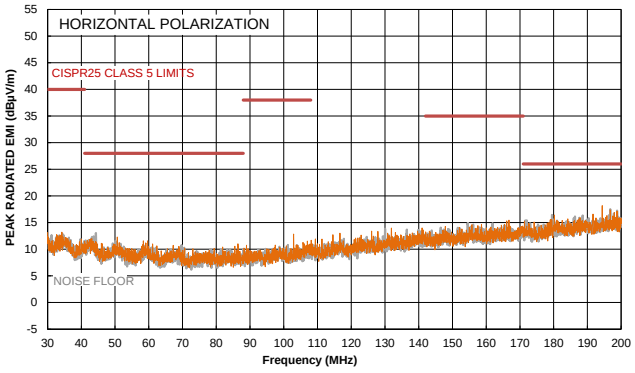
CISPR25 Class 5 Average Radiated Emissions

150kHz to 30MHz



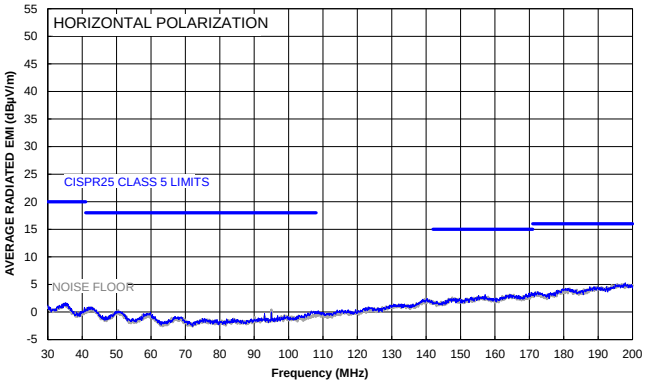
CISPR25 Class 5 Peak Radiated Emissions

Horizontal, 30MHz to 200MHz



CISPR25 Class 5 Average Radiated Emissions

Horizontal, 30MHz to 200MHz



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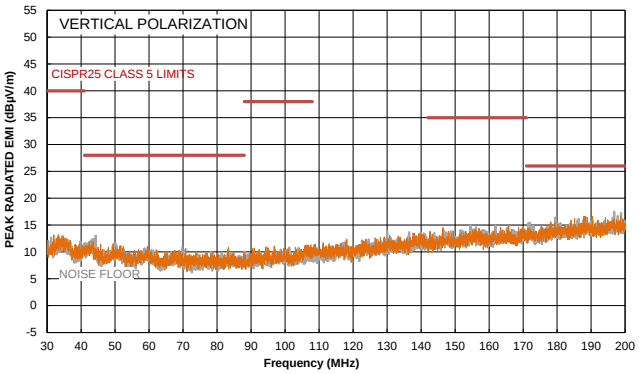
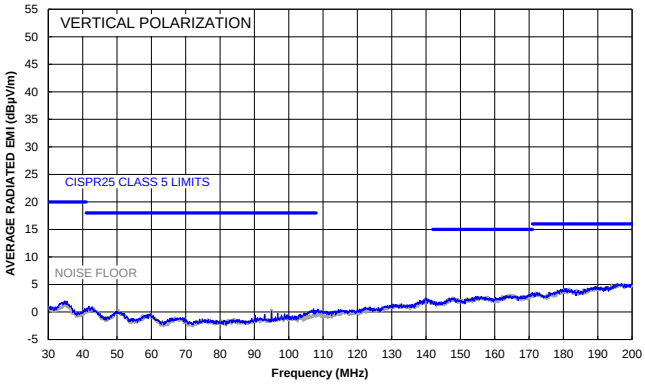
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Buck-boost mode, three LEDs in series (V_{LED} = 9V), V_{IN} = 13.5V, I_{LED} = 1.2A, f_{SW} = 1.25MHz, L = 3.3µH with EMI filters, T_A = 25°C, unless otherwise noted. (10)

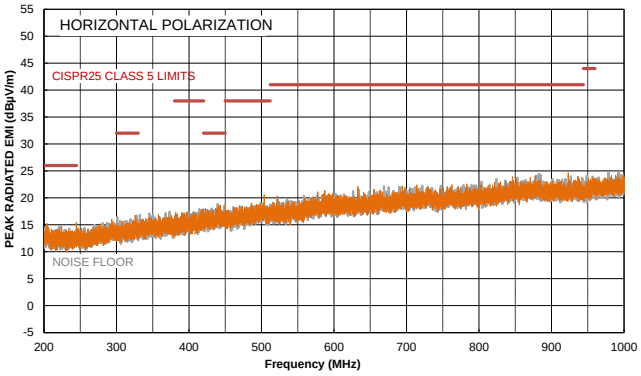
CISPR25 Class 5 Peak Radiated Emissions
Vertical, 30MHz to 200MHz



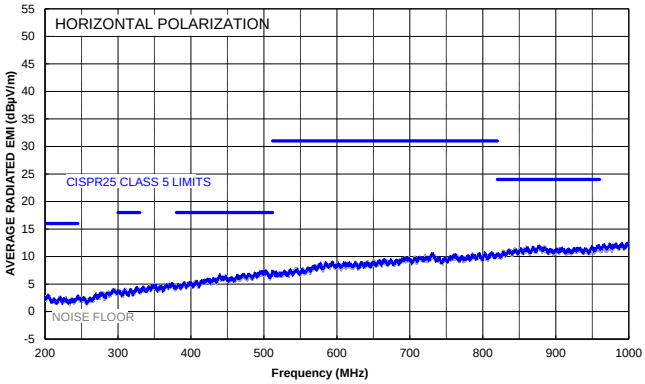
CISPR25 Class 5 Average Radiated Emissions
Vertical, 30MHz to 200MHz



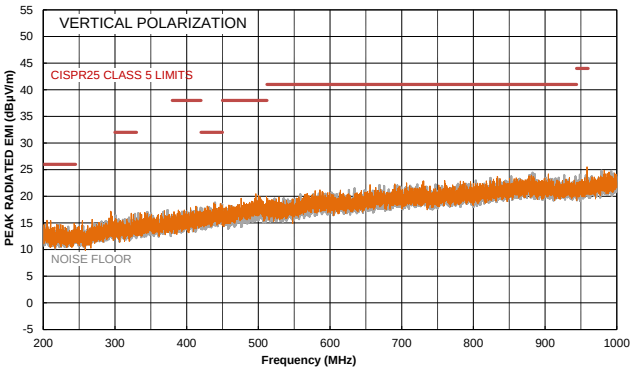
CISPR25 Class 5 Peak Radiated Emissions
Horizontal, 200MHz to 1GHz



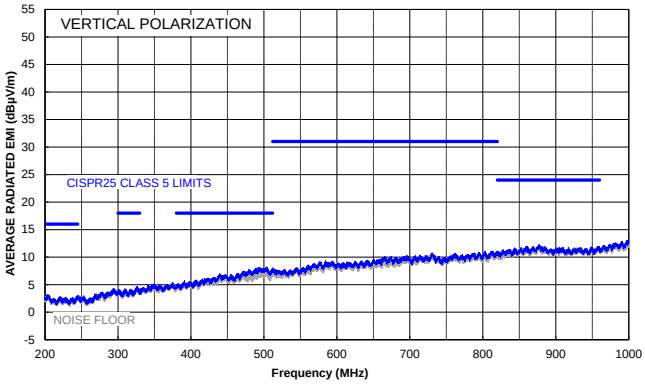
CISPR25 Class 5 Average Radiated Emissions
Horizontal, 200MHz to 1GHz



CISPR25 Class 5 Peak Radiated Emissions
Vertical, 200MHz to 1GHz



CISPR25 Class 5 Average Radiated Emissions
Vertical, 200MHz to 1GHz



Note:

10) The MPQ7231's buck-boost mode EMC test results are based on Figure 11 on page 46.

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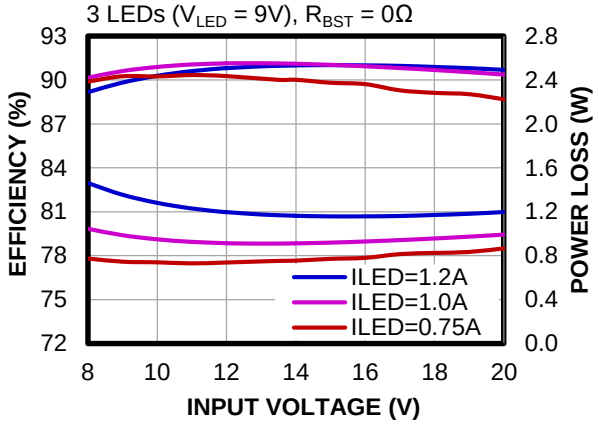
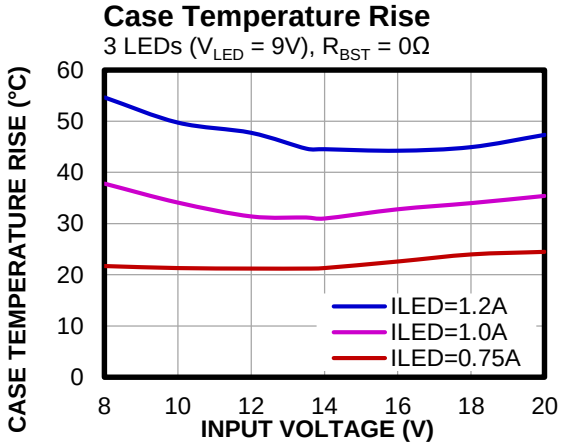
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Buck-boost mode, three LEDs in series (V_{LED} = 9V), V_{IN} = 13.5V, f_{SW} = 1.25MHz, L = 3.3µH, T_A = 25°C, unless otherwise noted. (11)

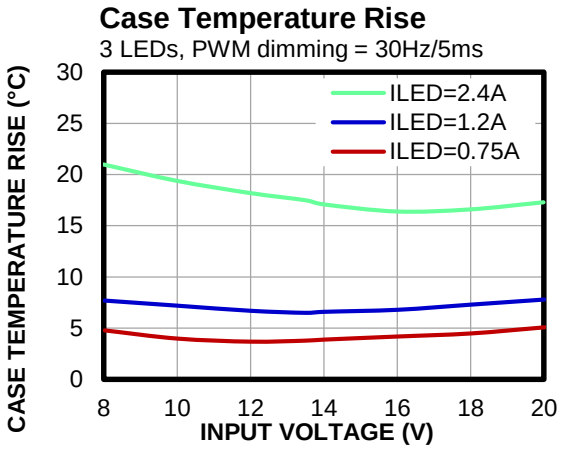
Efficiency vs. Input Voltage vs. Power Loss



Case Temperature Rise



Case Temperature Rise



Note:

11) The efficiency and thermal curves are based on Figure 11 on page 46 when R_{BST} = 0Ω, and the output and input filters have been removed. L = 3.3µH (XEL4030-332MEB).

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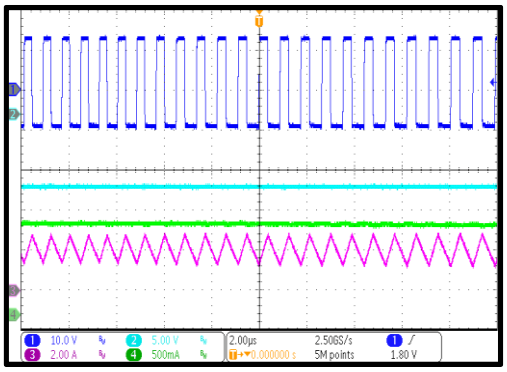
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Buck-boost mode, three LEDs in series (V_{LED} = 9V), V_{IN} = 13.5V, I_{LED} = 1.2A, f_{SW} = 1.25MHz, L = 3.3µH, T_A = 25°C, unless otherwise noted.

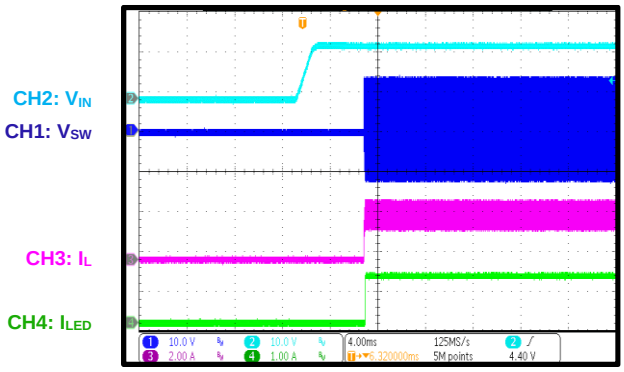
Steady State

I_{LED} = 1.2A



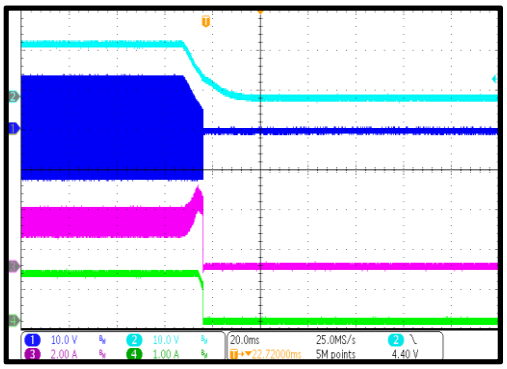
Start-Up through VIN

I_{LED} = 1.2A



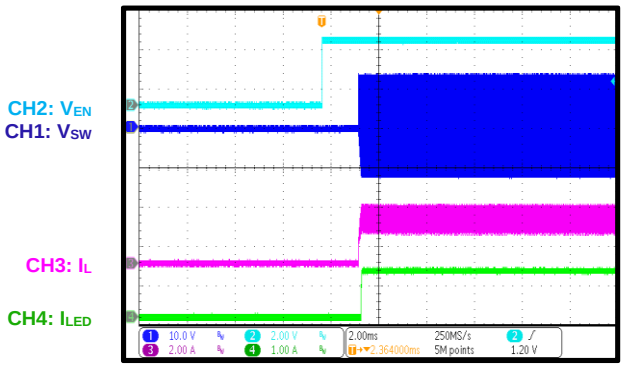
Shutdown through VIN

I_{LED} = 1.2A



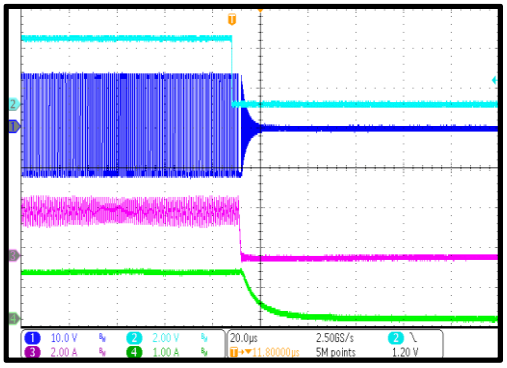
Start-Up through EN

I_{LED} = 1.2A



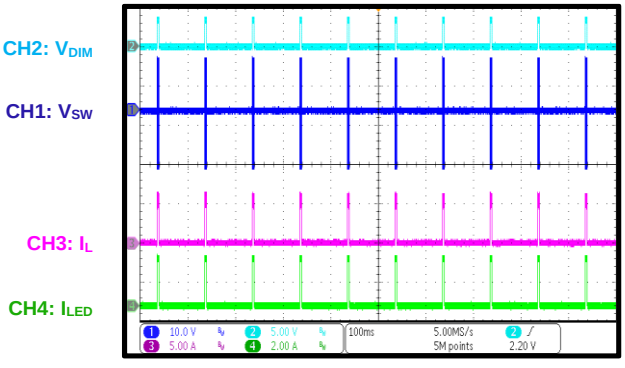
Shutdown through EN

I_{LED} = 1.2A



PWM Dimming Steady State

Dimming frequency = 10Hz/5ms,
I_{LED_PEAK} = 2.4A



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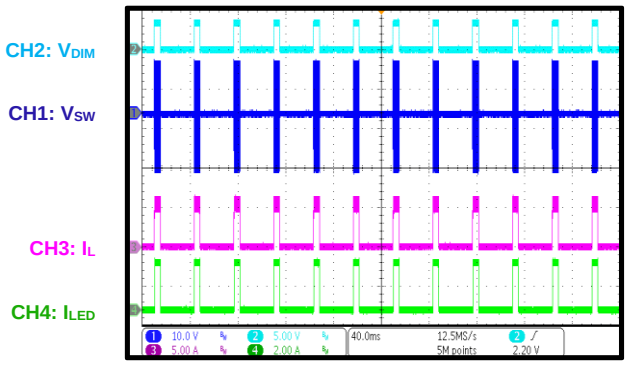
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Buck-boost mode, three LEDs in series (V_{LED} = 9V), V_{IN} = 13.5V, I_{LED} = 1.2A, f_{SW} = 1.25MHz, L = 3.3µH, T_A = 25°C, unless otherwise noted.

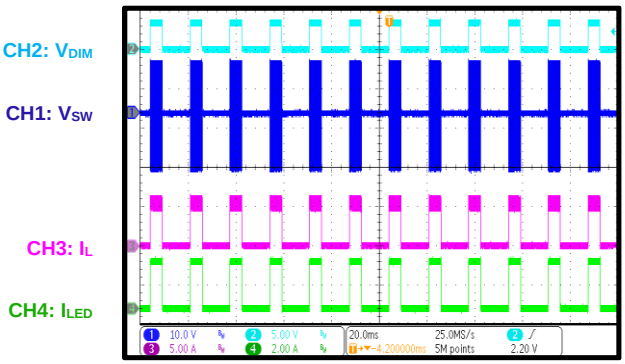
PWM Dimming Steady State

Dimming frequency = 30Hz/5ms,
I_{LED_PEAK} = 2.4A



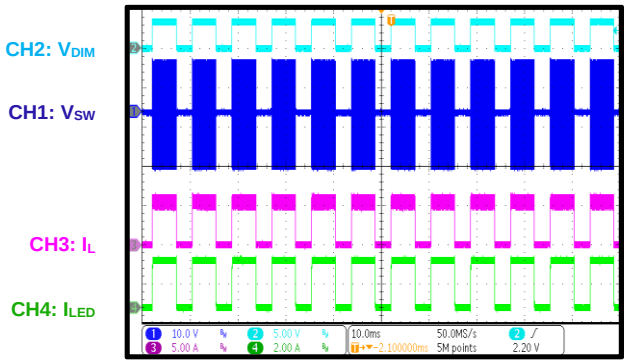
PWM Dimming Steady State

Dimming frequency = 60Hz/5ms,
I_{LED_PEAK} = 2.4A



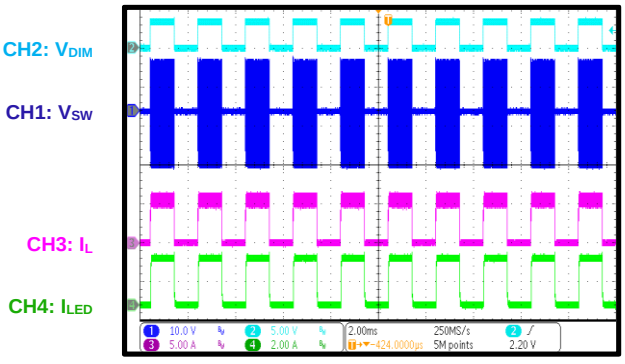
PWM Dimming Steady State

Dimming frequency = 120Hz/5ms,
I_{LED_PEAK} = 2.4A



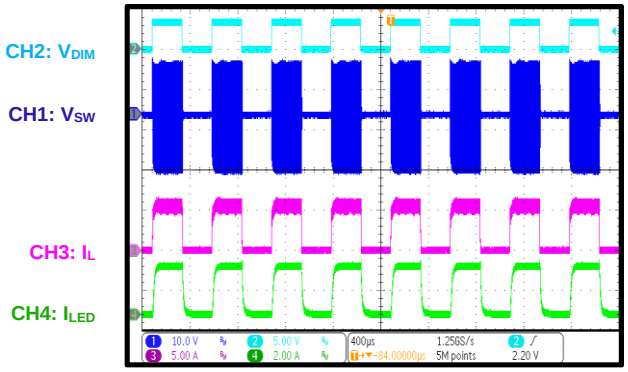
PWM Dimming Steady State

Dimming frequency = 500Hz/50%,
I_{LED_PEAK} = 2.4A



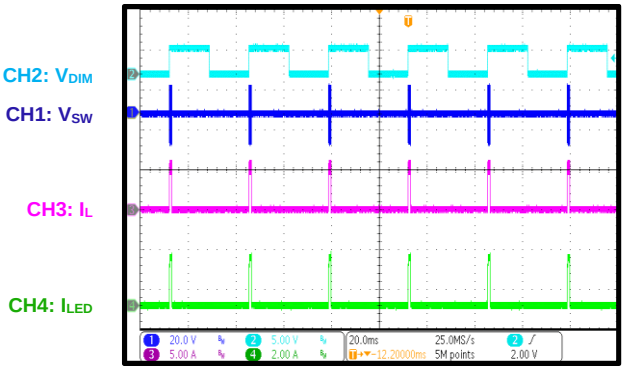
PWM Dimming Steady State

Dimming frequency = 2kHz/50%,
I_{LED_PEAK} = 2.4A



PWM Dimming Steady State

With 1ms DIM on time limit, I_{LED_PEAK} = 2.4A



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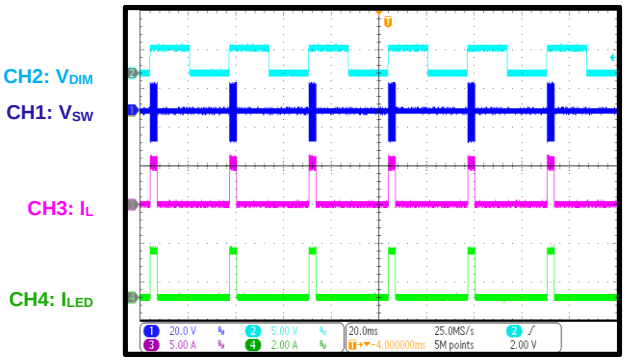
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Buck-boost mode, three LEDs in series (V_{LED} = 9V), V_{IN} = 13.5V, I_{LED} = 1.2A, f_{SW} = 1.25MHz, L = 3.3µH, T_A = 25°C, unless otherwise noted.

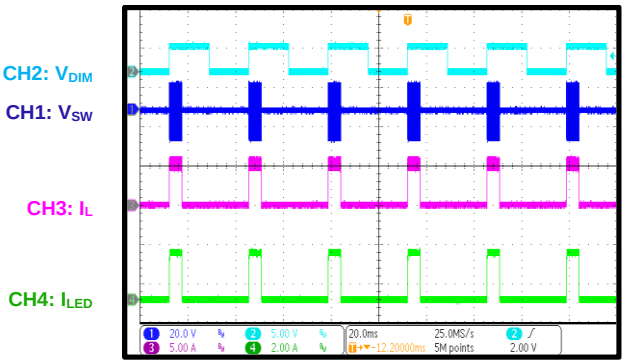
PWM Dimming Steady State

With 3ms DIM on time limit, I_{LED_PEAK} = 2.4A



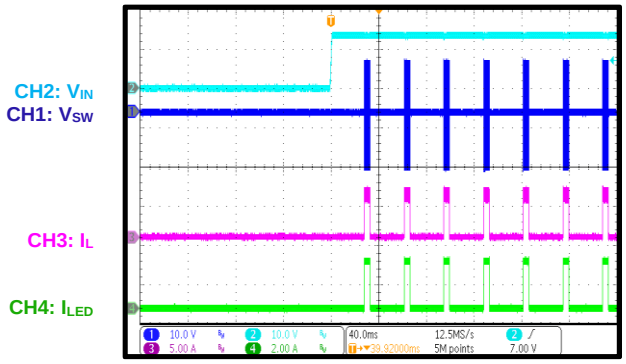
PWM Dimming Steady State

With 5ms DIM on time limit, I_{LED_PEAK} = 2.4A



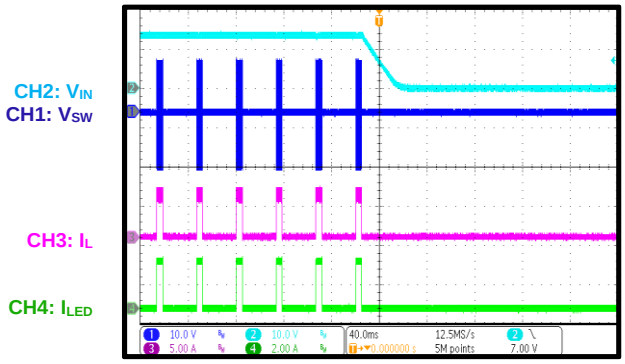
PWM Dimming

Start-up through VIN, I_{LED_PEAK} = 2.4A



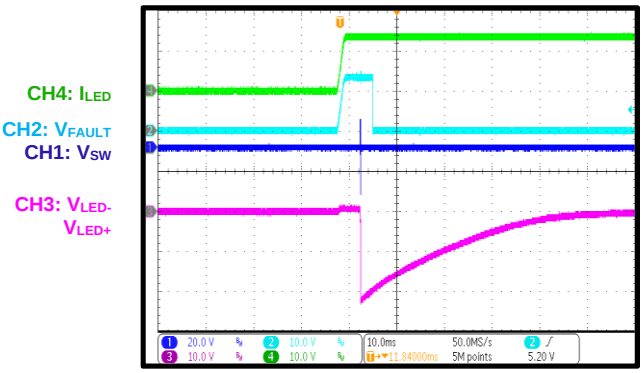
PWM Dimming

Shutdown through VIN, I_{LED_PEAK} = 2.4A



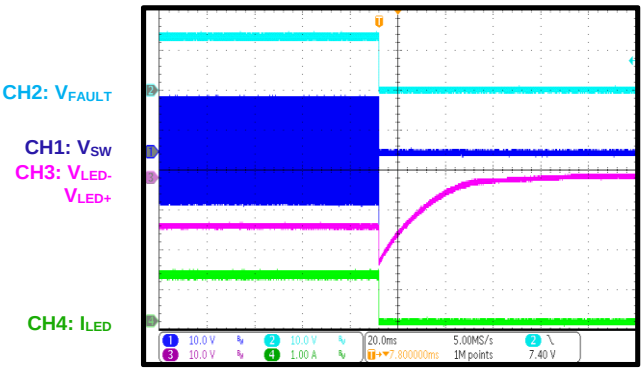
No Dimming

LED open input start-up



No Dimming

LED open entry



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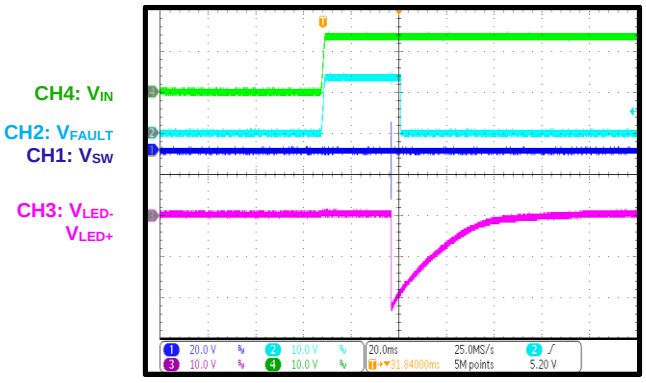
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Buck-boost mode, three LEDs in series (V_{LED} = 9V), V_{IN} = 13.5V, I_{LED} = 1.2A, f_{SW} = 1.25MHz, L = 3.3µH, T_A = 25°C, unless otherwise noted.

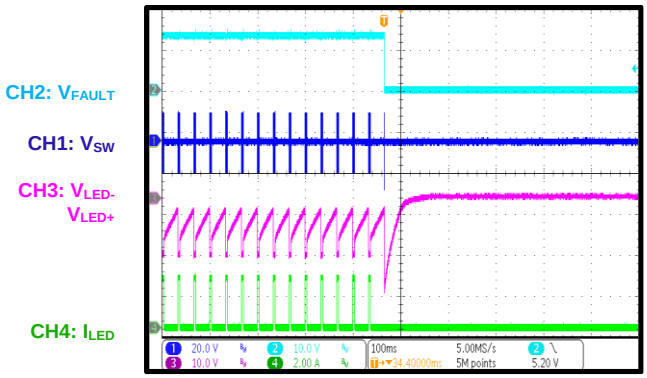
PWM Dimming

LED open input start-up, I_{LED_PEAK} = 2.4A



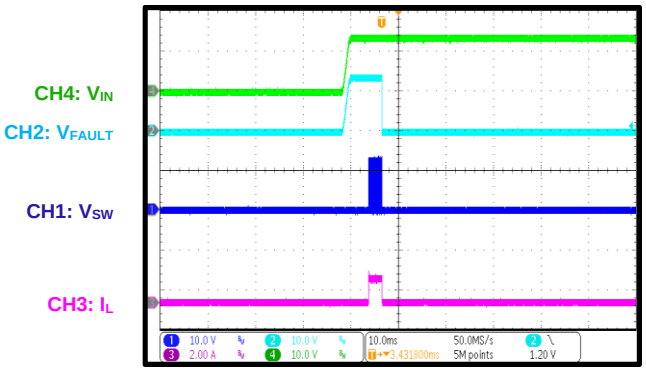
PWM Dimming

LED open entry, I_{LED_PEAK} = 2.4A



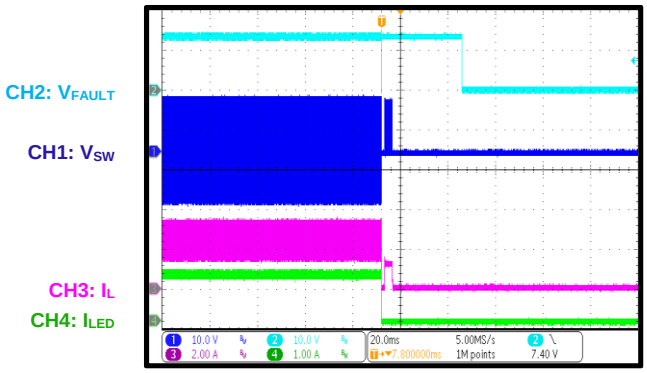
No Dimming

LED+ short to LED- start-up



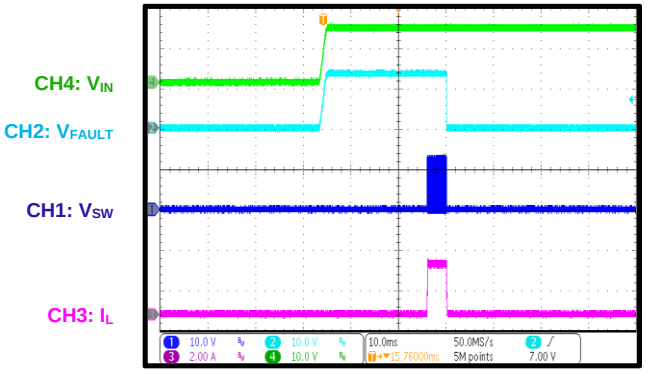
No Dimming

LED+ short to LED- entry



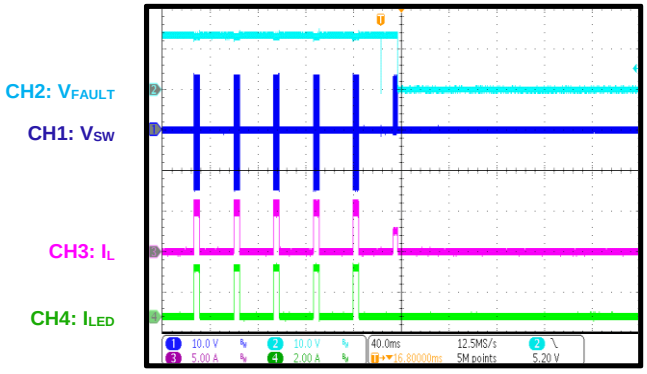
Start-Up through VIN

LED+ short to LED- start-up, I_{LED_PEAK} = 2.4A



Start-Up through VIN

LED+ short to LED- entry, I_{LED_PEAK} = 2.4A



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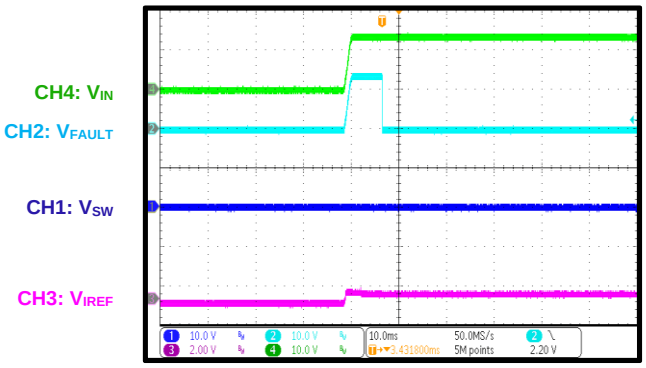
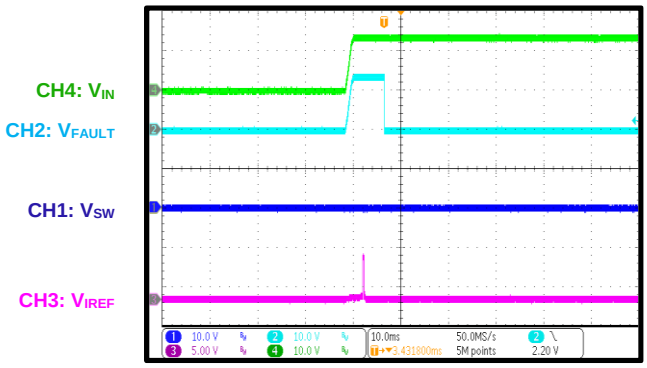
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Buck-boost mode, three LEDs in series (V_{LED} = 9V), V_{IN} = 13.5V, I_{LED} = 1.2A, f_{SW} = 1.25MHz, L = 3.3µH, T_A = 25°C, unless otherwise noted.

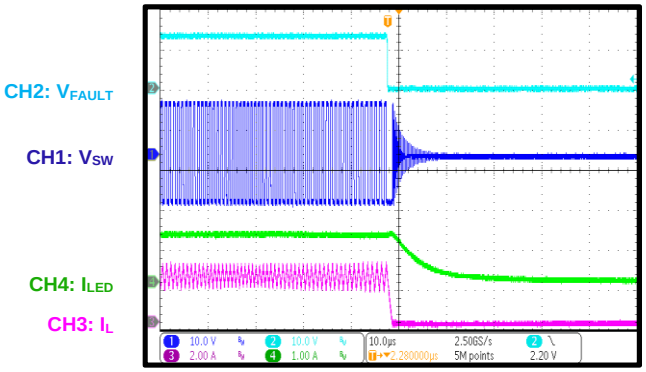
IREF Short Fault before IC Start-Up



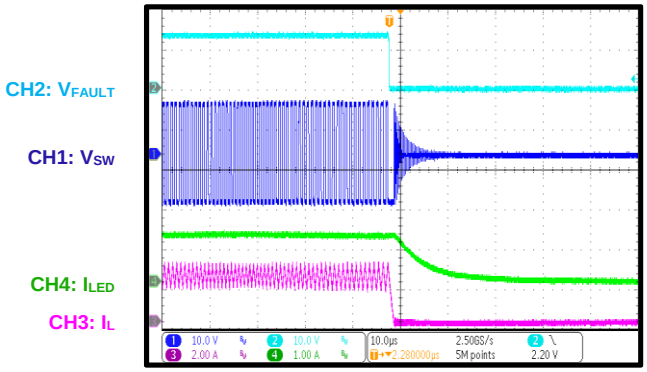
IREF Open Fault before IC Start-Up



IREF Short Fault after IC Start-Up

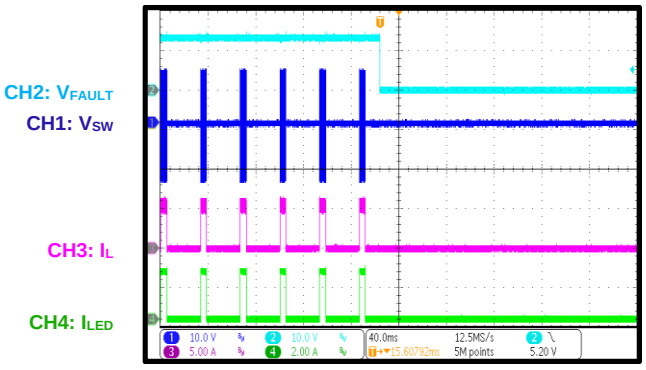


IREF Open Fault after IC Start-Up



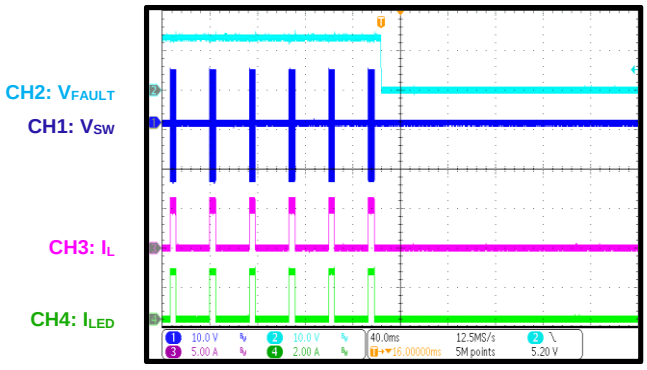
IREF Short Fault after IC Start-Up

PWM dimming, I_{LED_PEAK} = 2.4A



IREF Open Fault after IC Start-Up

PWM dimming, I_{LED_PEAK} = 2.4A



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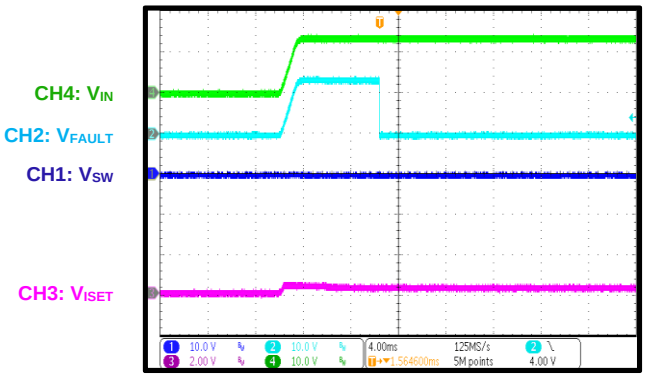
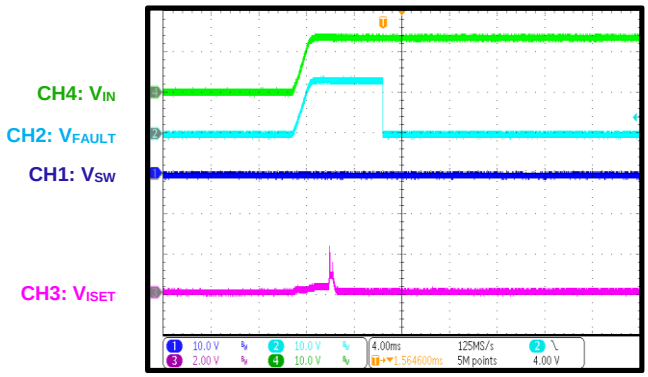
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Buck-boost mode, three LEDs in series (V_{LED} = 9V), V_{IN} = 13.5V, I_{LED} = 1.2A, f_{SW} = 1.25MHz, L = 3.3µH, T_A = 25°C, unless otherwise noted.

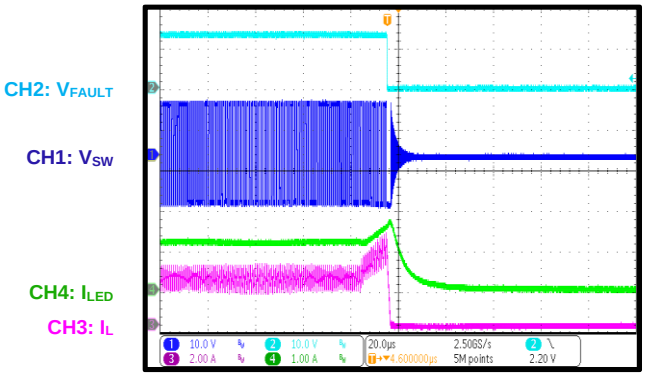
ISET Short Fault before IC Start-Up



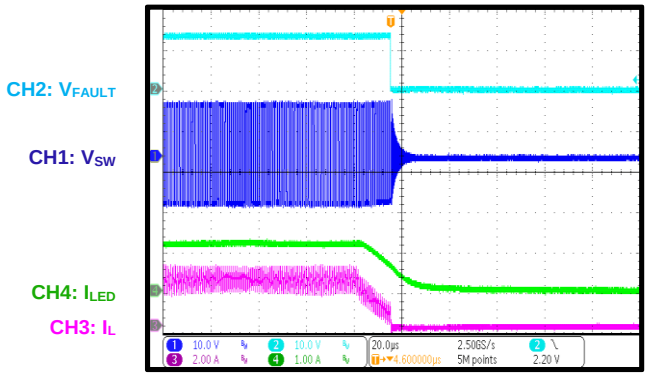
ISET Open Fault before IC Start-Up



ISET Short Fault after IC Start-Up

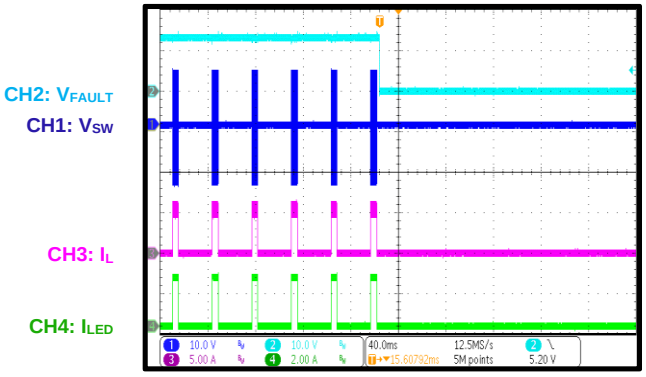


ISET Open Fault after IC Start-Up



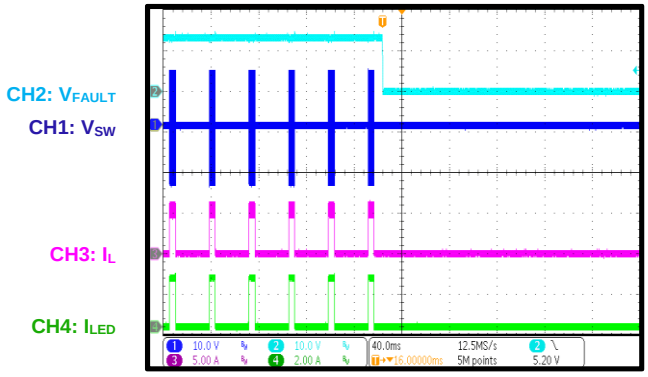
ISET Short Fault after IC Starts Up

PWM dimming, I_{LED_PEAK} = 2.4A



Start-Up through VIN

PWM dimming, I_{LED_PEAK} = 2.4A



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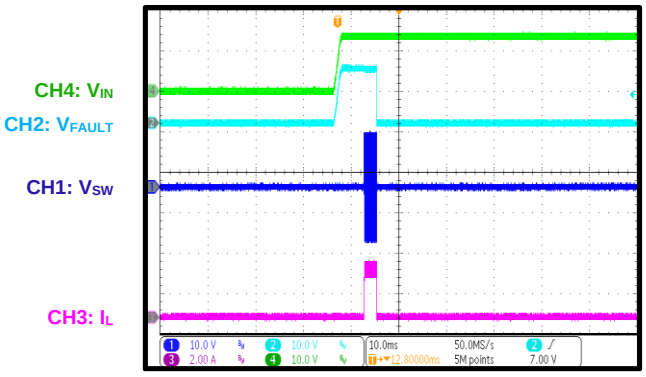
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Buck-boost mode, three LEDs in series (V_{LED} = 9V), V_{IN} = 13.5V, I_{LED} = 1.2A, f_{SW} = 1.25MHz, L = 3.3µH, T_A = 25°C, unless otherwise noted.

False Mode Detection during Start-Up through VIN



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FUNCTIONAL BLOCK DIAGRAM

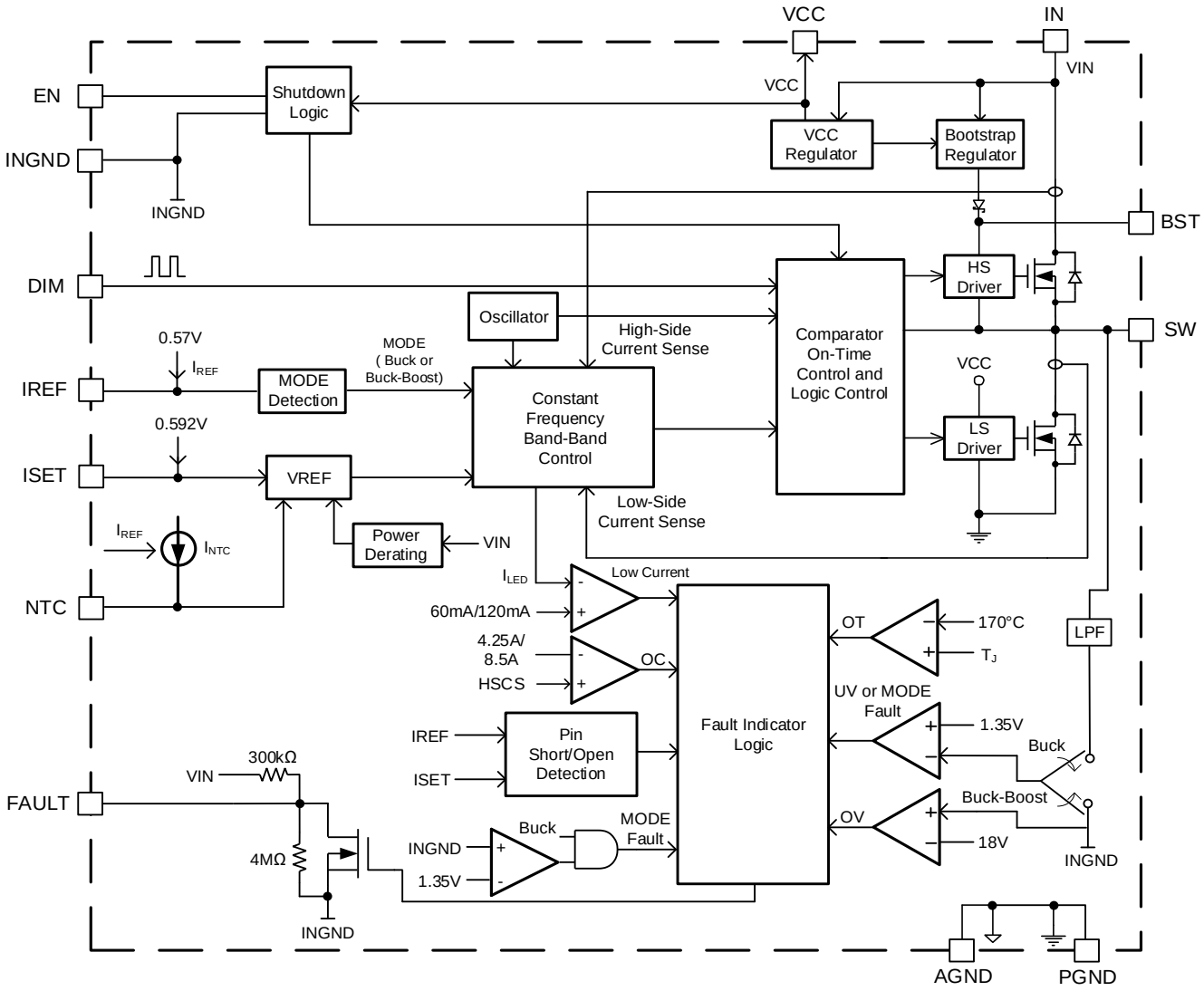

Figure 3: Functional Block Diagram

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OPERATION

The MPQ7231 is a fixed-frequency, synchronous, rectified, buck-boost or buck, switch-mode LED driver with integrated power MOSFETs. In buck mode, it offers a very compact solution to achieve 3A of continuous output current (I_{LED}). The MPQ7231 can also be configured to buck-boost mode to provide up to 1.2A of constant load current and 2.4A of peak current (I_{LED_PEAK}), with low pulse-width modulation (PWM) dimming frequencies at small dimming duty cycles. The device has excellent load and line regulation across a 6V to 42V input supply range.

Fixed-Frequency Band-Band Control

The MPQ7231 provides fixed-frequency band-band control combined with frequency spread spectrum (FSS) to reduce EMC noise. Compared to fixed-frequency PWM control, band-band control offers the advantages of a simpler control loop and faster transient response. The loop is stable without requiring an output capacitor. Band-band control compares the inductor current (I_L) to its internal peak current (I_{BAND_PEAK}) and valley current (I_{BAND_VALLEY}). If I_L exceeds I_{BAND_PEAK}, the high-side MOSFET (HS-FET) turns off. If I_L drops below I_{BAND_VALLEY}, the HS-FET turns on. (I_{BAND_PEAK} + I_{BAND_VALLEY}) / 2 is controlled by a PID loop to regulate the LED current (I_{LED}). I_{BAND_PEAK} - I_{BAND_VALLEY} is controlled by a PLL loop to regulate the switching frequency (f_{SW}) at 2.4MHz in buck mode or 1.25MHz in buck-boost mode. If the minimum on time (t_{ON_MIN}) or minimum off time (t_{OFF_MIN}) is triggered, f_{SW} is extended and the real f_{SW} is D / t_{ON_MIN} or (1 - D) / t_{OFF_MIN}, where D is the required duty cycle, and t_{ON_MIN} and t_{OFF_MIN} are both at 80ns (max).

FSS employs a 15kHz modulation frequency with a triangular profile to spread the internal f_{SW} across a ±10% nominal f_{SW} window.

Middle Point Inductor Current Sense

The MPQ7231 senses I_{LED} via the middle point of the inductor current (I_{L_MID}). I_{LMID} is sensed via the HS-FET or low-side MOSFET (LS-FET) depending on the duty cycle. If the duty cycle exceeds a set value (D_{TH_H}) (55% in buck or 60% in buck-boost), then I_{LMID} is sensed via the HS-FET; if the duty cycle drops below D_{TH_L} (45% in buck or 40% in buck-boost), then I_{LMID} is sensed through the LS-FET. The duty cycle hysteresis (D_{TH_HYS}) (10% in buck or 20% in buck-boost) is triggered to prevent the current sense switching between the HS-FET and LS-FET frequently at critical duty cycles.

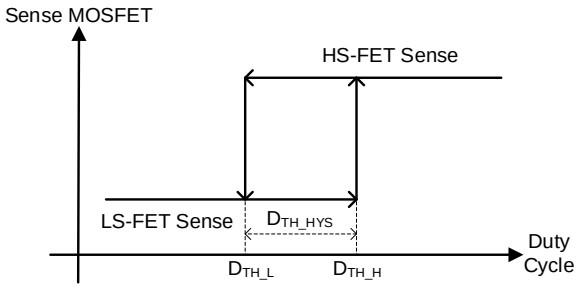

Figure 4: Current-Sense MOSFET vs. Duty Cycle

I_{LED} is equal to I_{LMID} in buck topology, while I_{LED} is equal to I_{LMID} x V_{IN} / (V_{IN} + V_{OUT}) in buck-boost topology.

Selecting Buck and Buck-Boost Mode

The MPQ7231 can be configured to buck or buck-boost topology by connecting different resistors (R_{IREF}) at the IREF pin. I_{LMID} is sensed via the sensing MOSFET. I_{LED} is equal to I_{LMID} in buck topology, while I_{LED} is equal to I_{LMID} x V_{IN} / (V_{IN} + V_{OUT}) in buck-boost topology.

Mode detection begins when V_{CC} reaches its UVLO threshold (V_{CC_UVLO}) (4.7V). A 240µA current source (I_{REF_DET}) flows from the IREF pin to detect the resistor voltage at the pin when the device is turned on. If the voltage generated by I_{REF_DET} x R_{IREF} < 2.6V, then buck-boost mode is selected; if the voltage generated by I_{REF_DET} x R_{IREF} > 2.8V, then buck mode is selected. The corresponding R_{IREF} is ≤9.09kΩ for buck-boost mode and ≥ 14.7kΩ for buck mode. To prevent an IREF short in buck-boost mode, set R_{IREF} between 1.05kΩ and 9.09kΩ. To prevent an IREF open fault in buck mode, set R_{IREF} between 14.7kΩ and 80.6kΩ. Once detection is finished, the mode latches and I_{REF} is set to 0.57V/R_{IREF} as the NTC pin current's reference. The latched mode signal is reset by V_{CC_UVLO}; it cannot be reset by pulling EN or DIM low. An internal 1MHz filter combined with a 250µs deglitch time protects the part from false mode detection, which is caused by noise coupling at the pin.

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Monitor V_{INGND} - V_{PGND} to ensure the detected mode is consistent with the real topology connection. If buck mode is detected with V_{INGND} - V_{PGND} exceeding 1.35V, or buck-boost mode is detected with V_{INGND} - V_{PGND} below 1.35V (detected as output UV), then the part latches off and FAULT asserts low.

Internal Regulator

The 5.1V internal regulator (VCC) powers most of the internal circuitries. VCC ramps up once the input voltage (V_{IN}) reaches its rising UVLO threshold ($V_{IN_UVLO_VTH_R}$), regardless of whether EN is high or low. VCC is the reference for PGND and AGND but not for INGND. Thus, in buck-boost mode, the ground level should not match between VCC and INGND. An insufficient VCC capacitor causes V_{CC} ringing and leads to switch instability. It is recommended to use a ≥3µF decoupling ceramic capacitor at the VCC pin. When choosing a real capacitor, consider the capacitance derating to ensure a ≥3µF real capacitance. A 10µF (X7R) capacitor with a ≥10V DC rated voltage is recommended. V_{CC} has a UVLO rising threshold ($V_{CC_UVLO_VTH_R}$) (4.7V) and a UVLO falling threshold ($V_{CC_UVLO_VTH_F}$) (4.05V). In addition to powering internal circuitries, VCC can power external circuitries in the system with a 25mA current capability.

Continuous Conduction Mode (CCM) and Discontinuous Conduction Mode (DCM)

The MPQ7231 provides continuous conduction mode (CCM) to ensure that the part works with a fixed frequency across a no load to full-load range. The advantage of CCM is the controllable frequency and lower output ripple under light-load conditions. If I_{BAND_VALLEY} is set to 0A, the MPQ7231 enters discontinuous conduction mode (DCM), and the LS-FET works as an ideal diode. Select a proper inductor to ensure that the part does not enter DCM, including during power or thermal derating. Otherwise, I_{LED} precision cannot be guaranteed.

Enable (EN) Control

EN is a control pin that turns the LED driver on and off. Drive V_{EN} - V_{INGND} above 1V to turn on the regulator; drive V_{EN} - V_{INGND} below 0.9V to turn the part off and reset FAULT. Note that the MPQ7231 begins thermal detection when EN is on, resulting in a delay of ~0.9ms between start-up through EN and switching.

An internal 1MΩ resistor placed between EN and INGND enables floating EN to shut down the chip. An integrated Zener diode is placed in parallel with EN to clamp the pin to 7V (see Figure 5). The MPQ7231 enables connecting EN to VIN via a pull-up resistor in both buck mode and buck-boost mode, or connecting EN to VCC via a pull-up resistor in buck mode. Once V_{IN} and V_{CC} exceed their respective UVLO thresholds, the chip automatically starts up. Choose a sufficient pull-up resistance to limit the EN input current below 1mA. A 100kΩ resistor is recommended.

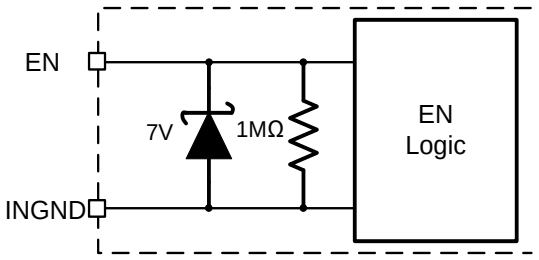

Figure 5: Internal EN Circuit

ISET Pin Configuration

The average I_{LED} can be configured by connecting a resistor at the ISET pin (R_{ISET}). I_{LED} can be calculated with Equation (1):

$$I_{LED}\ (A) = 21.3 / R_{ISET}\ (k\Omega) \quad (1)$$

The nominal voltage of ISET (V_{ISET}) is 0.592V. V_{ISET} is adjusted to below 0.592V to decrease I_{LED} in the power or thermal derating.

During the buck mode detection period at start-up, ISET current (I_{SET}) is monitored to detect whether I_{LED} is set above or below 600mA. If I_{SET} exceeds 22.2µA during this period, then I_{LED} is detected above 600mA and the MOSFETs are fully on. If I_{LED} is detected below 600mA, then the HS-FET and LS-FET is cut by half to improve current-sense accuracy. When the MOSFET is cut by half, the current limit (I_{LIMIT}) is also reduced from 8A to 4.25A. The signal to indicate above or below 800mA is latched once detection completes and can only be reset by V_{CC_UVLO}. After I_{LED} detection, the MOSFET on resistance ($R_{DS(ON)}$) does not change although I_{LED} exceeds or drops below 800mA. While in buck-boost mode, the MOSFET remains fully on, and I_{LIMIT} is constant at 8A.

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During normal operation, ISET is continuously monitored to detect open fault or short to ground conditions. When I_{SET} exceeds a set value, a pin short to ground is detected.

If I_{LED} is set below 800mA, the ISET short detection threshold is 220μA, corresponding to a 2.67kΩ resistor or 7.92A I_{LED}. If I_{LED} is set above 800mA, the threshold is 330μA, corresponding to a 1.78kΩ resistor or 11.87A I_{LED}.

If I_{SET} is below 1.4μA, corresponding to a 422kΩ resistor or 50.37mA I_{LED}, then a pin open fault is detected.

The part latches off once ISET detects a short or open fault, regardless of whether FAULT asserts. FAULT asserts low immediately if ISET detects a short or open fault after start-up. There is a 3ms to 5ms delay for FAULT assertion if a short or open fault is detected during start-up.

IREF Pin Configuration

The IREF pin configures buck or buck-boost mode (see Buck and Buck-Boost Mode Selection section on page 42). IREF then sets the current in the external NTC. After mode detection finishes, the IREF pin voltage (V_{IREF}) is set to 0.57V with a 10.5% tolerance. Connect R_{IREF} between IREF and ground to obtain a current (I_{REF}) equal to 0.57V/R_{IREF}. I_{REF} is used as the reference for the NTC's current source, where the NTC current is I_{REF} x 50 in buck mode and I_{REF} x5 in buck-boost mode. IREF is also continuously monitored to detect open fault as well short to ground conditions. If I_{REF} exceeds 85μA in buck mode (corresponding to a 6.7kΩ resistor) and 800μA in buck-boost mode (corresponding to a 0.71kΩ resistor), then the pin is shorted to ground. If I_{REF} is below 3μA in buck mode (corresponding to a 190kΩ resistor) and 40μA in buck-boost mode (corresponding to a 14.3kΩ resistor), then a pin open fault is detected.

The part latches off once a IREF short or open is detected, regardless of whether FAULT asserts. FAULT asserts low immediately if a pin short or open is detected after start-up. There is a 3ms to 5ms delay for FAULT assertion if a short or open is detected during start-up.

Pulse-Width Modulation (PWM) Dimming

An external 10Hz to 2kHz PWM waveform can be applied to the DIM pin to implement PWM dimming. The MPQ7231 stops switching when the DIM pin voltage (V_{DIM}) is below 0.9V and I_{LED} is at 0A. It resumes normal operation with a nominal I_{LED} when V_{DIM} exceeds 1V. The average I_{LED} is then proportional to the PWM duty. The maximum LED on time of the MPQ7231-D10, MPQ7231-D30, and MPQ7231-D50 is limited to 1ms, 3ms, and 5ms, respectively, even if the DIM high time is longer than 5ms. The MPQ7231-D00 has no dimming on time limit (see Figure 6).

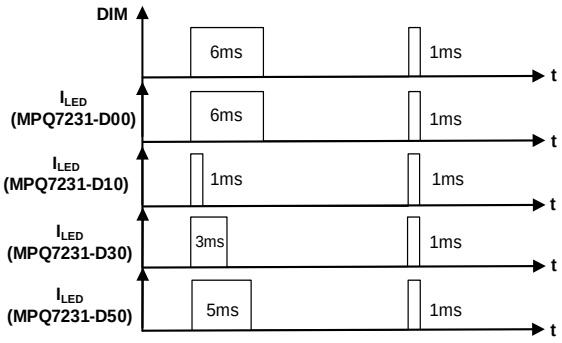

Figure 6: DIM High vs. LED Current

For applications a with low PWM dimming frequencies at small dimming duty cycles, the error amplifier (EA) output voltage (V_{COMP}) may be discharged by the leakage if the dimming off time is too long. The chip can support the maximum DIM low time for as long as 100ms, meaning the dimming frequency can reach below 10Hz.

Note that the DIM high voltage period should remain longer than 100μs. Otherwise, the part might not stop switching and latch even an LED open fault is detected.

Under-Voltage Lockout (UVLO)

UVLO protects the chip from operating at an insufficient supply voltage. Both V_{IN} - V_{INGND} and V_{CC} have their respective UVLO thresholds. The V_{IN} - V_{INGND} UVLO rising threshold is 6V, with a 1.1V hysteresis. $V_{CC_UVLO_VTH_R}$ is 4.7V with a 0.65V hysteresis. The V_{IN} and V_{CC} UVLO thresholds do not trigger faults.

Fault Detection and Indicator

The MPQ7231 also provides fault indication. FAULT is the open-drain pin of a MOSFET and is pulled to VIN via a 300kΩ resistor, as well as a 4MΩ resistor pulled down to INGND. During normal operation, FAULT is pulled high. During

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fault conditions such as LED short, LED open, thermal shutdown, false mode detection , and over-current (OC) conditions, FAULT is pulled low to indicate a fault status. ISET or IREF pin short/open faults during or after start-up can both assert FAULT.

The MPQ7231 senses the output by monitoring the average SW voltage (V_{SW}) in buck mode and INGND voltage (V_{INGND}) in buck-boost mode. If a LED+ short to LED- or ground is detected, then the output voltage (V_{OUT}) drops below the under-voltage (UV) threshold, a short circuit is detected, and FAULT asserts. If a LED+ short to battery or LED open fault is detected, then an output over-voltage (OV) occurs in buck-boost mode, the LS-FET and HS-FET current is detected in buck mode, and FAULT asserts.

If the low current rising threshold is falling when I_{LED} is set below 800mA, it reaches 82mA with a 22mA hysteresis; if the low current rising threshold is falling when I_{LED} is set above 800mA in buck mode, it reaches 166mA with a 46mA hysteresis. If the low current rising threshold is falling in buck-boost mode, it reaches 166mA with a 46mA hysteresis. In buck mode, the low current detection is disabled when V_{IN} drops below 7.5V to avoid latching the part under cold-crank conditions. In buck-boost mode, if a LED+ (INGND) short to battery is detected, V_{IN} - V_{INGND} is below its UV threshold, and FAULT cannot assert. If a LED- (PGND) short to INGND is detected, V_{INGND} is below the V_{INGND} UV threshold, and FAULT asserts. If an LED open fault is detected, V_{INGND} exceeds its OV threshold, and FAULT asserts.

At high temperatures, the MPQ7231 continues to operate with a lower current level. The part only shuts down when the internal temperature reaches the 170°C over-temperature protection (OTP) threshold, after which FAULT asserts.

During normal operation, the MPQ7231 stops switching immediately once a fault condition is detected. The FAULT output asserts after 20µs, and then the part latches. During latching, VCC remains present, and the part's consumption current is <2mA.

FAULT can be reset by V_{CC_UVLO} and EN going low. During start-up, FAULT remains not activated for at least 30ms and becomes activated within a maximum of 40ms. This prevents any false function of the system when the FAULT pins of multiple parts are connected together and share the same EN signal. However, individual parts are self-protected and latch off immediately once a fault condition detected, regardless of whether FAULT asserts.

FAULT can withstand a 30mA current and protect itself, even if the pin shorts to a high voltage such as battery voltage (V_{BATT}). At a low FAULT pin voltage (V_{FAULT}) (e.g. <1.6V), FAULT sink current is increased to improve pull-down capability. Figure 7 shows the FAULT sink current when the pin is pulled low at different V_{FAULT} levels.

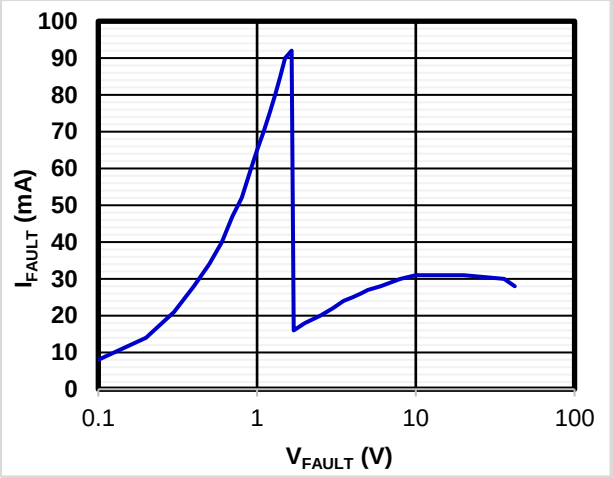

Figure 7: FAULT Sink Current vs. FAULT Voltage

During PWM dimming, fault conditions are not detected properly if the dimming on time is below 100µs. Ensure that the dimming on time remains above 100µs to ensure that fault detection operates correctly.

Table 1 on page 40 lists the fault detection under various conditions.

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Table 1: Fault Detection (12)

Fault Conditions	Detection	
	Buck	Buck-Boost
LED+ short to LED-	V_{OUT} UV (V_{OUT} < 1.1V)	INGND UV (V_{INGND} - V_{PGND} < 1.35V) (13)
LED+ short to PGND	V_{OUT} UV (V_{OUT} < 1.1V)	INGND UV (V_{INGND} - V_{PGND} < 1.35V) (13)
LED+ short to INGND	V_{OUT} UV (V_{OUT} < 1.1V)	Normal conditions
LED+ short to battery	Low I_{LED}	Cannot assert FAULT due to V_{IN} - V_{INGND} UVLO threshold
LED- short to INGND	Normal conditions	INGND UV (V_{INGND} - V_{PGND} < 1.35V) (13)
LED- short to battery	Cannot assert FAULT due to V_{IN} - V_{INGND} UVLO threshold	N/A (14)
LED open	Low I_{LED}	INGND OV (V_{INGND} - V_{PGND} > 18V)
False MODE detection	V_{INGND} - V_{PGND} > 1.35V	INGND UV (V_{INGND} - V_{PGND} < 1.35V)
Over-temperature protection (OTP)	T_J > 170°C or V_{NTC} < 0.37V for >256µs	
ISET short (15)	I_{SET} > 220µA when $I_{LED_SETTING}$ < 800mA, I_{SET} > 330µA when $I_{LED_SETTING}$ > 800mA	I_{SET} > 220µA
ISET open (15)	I_{ISET}<1.4µA	
IREF short (15)	I_{REF} > 85µA	I_{REF}>800µA
IREF open (15)	I_{REF} < 3µA	I_{REF}<40µA
Over-current protection (OCP)	Current limit triggered three times continuously	
Low I_{LED} protection (16)	$I_{LED_RISIING}$ < 82mA with a 22mA hysteresis if falling when $I_{LED_SETTING}$ < 800mA, I_{LED_RISING} < 166mA with 46mA hysteresis if falling when $I_{LED_SETTING}$ > 800mA	I_{LED_RISING} < 166mA with a 46mA hysteresis if falling

Notes:

12) Once FAULT is detected, the part latches and FAULT asserts, unless otherwise noted.
13) If a LED+ short to LED- is detected with a long cable, then FAULT might glitch if V_{INGND} - V_{PGND} is pulled below -0.3V.
14) Not applicable. Similar to an LED- short to battery in buck-boost mode, the negative voltage ($V_{INGND-PGND}$) risks damage to the IC.
15) The part latches when the ISET or IREF pin detect a short or open fault before or after start-up, with FAULT pulled low.
16) In order to avoid mistriggering low I_{LED} protection, I_{LED} should not be set below the low I_{LED} rising threshold. In addition, ensure I_{LED} does not drop below the low I_{LED} rising threshold when the power derating is active in buck-boost mode.

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Over-Current Protection (OCP)

The MPQ7231 supports cycle-by-cycle peak current-limit protection. I_L is monitored while the HS-FET is on. If I_L exceeds the current limit (8A when I_{LED} is set above 800mA, and 4.25A when I_{LED} is set below 800mA), the HS-FET turns off immediately. Then the LS-FET turns on to discharge the energy and I_L decreases. The HS-FET remains off unless I_L drops to 0A. Afterward, another HS-FET on cycle begins. If an OC condition remains after three continuous attempts, then the part latches off and reports a failure with FAULT asserted.

Load Dump Protection

The MPQ7231's internal MOSFETs have a 50V absolute maximum rating and an operating voltage up to 42V. In buck topology, this maximum voltage can handle load dump conditions up to 42V. In buck-boost topology, V_{IN} - V_{PGND} is the combination of V_{BATT} and LED voltage (V_{LED}). In load dump conditions, V_{IN} - V_{PGND} can exceed the absolute maximum value. To protect the part in buck-boost topology under load dump conditions, once V_{IN} - V_{PGND} exceeds 40V, the MPQ7231 stops switching and a 100mA sink current at INGND is activated to discharge V_{OUT}. As result, only the MOSFETs detect the V_{IN} stress. When V_{IN} - V_{PGND} drops back to 39V, the part automatically restarts. Load dump protection does not trigger faults and is not active in buck mode. While load dump protection can reset FAULT after the pin is pulled low by other fault conditions, it cannot reset the part's latch.

Power Derating

In buck-boost mode, when V_{IN} is below a set voltage (typical 7V), power derating is initiated and I_{LED} decreases with V_{IN} linearly using analog dimming. Derating continues to V_{IN} UVLO, with a -29% derating ratio at UVLO. During start-up, power derating is activated in buck-boost mode. In buck mode, power derating is always disabled.

Thermal Derating via the NTC

When the sensed temperature exceeds a configured value, connect a NTC resistor network (R_{NTC}) between the NTC pin and ground to reduce I_{LED} using analog dimming. A current source (I_{NTC}), which is I_{REF} x 50 in buck mode or I_{REF} x 5 in buck-boost mode, flows out the NTC pin and generates a voltage (V_{NTC}) equal to I_{NTC} x R_{NTC} at the pin. V_{NTC} is sensed to indicate the real temperature and determine the dimming ratio.

If V_{NTC} exceeds 1.25V, dimming does not occur. To prevent activating the NTC function, pull the NTC pin above 1.25V. The NTC pin can also be pulled to VCC. If V_{NTC} drops below 1.2V, dimming is activated, and the dimming ratio decreases as V_{NTC} decreases. If V_{NTC} drops by 30mV, the dimming ratio decreases by a 2% step. If V_{NTC} drops from 1.25V to 0.5V, the dimming ratio decreases to 50%. Thus, the average I_{LED} also decreases to 50% of the set value accordingly. I_{LED} does not drop below 50% even if V_{NTC} is below 0.5V. If V_{NTC} drops below 0.4V within 256µs, an over-temperature (OT) condition is detected. The part stops switching and does not recover until V_{NTC} rises back to 0.5V. FAULT does not assert for this NTC OT event.

Note that if the NTC pin is floated, V_{NTC} is charged to V_{CC}, the NTC circuitry is deactivated, and I_{LED} remains at the set value.

Thermal Shutdown

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. If the die temperature exceeds 170°C, the entire chip shuts down and FAULT asserts. Only IC start-up or start-up through EN can restart the chip.

Floating Driver and Bootstrap Charging

An external bootstrap (BST) capacitor (C_{BST}) powers the floating power MOSFET driver. The C_{BST} voltage is charged to ~5V from VCC via the pass transistor when the LS-FET is on. This floating driver has its own UVLO protection, with a rising threshold of 2.5V and 700mV hysteresis. When the BST to SW voltage (V_{BST-SW}) drops to 2.2V, the LS-FET is forced on to refresh the BST voltage (V_{BST}). A 22nF to 220nF ceramic capacitor is recommended for C_{BST}. The real capacitor follows the DC voltage and temperature derating. Consider this derating when selecting the capacitor to ensure a real capacitance within the 22nF to 200nF range. A resistor (max 22Ω) in series with C_{BST} is optional to reduce the SW spike voltage.

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APPLICATION INFORMATION

Buck and Buck-Boost Mode Selection

The operation mode can be configured by connecting different resistors (R_{IREF}) at the IREF pin. Select $R_{IREF} \leq 9.09k\Omega$ for buck-boost mode and $R_{IREF} \geq 14.7k\Omega$ for buck mode.

Setting the LED Current (I_{LED})

The external resistor connected to the ISET pin sets I_{LED}. The value of the external resistor (R3) can be determined with Equation (2):

$$R3 = \frac{21.3}{I_{LED}(A)}(k\Omega) \quad (2)$$

Table 2 shows recommended resistor values for common I_{LED} levels.

Table 2: Resistor Selection for Common I_{LED} Current

I_{LED} (A)	R3 (kΩ)
3	6.98
2	10.50

It is recommended to set I_{LED} above 300mA for BBI mode. It is recommended to I_{LED} set above the typical value (60mA) when $I_{LED_SETTING}$ is below 800mA, or 120mA when $I_{LED_SETTING}$ exceeds 800mA for buck mode, as it is likely to trigger the low I_{LED} latch protection.

Selecting the Inductor

For most applications, use a 3.3µH to 33µH inductor with a DC current rating exceeding the maximum I_L. Use the inductor's DC resistance and power consumption when estimating I_{LED}.

For buck converter designs, the required inductance (L) can be calculated with Equation (3):

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{SW}} \quad (3)$$

Choose the inductor ripple current to exceed I_{LED} by 20%. The peak inductor current (I_{L_PEAK}) can be calculated with Equation (4):

$$I_{L_PEAK} = I_{L_AVG} + \frac{\Delta I_L}{2} \quad (4)$$

Where I_{L_AVG} is the average current through the inductor and is equal to the output load current (I_{LED}) for buck applications. Under light-load conditions, use a larger inductor for improved efficiency and current precision. Table 3 shows the recommended inductances for common I_{LED} values in buck mode.

Table 3: Inductances for Common I_{LED} Values in Buck Mode

I_{LED} (A)	Recommended Inductance (µH)
[2A, 3A)	3.3
[1A, 2A)	4.7

For buck-boost converter designs, L can be calculated with Equation (5):

$$L = \frac{V_{OUT} \times V_{IN}}{(V_{OUT} + V_{IN}) \times \Delta I_L \times f_{SW}} \quad (5)$$

Where ΔI_L is the inductor peak-to-peak current ripple.

Select ΔI_L to exceed I_{L_AVG} by 25% when I_{LED} exceeds 0.7A. Select ΔI_L to exceed I_{L_AVG} by 20% when I_{LED} is below 0.7A. I_{L_AVG} can be calculated with Equation (6):

$$I_{L_AVG} = I_{LED} \times (1 + \frac{V_{OUT}}{V_{IN}}) \quad (6)$$

I_{L_PEAK} can be calculated with Equation (7):

$$I_{L_PEAK} = I_{L_AVG} + \frac{1}{2} \times \Delta I_L \quad (7)$$

Note that I_{L_PEAK} should not exceed 6A. Otherwise, it triggers the current limit (where the minimum is 6.85A). Under light-load conditions, use a larger inductor to improve efficiency and current precision. Table 4 shows the recommended inductances at common I_{LED} levels in buck-boost mode.

Table 4: Inductances at Common I_{LED} Values in Buck-Boost Mode

I_{LED} (A)	Recommend Inductances (µH)
(1A, 2.4A]	3.3
[0.8A, 1A]	4.7
[0.6A, 0.8A)	6.8

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Selecting the Input Capacitor

The discontinuous input current in buck or buck-boost mode requires a capacitor to supply AC current to the converter while maintaining the DC V_{IN}. For the best performance, use low-ESR capacitors. Ceramic capacitors with X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients.

For most applications, use a 4.7µF to 22µF capacitor. The input capacitor (C_{IN}) can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, it is strongly recommended to use another lower-value capacitor (e.g. 0.1µF) with a small package size (0603) to absorb high-frequency switching noise. Place the smaller capacitor as close to VIN and ground (INGND = PGND in buck, for both INGND and PGND in buck-boost) as possible.

Since C_{IN} absorbs the input switching current in buck mode, it requires an adequate ripple current rating. The RMS current in C_{IN} can be estimated with Equation (8):

$$I_{CIN} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (8)$$

The worst-case condition occurs at V_{IN} = 2 x V_{OUT}. In this scenario, I_{CIN} can be calculated with Equation (9):

$$I_{CIN} = \frac{I_{LOAD}}{2} \quad (9)$$

For simplification, choose C_{IN} with an RMS current rating greater than half of the maximum load current. The input voltage ripple (ΔV_{IN}) caused by the capacitance can be estimated with Equation (10):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (10)$$

In buck-boost mode, if $I_{BAND_VALLEY} \geqslant I_{LED}$, ΔV_{IN} can be calculated with Equation (11):

$$\Delta V_{IN} = \frac{I_{LED} \times V_{OUT}}{(V_{IN} + V_{OUT}) \times f_{SW} \times C_{IN}} \quad (11)$$

In buck-boost mode, the capacitor placed between VIN and PGND improves EMC performance. However, placing too large of a capacitor between VIN and PGND results in a substrate injection between PGND and INGND. A combination of 0.1µF x 2 and 0.47µF x 2 capacitors is recommended.

Selecting the Output Capacitor

The output capacitor (C_{OUT}) maintains the DC V_{OUT}. Ceramic, tantalum, or low ESR electrolytic capacitors are recommended. For the best results, use low-ESR capacitors to keep the output voltage ripple (ΔV_{OUT}) low.

In buck mode, ΔV_{OUT} can be estimated with Equation (12):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 \times f_{sw} \times C_{OUT}}) \quad (12)$$

Where R_{ESR} is the equivalent series resistance (ESR) value of C_{OUT}.

For ceramic capacitors, the capacitance dominates the impedance at f_{SW} and causes the majority of ΔV_{OUT}. For simplification, ΔV_{OUT} can be estimated with Equation (13):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^{\ 2} \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (13)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at f_{SW}. For simplification, ΔV_{OUT} can be estimated with Equation (14):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (14)$$

For buck-boost applications, if $I_{BAND_VALLEY} \geq I_{LED}$, C_{OUT} can be selected by calculating ΔV_{OUT} with Equation (15):

$$\Delta V_{OUT} = I_{LED} \times (R_{ESR} + \frac{V_{OUT}}{f_{sw} \times C_{OUT} \times (V_{IN} + V_{OUT})}) \quad (15)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at f_{SW}. For simplification, ΔV_{OUT} can be approximated with Equation (16):

$$\Delta V_{OUT} = I_{LED} \times R_{ESR} \quad (16)$$

A 2.2µF to 10µF ceramic capacitor is sufficient for most applications.

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Selecting the Diode from PGND to INGND in Buck-Boost Mode

In buck-boost mode, a Schottky diode is required between the INGND and PGND pins to handle the charge current for the VIN to PGND capacitor, especially under high V_{IN} slew rate conditions. When (V_{INGND} - V_{PGND}) < 5.1V, V_{CC} is powered from VIN. In this scenario, a Schottky diode is also required since the VCC charge current flows from the VCC capacitor to PGND, then flows back to INGND and the car battery. Typically, a Schottky diode with a low forward voltage (V_F) (~0.32V), >1A current rating, and >20V VRRM voltage (V_{RRM}) is sufficient for the application. A PMEG2010EPAS Schottky is recommended.

Selecting the VCC Capacitor

Selecting an insufficient VCC capacitor causes V_{CC} ringing and switch instability. A ≥3µF decoupling ceramic capacitor is recommended at the VCC pin. When selecting the real capacitor, consider the capacitance derating to ensure a ≥3µF real capacitance. A 10µF (X7R) capacitor with a ≥10V DC rated voltage is recommended. VCC is the reference for PGND and AGND.

Selecting the Bootstrap (BST) Resistor and Capacitor

A resistor in series with C_{BST} is recommended to reduce the SW spike voltage. Higher resistance is better for reducing the SW spike, with the tradeoff of compromising efficiency.

The 22nF to 220nF ceramic capacitor with a 10V or 16V DC derating is recommended for the external C_{BST}. Considering the efficiency and EMI performance, a max 22Ω resistor with a 0603 or 0402 package is recommended. It is not necessary to use a large resistor package.

During normal operation, the average current flowing through the BST resistor (R_{BST}) is about 20mA (buck) and 10mA (buck-boost). If the capacitor is short-circuited, the current inside the resistor is limited by the internal LDO. The part also quickly detects I_{LED} below the lower limit as well as failures. Then the part latches off, resulting in no more current to be sourced to the resistor. The 0402 package is sufficient to handle the power dissipation on R_{BST}.

Low Dimming Frequency Applications

For applications with low PWM dimming frequencies at small dimming duty cycles, V_{COMP} may be discharged by the leakage current if the dimming off time lasts too long (>100ms). It is recommended to not set the minimum dimming frequency below 10Hz.

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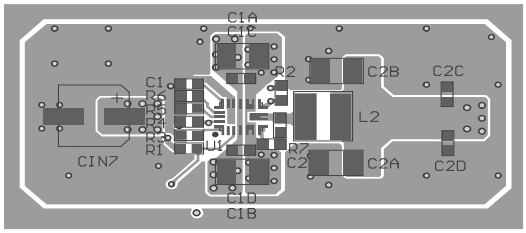
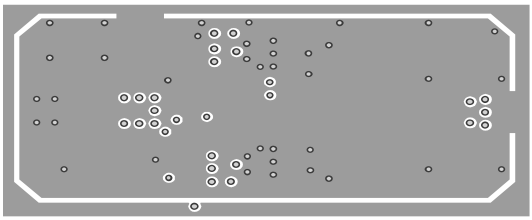
PCB Layout Guidelines

Efficient PCB layout is critical for stable operation, especially for input capacitor placement. A 4-layer layout is strongly recommended to improve thermal performance. For the best results, refer to Figure 8 and Figure 9, and follow the guidelines below:

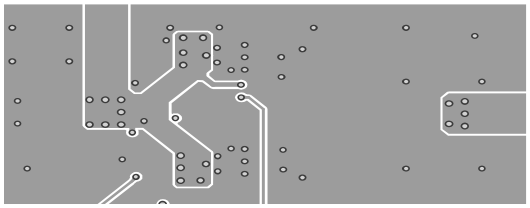
1. Use a large ground plane to connect directly to PGND. If the bottom layer is a ground plane, add vias near PGND.
2. Ensure that the high-current paths at PGND and IN have short, direct, and wide traces.
3. Place the ceramic input capacitor, especially the small package (0603) input bypass capacitor, as close to the IN and PGND pins as possible to minimize high-frequency noise. Keep the connection between the input capacitor and IN as short and wide as possible.
4. Place the VCC capacitor as close to the VCC pin and ground as possible.
5. Route SW and BST away from sensitive analog areas, such as FB.
6. Place the feedback resistors close to the chip to ensure the trace connected to FB is as short as possible.
7. Use multiple vias to connect the power planes to the internal layers.



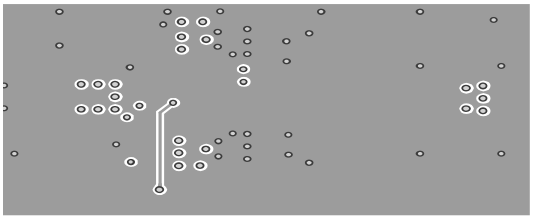
Top Layer



Mid-Layer 1

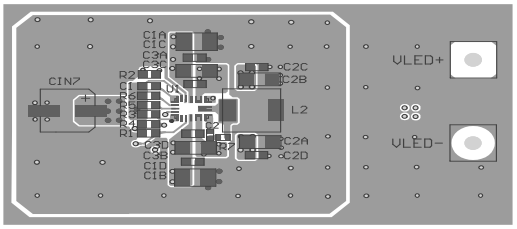


Mid-Layer 2

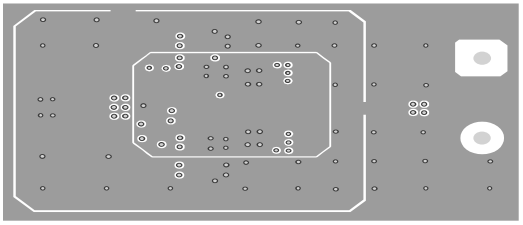


Bottom Layer

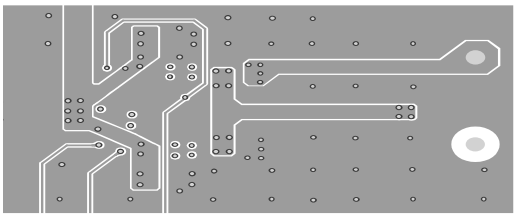
Figure 8: Recommended PCB Layout for Buck Mode (17)



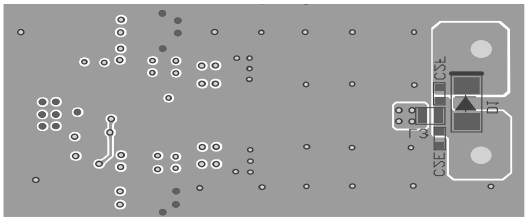
Top Layer



Mid-Layer 1



Mid-Layer 2



Bottom Layer

Figure 9: Recommended PCB Layout for Buck-Boost Mode (18)

Notes:

17) The recommended layout is based on Figure 10 on page 46.
18) The recommended layout is based on Figure 11 on page 46.

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TYPICAL APPLICATION CIRCUITS

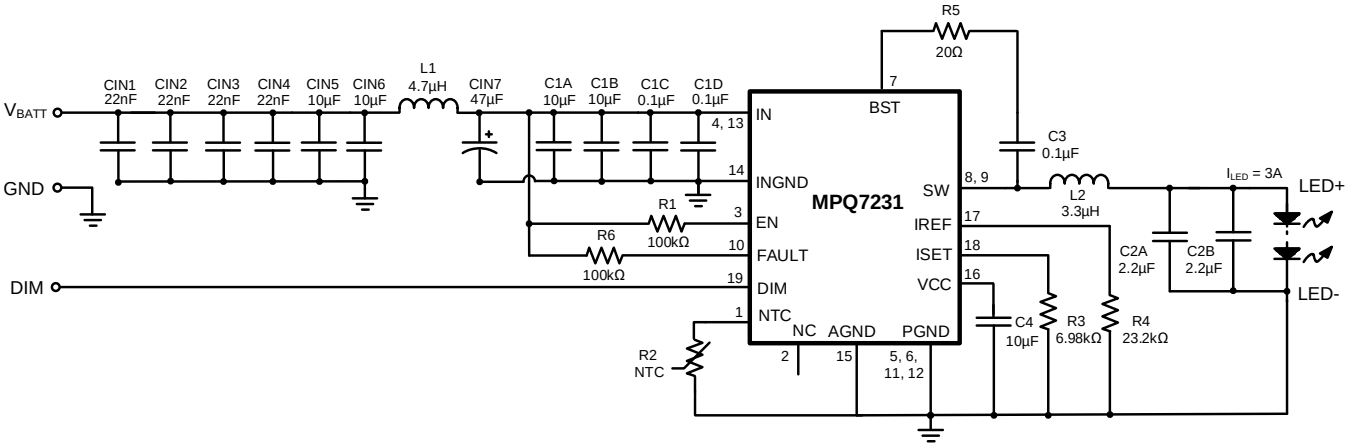

Figure 10: Typical Application Circuit (I_{LED} = 3A Buck)

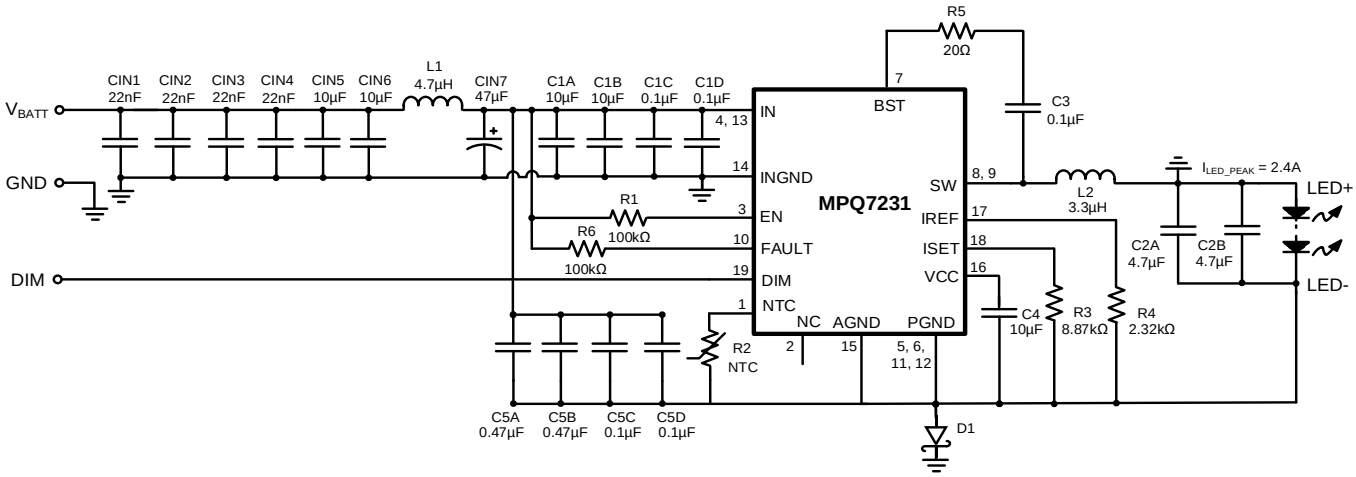

Figure 11: Typical Application Circuit (I_{LED_PEAK} = 2.4A Buck-Boost)

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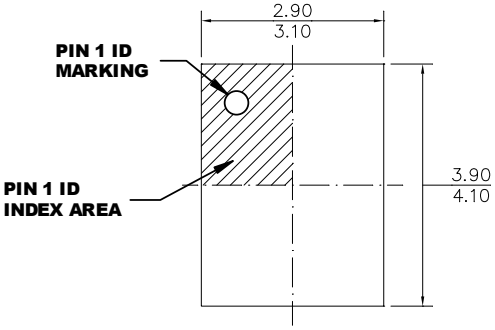
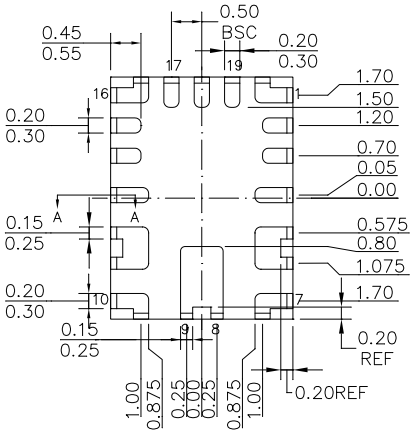
PACKAGE INFORMATION

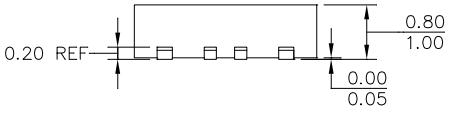
QFN-19 (3mmx4mm)
Wettable Flank



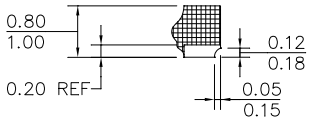
TOP VIEW



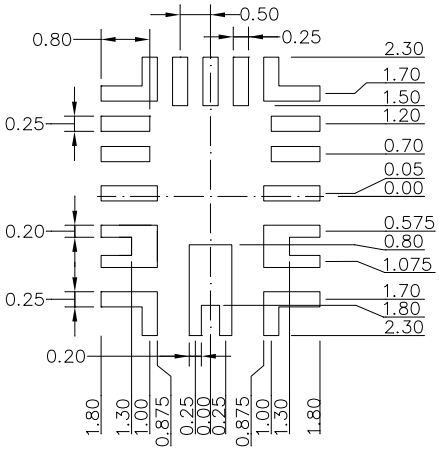
BOTTOM VIEW



SIDE VIEW



SECTION A-A



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

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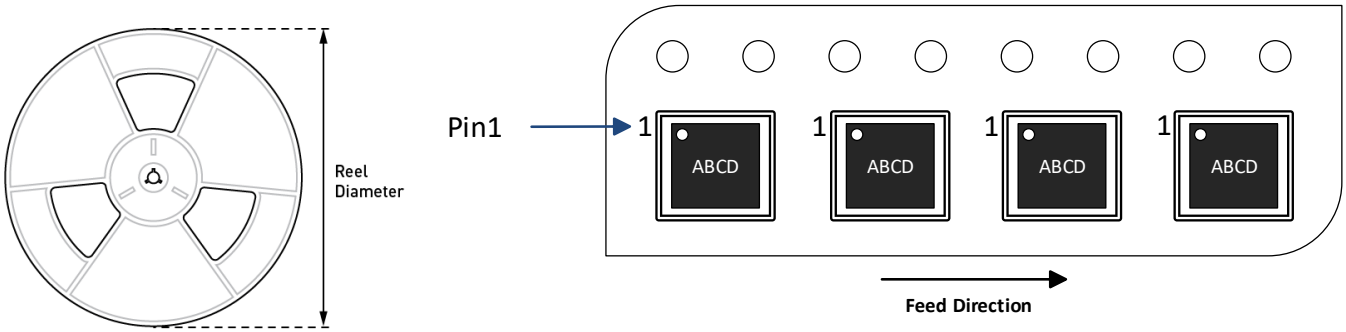
CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ7231GLE-D00-AEC1	QFN-19 (3mmx4mm)	5000	N/A	N/A	13in	12mm	8mm
MPQ7231GLE-D10-AEC1							
MPQ7231GLE-D30-AEC1							
MPQ7231GLE-D50-AEC1							

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REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	8/14/2023	Initial Release	-

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