

R2J20751NP

Peak Current Mode Synchronous Buck Controller with Power MOS FETs

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Description

This all-in-one SiP for POL (point-of-load) applications is a multi-chip module incorporating a high-side MOS FET, low-side MOS FET, and PWM controller in a single QFN package. The on and off timing of the power MOS FET is optimized by the built-in driver circuit, making this device suitable for large-current high-efficiency buck converters. In a simple peak-current mode topology, stable operation is obtained in a closed power loop, and a fast converter is easily realized with the addition of simple components. Furthermore, the same topology can be applied to realize converters for parallel synchronized operation with current sharing, and multi-phase operation. The package also incorporates a high-side bootstrap switch (Boot switch), eliminating the need for an external SBD for this purpose.

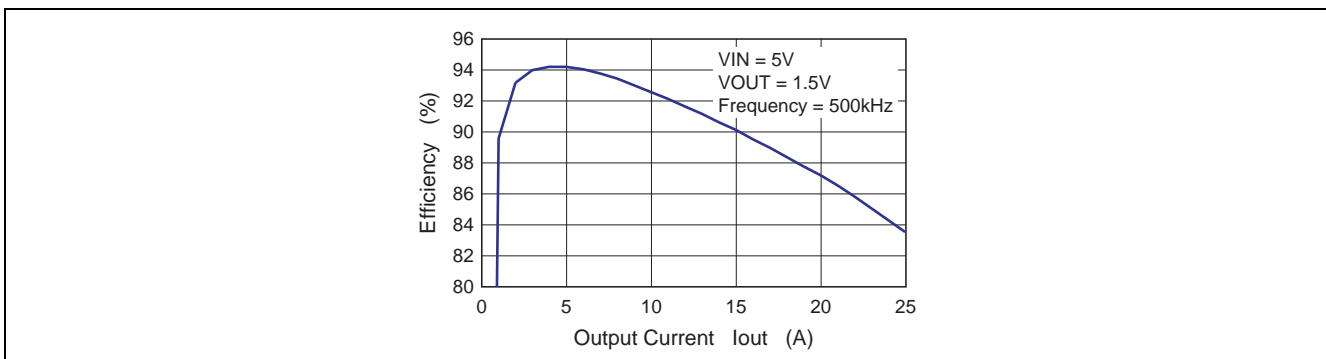
Features

- Three chip in one package for high efficiency and space saving
- Large average output current (25 A)
- Wide input voltage range: 3.3 V to 27 V
- 0.6 V reference voltage accurate to within 2%
- Wide programmable switching frequency: 200 kHz to 1 MHz
- Peak current mode topology with Active Current Sensing
- Slope compensation function
- Current sensing error: 1.5 A maximum @15 A load current
- Built-in Boot switch for boot strapping
- ON/OFF control
- Hiccup operation under over load condition
- Tracking function
- Thin and small package: QFN40 pins (6 mm × 6 mm)
- Power Good function
- Over voltage protection
- Pre-OVP function

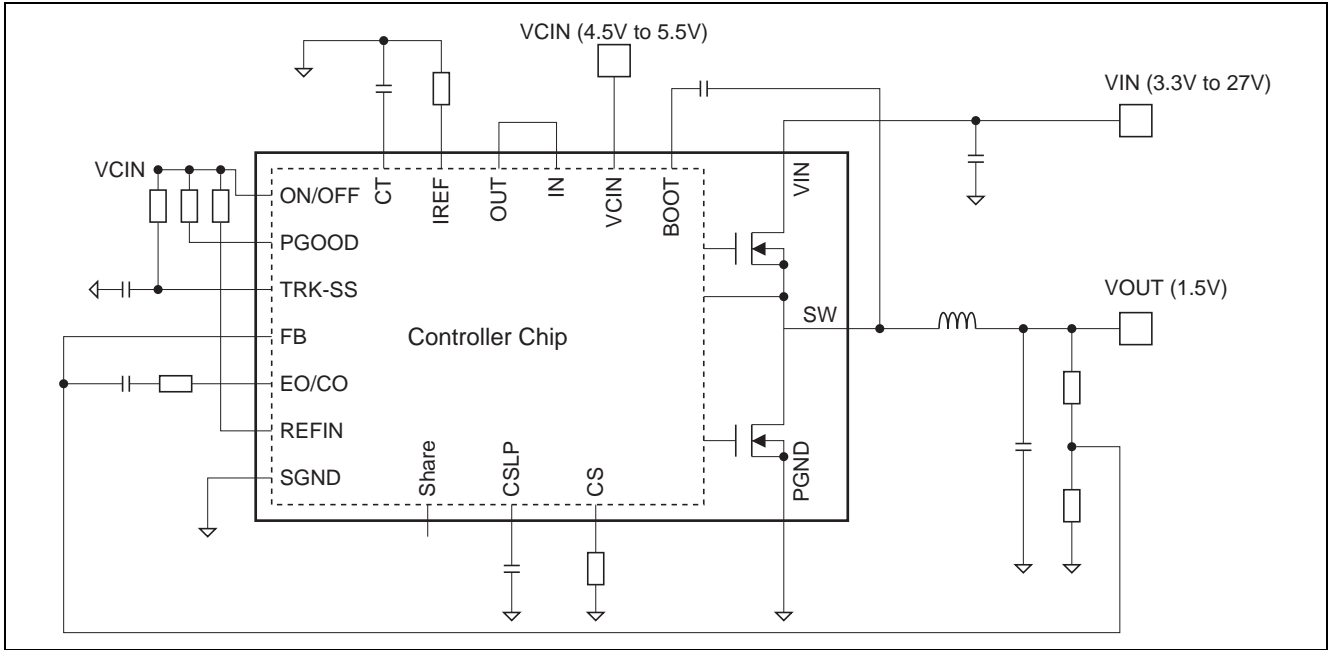
Applications

- Mother board
- Servers

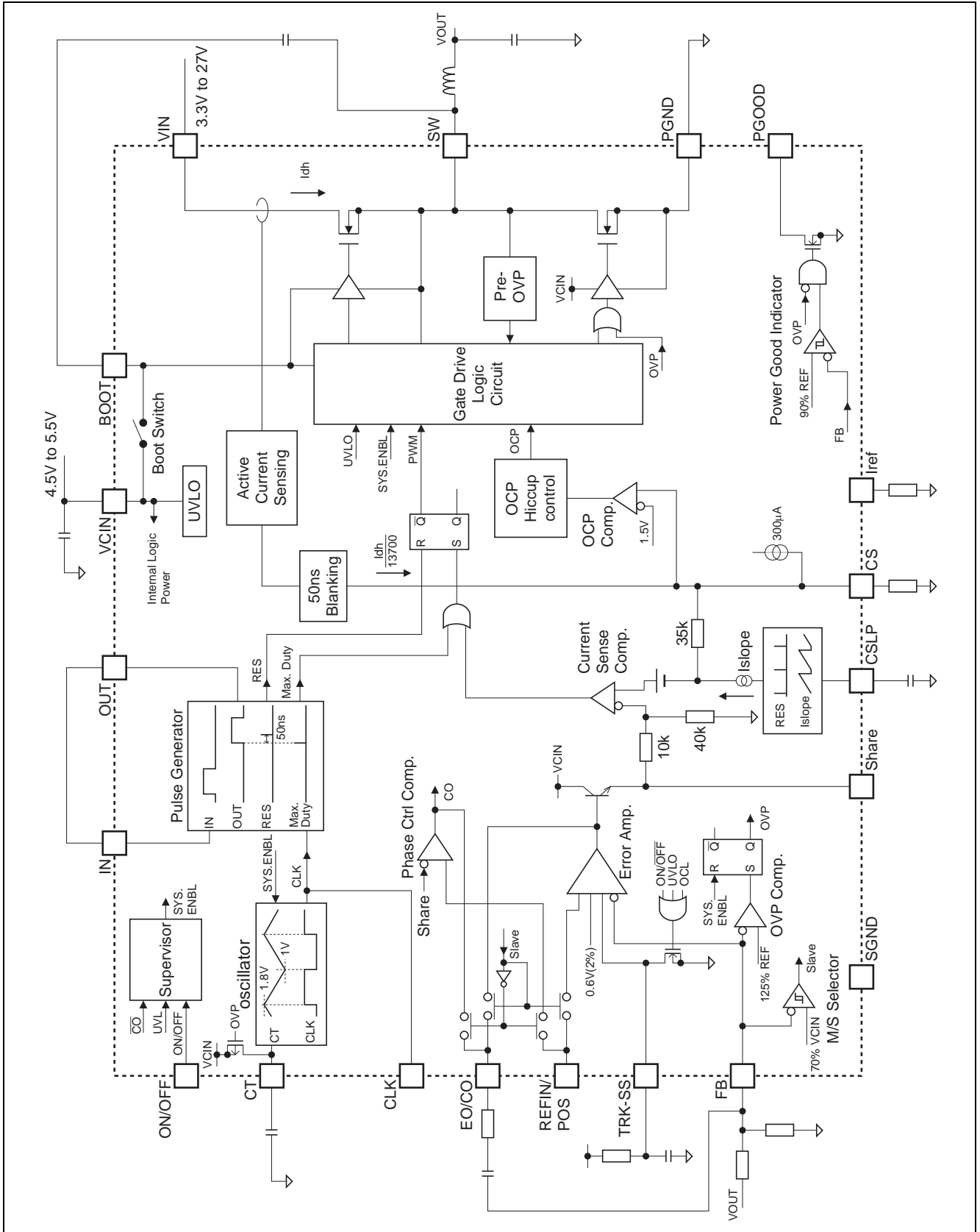
Typical Characteristic Curve



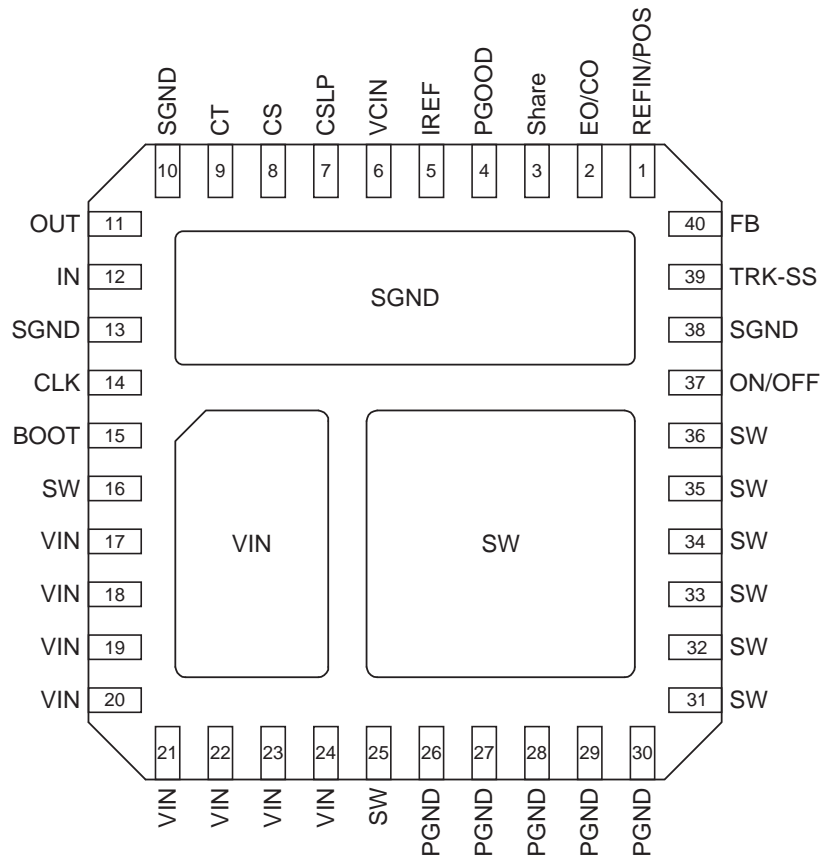
Application Circuit Example



Block Diagram



Pin Arrangement



Top view
 Package: QFN40 pin (6 mm × 6 mm, 0.5-mm pin pitch)

Pin Description

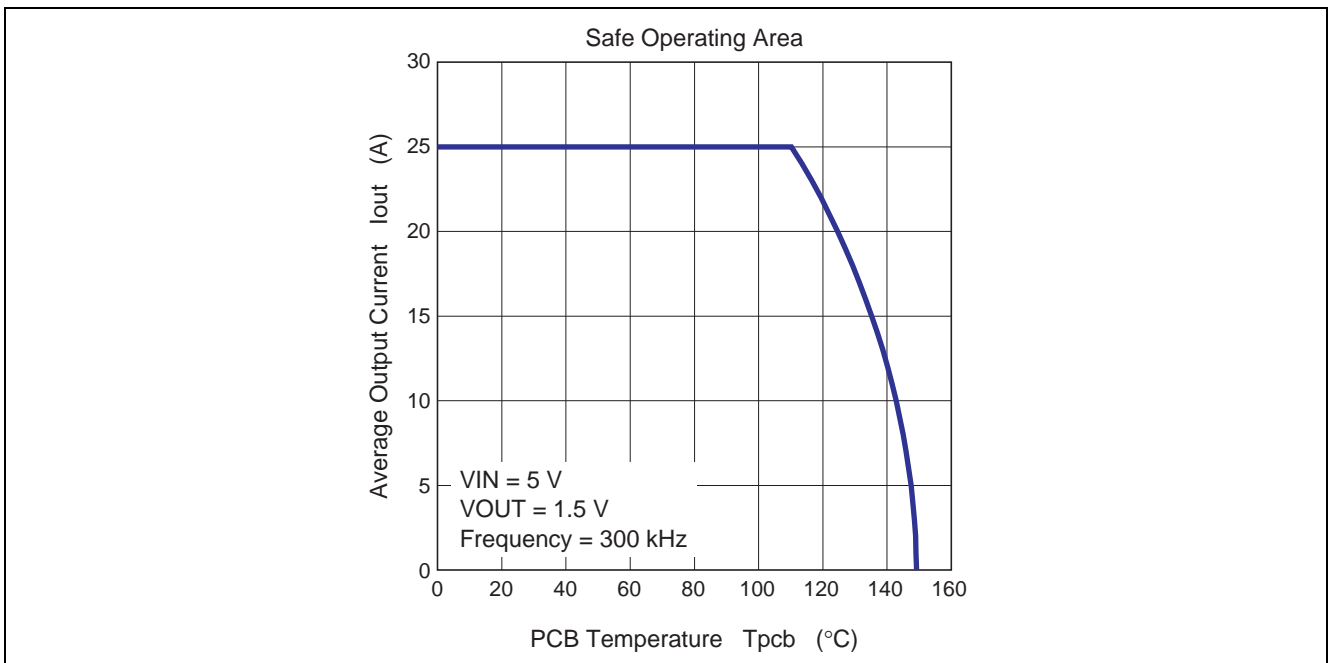
| Pin Name | Pin No. | Description | Remarks |
|-----------|------------------|---|---|
| VIN | 17 to 24 | Input voltage for buck converter. | |
| SW | 16, 25, 31 to 36 | Switching node. Connect a choke coil between the SW pin and dc output node of the converter. | |
| PGND | 26 to 30 | Ground of the power stage. | Should be connected to SGND externally. |
| SGND | 10, 13, 38 | Ground of the IC chip. | Should be connected to PGND externally. |
| VCIN | 6 | Input voltage for control circuit. | Should be connected to 5 V power supply. |
| BOOT | 15 | Bootstrap voltage pin. A bootstrap capacitance should be connected between BOOT pin and SW pin. | To be supplied +5 V through the internal SBD. |
| TRK-SS | 39 | Start-up timing control input. | |
| FB | 40 | Feedback voltage input for the closed loop. | |
| EO/CO | 2 | Error amplifier output pin. (Master mode) Comparator output pin. (Slave mode) | |
| Share | 3 | Current share bus. | Should be connected to each Share pin in multi phase operation. |
| IREF | 5 | Reference current generator for the IC. | Need a 18 k Ω resistance between IREF to GND plane. |
| CSLP | 7 | Additional current slope input pin. | Should be connected capacitor between CSLP to GND. |
| CS | 8 | Current output pin of Active Current Sensing circuit. | Need a resistance appropriately between CS to GND plane. |
| CT | 9 | Timing capacitor pin for the oscillator. | |
| OUT | 11 | Switching trigger output. | Tie to IN pin of previous device in multi phase operation. |
| IN | 12 | Switching trigger input. | Tie to OUT pin of next device in multi phase operation. |
| CLK | 14 | I/O pin for synchronous operation. | Should be connect to each CLK pin in multiphase operation. |
| ON/OFF | 37 | Signal disable pin. | Disabled when ON/OFF pin is low state. |
| PGOOD | 4 | Power Good Indicator output. (Open drain) | Pulled low when No Good. |
| REFIN/POS | 1 | Reference voltage input. (Master mode) Comparator positive pin. (Slave mode) | |

Absolute Maximum Ratings

(Ta = 25°C)

| Item | Symbol | Rating | Unit | Note |
|--------------------------------|------------------------|-------------------------|------|------|
| Power dissipation | Pt(25) | 25 | W | 1 |
| | Pt(100) | 8 | | |
| Average output current | I _{out} | 25 | A | |
| Input voltage | V _{IN} (DC) | -0.3 to +27 | V | 2 |
| | V _{IN} (AC) | 30 | | 2, 5 |
| Supply voltage | V _{CIN} (DC) | -0.3 to +6 | V | 2 |
| Switch node voltage | V _{sw} (DC) | 27 | V | 2 |
| | V _{sw} (AC) | 30 | | 2, 5 |
| BOOT pin voltage | V _{boot} (DC) | 32 | V | 2 |
| | V _{boot} (AC) | 36 | | 2, 5 |
| ON/OFF pin voltage | V _{on/off} | -0.3 to V _{IN} | V | 2 |
| PGOOD voltage | V _{pgood} | 0 to V _{IN} | V | 3 |
| Other pins voltage | V _{ic} | -0.3 to (REG5 + 0.3) | V | 2 |
| TRK-SS dc current | I _{trk} | 0 to 1 | mA | 3 |
| IREF current | I _{ref} | -120 to 0 | μA | 3 |
| EO sink current | I _{leo} | 0 to 2 | mA | 3 |
| CO sink current | I _{lico} | 0 to 1 | mA | 3, 4 |
| CO source current | I _{loco} | 0 to 1 | mA | 3, 4 |
| Operating junction temperature | T _{j-opr} | -40 to +150 | °C | |
| Storage temperature | T _{stg} | -55 to +150 | °C | |

- Notes: 1. Pt(25) represents a PCB temperature of 25°C, and Pt(100) represents 100°C.
 2. Rated voltages are relative to voltages on the SGND and PGND pins.
 3. For rated current, (+) indicates inflow to the chip and (-) indicates outflow.
 4. Rated currents are only for slave mode.
 5. Ratings for which "ac" is indicated are limited to within 100 ns.



Electrical Characteristics

(Ta = 25°C, VIN = VCIN = 5 V, unless otherwise specified)

| | Item | Symbol | Min | Typ | Max | Unit | Test Conditions |
|-----------------------------|------------------------------------|----------------------|-------|----------------------|-------|------|---------------------------------------|
| Supply | VCIN start threshold | VH | 4.1 | 4.3 | 4.5 | V | |
| | VCIN shutdown threshold | VL | 3.6 | 3.8 | 4.0 | V | |
| | UVLO hysteresis | dUVL | — | 0.5 * ¹ | — | V | |
| | Input bias current | lin | 15 | 30 | 45 | mA | Freq = 500 kHz, Duty = 50% |
| | Slave standby current | I-sin | 2.1 | 3.5 | 4.9 | mA | Von/off = 5 V, Vfb = 5 V |
| | Input shutdown current | I _{sd} | 3.1 | 4.5 | 5.9 | mA | ON/OFF = 0 V |
| Remote On/off | Disable threshold | Voff | 1.0 | 1.3 | 1.6 | V | |
| | Enable threshold | Von | 2.0 | 2.5 | 3.0 | V | |
| | Input current | I _{on/off} | 0.5 | 2.0 | 5.0 | μA | Von/off = 1 V |
| Reference current generator | IREF pin voltage | V _{lref} | 1.75 | 1.80 | 1.85 | V | R _{lref} = 18 kΩ |
| Oscillator | CT oscillating frequency | F _{ct} | — | 500 | — | kHz | CT = 180 pF |
| | CT higher trip voltage | V _{hct} | — | 1.8 * ¹ | — | V | CT = 180 pF |
| | CT lower trip voltage | V _{lct} | — | 1 * ¹ | — | V | CT = 180 pF |
| | CT source current | I _{ct-src} | -176 | -160 | -144 | μA | CT = 0.5 V |
| | CT sink current | I _{ct-snk} | 144 | 160 | 176 | μA | CT = 2.3 V |
| Error amplifier | Feedback voltage | V _{fb} | 588 | 600 | 612 | mV | TRK-SS = 1 V |
| | FB input bias current | I _{fb} | -0.1 | 0 | +0.1 | μA | |
| | REFIN input bias current | I _{refin} | 0.5 | 2 | 5 | μA | |
| | Output source current | I _{eo-src} | 150 | 200 | 250 | μA | EO = 4 V, FB = 0 V |
| | Output sink current | I _{eo-snk} | 3.5 | 7.0 | 14.0 | mA | EO = 1 V, FB = 0.7 V |
| | Voltage gain | A _v | — | 80 * ¹ | — | dB | |
| | Band width | BW | — | 15 * ¹ | — | MHz | |
| | Share pin resistance | R _{share} | 35 | 50 | 65 | kΩ | EO = 0 V. I _{share} = 1 V |
| Phase control comparator | Output source current | I _{co-src} | -3.0 | -2.0 | -1.0 | mA | Share = 0 V, POS = 1 V, CO = 4.5 V |
| | Output sink current | I _{co-snk} | 2.0 | 3.0 | 4.0 | mA | Share = 1 V, POS = 0 V, CO = 0.5 V |
| | Input bias current | I _{pos} | 0.5 | 2 | 5.0 | μA | POS = 1.0 V |
| Current sense | CS current accuracy | I _{dh/lcs} | — | 13700 * ¹ | — | — | |
| | Leading edge blanking time | TLD | — | 60 * ¹ | — | ns | |
| | CS comparator delay to output | T _{d-cs} | — | 65 * ¹ | — | ns | |
| | OCP comparator threshold on CS pin | V _{ocp} | 1.4 | 1.5 | 1.6 | V | |
| | Hiccup interval | T _{ocp} | 1.85 | 2.05 | 2.26 | ms | CT = 180 pF |
| | RAMP offset voltage | V _{ramp-dc} | 70 | 100 | 130 | mV | CT = 180 pF |
| | CS offset current | I _{cs-dc} | — | 300 | — | μA | CS = 0 V |
| Power good indicator | Rising threshold on FB | V _{good} | 0.855 | 0.9 | 0.945 | V | REFIN = 1.0 V |
| | Power good hysteresis | dV _{good} | — | 50 * ¹ | — | mV | |
| | Power good output low voltage | V _{pglow} | 0.6 | 1.0 | 1.4 | V | I _{pgood} = 2 mA |

Note: 1. Reference values for design. Not 100% tested in production.

(Ta = 25°C, VIN = VCIN = 12 V, unless otherwise specified)

| Item | | Symbol | Min | Typ | Max | Unit | Test Conditions |
|-------------------------|-----------------------|---------|------|------|------|------|----------------------|
| Over-voltage protection | OVP trip voltage | Vtovp | 1.19 | 1.25 | 1.31 | V | REFIN = 1.0 V |
| | Pre-OVP trip voltage | Vpovp | — | 1.67 | — | V | |
| Slope generator | Slope current | ISLP | 7 | 10 | 13 | μA | VSLP = 0 V |
| Clock generator | Clock frequency | Fclk | 450 | 500 | 550 | kHz | CT = 180 pF |
| | OUT high voltage | Vh-out | 4.0 | 5.0 | — | V | Rout = 51 kΩ to GND |
| | OUT low voltage | Vl-out | 0 | — | 1.0 | V | Rout = 51 kΩ to VCIN |
| | IN input bias current | Ibin | 0.5 | 2.0 | 5.0 | μA | V-in = 1 V |
| | IN input threshold | Vth-in | — | 2.2 | — | V | |
| | IN input hysteresis | Vth-hys | — | 0.25 | — | V | |

Note: 1. Reference values for design. Not 100% tested in production.

Description of Operation

Peak Current Control

The control IC operates as current programmed control mode, in which output of the converter is controlled by the choice of the peak current from the high-side MOS FET. The current from this MOS FET is sensed by an active current sensing circuit (ACS), the output current of which is 1/13700 (50 ppm) of the MOS FET current. The ACS current is then converted to certain voltage by external resistor on the CS pin. The CS voltage is fed to the internal current sense comparator via the slope compensation circuit, and then compared with current control signal which determined from the error amplifier output voltage (EO) via an NPN transistor and resistor network.

To start with, the RES pulse from pulse generator resets a latch, then the high-side MOS FET is turned on. The latch output (Q bar) is toggled when CS voltage reaches the level of the current control signal on EO, the high-side MOS FET is turned off, and the low-side MOS FET is turned off after a certain dead time interval. The IC remains in this state until the arrival of the next RES pulse.

Applying current information for the control loop, the converter loop compensation design will be simple.

Maximum Duty-Cycle Limitation

If the current-sense comparator output is not toggled 60-ns prior to the arrival of the next RES pulse, an internal maximum duty pulse is generated and forces toggling of SR latch. So, the duty cycle of the high-side MOS FET is limited by the maximum duty period.

The maximum duty period of the high-side MOS FET depends on its switching frequency.

$$\text{Max. duty} = 1 - 60 \text{ ns} \times F_{\text{sw}}$$

OCP Hiccup Operation

Eight times the voltage of CS exceeds 1.5 V, OCP hiccup circuit disables switching operation of the IC and MOS FETs. Internal circuitry also pulls the TRK-SS pin down to SGND. The IC is turned off for a period of 1024 RES pulses; after this has elapsed, switching operation of the IC is restarted from the soft-start state.

UVLO and ON/OFF Control

When VCIN is under the start-up voltage, it is in the UVLO condition, functioning of the IC is disabled. The oscillator is turned off, both high and low-side MOS FETs are turned off, and the TRK-SS pin is pulled down. Furthermore, if the ON/OFF pin is the low state or left open, functioning of the IC is disabled and both MOS FETs are turned off.

Oscillator and Pulse Generator

The frequency of the oscillator (Fct) is set by the value of the external capacitor connected to the CT pin. The switching frequency (Fsw) is not the same as Fct, which also depends on the phase number N. The following equations determine these frequencies.

$$\text{Oscillator frequency: } F_{\text{ct}} = 160 \mu\text{A} / (2 \times C_{\text{T}}(\text{F}) \times 0.8 \text{ V}) \times N \quad (\text{Hz})$$

$$\text{Switching frequency: } F_{\text{sw}} = F_{\text{ct}} / N \quad (\text{Hz})$$

In multi-phase operation, connect the CT pins for all devices.

Soft Start

TRK-SS pin is provided for start-up setup. Both simple soft start and sequential start up can be realized with this pin setup. The error amp has two reference inputs and one input for soft start. One of lower voltage inputs of the two positive inputs is dominant for the amplifier. Therefore simply having CR charging circuit on TRK-SS pin is easier for soft start design.

The soft start period is determined with the equation as follows when TRK-SS pin has CR charging circuit.

$$T_{ss} = -C \cdot R \cdot \ln(1 - REF / VCIN) \quad (s)$$

REF is REFIN voltage or 0.6 V in internal reference voltage.

Power Good Indicator

The power good indicator is useful for controlling timing when multiple converter systems are started up or shut down. Voltage on the FB pin is internally monitored by a power good comparator. The power good comparator compares the voltage on the pin with 90% of the reference voltage. When the comparator detects the FB voltage reaching the reference voltage, the Power Good pin becomes high impedance. If the voltage on FB goes over 125% or falls below 80% of the reference voltage, the pin is pulled down to SGND. PGOOD has an n-channel MOS FET operating as an open drain output and capable of sinking up to 2 mA of current.

Overvoltage Protection

When the output voltage (FB voltage) reaches or exceeds 125% of the reference voltage, switching stops immediately, the gate of the low-side MOS FET is latched in the high level, which causes shorting of the SW pin to GND. Resetting to leave the OVP mode is by resupplying VCIN or switching the circuit OFF and ON.

Pre-Overvoltage Protection

When the IC is starting up, an internal circuit monitors the voltage at the switch node and detects the output of excessive voltages. When a voltage exceeding 1.67 V is detected on the SW pin after release from the UVL state, the gate of the low-side MOS FET is latched in the high level, which causes shorting of the SW pin to GND. The low-side MOS FET remains in this state until VCIN is resupplied.

Multi Phase Operation

The R2J20751NP is a scalable solution. Pulling the FB pin of a device up to VCIN causes the device to operate as a slave. Clock timing is synchronized by connecting the CLK and CT pins of all devices. Current sharing is available by connecting the Share pins. The timing of switching of the signal on the SW pin is generated from the switching trigger signal on the IN pin. A device that has received the switching trigger signal outputs the same signal on its OUT pin for the next device one clock cycle later. The phase number is controllable by the internal phase control comparators of slave devices.

Slope Compensation

If peak current control leads to the duty cycle being over 50%, sub-harmonic oscillation is generated and the output voltage becomes unstable regardless of the negative feedback for constant voltage control. The duty cycle, D, is obtained from the following equation.

$$D = V_{out} / V_{IN} \times 100 (\%)$$

To prevent such oscillation, add a constant slope to the slope of the voltage on the CS pin. This added slope is determined by 10 μ A constant current output through the CSLP pin and the value of the connected external capacitor. Insufficient added slope leads to sub-harmonic oscillation. Too much added slope leads to voltage-mode operation and poorer response characteristics. An optimal slope (determined by the value of the external capacitor) needs to be set. The capacitance (Cslp) is determined by the following equation.

$$C_{slp} = 70 \mu A \times 13700 \times T_{off} / (2 \times I_{pp} \times R_{cs} \times M)$$

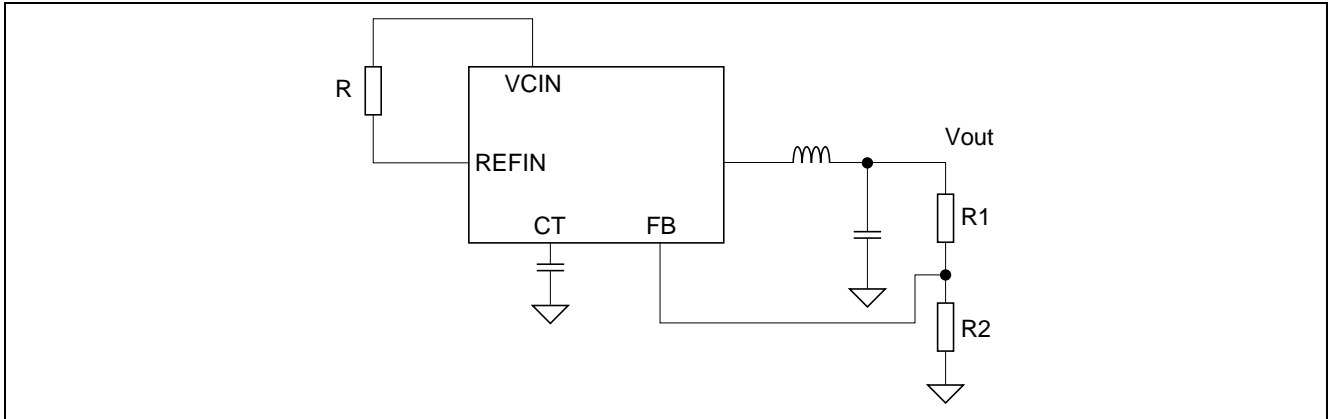
In the above equation, Toff is the off portion of the duty cycle (as time), Ipp is the ripple current of the output inductor, Rcs is the value of the external resistor connected to the CS pin, and M is the rate of the added slope. A capacitor value that leads to a greater setting of M in the range from 0.5 to 1.0 will lead to a greater added slope.

Output Voltage Setting

The error amplifier of the device has an accurate 0.6 V reference voltage and REFIN pin which can input reference voltage from external voltage. When reference voltage is 0.6 V, feedback loop leads to the FB pin a voltage of 0.6 V in case of stable condition on the converter. Therefore the output voltage is;

$$V_{out} = 0.6 \text{ V} \times (R1 + R2) / R2$$

REFIN pin should be pulled up to VCIN, when reference voltage refer to internal 0.6 V.



Loop Compensation

Peak-current control makes design in terms of phase margins easier than is the case with voltage control. This is because of differences between the characteristics of the PWM modulator and power stage in the two methods.

Figure 1 and 2 shows the behavior of the PWM modulator and power stage in the case of voltage control and peak current control, respectively.

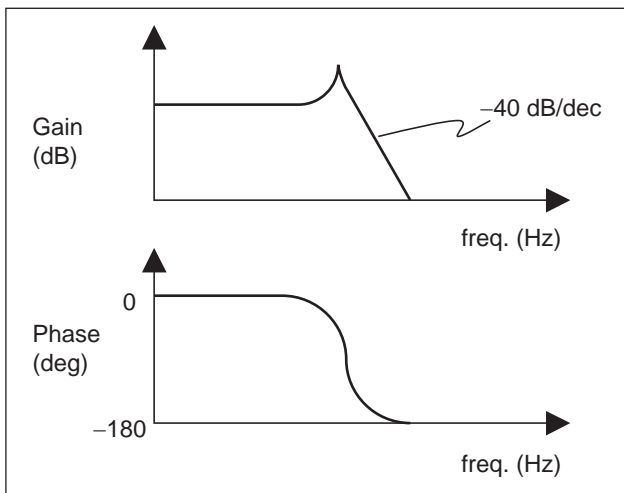


Figure 1 Bode Plot (Voltage Mode)

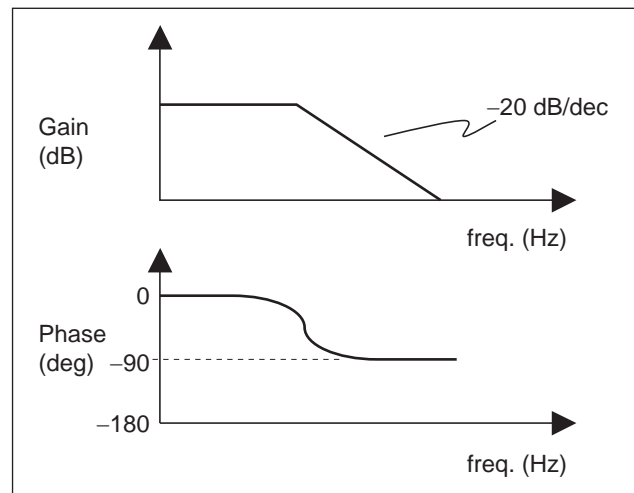


Figure 2 Bode Plot (Peak Current Mode)

Feed-forward current to the modulator in the case of peak-current control means that the system is single pole, so we see a -20 dB/decade cutoff and phase margin of 90° in the Bode plot. In voltage control, the system configures a two-pole system. That is why rather complicated loop compensation of the error amplifier is required. Such as type-III compensation. The design of effective compensation is thus much simpler in the case of peak-current control (refer to figure 3).

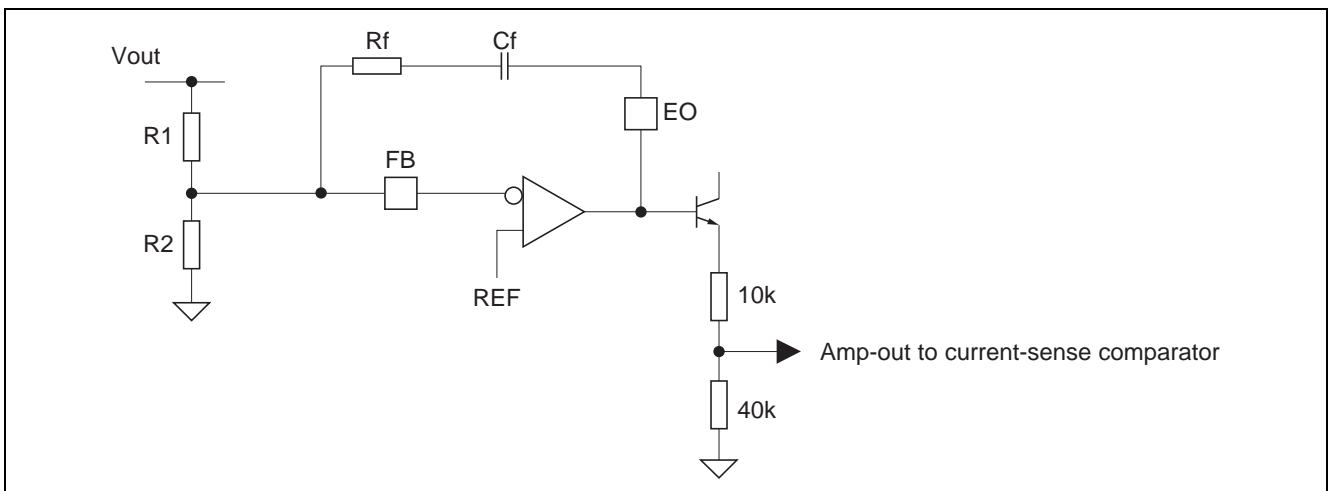


Figure 3 Error Amplifier Compensation

Design example;

Specification: $L = 470 \text{ nH}$, $C_o = 600 \text{ }\mu\text{F}$, $F_{sw} = 500 \text{ kHz}$, $V_{in} = 5 \text{ V}$, $V_{out} = 1.5 \text{ V}$, $R_1 = 1 \text{ k}\Omega$, $R_2 = 1 \text{ k}\Omega$, $RCS = 820 \text{ }\Omega$

1. Flat band gain of error amplifier

The flat band gain is; $A_f = R_f / (R_1 // R_2) \times 4 / 5 \times \{R_2 / (R_1 + R_2)\}$

Hence,

$$R_f = 5 / 4 \times A_f \times (R_1 // R_2) / \{R_2 / (R_1 + R_2)\} \dots\dots(1)$$

In the Bode plot, the total gain should be lower than 1 (0 dB) at the switching frequency.

The total gain at F_{sw} ($= A_{sw}$) depends on the flat-band gain, so A_f should be expressed as follows;

$$A_f = A_{sw} \times 2 \pi \times F_{sw} \times C_o \times RCS / N_t \dots\dots(2)$$

$$\text{Here, } N_t = I_{dh} / I_{cs} = 13700$$

In the typical way, the value chosen for A_{sw} is in the range from 0.1 to 0.5, since this produces a stable control loop. The transient response will be faster if a large A_{sw} is adopted, but the system might be unstable.

We choose 0.2 for A_{sw} in the example below.

$$A_f = 0.2 \times 2 \pi \times 500 \text{ kHz} \times 600 \text{ }\mu\text{F} \times 820 \text{ }\Omega / 13700 = 22.564$$

$$R_f = 5 / 4 \times 22.564 \times 0.6 \text{ k}\Omega / (2 / 3) = 25.385 \text{ k}\Omega$$

Therefore, we select a value of 24 k Ω for R_f .

2. Selecting the C_f value to determine the frequency of the zero.

The frequency of the zero established by C_f and R_f is about ten times the frequency of the pole for the power stage and modulator.

We must start with the dc gain of the power stage and modulator.

$$A_0 = \frac{N_t / RCS \times L \times V_{in} \times F_{sw}}{\text{SQRT} \{V_{in}^2 - 8 \times L \times V_{in} \times F_{sw} \times (V_{CS0} \times N_t / RCS)\}} \dots\dots(3)$$

Here V_{CS0} is the peak ac voltage on CS pin when the load current is zero, thus

$$V_{CS0} = 0.5 \times RCS \times (V_{in} - V_{out}) \times V_{out} / (L \times V_{in} \times F_{sw}) / 13700 \dots\dots(4)$$

$$= 0.5 \times 820 \text{ }\Omega \times (5 \text{ V} - 1.5 \text{ V}) \times 1.5 \text{ V} / (470 \text{ nH} \times 5 \text{ V} \times 500 \text{ kHz}) / 13700$$

$$= 0.134 \text{ V}$$

equation (3),

$$A0 = \frac{Nt/RCS \times L \times Vin \times Fsw}{\text{SQRT} \{Vin^2 - 8 \times L \times Vin \times Fsw \times (VCS0 \times Nt / RCS) \}} \dots\dots(3)$$

$$= \frac{13700 / 820 \Omega \times 470 \text{ nH} \times 5 \text{ V} \times 500 \text{ kHz}}{\text{SQRT} \{5 \text{ V}^2 - 8 \times 470 \text{ nH} \times 5 \text{ V} \times 500 \text{ kHz} \times (0.134 \text{ V} \times 13700 / 820 \Omega) \}}$$

$$= \frac{19.63}{\text{SQRT} \{3.955\}}$$

$$= 9.871$$

The frequency of the pole established by the power stage and modulator is

$$F0 = Nt / (2 \pi \times Co \times RCS \times A0) \dots\dots(5)$$

Thus,

$$F0 = 13700 / (2 \pi \times 600 \mu\text{F} \times 820 \Omega \times 9.871) = 448.967 \text{ Hz}$$

Thus,

$$Fzero = 10 \times F0 = 4.489 \text{ kHz}$$

$$Cf = (2 \pi \times Fzero \times Rf)^{-1} = (2 \pi \times 4.489 \text{ kHz} \times 24 \text{ k}\Omega)^{-1} = 1477 \text{ pF}$$

Therefore, we select 1500 pF for Cf.

Basically, the transient response is faster when Cf is smaller, but too small a value will make the system-loop unstable.

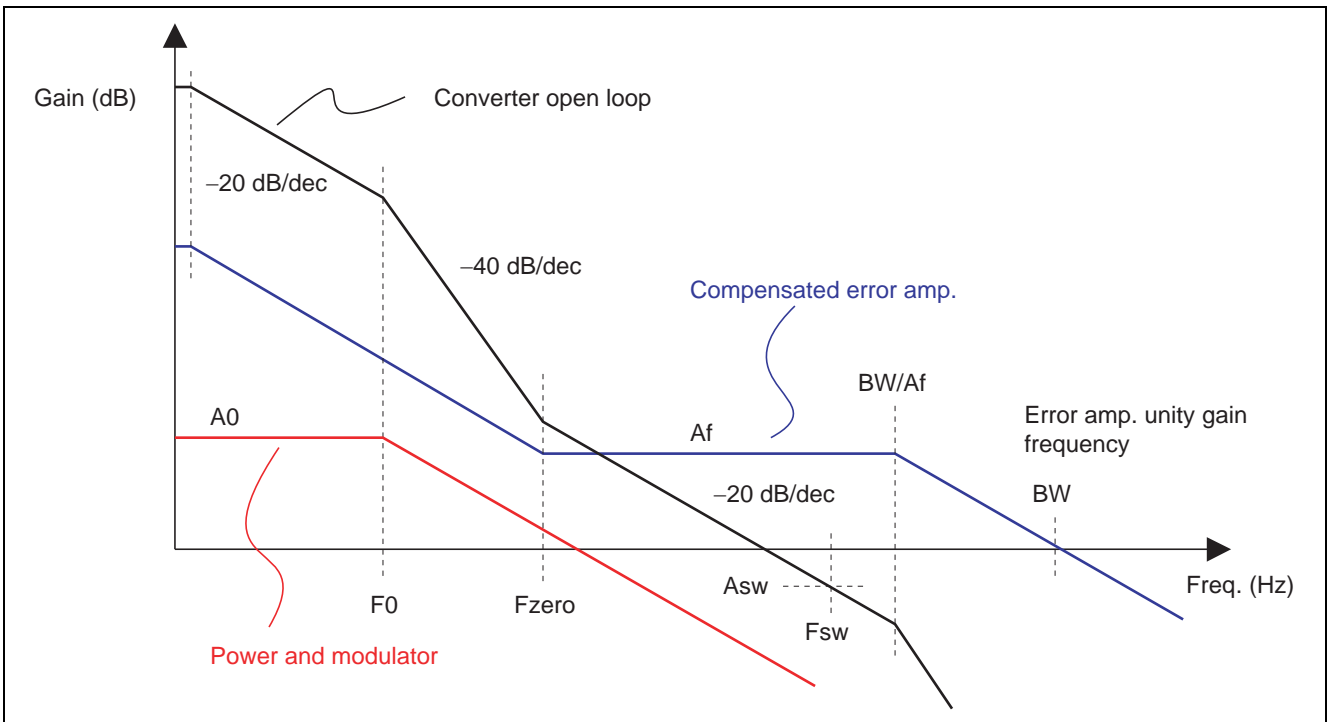


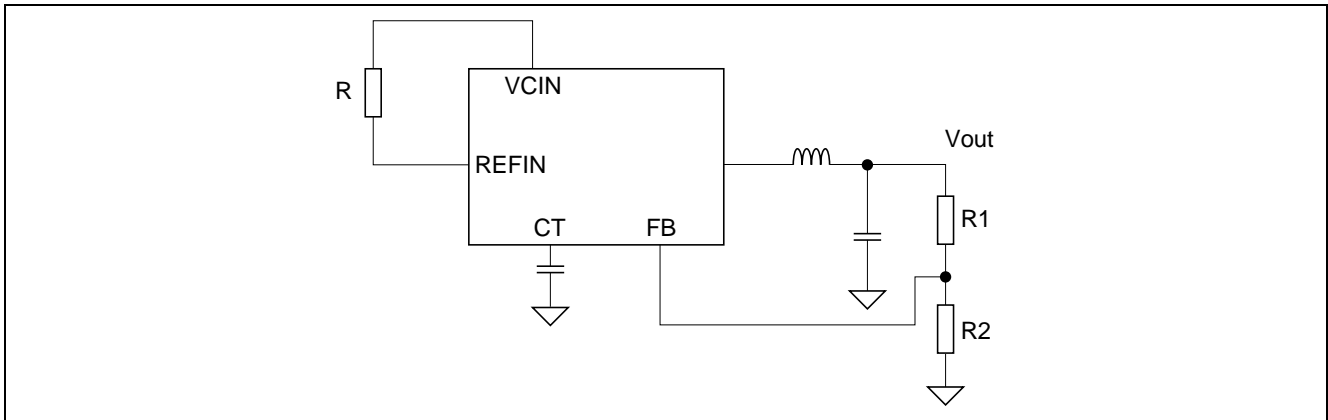
Figure 4

Study of Vout Accuracy

The nominal output voltage is calculated as

$$V_{out} = V_{FB} \times (R1 + R2) / R2 \dots\dots(6)$$

Here, the typical FB voltage is 0.6 V.



The accuracy of Vout is strongly dependent on the variation of VFB, R1 and R2. VFB has variation of 1% and resistance intrinsically has a certain variation. When we take the variation in resistance into account, equation (6) is extended to produce equation (7).

$$\begin{aligned} V_{out} &= \frac{R1 \times K1 + R2 \times K2}{R2 \times K2} \times V_{FB} \\ &= \frac{R1 \times K1 / K2 + R2}{R2} \times V_{FB} \dots\dots(7) \end{aligned}$$

Here, K1 and K2 are coefficients, Both are 1.00 in the ideal case.

By equation (6), R1 is chosen as;

$$R1 = \left[\frac{V_{out} \text{ (typical)}}{V_{FB} \text{ (typical)}} - 1 \right] \times R2 \dots\dots(8)$$

Substituting the expression for R1 into equation (7) yields the following

$$V_{out} = V_{FB} \times \left\{ \left[\frac{V_{out} \text{ (typical)}}{V_{FB} \text{ (typical)}} - 1 \right] \times \frac{K1}{K2} + 1 \right\} \dots\dots(9)$$

Therefore, variation in Vout is expressed as

$$\frac{V_{out}}{V_{out} \text{ (typical)}} = \left[\frac{V_{FB}}{V_{out} \text{ (typical)}} \times \left\{ \left[\frac{V_{out} \text{ (typical)}}{V_{FB} \text{ (typical)}} - 1 \right] \times \frac{K1}{K2} + 1 \right\} - 1 \right] \times 100 \text{ (\%)} \dots\dots(10)$$

The accuracy of Vout can be estimated by using equation (10).

For Example, if Vout (typical) = 1.5 V, resistance variation is 1% (i.e K1, K2 = 1.01 and 0.99), and VFB = 588 mV to 612 mV.

$$\frac{V_{out}}{V_{out} \text{ (typical)}} = \left[\frac{V_{FB}}{V_{out} \text{ (typical)}} \times \left\{ \left[\frac{V_{out} \text{ (typical)}}{V_{FB} \text{ (typical)}} - 1 \right] \times \frac{K1}{K2} + 1 \right\} - 1 \right] \times 100 \text{ (\%)} \dots\dots(10)$$

$$= \left[\frac{612 \text{ mV}}{1.5 \text{ V}} \times \left\{ \left[\frac{1.5 \text{ V}}{600 \text{ mV}} - 1 \right] \times \frac{1.01}{0.99} + 1 \right\} - 1 \right] \times 100 \text{ (\%)}$$

$$= 3.23\%$$

or

$$= \left[\frac{588 \text{ mV}}{1.5 \text{ V}} \times \left\{ \left[\frac{1.5 \text{ V}}{600 \text{ mV}} - 1 \right] \times \frac{0.99}{1.01} + 1 \right\} - 1 \right] \times 100 \text{ (\%)}$$

$$= -3.16\%$$

Therefore, the output accuracy will be ±3.2% under the above conditions.

Figure 5 shows the relationship between the accuracy of the resistance and the accuracy of the output voltage. The resistor value must have an accuracy of 0.5% if the variation in output voltage from the system is to be kept within three percent across the voltage range from 0.6 V to 3.3 V.

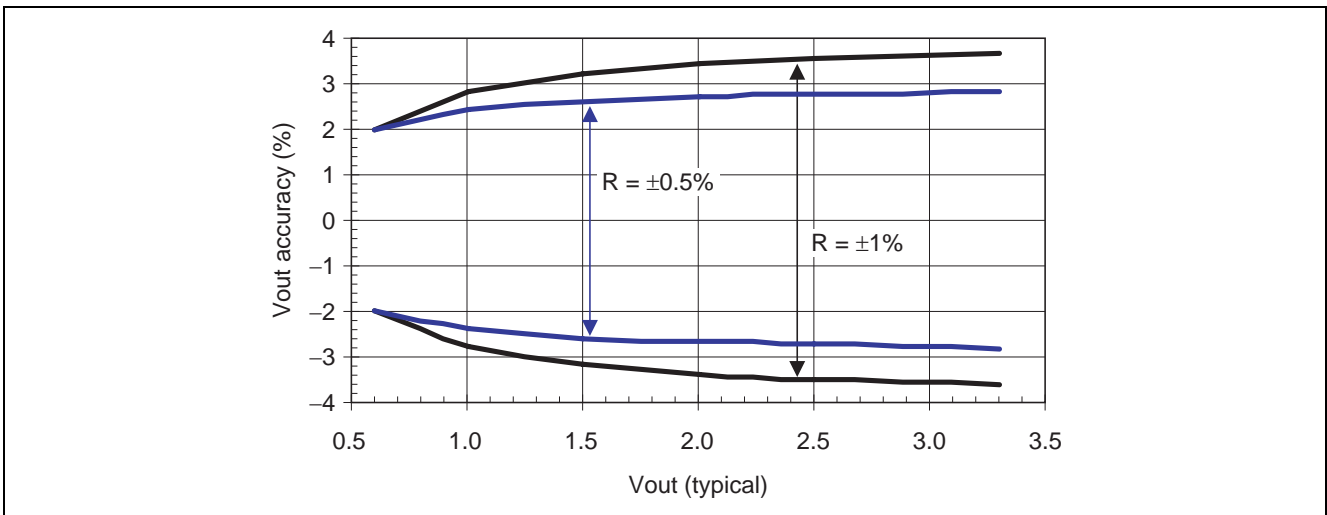
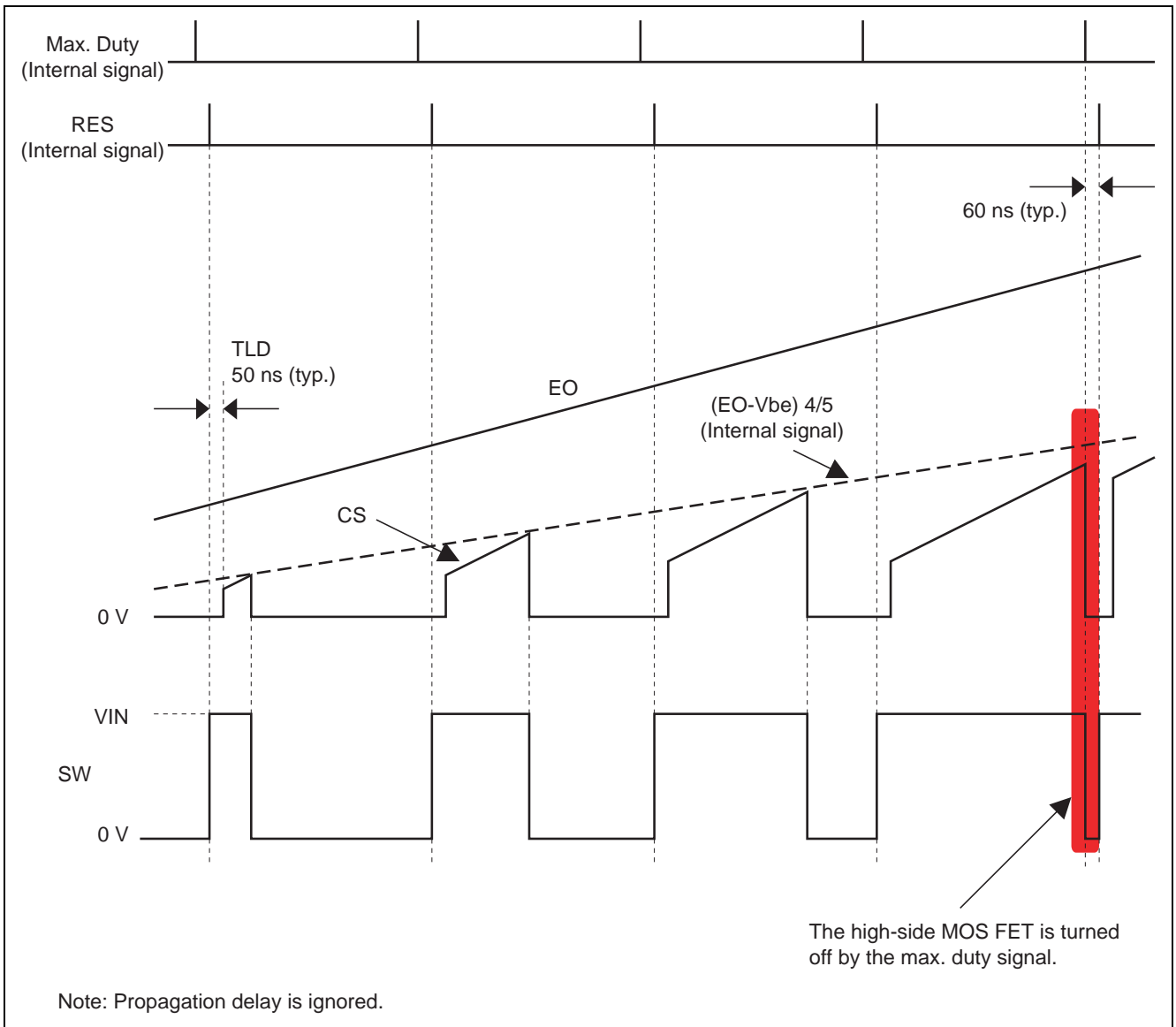


Figure 5 Vout Accuracy vs. Vout Set Voltage

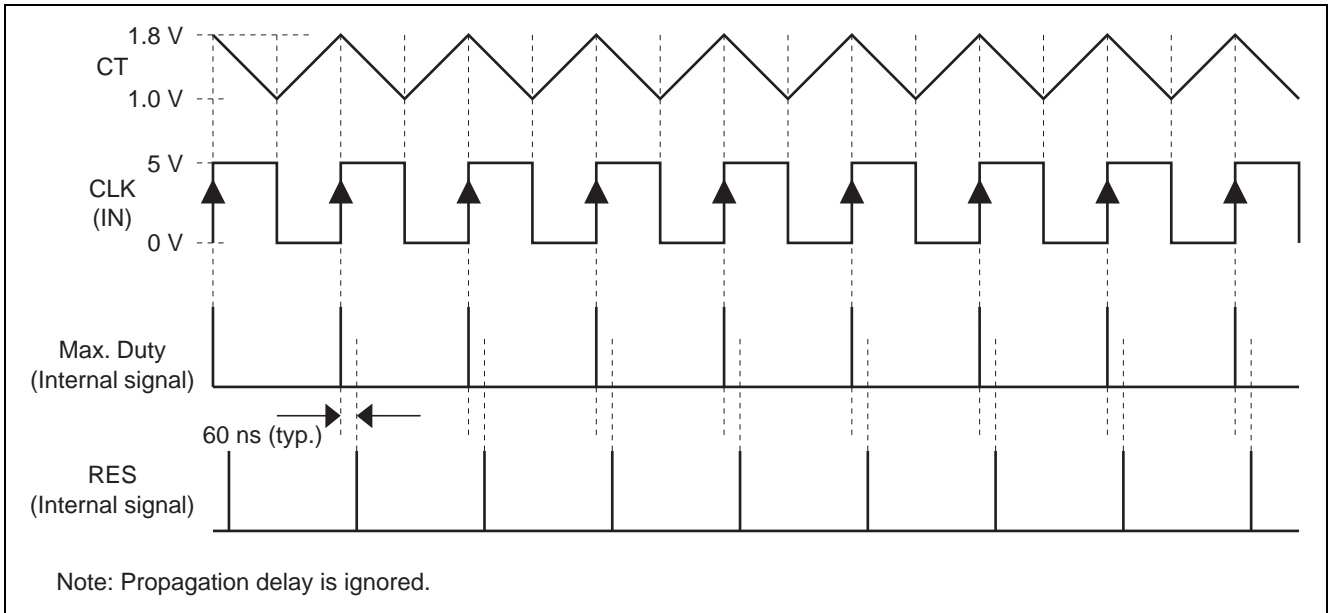
Timing Chart

Peak Current Control



Oscillator and Pulse Generator

1. Standalone operation or working as Master Chip in parallel configuration with other chips.

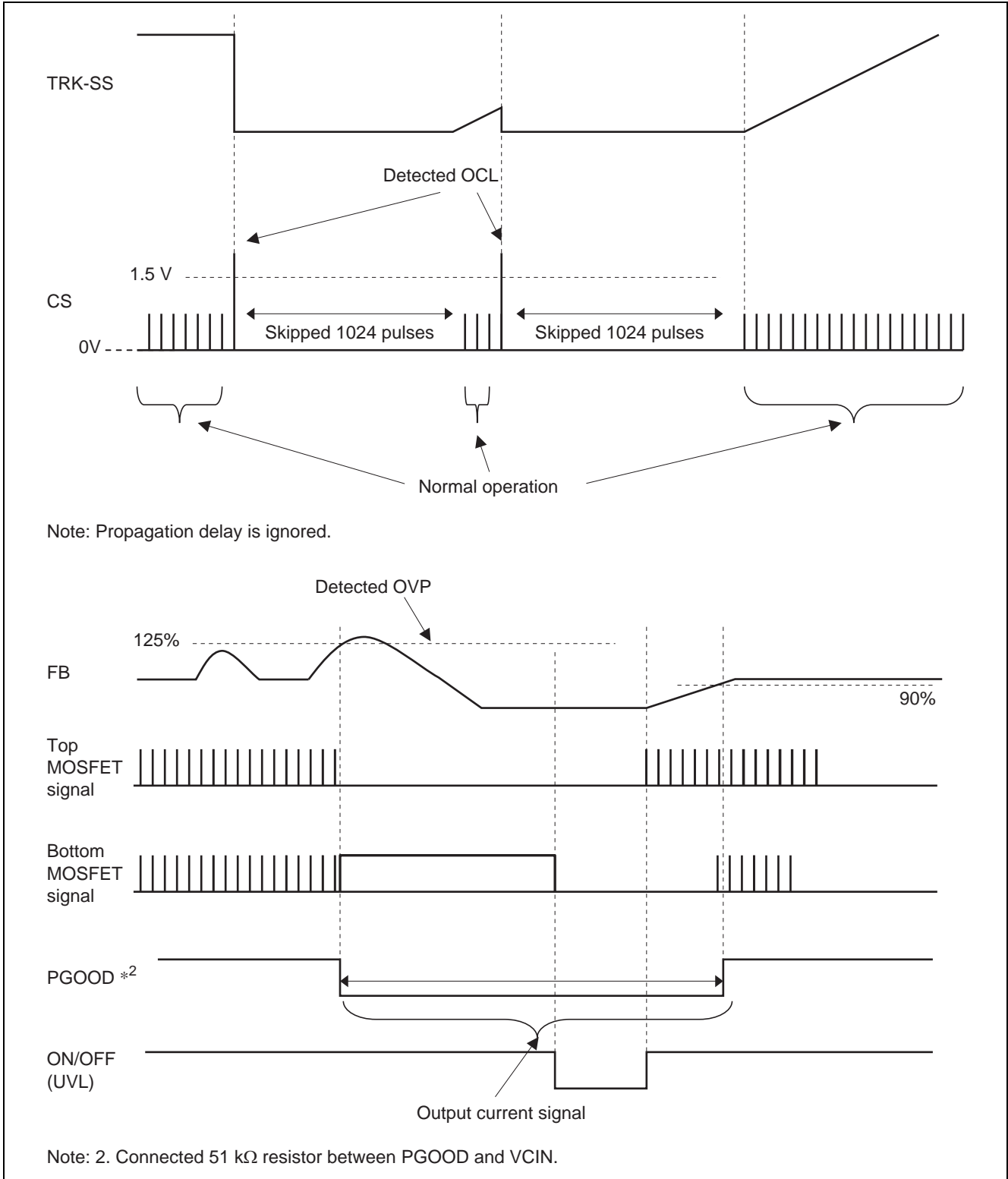


Switching frequency for CT

$$F_{sw} = \frac{160 \mu A}{2 \times (CT(F) + 20 \text{ pF}) \times 0.8 \text{ V} \times N} \text{ (Hz)}$$

Frequency set range: 200 kHz to 1 MHz

Hiccup Operation when the Over-Current Limit (OCL) is Reached

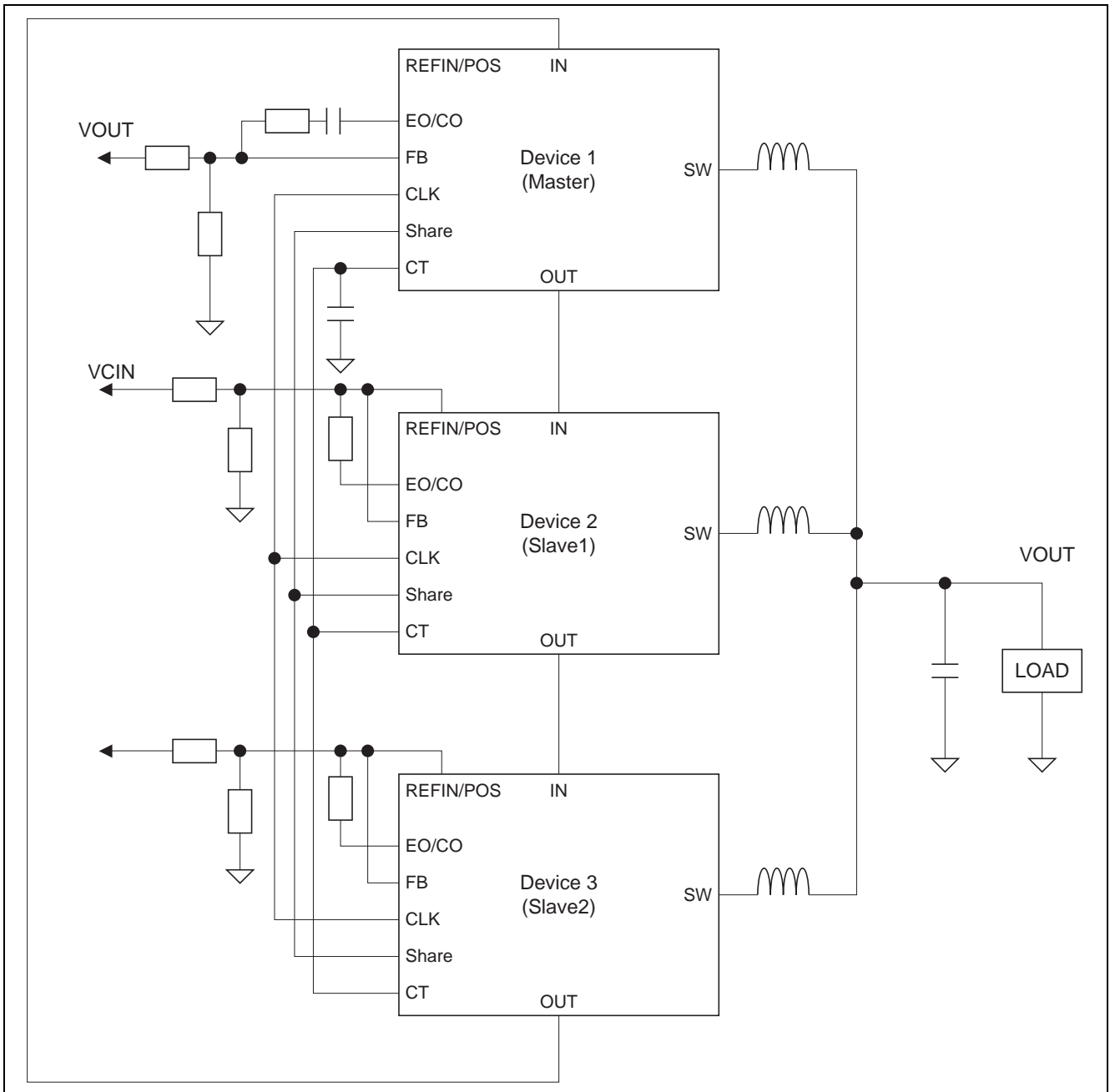


Applications

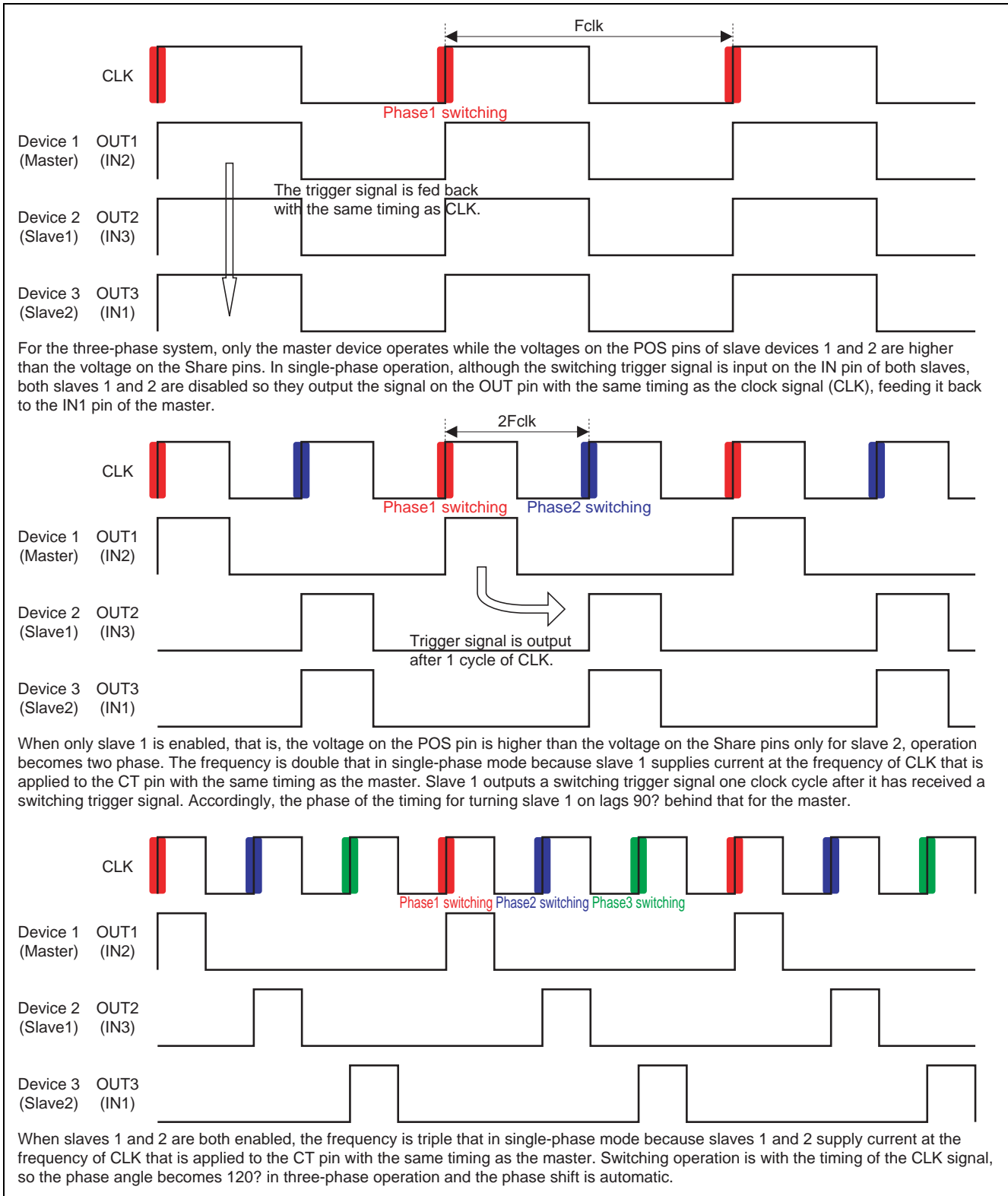
Multi Phase Operation

Tie each CT, CLK and Share pin.

Connect OUT pin to IN pin of next switching device.



Multi Phase Operation Waveforms (3 Phase)



Phase Control

The device incorporates a comparator for control of the phase number. Pulling the voltage on the FB pin up to that on VCIN exchanges the phase control comparator for the error amplifier, and the device operates as a slave. In this case, the output of the comparator (CO) is exchanged for the output of the error amplifier (EO), and the positive input (REFIN) of the error amplifier is exchanged for the positive input (POS) for the comparator. Furthermore, the inverse input for the comparator is internally connected to the Share pin. The level where the phase number is switched is set by an external resistor.

Design example;

Specification: $L = 470 \text{ nH}$, $F_{sw} = 500 \text{ kHz}$, $V_{in} = 5 \text{ V}$, $V_{out} = 1.5 \text{ V}$, $R_{CS} = 820 \Omega$,
Phase switching level is $I_{out} = 10 \text{ A}$, hysteresis = 3.48 A

- Deriving the voltage on the Share pins to return to single-phase operation with $I_{out} = 6.52 \text{ A}$ (3.48 A of hysteresis) from two-phase operation with $I_{out} = 10 \text{ A}$.

The peak of the output ripple current is:

$$I_{pp} (10 \text{ A}) = (V_{IN} - V_{out}) / L \times V_{out} / V_{IN} / F_{sw} / 2 + I_{out} (10 \text{ A}) = 12.23 \text{ A}$$

When $I_{out} = 6.52 \text{ A}$ in two-phase mode, current from each device is 3.26 A . Thus,

$$I_{pp} (3.26 \text{ A}) = (V_{IN} - V_{out}) / L \times V_{out} / V_{IN} / F_{sw} / 2 + I_{out} (3.26 \text{ A}) = 5.49 \text{ A}$$

The ratio between currents for the sense MOS FET and main MOS FET is 1:13700, so a bias current of $300 \mu\text{A}$ flows through the CS pin.

Thus, voltages on the CS pin are:

$$V_{cs} (10 \text{ A}) = (I_{pp} (10 \text{ A}) / 13700 + 300 \mu\text{A}) \times R_{cs} = 978 \text{ mV and}$$

$$V_{cs} (3.26 \text{ A}) = (I_{pp} (3.26 \text{ A}) / 13700 + 300 \mu\text{A}) \times R_{cs} = 575 \text{ mV.}$$

The non-inverted input terminal of the internal current sense comparator has an offset voltage of 0.2 V , and $40\text{-k}\Omega$ and $10\text{-k}\Omega$ resistors are connected to the inverted input terminal.

Therefore, the Share voltages are:

$$V_{share} (10 \text{ A}) = (V_{cs} (10 \text{ A}) + 0.2 \text{ V}) \times 5 / 4 = 1.473 \text{ V and(11)}$$

$$V_{share} (3.26 \text{ A}) = (V_{cs} (3.26 \text{ A}) + 0.2 \text{ V}) \times 5 / 4 = 0.969 \text{ V.(12)}$$

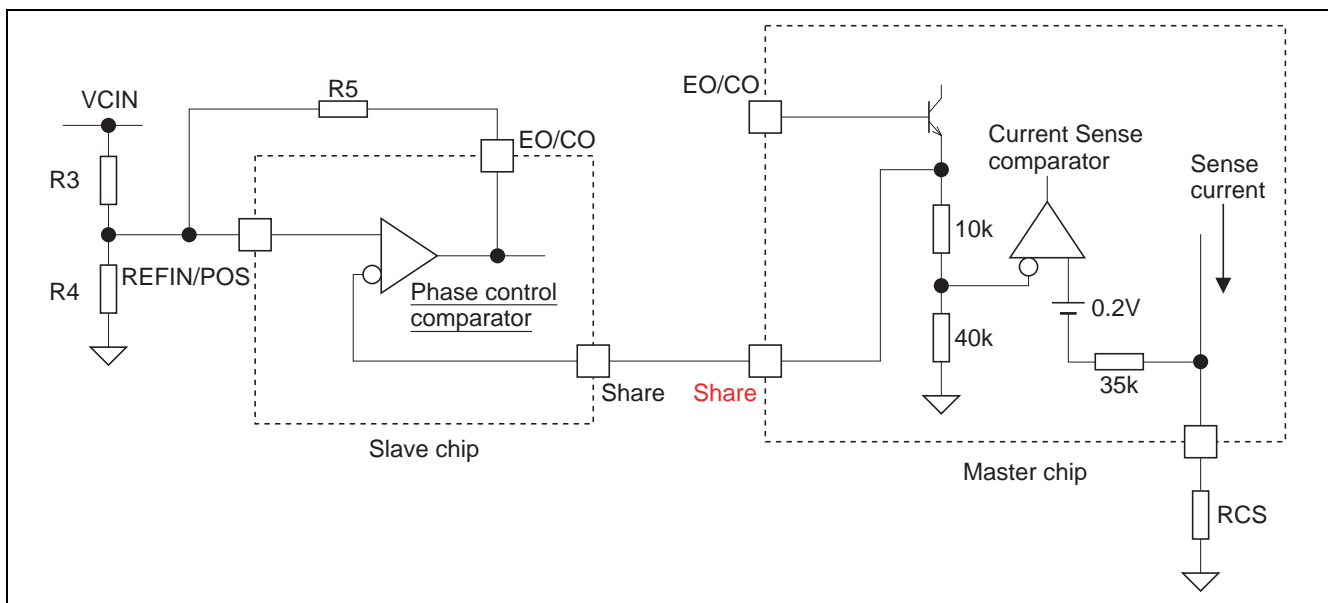
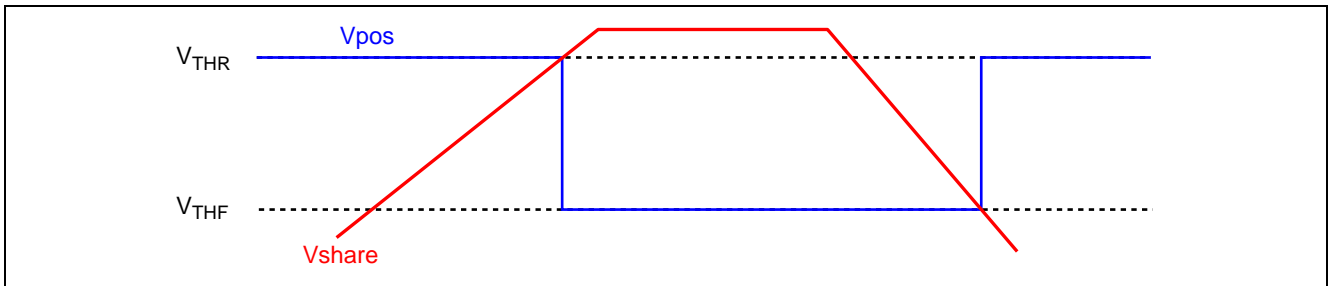


Figure 6 Phase Switching Control



2. Selecting the external resistors

When the output of phase control comparator becomes low, switching operation of the slave device starts and operation becomes two phase. According to the results of (11) and (12), V_{THR} and V_{THF} are 1.473 V and 0.969 V. These become the voltages on the POS pins (comparator non-inverted input pin). V_{THR} is the start-up level for the slave device and V_{THF} is the shut-down level for the slave device.

We set the output current of CO at around 100 μA when the voltage on Share is 1.379 V. In this case, R5 is:

$$R5 = (V_{CIN} - 1.379) / 100 \mu\text{A} = 35.27 \text{ k}\Omega$$

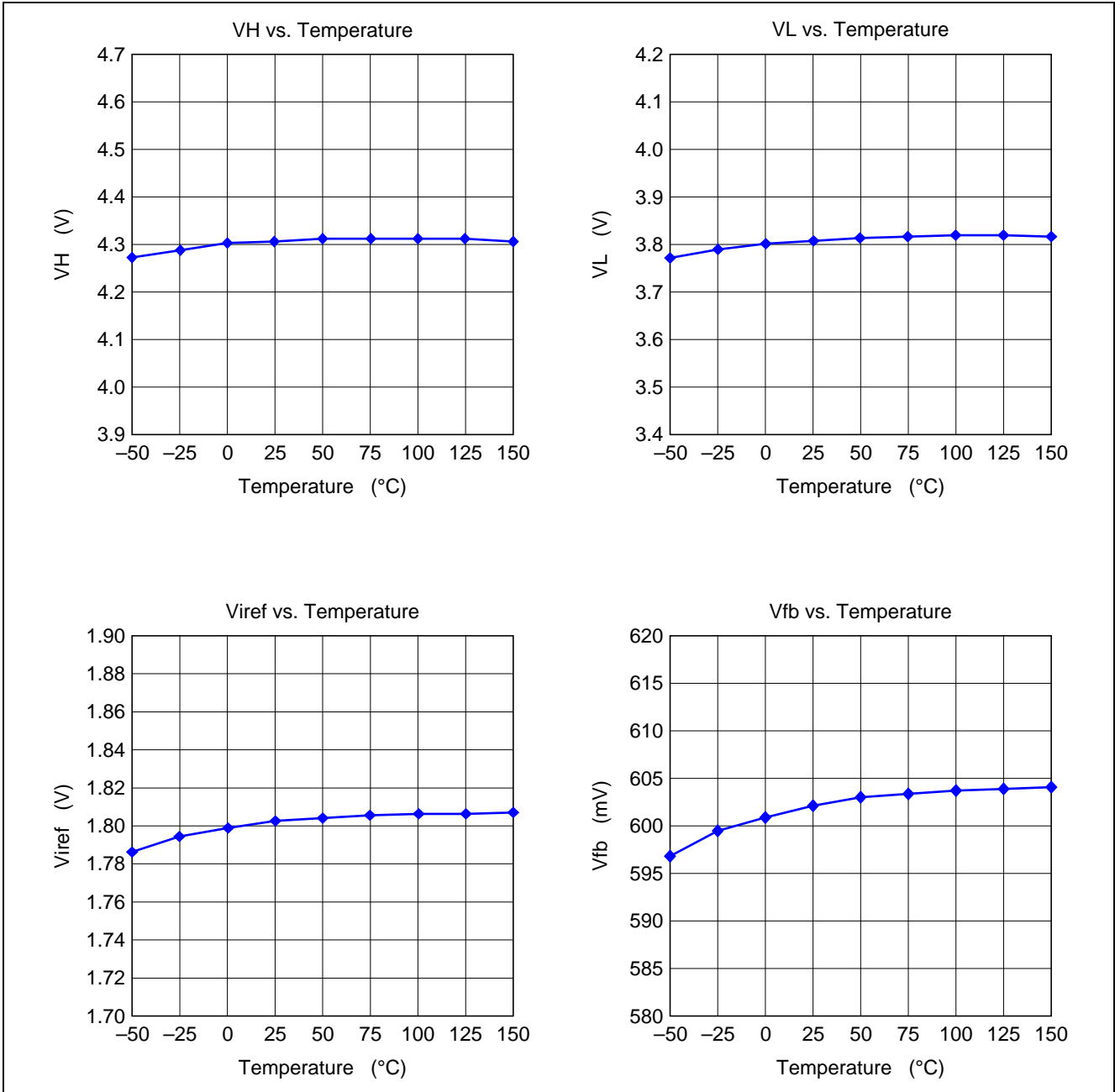
The formulae that express R3 and R4 are:

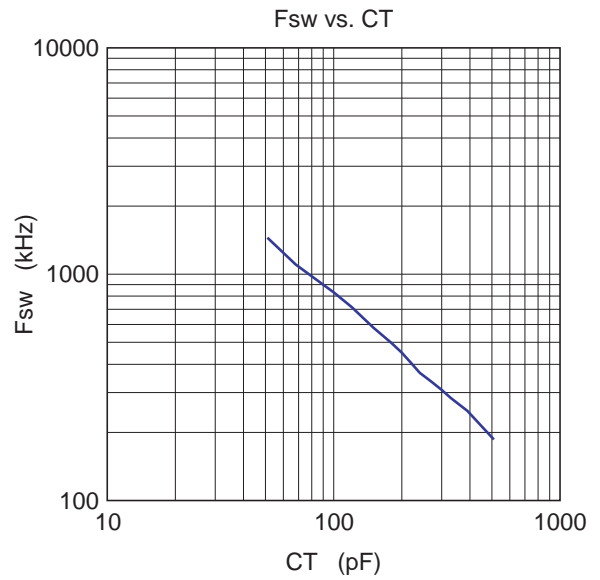
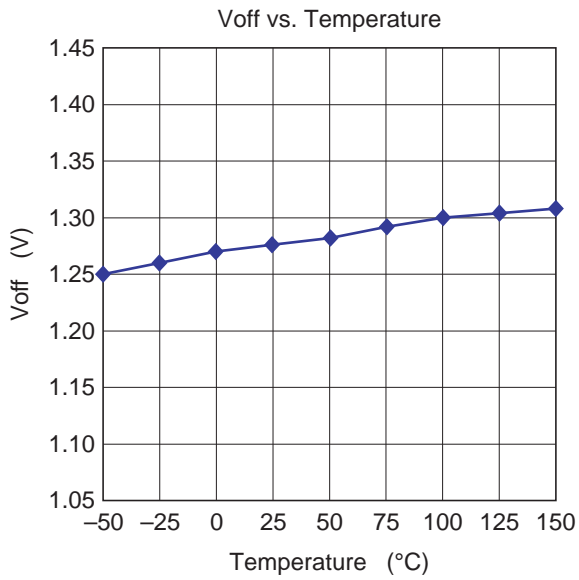
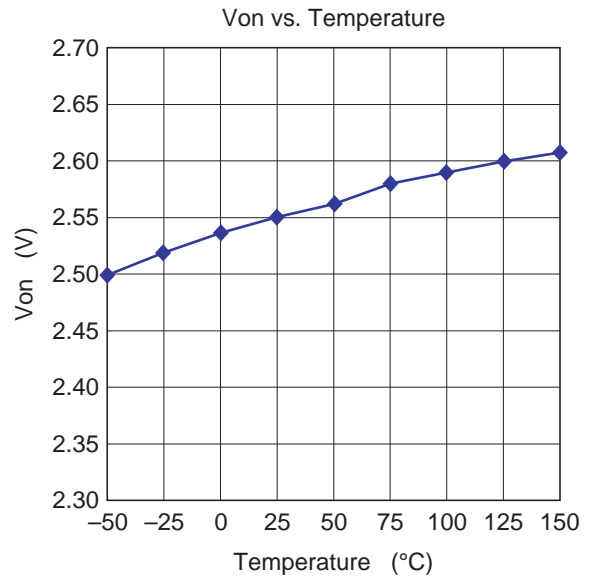
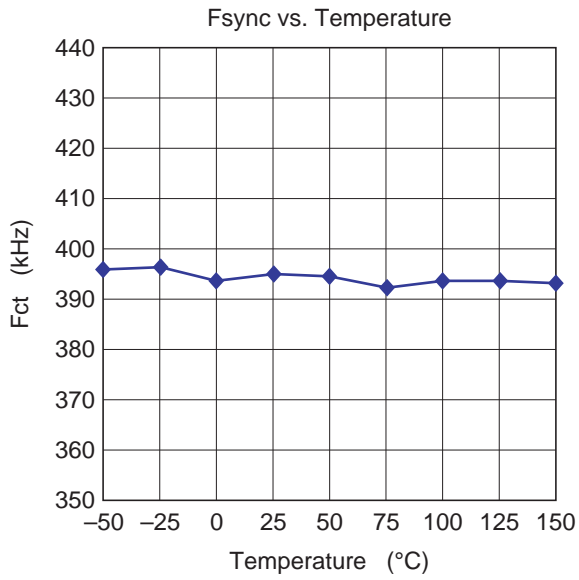
$$R3 = R4 \times R5 / (R4 + R5) \times (V_{CIN} - V_{THF}) / V_{THF} = 18.34 \text{ k}\Omega \text{ and}$$

$$R4 = R5 \times (V_{THR} - V_{THF}) / (V_{CIN} - V_{THR}) = 5.04 \text{ k}\Omega.$$

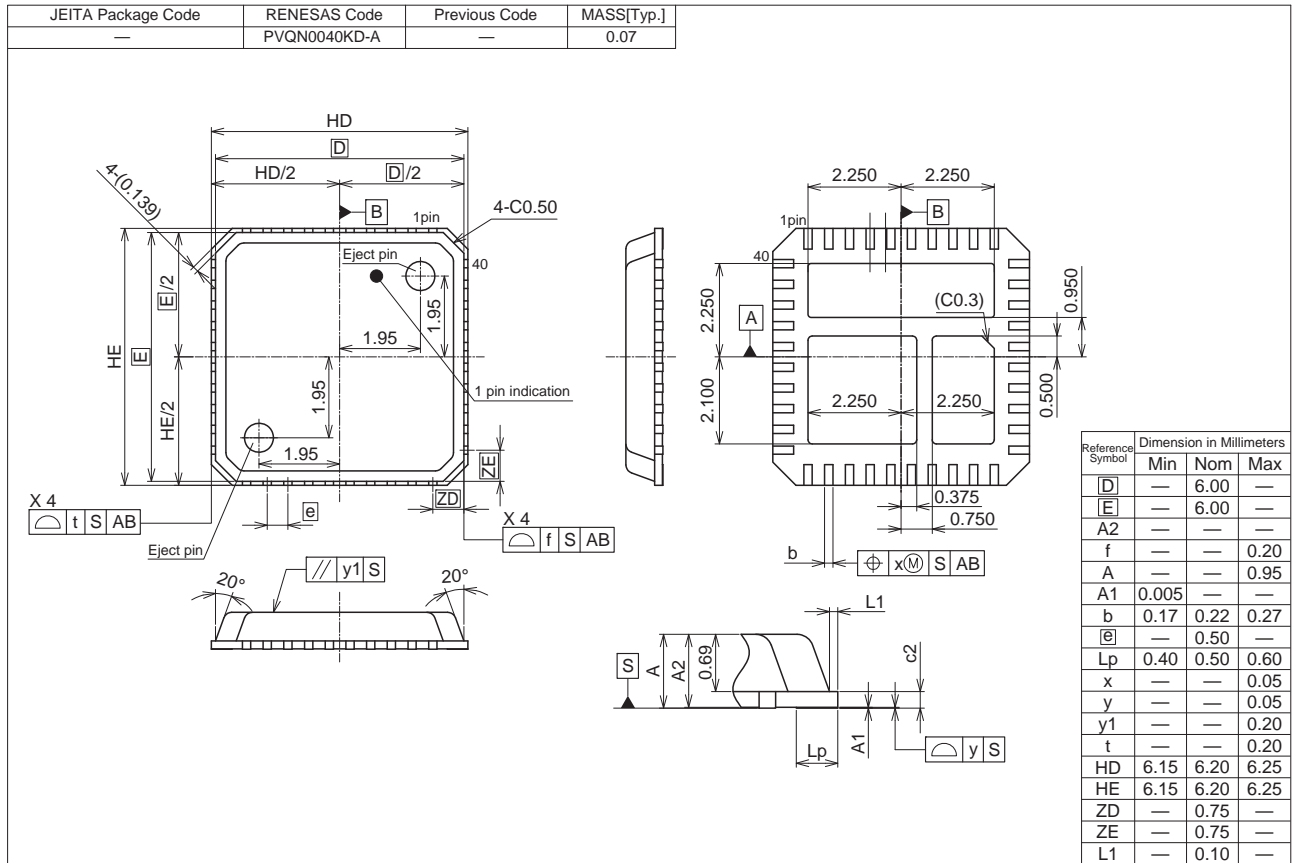
With E24-series resistors, $R3 = 18 \text{ k}\Omega$, $R4 = 5.1 \text{ k}\Omega$, and $R5 = 36 \text{ k}\Omega$.

Main Characteristics





Package Dimensions



Ordering Information

| Part Name | Quantity | Shipping Container |
|---------------|----------|--------------------|
| R2J20751NP#G0 | 2500 pcs | Taping Reel |

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