# Industrial micro SD card

## SD Series

**Customer:** _____

**Customer
Part Number:** _____

**InnoDisk
Part Number:** _____

**InnoDisk
Model Name:** _____

**Date:** _____

| InnoDisk Approver | Customer Approver |
|---|---|
|  |  |

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# REVISION HISTORY

| Revision | Description | Date |
|---|---|---|
| Preliminary | First released | Jan. 2012 |
| 1.0 | Add 8GB in available capacities. | Sep. 2012 |
| 1.1 | 1. Update product picture<br>2. Add features<br>3. Add description of enhanced power cycling<br>4. Add chapter of i-S.M.A.R.T Utility | Nov. 2012 |

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# 1.  Product Introduction

## 1.1. Overview

While micro SD card has been a popular embedded storage device for mobile market, InnoDisk has been developing a more reliable micro SD card that will support ruggedized applications in the embedded fields. Therefore, InnoDisk would like to introduce you the industrial-grade micro SD card built with SLC (Single Level Cell) flash, delivering the most reliable micro SD card with outstanding performance and excellent endurance.

In additional to the traditional SD Cards, InnoDisk's industrial micro SD card supports S.M.A.R.T function that can be used to monitor the health of storage.

## 1.2. Product Picture



**Figure 1: Industrial micro SD card picture**

## 1.3. Product Features

· Interface: 8 pins SD standard interface

· SLC NAND Flash

· Compatible with SD 1.1/2.0

· Support SD/SPI mode

· Capacity: 1GB, 2GB, 4GB, 8GB

· Built-in ECC corrects up to 16 bits per 1 KB

· Dimension (W x L x H): 11 x 15 x 1 mm

· Sequential read/write performance: 20/16 MB/sec (max.)

· Resistance to Shock and Vibration

· Enhanced endurance by Global Wear-Leveling algorithm

· Support i.S.M.A.R.T utility to monitor status of InnoDisk micro SD card.

- Enhanced Power Cycling: Pass 1,000 times copy and compare test under Non-Safe Mode/Safe Mode.

- RoHS Compliance

- Support CPRM

- CE & FCC Compatibility


# 2. Theory of operation

## 2.1. Overview

Figure 2 shows the operation of InnoDisk Industrial micro SD Card from the system level, including the major hardware blocks.
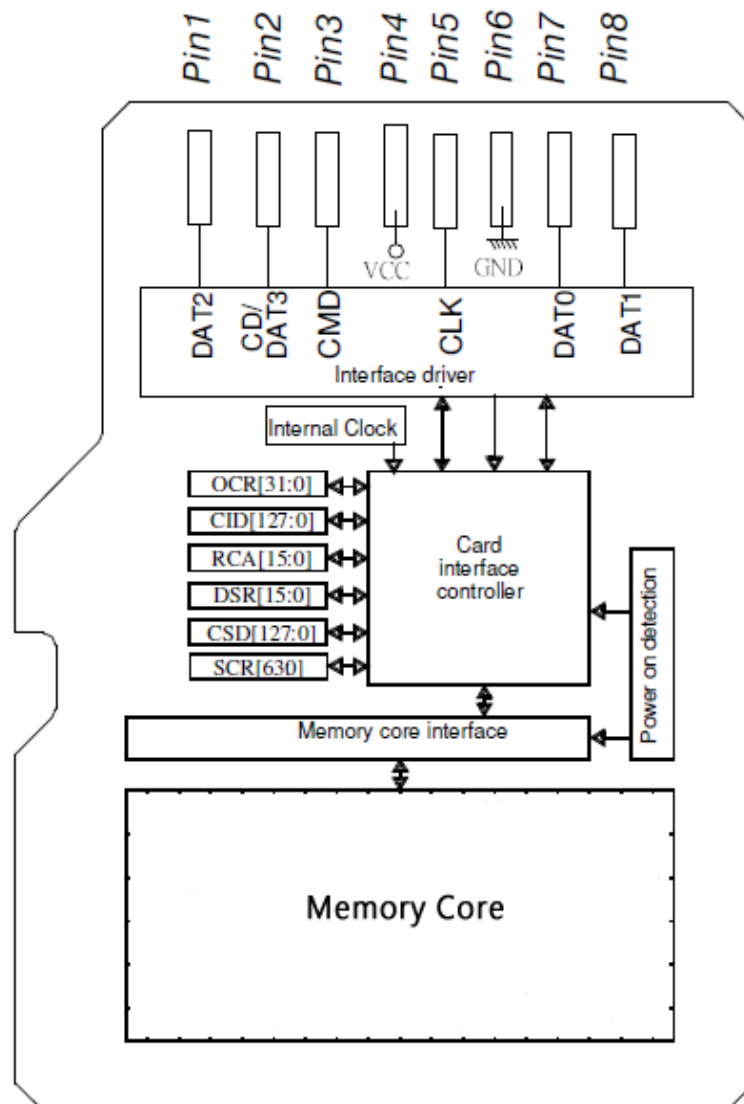


**Figure 2: InnoDisk Industrial micro SD Card Architecture**

## 2.2. Error Detection and Correction ECC

Highly sophisticated Error Correction Code algorithms are implemented. The ECC unit consists of the Parity Unit (parity-byte generation) and the Syndrome Unit (syndrome-byte computation). This unit implements an algorithm that can correct 16 bits per 1 KB in an ECC block. Code-byte generation during write operations, as well as error detection during read operation, is implemented on the fly without any speed penalties.

## 2.3. Wear-Leveling

Flash memory can be erased within a limited number of times. This number is called the **erase cycle limit** or **write endurance limit** and is defined by the flash array vendor. The erase cycle limit applies to each individual erase block in the flash device.

InnoDisk Industrial micro SD Card uses a wear-leveling algorithm to ensure that consecutive writes of a specific sector are not written physically to the same page and block in the flash. This spreads flash media usage evenly across all pages, thereby extending flash lifetime.

## 2.4. Bad Blocks Management

Bad Blocks are blocks that contain one or more invalid bits whose reliability are not guaranteed. The Bad Blocks may be presented while the micro SD is shipped, or may develop during the life time of the SD. The Bad Blocks will not exceed more than 3% of the total device volume. When the Bad Blocks is detected, it will be flagged, and not be used anymore. The micro SD implement Bad Blocks management, Bad Blocks replacement, Error Correct Code to avoid data error occurred. The functions will be enabled automatically to transfer data from Bad Blocks to spare blocks, and correct error bit.

# 3. Specifications

## 3.1. Performance

Data Transfer Rate (Sequential Read/Write MB/sec, Max.)
- 8GB: 20/16
- 4GB: 20/14
- 2GB: 16/9
- 1GB: 14/8

### 3.2. NAND Flash Memory

InnoDisk Industrial SLC micro SD Card uses Single Level Cell (SLC) NAND flash memory, which is non-volatility, high reliability and high speed memory storage.

### 3.3. Power Requirement

### 3.3.1. DC Input Voltage

2.7V to 3.6V

### 3.3.2. Power Mode

Auto stand-by and sleep mode

### 3.3.3. Power Consumption

**Table 1*: InnoDisk Industrial micro SD Card power consumption***

| | |
|---|---|
| Sustained Read | 30 mA |
| Sustained Write | 50 mA |
| IDLE | 160 µA |

### 3.4. Storage Temperature Range

- Operating Temperature Range

  ■ Standard: 0°C to +70°C

  ■ Industrial: -40°C to +85°C

- Storage Temperature Range: -55°C to +95°C

### 3.5. Humidity

Relative Humidity: 10-95%, non-condensing

### 3.6. Shock and Vibration

**Table 2: Shock/Vibration Testing for InnoDisk Industrial micro SD Card**

| Reliability | Test Conditions |
|---|---|
| Vibration | 7 Hz to 2000 Hz, 5G, 3 axes |
| Mechanical Shock | Duration: 10ms, 50G, 3 axes |

### 3.7. System Reliability

### 3.7.1. ECC Technology

High reliability based on the internal error correct code (ECC) function. Built-in

ECC corrects up to 16 bits per 1 KB.

### 3.7.2. Mean Time between Failures (MTBF)

Table 2 summarizes the MTBF prediction results for various InnoDisk Industrial SD Card configurations. The analysis is performed using a RAM Commander™ failure rate prediction.

- **Failure Rate**: The total number of failures within an item population, divided by the total number of life units expended by that population, during a particular measurement interval under stated condition.

- **Mean Time between Failures (MTBF)**: A basic measure of reliability for repairable items: The mean number of life units during which all parts of the item perform within their specified limits, during a particular measurement interval under stated conditions.

**Table 3: InnoDisk Industrial micro SD Card MTBF**

| Product | Condition | MTBF (Hours) |
|---|---|---|
| InnoDisk Industrial micro SD Card | Telcordia SR-332 GB, 25°C | > 3,000,000 |

### 3.7.3. Enhanced Power Cycling Technology

In order to make sure InnoDisk Industrial micro SD Card can work well under unstable power supply environments. Our FW enhance the power cycling ability and pass following test modes with 1,000 times.

- **Non-Safe Mode test**: Power off when accessing files.

- **Safe Mode test**: Power off when accessing files finish.

### 3.8. Certificate

- **CE and FCC Compatibility**
  InnoDisk Industrial micro SD Card conforms to CE and FCC requirements.

- **RoHS Compliance**
  InnoDisk Industrial micro SD Card is fully compliant with RoHS directive.

### 3.9. Pin Description

### 3.9.1. Industrial micro SD Card Pin Direction
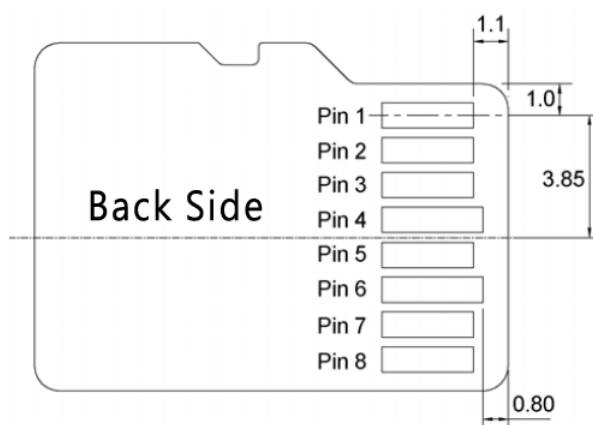
**Figure 3: Industrial micro SD Card Pin Direction**

### 3.9.2. Pin Assignment

Table 4 demonstrates InnoDisk Industrial micro SD Card pin assignments.

**Table 4: InnoDisk Industrial micro SD Card Pin Assignment**

| Pin # | micro SD Mode | | | SPI Mode | | |
|-------|------|------|-------------|------|------|-------------|
|       | **Name** | **Type** | **Description** | **Name** | **Type** | **Description** |
| 1 | DAT2 | Bi-directionally I/O, I/O using Push-Pull Drivers | Data line bit 2. For read only cards, DAT2 is output only. | - | - | Reserved for future use. Host should pull up with 10 to 100K ohm resistance. |
| 2 | CD, DAT3 | Bi-directionally I/O, I/O using Push-Pull Drivers | Card Detect, Data line bit 3. See Notes 1 and 2. | /CS | Input | Chip select ("/" indicates low active) |
| 3 | CMD | I/O using Push-Pull Drivers | Command/Response | DI | Input | Data in |
| 4 | VDD | Supply | Supply voltage | VDD | Supply | Supply voltage |
| 5 | CLK | Input | Clock | CLK | Input | Clock |
| 6 | VSS | Supply | Supply voltage ground | VSS | Supply | Supply voltage ground |
| 7 | DAT0 | Bi-directionally I/O, I/O using Push-Pull Drivers | Data line bit 0. For read only cards, DAT0 is output only. | DO | Output, I/O using Push Pull Drivers | Data out |
| 8 | DAT1 | Bi-directionally I/O, I/O using Push-Pull Drivers | Data line bit 1. For read only cards, DAT1 is output only. | - | - | Reserved for future use. Host should pull up with 10 to 100K ohm resistance. |

Notes:

1. The extended DAT lines (DAT1-DAT3) are input on power up. They start to operate as DAT lines after SET_BUS_WIDTH command. The Host shall keep its own DAT1-DAT3 lines in input mode, as well, while they are not used. It is defined so, in order to keep compatibility to MultiMediaCards.

2. After power up the CD line is input with 50KOhm pull-up (can be used for card detection or SPI mode selection). The pull-up should be disconnected by the user, during regular data transfer, with SET_CLR_CARD_DETECT (ACMD42) command.

# 4. Electrical Specifications

## 4.1. General DC Character

### Table 5: General DC Character

| Parameter | Symbol | Min. | Max. | Unit | Remark |
|---|---|---|---|---|---|
| Peak voltage on all lines | | -0.3 | 3.6 | V | |
| All input leakage current | | -10 | 10 | µA | |
| All output leakage current | | -10 | 10 | µA | |
| Supply voltage for low voltage range | $V_{DDL}$ | 1.7 | 1.95 | V | |
| Supply voltage for high voltage range | $V_{DDH}$ | 2.7 | 3.6 | V | |
| Supply voltage differential | | -0.5 | 0.5 | V | |

## 4.2. Bus Signal Line Loading

### Table 6: Bus Signal Line Loading

| Parameter | Symbol | Min. | Max. | Unit | Remark |
|---|---|---|---|---|---|
| Pull up resistance for SDC line | $R_{CMD}$ | 10 | 100 | K Ohm | To prevent bus floating |
| Pull up resistance for SDD line | $R_{DAT}$ | 10 | 100 | K Ohm | To prevent bus floating |
| Total Bus capacitance for each signal line | $C_L$ | | 40 | pF | Single card $C_{HOST}+C_{BUS}$ shall not exceed 30 pF |
| Signal line inductance | | | 16 | nH | $f_{PP} <= 20$ MHZ |
| Pull-up resistance inside card (pin 1) | $R_{DAT3}$ | 10 | 90 | K Ohm | May be used for card detection |

## 4.3. Bus Signal Level
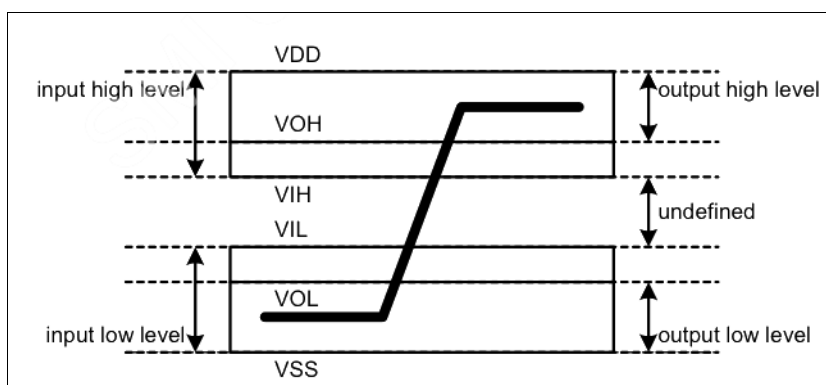


**Figure 4: Bus Signal Level**

**Table 7: Bus Signal Level**

| Parameter | Symbol | Min. | Max. | Unit | Remark |
|---|---|---|---|---|---|
| Output High voltage | $V_{OH}$ | 2.4 | | V | $V_{DD}$ = 3.3V |
| Output Low voltage | $V_{OL}$ | | 0.4 | V | $V_{DD}$ = 3.3V |
| Input High voltage | $V_{IH}$ | 2 | 3.6 | V | $V_{DD}$ = 3.3V |
| Input Low voltage | $V_{IL}$ | -0.3 | 0.8 | V | $V_{DD}$ = 3.3V |
| Output High voltage | $V_{OH}$ | 1.6 | | V | $V_{DD}$ = 1.8V |
| Output Low voltage | $V_{OL}$ | | 0.2 | V | $V_{DD}$ = 1.8V |
| Input High voltage | $V_{IH}$ | 1.26 | 2.1 | V | $V_{DD}$ = 1.8V |
| Input Low voltage | $V_{IL}$ | -0.3 | 0.54 | V | $V_{DD}$ = 1.8V |

## 4.4. Bus Timing (High Speed Mode)
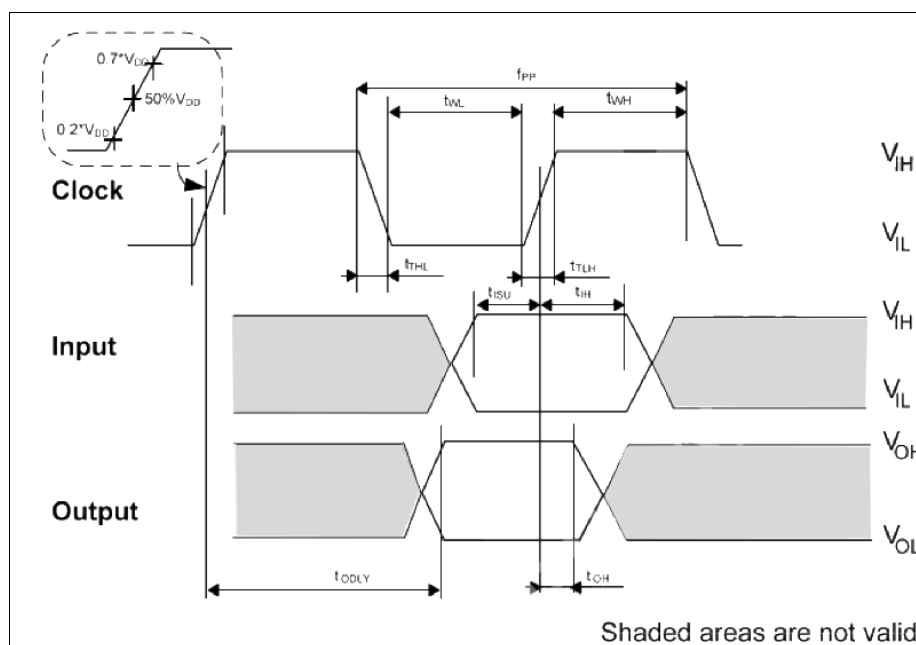


**Figure 5: Timing diagram data input/output referenced to clock**

## Table 8: High Speed Mode Bus Timing

| Parameter | Symbol | Min. | Max. | Unit | Remark |
|---|---|---|---|---|---|
| **Input SDCK** | | | | | |
| Clock frequency data transfer mode | $f_{PP}$ | 0 | 50 | MHz | $C_{CARD}$ <= 10pF (1 card) |
| Clock low time / Clock high time | $t_{WL}$ / $t_{WH}$ | 7 | | ns | $C_{CARD}$ <= 10pF (1 card) |
| Clock rise time / Clock fall time | $t_{TLH}$ / $t_{THL}$ | | 3 | ns | $C_{CARD}$ <= 10pF (1 card) |
| **Input SDD/SDC, reference to SDCK** | | | | | |
| Input set-up time | $t_{ISU}$ | 6 | | ns | $C_{CARD}$ <= 10pF (1 card) |
| Input hold time | $t_{IH}$ | 2 | | ns | $C_{CARD}$ <= 10pF (1 card) |
| **Output SDD/SDC, reference to SDCK** | | | | | |
| Output delay time during Data Transfer Mode | $t_{ODLY}$ | | 14 | ns | $C_L$ <= 40pF (1 card) |
| Output hold time | $t_{OH}$ | 2.5 | | ns | $C_L$ >= 15pF (1 card) |
| Total System capacitance for each line | $C_L$ | | 40 | pF | |

# 5. Register Table

## 5.1. Operation Condition Register (OCR)

The 32-bit operation conditions register stores the VDD voltage profile of the card. In addition, this register includes status information bits. One status bit is set if the card power up procedure has been finished. This register includes another status bit indicating the card capacity status after set power up status bit. The OCR register shall be implemented by all cards. As long as the card is busy, the corresponding bit (31) is set to LOW.

Additionally, this register includes 2 more status information bits. Bit 31 – Card power up status bit, this status bit is set if the card power up procedure has been finished. Bit 30 – Card capacity status bit, this status bit is set to 1 if card is High Capacity SD Memory Card. 0 indicates that the card is Standard Capacity SD Memory Card. The Card Capacity status bit is valid after the card power up procedure is completed and the card power up status bit is set to 1. The Host shall read this status bit to identify a Standard or High Capacity SD Memory Card.

## Table 9: InnoDisk Industrial micro SD Card OCR Table

| OCR bit | VDD voltage window | Value |
|---|---|---|
| [6:0] | Reserved | 000 0000 b |
| [7] | 1.7V – 1.95V | 0 b |
| [14:8] | 2.0V – 2.6V | 000 0000 b |
| [23:15] | 2.7V – 3.6V | 1 1111 1111 b |

| [29:24] | Reserved | 00 0000 b |
|---------|----------|-----------|
| [30] | Card capacity status | |
| [31] | Card power status | |

## 5.2. Card Identification Register (CID)

The Card IDentification (CID) register is 128 bits wide. It contains the card identification information used during the card identification phase. Every individual flash card shall have a unique identification number. The structure of the CID register is defined in the following table.

**Table 10: InnoDisk Industrial micro SD Card CID Table**

| CID bit | Width | Name | Field |
|---------|-------|------|-------|
| [127:120] | 8 | Manufacturer ID | MID |
| [119:104] | 16 | OEM/Application ID | OID |
| [103:64] | 40 | Product Name | PNM |
| [63:56] | 8 | Product Revision | PRV |
| [55:24] | 32 | Product Serial Number | PSN |
| [23:20] | 4 | Reserved | --- |
| [19:8] | 12 | Manufacturing Date | MDT |
| [7:1] | 7 | CRC7 check sum | CRC |
| [0] | 1 | Not used, always '1' | --- |

## 5.3. Relative Card Address Register (RCA)

The writable 16-bit relative card address register carries the card address this is published by the card during the card identification. This address is used for the addressed host-card communication after the card identification procedure. The default value of the RCA register is 0x0000. The value 0x0000 is reserved to set all cards into the Stand-by State with CMD7

## 5.4. Card Specific Data Register (CSD)

The Card-Specific Data register provides information on how to access the card contents. The CSD defines the data format, error correction type, maximum data access time, data transfer speed, whether the DSR register can be used etc. The programmable part of the register can be changed by CMD27.

**Table 11: InnoDisk Industrial micro SD Card CSD Table for High Capacity**

| CSD bit | Width | Name | Field | Value | Note |
|---------|-------|------|-------|-------|------|
| [127:126] | 2 | CSD Structure | CSD_STRUCTURE | 01 b | v.2.0 |

| [125:120] | 6 | Reserved | --- | --- | --- |
|---|---|---|---|---|---|
| [119:112] | 8 | Data read access time 1 | TAAC | 0E h | 1ms (*3) |
| [111:104] | 8 | Data read access time 2 | NSAC | 00 h | (*3) |
| [103:96] | 8 | Max. data transfer rate | TRAN_SPEED | 32 h | 25MHz |
| [95:84] | 12 | Card command classes | CCC | 5F5h | (*1) |
| [83:80] | 4 | Max. read data block length | READ_BL_LEN | 9 h | 512bytes(*3) |
| [79] | 1 | Partial block read allowed | READ_BL_PARTIAL | 0 b | Not Supported (*3) |
| [78] | 1 | Write block misalignment | WRITE_BLK_MISALIGN | 0 b | Not Supported (*3) |
| [77] | 1 | Read block misalignment | READ_BLK_MISALIGN | 0 b | Not Supported (*3) |
| [76] | 1 | DSR implemented | DSR_IMP | 0 b | Not supported (*3) |
| [75:70] | 6 | Reserved | --- | 000000b | --- |
| [69:48] | 22 | Device size | C_SIZE | (*2) | (*2) |
| [47] | 1 | Reserved | --- | 0 b | --- |
| [46] | 1 | Erase single block enable | ERASE_BLK_EN | 1 b | Allowed (*3) |
| [45:39] | 7 | Erase sector size | SECTOR_SIZE | 7Fh | 64KB (*3) |
| [38:32] | 7 | Write protect group size | WP_GRP_SIZE | 00h | (*3) |
| [31] | 1 | Write protect group enable | WP_GRP_ENABLE | 0 b | Not Supported (*3) |
| [30:29] | 2 | Reserved | --- | --- | --- |
| [28:26] | 3 | Write speed factor | R2W_FACTOR | 010 b | 4X (*3) |
| [25:22] | 4 | Max. write data block length | WRITE_BL_LEN | 9 h | 512bytes (*3) |
| [21] | 1 | Partial block write allowed | WRITE_BL_PARTIAL | 0 b | Not Supported (*3) |
| [20:16] | 5 | Reserved | --- | --- | --- |
| [15] | 1 | File format group | FILE_FORMAT_GRP | 0 b | HD like FAT (*3) |
| [14] | 1 | Copy flag | COPY | 0 b | Not copied |
| [13] | 1 | Permanent write protection | PERM_WRITE_PROTECT | 0 b | Not protected |
| [12] | 1 | Temporary write protection | TMP_WRITE_PROTECT | 0 b | Not protected |
| [11:10] | 2 | File format | FILE_FORMAT | 00 b | HD like FAT (*3) |
| [9:8] | 2 | ECC code | ECC | 00 b | None |
| [7:1] | 7 | CRC | CRC | --- | --- |
| [0] | 1 | Not used, always '1' | --- | 1 b | --- |

(*1) Support command class 0,2,4,5,6,7,8,10, including: Basic, Block read/write, Erase, Write protection, Application command, Lock card and switch function. Not support 1,3, including: Stream read/write.

(*2) The value will be changed by different flash memory.

(*3) The field name in parenthesis is set to fixed value and indicates that the host is not necessary to refer these fields. The fixed values enable host, which refers to these fields, to keep compatibility to CSD Version 1.0.

## Table 12: InnoDisk Industrial micro SD Card CSD Table for Standard Capacity

| CSD bit | Width | Name | Field | Value | Note |
|---|---|---|---|---|---|
| [127:126] | 2 | CSD Structure | CSD_STRUCTURE | 00 b | v1.0-v1.1 <br> v2.0 (<= 2GB) |
| [125:120] | 6 | Reserved | --- | --- | --- |
| [119:112] | 8 | Data read access time 1 | TAAC | 7F h | 80ms |
| [111:104] | 8 | Data read access time 2 | NSAC | FF h | 25.5K clocks |
| [103:96] | 8 | Max. data transfer rate | TRAN_SPEED | 32 h | 25MHz |
| [95:84] | 12 | Card command classes | CCC | 5F5h | (*1) |
| [83:80] | 4 | Max. read data block length | READ_BL_LEN | 9 h | 512bytes |
| [79] | 1 | Partial block read allowed | READ_BL_PARTIAL | 1 b | Supported |
| [78] | 1 | Write block misalignment | WRITE_BLK_MISALIGN | 1 b | Supported |
| [77] | 1 | Read block misalignment | READ_BLK_MISALIGN | 1 b | Supported |
| [76] | 1 | DSR implemented | DSR_IMP | 0 b | Not supported |
| [75:74] | 2 | Reserved | --- | --- | --- |
| [73:62] | 12 | Device size | C_SIZE | (*2) | (*2) |
| [61:59] | 3 | Max. R_curr @ V$_{DD}$ min | VDD_R_CURR_MIN | 101 b | 35mA |
| [58:56] | 3 | Max R_curr @ V$_{DD}$ max | VDD_R_CURR_MAX | 101 b | 45mA |
| [55:53] | 3 | Max. W_curr @ V$_{DD}$ min | VDD_W_CURR_MIN | 101 b | 35mA |
| [52:50] | 3 | Max W_curr @ V$_{DD}$ max | VDD_W_CURR_MAX | 101 b | 45mA |
| [49:47] | 3 | Device size multiplier | C_SIZE_MULT | (*2) | (*2) |
| [46] | 1 | Erase single block enable | ERASE_BLK_EN | 0 b | Not Allowed |
| [45:39] | 7 | Erase sector size | SECTOR_SIZE | (*3) | (*3) |
| [38:32] | 7 | Write protect group size | WP_GRP_SIZE | (*4) | (*4) |
| [31] | 1 | Write protect group enable | WP_GRP_ENABLE | 1 b | Supported |
| [30:29] | 2 | Reserved | --- | --- | --- |
| [28:26] | 3 | Write speed factor | R2W_FACTOR | 101 b | 32X |
| [25:22] | 4 | Max. write data block length | WRITE_BL_LEN | 9 h | 512bytes |
| [21] | 1 | Partial block write allowed | WRITE_BL_PARTIAL | 1 b | Supported |
| [20:16] | 5 | Reserved | --- | --- | --- |
| [15] | 1 | File format group | FILE_FORMAT_GRP | 0 b | HD like FAT |
| [14] | 1 | Copy flag | COPY | 0 b | Not copied |
| [13] | 1 | Permanent write protection | PERM_WRITE_PROTE CT | 0 b | Not protected |
| [12] | 1 | Temporary write protection | TMP_WRITE_PROTEC T | 0 b | Not protected |
| [11:10] | 2 | File format | FILE_FORMAT | 00 b | HD like FAT |

| [9:8] | 2 | ECC code | ECC | 00 b | None |
|---|---|---|---|---|---|
| [7:1] | 7 | CRC | CRC | --- | --- |
| [0] | 1 | Not used, always '1' | --- | 1 b | --- |

(*1) Support command class 0,2,4,5,6,7,8,10, including: Basic, Block read/write, Erase, Write protection, Application command, Lock card and switch function. Not support 1,3, including: Stream read/write.

(*2)~(*4) The value will be changed by different flash memory.

### 5.5. micro SD card Configuration Register (SCR)

The CSD register is another configuration register in SD card. SCR provides on SD card's special features that were configured into the given card. The size of SCR is 64 bit. SCR is a read only register.

**Table 13: InnoDisk Industrial micro SD Card SCR Table**

| SCR bit | Width | Name | Field | Value | Note |
|---|---|---|---|---|---|
| [63:60] | 4 | SCR structure | SCR_STRUCTURE | 0000 b | v1.0-v2.0 |
| [59:56] | 4 | SD Card spec. version | SD_SPEC | 0010 b | v2.0 |
| [55] | 1 | Data status after erase | DATA_STAT_AFTER_ ERASE | 0 b | Zero after erase |
| [54:52] | 3 | SD security support | SD_SECURITY | 011 b | Secure-Protocol 2.0 |
| [51:48] | 4 | DAT bus width support | SD_BUS_WIDTH | 0101 b | Support 1 / 4 bits |
| [47:32] | 16 | Reserved | --- | --- | --- |
| [31:0] | 32 | Reserved | --- | --- | --- |

## 6.  Commands

The following table describe in detail all micro SD Memory Card bus commands.

**Table 14: micro SD Bus Mode Command Table**

| CMD Index | Abbreviation | Description |
|---|---|---|
| CMD0 | GO_IDLE_STATE | Resets all cards to idle state |
| CMD1 | Reserved | |
| CMD2 | ALL_SEND_CID | Asks any card to send the CID numbers on the CMD line (any card that is connected to the host will respond) |
| CMD3 | SEND_RELATIVE_ ADDR | Ask the card to publish a new relative address (RCA) |
| CMD4 | SET_DSR | Programs the DSR of all cards |
| CMD5 | Reserved for I/O cards | |

| CMD6 | Reserved | |
|---|---|---|
| CMD7 | SELECT/DESELECT_CARD | Command toggles a card between the stand-by and transfer states or between the programming and disconnect states. In both cases the card is selected by its own relative address and gets deselected by any other address; address 0 deselects all. In the case that the RCA equals 0, then the host may do one of the following:<br>- use other RCA number to perform card de-selection.<br>- re-send CMD3 to change its RCA number to other than 0 and then use CMD7 with RCA-0 for card de-selection |
| CMD8 | SEND_IF_COND | Send SD Memory Card interface condition, which includes host supply voltage information and asks the card whether card supports voltage. Reserved bits shall be set to '0' |
| CMD9 | SEND_CSD | Addressed card sends its card-specific data (CSD) on the CMD line. |
| CMD10 | SEND_CID | Addressed card sends its card identification (CID) on CMD the line. |
| CMD11 | VOLTAGE_SWITCH | Switch to 1.8V bus signaling level. |
| CMD12 | STOP_ TRANSMISSION | Forces the card to stop transmission |
| CMD13 | SEND_STATUS | Addressed card sends its status register. |
| CMD14 | Reserved | |
| CMD15 | GO_INACTIVE_ STATE | Sends an addressed card into the Inactive State. This command is used when the host explicitly wants to deactivate a card. Reserved bits shall be set to '0'. |
| CMD16 | SET_BLOCKLEN | In the case of a Standard Capacity SD Memory Card, this command sets the block length (in bytes) for all following block commands (read, write, lock). Default block length is fixed to 512 Bytes. Set length is valid for memory access commands only if partial block read operation are allowed in CSD. In the case of SDHC and SDXC Cards, block length set by CMD16 command doesn't affect memory read and write commands. Always 512 Bytes fixed block length is used. This command is effective for LOCK_UNLOCK command.In both cases, if block length is set larger than 512 Bytes, the card sets the BLOCK_LEN_ERROR bit.In DDR50 mode, data is |

| | | sampled on both edges of the clock. Therefore, block length shall always be even. |
|---|---|---|
| CMD17 | READ_SINGLE_ BLOCK | In the case of a Standard Capacity SD Memory Card, this command reads a block of the size selected by the SET_BLOCKLEN command. In caes of SDHC and SDXC Cards, block length is fixed 512 Bytes regardless of the SET_BLOCKLEN command. |
| CMD18 | READ_MULTIPLE_ BLOCK | Continuously transfers data blocks from card to host until interrupted by a STOP_TRANSMISSION command. Block length is fixed 512 Bytes regardless of the SET_BLOCKLEN command. |
| CMD19 | SEND_TUNING_BLOCK | 64 bytes tuning pattern is sent for SDR50 and SDR104. |
| CMD20 | SPEED_CLASS_CONTROL | Speed Class control command. |
| CMD21-22 | Reserved | |
| CMD23 | SET_BLOCK_COUNT | Specify block count for CMD18 and CMD25. |
| CMD24 | WRITE_BLOCK | In case of SDSC Card, block length is set by the SET_BLOCKLEN command. In case of SDHC and SDXC Cards, block length is fixed 512 Bytes regardless of the SET_BLOCKLEN command. |
| CMD25 | WRITE_MULTIPL E_BLOCK | Continuously writes blocks of data until a STOP_TRANSMISSION follows. Block length is specified the same as WRITE_BLOCK command. |
| CMD26 | Reserved For Manufacturer | |
| CMD27 | PROGRAM_CSD | Programming of the programmable bits of the CSD. |

| CMD28 | SET_WRITE_PROT | If the card has write protection features, this command sets the write protection bit of the addressed group. The properties of write protection are coded in the card specific data (WP_GRP_SIZE).SDHC and SDXC Cards do not support this command. |
|---|---|---|
| CMD29 | CLR_WRITE_PROT | If the card provides write protection features, this command clears the write protection bit of the addressed group.<br>SDHC and SDXC Cards do not support this command. |
| CMD30 | SEND_WRITE_ PROT | If the card provides write protection features, this command asks the card to send the status of the write protection bits.<br>SDHC and SDXC Cards do not support this command. |
| CMD31 | Reserved | |
| CMD32 | ERASE_WR_BLK_START | Sets the address of the first sector to be erased. |
| CMD33 | ERASE_WR_BLK_END | Sets the address of the last sector of the continuous range to be erased. |
| CMD34-37 | Reserved | |
| CMD38 | ERASE | Erases all previously selected write blocks. |
| CMD39 | Reserved | |
| CMD40 | Reserved for Secutiry Specification | |
| CMD41 | Reserved | |
| CMD42 | LOCK_UNLOCK | Used to set/reset the password or lock/unlock the card. The size of the data block is set by the SET_BLOCK_LEN command.<br>Reserved bits in the argument and in Lock Card Data Structure shall be set to 0. |
| CMD43-51 | Reserved | |
| CMD52-54 | Commands for SDIO | |
| CMD55 | APP_CMD | Indicates to the card that the next command is an application specific command rather than a standard command. |

| CMD56 | GEN_CMD | Used either to transfer a data block to the card or to get a data block from the card for general purpose / application specific commands. In case of a SDSC Card, block length is set by the SET_BLOCK_LEN command. In case of SDHC and SDXC Cards, block length is fixed to 512 Bytes. The host sets RD/WR=1 for reading data from the card and sets to 0 for writing data to the card. |
|---|---|---|
| CMD57-59 | Reserved | |
| CMD60-63 | Reserved For Manufacturer | |
| **Application-specific Commands** | | |
| **ACMD Index** | **Abbreviation** | **Description** |
| ACMD1-5 | Reserved | |
| ACMD6 | SET_BUS_WIDTH | Defines the data bus width ('00'-1bit or '10'=4 bits bus_ to be used for data transfer. The allowed data bus widths are given in SCR register. |
| ACMD7-12 | Reserved | |
| ACMD13 | SD_STATUS | Send the SD Status. |
| ACMD14-16 | Reserved for Security Specification | |
| ACMD17 | Reserved | |
| ACMD18 | Reserved for SD security applications | |
| ACMD19-21 | Reserved | |
| ACMD22 | SEND_NUM_WR_BLOCKS | Send the number of the written (without error) write blocks. Responds with 32bit+CRC data block. If WRITE_BL_PARTIAL='0', the unit of ACMD22 is always 512 byte. If WRITE_BL_PARTIAL='1', the unit of ACMD22 is a block length which was used when the write command was executed. |
| ACMD23 | SET_WR_BLK_ERASE_COUNT | Set the number of write blocks to be pre-erased before writing (to be used for faster Multiple Block WR command). "1"=default (one wr block). |
| ACMD24 | Reserved | |
| ACMD25-28 | Reserved for SD security applications | |
| ACMD29 | Reserved | |
| ACMD30-35 | Reserved for Security Specification | |
| ACMD36-37 | Reserved | |
| ACMD38 | Reserved for SD security applications | |
| ACMD39-40 | Reserved | |

| | | |
|---|---|---|
| ACMD41 | SD_SEND_OP_COND | Sends host capacity support information (HCS) and asks the accessed card to send its operating confition register (OCR) content in the response on the CMD line. HCS is effective when card receives SEND_IF_COND command.<br>Sends request to switch to 1.8V signaling (S18R). Reserved bit shall be set to '0'. CCS bit is assigned to OCR[30].<br>XPC controls the maximum current in the default speed mode of SDXC card. XPC=0 means 100mA (max.) but speed class is not supported. XPC=1 means 150mA (max.) and speed class is supported. |
| ACMD42 | SET_CLR_CARD_DETECT | Connect[1]/Disconnect[0] the 50 Kohm pull-up resistor on CD/DAT3 (pin 1) of the card. |
| ACMD43-49 | Reserved for SD security applications | |
| ACMD50 | Reserved | |
| ACMD51 | SEND_SCR | Reads the SD Configuration Register (SCR). |
| ACMD52-54 | Reserved for Security Specification | |
| ACMD55 | Not exist | Equivalent to CMD55. |
| ACMD56-59 | Reserved for Security Specification | |

## 7.  i-S.M.A.R.T Utility

The health of Industrial Nano USB can be monitored by a specific i-S.M.A.R.T utility as below:
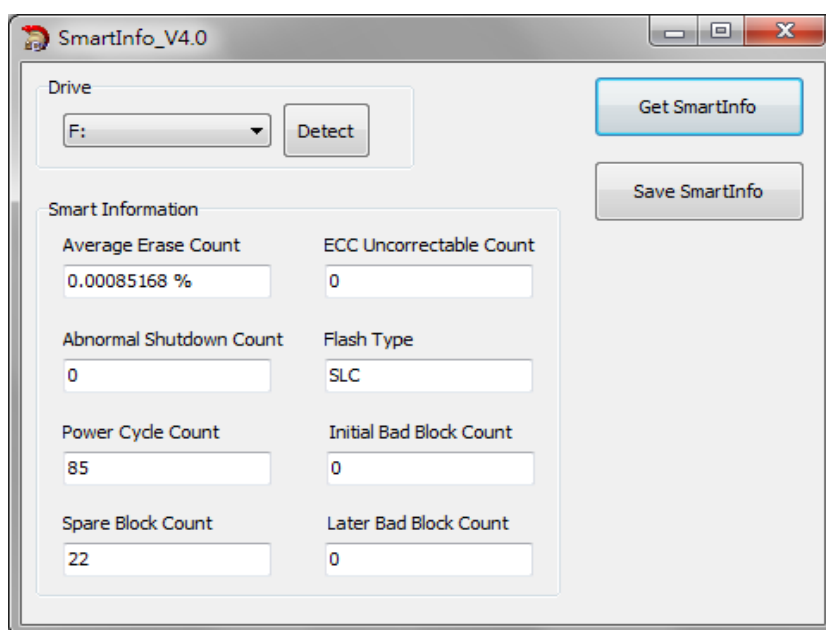


**Figure 6: User Interface of i-S.M.A.R.T Utility**

Detailed Description for SMART Information:

- **Average Erase Count**

    Value: To record average erase ratio. This value is calculated by "total

    erase counts", "Flash P/E cycles", "Flash total blocks".

    Initial value = 00.00%

    Maximum value = 100.00%

- **Abnormal Shutdown Count**

    Value: To record abnormal shutdown condition. Increasing this value by 1

    when detected error in the power on stage.

    Initial value = 0.

    Maximum value = 4294967295.

- **Power Cycle Count**

    Value: To record power cycle condition. Increasing this value by 1 when a

    power cycle (both normal and abnormal) occurred.

    Initial value = 0.

    Maximum value = 4294967295.

- **Spare Block Count**

    Value: To record spare block counts. Decreasing this variable when

    detected run-time bad blocks. (note: run-time bad blocks may be

    "erase error", "program error", "read error".)

    Initial value = depends on Flash.

    Maximum value = 255.

    Minimum value = 0.

- **ECC Uncorrectable Count**

    Value: To record ECC uncorrectable block counts. Increase this value by 1

    when fetal error occurred in Flash read operation.

Initial value = 0.

Maximum value = 255.

- **Flash Type**

    Value: To determinate mounted Flash type, and always keep in original

    value.

    0: SLC, 1: MLC.

    Initial value = depends on Flash.

- **Initial Bad Block Count**

    Value: To record initial bad blocks when MP process, and always keep in

    original value.

    Initial value = depends on Flash.

    Maximum value = 65535.

- **Later Bad Block Count**

    Value: To record run time bad blocks. Increasing this variable when

    detected run-time bad blocks.

    Initial value = 0.

    Maximum value = 65535.

## 8. Part Number Rule

| CODE | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | D | S | 2 | M | - | 0 | 4 | G | I | 8 | 1 | A | C | 1 | S | T | | | | |
| Description | Disk | micro SD card | | | - | Capacity | | | Category | | | FW | Operation Temp. | Internal Control | CH. | Flash | - | Customized Code | | |
| **Definition** | | | | | | | | | | | | | | | | | | | | |

| Code 1st (Disk) | Code 12th (Firmware version) |
|---|---|
| D : Disk | A: Standard F/W version |

| Code 2nd ~ 4th (Form Factor) | Code 13th (Operation Temperature) |
|---|---|
| S2M: micro SD card | C: Standard Grade (0℃ ~ +70℃) |

| Code 6th ~8th (Capacity) | W: Industrial Grade ( -40℃ ~ +85℃) |
|---|---|
| 01G: 1GB | Code 14th (Internal control) |
| 02G: 2GB | Code 15th (Channel of data transfer) |
| 04G: 4GB | S: Single Channel |
| 08G: 8GB | Code 16th (Flash Type) |
| Code 9th ~11th (Category) | B: Toshiba (1GB) |
| I81: SD series | T: Micron (2GB, 4GB, 8GB) |