Getting Started Guide



Version 1.0

Xilinx[®] Kintex[™]-7 FPGA DSP Development Kit with High-Speed Analog



Revision History

DATE	VERSION	REVISION
02/06/2012	1.0	Initial Release

AVNET DESIGN KIT TECHNICAL SUPPORT FILES AND DOWNLOADS WEB ACCESS INSTRUCTIONS

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On your first visit to the DRC, You will be required to site register before you can download the documents. To get started, select the name of the manufacturer associated with your design kit from the drop down menu. A complete listing of avail¬able design kits will appear. Select the kit you purchased. Scroll to the bottom of the design kit page to access the support files. Before you download a file, you will be prompted to login. If you are an existing user, please login. If you are a new user, click on the "Need to sign-up?" text. Please complete the short registration form. Upon completion, be sure to retain your login and password information for future visits to Avnet's DRC. Logging in once, gives you unlimited access to all technical support files and downloads. You will also have the chance to request e-mail notifications whenever there are updates to your design kit.

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ABOUT THIS GUIDE

This guide provides detailed information for getting started with the Xilinx Kintex-7 FPGA DSP Development Kit with High-Speed Analog. If the ISE® Design Suite: System Edition has already been installed and the steps in the Hardware Setup Guide have been completed, then proceed to the "Next Steps" section of this document to learn more about additional tutorials available for this kit. Otherwise, follow the steps outlined below to install and enable the required software for this kit.

Additional Documentation

The following documents are available for download at: http://www.xilinx.com/products/silicon-devices/fpga/kintex-7/index.htm http://www.xilinx.com/support/documentation/7_series.htm

- 7 Series FPGAs Overview: This overview outlines the features of 7 Series FPGAs, along with product selection parameters.
- Kintex-7 FPGA Data Sheet: DC and Switching Characteristics: This data sheet contains the DC and switching characteristic specifications for Kintex-7 FPGAs.
- 7-Series FPGAs Packaging and Pinout Specifications: This specification includes the tables for device/package combinations and maximum I/Os, pin definitions, pinout tables, pinout diagrams, mechanical drawings, and thermal specifications.
- 7 Series FPGAs Configuration User Guide: This all-encompassing configuration guide includes chapters on configuration interfaces (serial and parallel), multi-bitstream management, bitstream encryption, boundary-scan and JTAG configuration, and reconfiguration techniques for Xilinx 7 Series FPGAs.
- 7 Series FPGAs SelectIO Resources User Guide: This guide describes the SelectIO[™] resources available in 7 Series FPGAs.
- 7 Series FPGAs Clocking Resources User Guide: This guide describes the clocking resources available in 7 Series FPGAs.
- 7 Series FPGAs Memory Resources User Guide: This guide describes the block RAM and FIFO capabilities of 7 Series FPGAs.
- 7 Series FPGAs GTX Transceivers User Guide: This guide describes the GTP transceivers available in 7 Series FPGAs.
- 7 Series FPGAs FPGA DSP48E1 Slice User Guide: This guide describes the DSP48E1 slice in 7 Series FPGAs and provides configuration examples.
- 7 Series FPGAs FPGA PCB and Pin Planning Guide: This guide provides information on the PCB design for 7 Series FPGAs, with a focus on strategies for making design decisions at the PCB interface level.
- System Generator Users Guide: This guide provides information using System Generator with Simulink[®] to create DSP designs targeted to Xilinx FPGAs.

Additional Support Resources

To search the database of silicon and software questions and answers or to create a technical support case in WebCase, see the Xilinx website at: http://www.xilinx.com/support.

INTRODUCTION

The Xilinx Kintex-7 FPGA DSP Development Kit with High-Speed Analog, designed by Avnet, combines the key components of the Xilinx DSP Design Platform for developing FPGA-based high-speed data acquisition in a wide range of applications, including wireless communications, aerospace and defense, medical and instrumentation. For algorithm developers, a familiar digital signal processing design flow is provided based on Simulink[®] and MATLAB[®] from Mathworks for FPGA hardware development without the need to learn RTL. Traditional RTL design methodologies are also supported through reference designs that use ISE[®] Design Suite: Logic Edition and LogicCORE DSP IP.

The Xilinx Kintex-7 FPGA DSP Development Kit with High-Speed Analog includes the 4DSP FMC150 module. This card provides two 14-bit A/D channels and two 16-bit D/A channels, which can be clocked by an on-board VCXO-based clock generator (optionally locked to an external reference) or an externally supplied sample clock. In addition, there is one trigger input for customized sampling control. The FMC150 daughter card is mechanically and electrically compliant with the FMC standard (ANSI/VITA 57.1).

This Getting Started Guide will walk you through the steps to setup the KC705 Kintex-7 development board and the FMC150 daughter card and to run the out-of-box DSP demonstration. The demonstration illustrates the hardware flexibility of FPGAs for high-performance digital signal processing through parallelized hardware on a single device. If you have not already installed the Xilinx ISE® software, you will be directed through the steps to install the software, get updates and generate a license. If you plan to use or evaluate the Simulink-based design flow and do not already have Mathworks, products installed you, will be guided to the Mathworks website. Finally, this guide will provide hardware design tutorials for both Simulink and RTL design flows.

Kintex-7 FPGA DSP Development Kit Contents: What's Inside the Box

- KC705 Board with the XC7K325T-2FFG900 FPGA along with:
 - Power Supply
 - One USB Type-A to Micro 5-pin Cable
 - One USB Type-A to Mini 5-pin Cable
 - Ethernet Cable
 - Two MMCX RF Coax Cables
- 4DSP FMC150 DAC/ADC Daughter Card with the following:
 - TI DAC3283, Dual-Channel 800 MSPS, 16-bit DAC
 - TI ADS62P49 Dual-Channel, 250 MSPS, 14-bit ADC
 - TI CDCE72010 Clock Distribution Device
- Xilinx ISE Design Suite DVD which includes:
 - ISE Project Navigator with ISIM HDL Simulator
 - PlanAhead Design and Analysis Tool
 - Embedded Development Kit (EDK)
 - Xilinx Platform Studio (XPS)
 - Software Development Kit (SDK)
 - ChipScope[™] Pro
 - System Generator for DSP®

- ISE Design Suite System Edition License Voucher (device-locked for the Kintex-7 325T FPGA)
- Documentation
 - Getting Started with the Xilinx Kintex-7 FPGA DSP Development Kit with High-Speed Analog
- Reference Designs
 - Getting Started Reference Design
 - System Generator Design Tutorial
 - RTL Design Tutorial

What's Available Online

- License for ISE Design Suite: System Edition
 - http://www.xilinx.com/getproduct
 - http://www.xilinx.com/tools/faq.htm
- Technical Support
 - http://www.xilinx.com/support
- Development Kit home page with Documentation and Reference Designs
 - http://www.xilinx.com/k7dspkit
 - http://www.em.avnet.com/k7dspkit

If you already have the ISE Design Suite installed on your computer, then you can proceed to the the next section, "GETTING STARTED WITH KINTEX-7 FPGA DSP DEVELOPMENT." If you need to install ISE Design Suite, then go to the "INSTALLATION AND LICENSING OF ISE DESIGN SUITE" section of this document.

GETTING STARTED WITH KINTEX-7 FPGA DSP DEVELOPMENT

This Kintex-7 FPGA DSP Development Kit with High-Speed Analog comes with a DSP 'Getting Started' demonstration, which is included in the Web download documentation package. You can run this demo after installing ISE Design Suite to get an overview of the features of the KC705 board using the RTL-based digital up converter (DUC) / digital down converter (DDC) reference design.

The DSP Reference Design Demonstration

The provided DSP demo uses a pre-built Kintex-7 FPGA design (shown in the figure below) with the following features:

- Fast IO interfaces to the DAC and ADC
- · ADC auto-calibration at reset time for robust data capture at high sampling rates
- · Modular DUC/DDC backend for sample rate conversion; can be easily replaced by user's design
- Parameterizable DSP IP to reduce development time and exploit device hardware resources such as the DSP48E1 slice
- · Support for isolation of the digital and analog components of the design to assist with debug
- · ChipScope Pro to view results without external test equipment



Figure 1: Kintex-7 Reference Design Simplified Block Diagram

DSP Demo Hardware Requirements

All hardware required to run the DSP demonstrations and tutorials is provided with the Kintex-7 FPGA DSP Development Kit.

DSP Demo Setup Instructions

- Connect DAC Output C to ADC Input A through an MMCX-to-MMCX cable on the FMC150 daughter card. Make sure you use enough force to make a solid connection. You should hear a click.
- Connect DAC Output D to ADC Input B through an MMCX-to-MMCX cable on the FMC150 daughter card. Make sure you use enough force to make a solid connection. You should hear a click.



Figure 2

- 3. Connect the FMC150 to the LPC FMC connector J2 on the KC705.
- 4. Setup the GPIO DIP switches on SW11 on the KC705 to select a DEMO mode (all OFF).
- 5. Connect the micro USB cable to the JTAG port as shown in Figure 2.
- 6. Attach the 12V wall power supply to J49.
- 7. Power up the board by turning SW15 ON.



Figure 3

Download the Kintex-7 FPGA DSP Development Kit Reference Design

- 8. Go to the Avnet Kintex-7 FPGA DSP Development Kit Web page: http://www.em.avnet.com/k7dspkit.
- 9. At the bottom of this web page, click on the link "Support Files and Downloads."
- To download the Getting Started Design files, click on the link "Kintex7 DSP Kit Getting Started Reference Design." This will download the file, "kintex7dsp_getting_started_reference_design.zip" to your computer.
- 11. To install the getting started design files, unzip this file using the "Extract to Here" option and then extract the files to the root C: drive of your computer. The top-level folder name should be "kintex7dsp_ getting_started_reference_design." If this is not the name of the folder, then rename it. There are hard paths in the design files that require this exact naming convention.



Getting Started with the Kintex-7 FPGA DSP Development Kit Demo

In this demo, the RTL version of the DUC / DDC design will be downloaded to the KC705 board. This design includes Xilinx ChipScope probes to capture the output data from the hardware and then send it back to the ChipScope analyzer software to be displayed. ChipScope can display the data as a signed integer, which allows the DUC / DDC output to be viewed in analog format.

1. Launch the Xilinx ChipScope Pro Analyzer from either Lab Tools or a Design Suite install of the ISE software.

To launch ChipScope Pro from Lab Tools, use the start menu command "Xilinx ISE Design Suite -> Lab Tools -> ChipScope Pro Analyzer." Note that this is version dependent.





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To launch ChipScope Pro from the ISE Design Suite, use the start menu command "Xilinx ISE Design Suite -> ChipScope Pro -> Analyzer." Note that this will be version dependent.



 Initialize the JTAG chain by clicking on the toolbar command "Open Cable / Search JTAG Chain" in ChipScope.



Figure 6: Initialize the JTAG Chain

3a. From the ChipScope Project window, select "DEV:0 MyDevice0 (XC7K325T) and right-click to execute the pop-up command "Configure." Click OK on the window that opens.

Elle View JTAG Chain (Device Window Help
New Project JTAG Chain P DEV:0 MyDevice0 (XC7K - XADC Console	22512 Rename
	Contigure
**	Show [DCODE Show USERCODE Show Configuration Status Show JTAC Instruction Register

Figure 7a: Execute Configure Pop-Up Command

3b. Once the dialog box appears, verify the target bitfile is 'kc705_fmc150.bit,' with the pathname shown in Figure 7b. Click OK to start configuration.

	figuration
File:	kc705_fmc150.bit
Directory:	$C'\@intex7dsp_getting_started_reference_design/\@RTLiReference_Design\@integlementation\@integlement$
Partia	Reconfiguration Bitstream
Clean	previous project setting
	Select New File
	Construct a rest
Innont	Design-level CDC File
	his operation cannot be undone.
Design-le	vel CDC File
Auto-	reate Buses
File:	
Directory:	C:trantex?dsp_ml_reterence_design_tutoria7/RTUDesign_Tutoria7/imptementation/V/IDL30E

Figure 7b: Start Configuration

4. Load ChipScope project 'kc705_fmc150.cpj' from menu File -> Open Project



Figure 8

5. Under 'Unit 1,' start ADC data capture by clicking the black triangle icon beneath the Trigger Setup menu. The I/Q output of the DDC is captured and displayed. A second ILA unit captures signals at the DUC outputs driving the DACs. Refer to the block diagram in Figure 1. If you wish to capture signals at the DUC outputs, select Unit 2 and repeat the process. Refer to Figure 1 for the location of ILA units within the signal flow.



Figure 9: Apply Settings and Arm Trigger



Figure 10: Correct Bus Plot Waveform

Congratulations!

You have now run the Kintex-7 FPGA DSP Development Kit with High-Speed Analog reference design through the FMC150 daughter card and observed data capture in ChipScope. Using this fully functional DSP design, you may now develop your DSP application on Xilinx Kintex-7 FPGAs.

Tutorials

Kintex-7 FPGA DSP Development Kit RTL Tutorial

The following additional tutorials for the Kintex-7 FPGA DSP Development Kit are available from the Avnet website for download.

- Useful design techniques for implementing DSP algorithms onto Xilinx FPGAs using RTL design methodologies
- · How to use ISim to analyze the design and compare the response to golden vectors from MATLAB
- · How to use ChipScope to verify the hardware using an impulse input
- Drive the D/A and A/D on the FMC150 in loopback mode

Kintex-7 FPGA DSP Development Kit System Generator Tutorial

- Generate input test data from MATLAB/Simulink and use that data to drive the FMC150 D/A analog interface
- · Bring analog data from the FMC150 daughter card into the MATLAB/Simulink environment for analysis
- · Modify data converter configuration registers from Simulink to tune overall system performance
- · Use digital filtering and Xilinx IP to improve signal to noise ratios and remove aliasing

Getting Help and Support

For questions regarding products within a Product Entitlement Account, send an e-mail message to the regional customer services representative.

- Canada, USA and South America isscs_cases@xilinx.com
- Europe, Middle East, and Africa eucases@xilinx.com
- Asia Pacific including Japan apaccase@xilinx.com

For technical support, including the installation and use of a product license file, contact Xilinx Online Technical Support at http://www.support.xilinx.com. This site also provides the following support resources:

- · Software, IP and documentation updates
- · Access to technical support Web tools
- Searchable answer database with over 4,000 solutions
- User forums
- · Training Select instructor-led classes and recorded e-learning options

Contact Avnet Support for any questions regarding the Kintex-7 FPGA DSP Development Kit reference designs or kit hardware. http://www.em.avnet.com/kintex7dspkit

INSTALLATION AND LICENSING OF LAB TOOLS

This Kintex-7 FPGA DSP Development Kit comes with entitlement to a full seat of the ISE Design Suite: System Edition that is device locked to a Kintex-7 XC7K325T-2FFG900 FPGA. This software can be installed from the DVD or the Web installer can be downloaded at:

http://www.xilinx.com/support/download/index.htm.

Lab Tools Software Installation

Note: If you have the ISE Design Suite Software on your computer, this step can be skipped and the ChipScope Pro from that installation may be used.

- 1. Run the ISE Design Suite Installer:
 - a. Option 1: Insert the ISE Design Suite DVD included in this kit into the computer
 - If the Installer does not start automatically, run the "xsetup" executable from the DVD
 - b. Option 2: Run the Web Installer that can be downloaded from http://www.xilinx.com/support/download/index.htm

A screen will appear with a welcome dialog, two license agreement dialogs and an opportunity to select the location for the software installation.

Note: Lab Tools software does not require a license file so that step can be skipped.



Figure 11: ISE Install Welcome Screen







Figure 13: ISE Third-Party Usage License Agreement







Figure 15: Select Installation Options



Figure 16: Select Destination Directory and Program Folder



Figure 17: Installation Summary



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