

# DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

## **HEF4023B**

### **gates**

### **Triple 3-input NAND gate**

Product specification  
File under Integrated Circuits, IC04

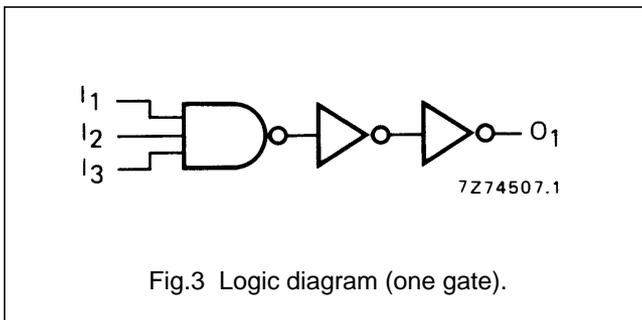
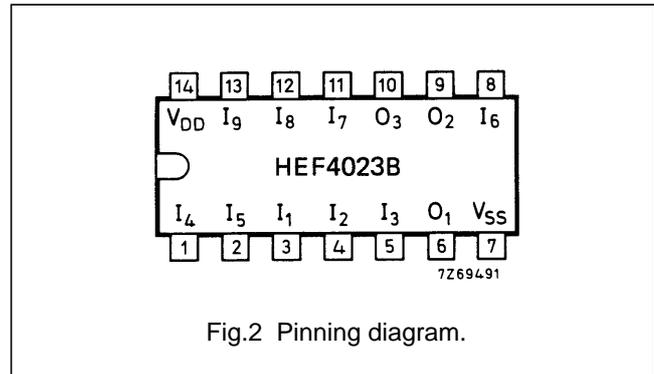
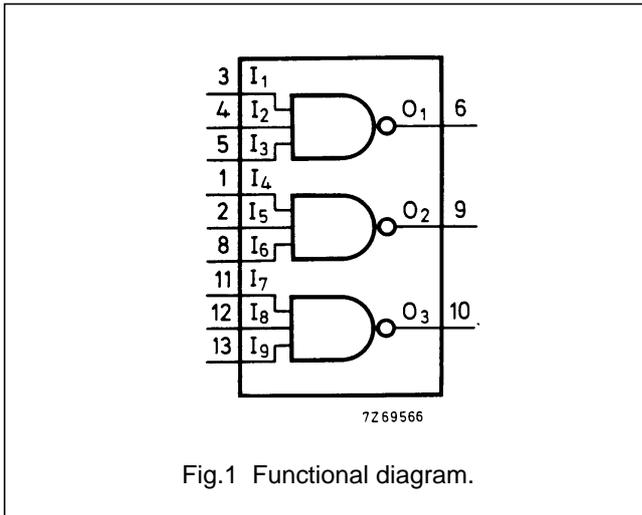
January 1995

**Triple 3-input NAND gate**

**HEF4023B  
gates**

**DESCRIPTION**

The HEF4023B provides the positive triple 3-input NAND function. The outputs are fully buffered for highest noise immunity and pattern insensitivity of output impedance.



- HEF4023BP(N): 14-lead DIL; plastic (SOT27-1)
- HEF4023BD(F): 14-lead DIL; ceramic (cerdip) (SOT73)
- HEF4023BT(D): 14-lead SO; plastic (SOT108-1)
- ( ): Package Designator North America

**FAMILY DATA, I<sub>DD</sub> LIMITS category GATES**

See Family Specifications

## Triple 3-input NAND gate

HEF4023B  
gates**AC CHARACTERISTICS** $V_{SS} = 0$  V;  $T_{amb} = 25$  °C;  $C_L = 50$  pF; input transition times  $\leq 20$  ns

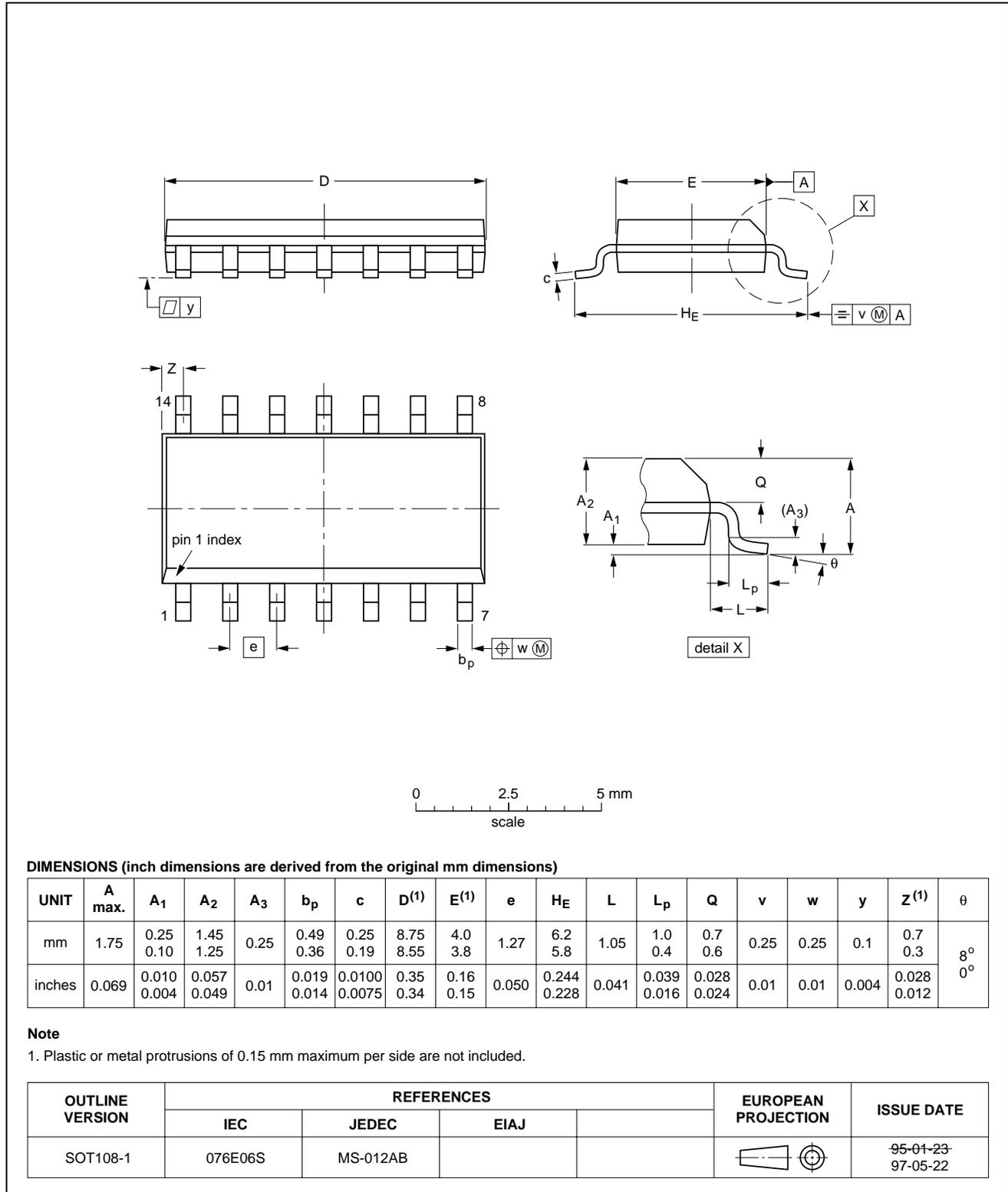
	$V_{DD}$ V	SYMBOL	TYP.	MAX.		TYPICAL EXTRAPOLATION FORMULA
Propagation delays $I_n \rightarrow O_n$	5 10 15	$t_{PHL}$	65	135	ns	$38 \text{ ns} + (0,55 \text{ ns/pF}) C_L$
			25	50	ns	$14 \text{ ns} + (0,23 \text{ ns/pF}) C_L$
			15	30	ns	$7 \text{ ns} + (0,16 \text{ ns/pF}) C_L$
	5 10 15	$t_{PLH}$	65	130	ns	$38 \text{ ns} + (0,55 \text{ ns/pF}) C_L$
			30	60	ns	$19 \text{ ns} + (0,23 \text{ ns/pF}) C_L$
			25	45	ns	$17 \text{ ns} + (0,16 \text{ ns/pF}) C_L$
Output transition times	5 10 15	$t_{THL}$	60	120	ns	$10 \text{ ns} + (1,0 \text{ ns/pF}) C_L$
			30	60	ns	$9 \text{ ns} + (0,42 \text{ ns/pF}) C_L$
			20	40	ns	$6 \text{ ns} + (0,28 \text{ ns/pF}) C_L$
	5 10 15	$t_{TLH}$	60	120	ns	$10 \text{ ns} + (1,0 \text{ ns/pF}) C_L$
			30	60	ns	$9 \text{ ns} + (0,42 \text{ ns/pF}) C_L$
			20	40	ns	$6 \text{ ns} + (0,28 \text{ ns/pF}) C_L$

	$V_{DD}$ V	TYPICAL FORMULA FOR P ( $\mu$ W)	
Dynamic power dissipation per package (P)	5	$1200 f_i + \sum (f_o C_L) \times V_{DD}^2$	where $f_i$ = input freq. (MHz) $f_o$ = output freq. (MHz) $C_L$ = load capacitance (pF) $\sum (f_o C_L)$ = sum of outputs $V_{DD}$ = supply voltage (V)
	10	$5500 f_i + \sum (f_o C_L) \times V_{DD}^2$	
	15	$16\,400 f_i + \sum (f_o C_L) \times V_{DD}^2$	

SO

SO14: plastic small outline package; 14 leads; body width 3.9 mm

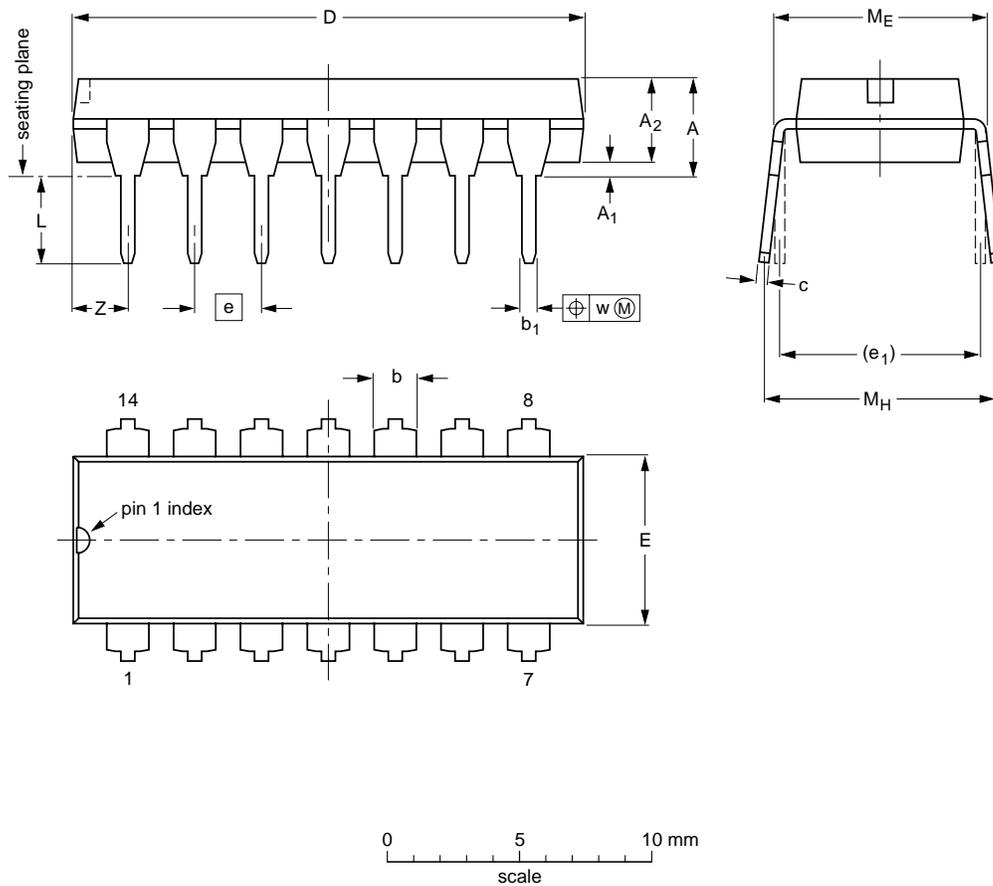
SOT108-1



DIP

DIP14: plastic dual in-line package; 14 leads (300 mil)

SOT27-1



**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

UNIT	A max.	A <sub>1</sub> min.	A <sub>2</sub> max.	b	b <sub>1</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	e <sub>1</sub>	L	M <sub>E</sub>	M <sub>H</sub>	w	Z <sup>(1)</sup> max.
mm	4.2	0.51	3.2	1.73 1.13	0.53 0.38	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.2
inches	0.17	0.020	0.13	0.068 0.044	0.021 0.015	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.087

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT27-1	050G04	MO-001AA			92-11-17 95-03-11