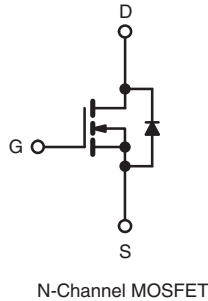
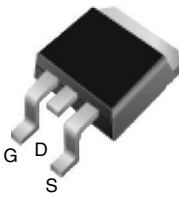


Power MOSFET

| PRODUCT SUMMARY | |
|---------------------------|-----------------------------|
| V_{DS} (V) | 100 |
| $R_{DS(on)}$ (Ω) | $V_{GS} = 10\text{ V}$ 0.16 |
| Q_g (Max.) (nC) | 26 |
| Q_{gs} (nC) | 5.5 |
| Q_{gd} (nC) | 11 |
| Configuration | Single |

D²PAK (TO-263)

FEATURES

- Halogen-free According to IEC 61249-2-21
- Definition
- Surface Mount
- Available in Tape and Reel
- Dynamic dV/dt Rating
- Repetitive Avalanche Rated
- 175 °C Operating Temperature
- Fast Switching
- Ease of Paralleling
- Compliant to RoHS Directive 2002/95/EC



RoHS*
COMPLIANT
HALOGEN
FREE
Available

DESCRIPTION

Third generation Power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The D²PAK (TO-263) is a surface mount power package capable of accommodating die size up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface mount package. The D²PAK (TO-263) is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0 W in a typical surface mount application.

ORDERING INFORMATION

| Package | D ² PAK (TO-263) | D ² PAK (TO-263) | D ² PAK (TO-263) |
|---------------------------------|-----------------------------|------------------------------|------------------------------|
| Lead (Pb)-free and Halogen-free | SiHF530S-GE3 | SiHF530STRL-GE3 ^a | SiHF530STRR-GE3 ^a |
| Lead (Pb)-free | IRF530SPbF | IRF530STRLPbF ^a | IRF530STRRPbF ^a |
| | SiHF530S-E3 | SiHF530STL-E3 ^a | SiHF530STR-E3 ^a |

Note

a. See device orientation.

ABSOLUTE MAXIMUM RATINGS $T_C = 25\text{ }^\circ\text{C}$, unless otherwise noted

| PARAMETER | SYMBOL | LIMIT | UNIT |
|--|------------------|-----------------------------------|---------------------|
| Drain-Source Voltage | V_{DS} | 100 | V |
| Gate-Source Voltage | V_{GS} | ± 20 | |
| Continuous Drain Current | V_{GS} at 10 V | $T_C = 25\text{ }^\circ\text{C}$ | A |
| | | $T_C = 100\text{ }^\circ\text{C}$ | |
| Pulsed Drain Current ^a | I_{DM} | 56 | |
| Linear Derating Factor | | 0.59 | W/ $^\circ\text{C}$ |
| Linear Derating Factor (PCB Mount) ^e | | 0.025 | |
| Single Pulse Avalanche Energy ^b | E_{AS} | 69 | mJ |
| Avalanche Current ^a | I_{AR} | 14 | A |
| Repetitive Avalanche Energy ^a | E_{AR} | 8.8 | mJ |
| Maximum Power Dissipation | P_D | $T_C = 25\text{ }^\circ\text{C}$ | W |
| | | $T_A = 25\text{ }^\circ\text{C}$ | |
| Maximum Power Dissipation (PCB Mount) ^e | | 3.7 | |
| Peak Diode Recovery dV/dt ^c | dV/dt | 5.5 | V/ns |
| Operating Junction and Storage Temperature Range | T_J, T_{stg} | - 55 to + 175 | $^\circ\text{C}$ |
| Soldering Recommendations (Peak Temperature) | for 10 s | 300 ^d | |

Notes

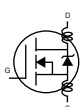

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- $V_{DD} = 25\text{ V}$, starting $T_J = 25\text{ }^\circ\text{C}$, $L = 528\text{ }\mu\text{H}$, $R_g = 25\text{ }\Omega$, $I_{AS} = 14\text{ A}$ (see fig. 12).
- $I_{SD} \leq 14\text{ A}$, $dI/dt \leq 140\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{DS}$, $T_J \leq 175\text{ }^\circ\text{C}$.
- 1.6 mm from case.
- When mounted on 1" square PCB (FR-4 or G-10 material).

* Pb containing terminations are not RoHS compliant, exemptions may apply

| THERMAL RESISTANCE RATINGS | | | | | | |
|--|------------|------|------|------|--|--|
| PARAMETER | SYMBOL | TYP. | MAX. | UNIT | | |
| Maximum Junction-to-Ambient | R_{thJA} | - | 62 | °C/W | | |
| Maximum Junction-to-Ambient (PCB Mount) ^a | R_{thJA} | - | 40 | | | |
| Maximum Junction-to-Case (Drain) | R_{thJC} | - | 1.7 | | | |

Note

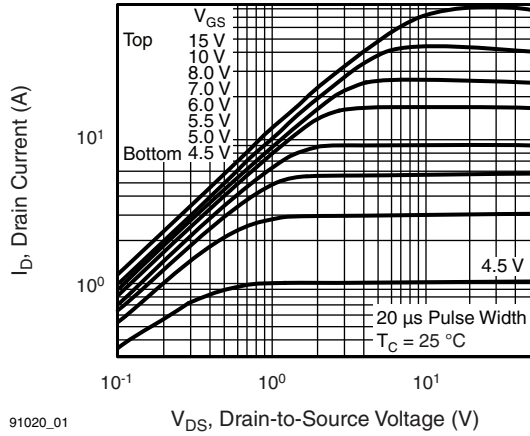
a. When mounted on 1" square PCB (FR-4 or G-10 material).

| SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted | | | | | | | |
|--|---------------------|--|--|------|------|-----------------------------|---------------|
| PARAMETER | SYMBOL | TEST CONDITIONS | | MIN. | TYP. | MAX. UNIT | |
| Static | | | | | | | |
| Drain-Source Breakdown Voltage | V_{DS} | $V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$ | | 100 | - | - V | |
| V_{DS} Temperature Coefficient | $\Delta V_{DS}/T_J$ | Reference to $25\text{ }^\circ\text{C}$, $I_D = 1\text{ mA}$ | | - | 0.12 | - $\text{V}/^\circ\text{C}$ | |
| Gate-Source Threshold Voltage | $V_{GS(th)}$ | $V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$ | | 2.0 | - | 4.0 V | |
| Gate-Source Leakage | I_{GSS} | $V_{GS} = \pm 20\text{ V}$ | | - | - | $\pm 100\text{ nA}$ | |
| Zero Gate Voltage Drain Current | I_{DSS} | $V_{DS} = 100\text{ V}, V_{GS} = 0\text{ V}$ | | - | - | 25 μA | |
| | | $V_{DS} = 80\text{ V}, V_{GS} = 0\text{ V}, T_J = 150\text{ }^\circ\text{C}$ | | - | - | 250 μA | |
| Drain-Source On-State Resistance | $R_{DS(on)}$ | $V_{GS} = 10\text{ V}$ | $I_D = 8.4\text{ A}^b$ | - | - | 0.16 Ω | |
| Forward Transconductance | g_{fs} | $V_{DS} = 50\text{ V}, I_D = 8.4\text{ A}^b$ | | 5.1 | - | - S | |
| Dynamic | | | | | | | |
| Input Capacitance | C_{iss} | $V_{GS} = 0\text{ V}, V_{DS} = 25\text{ V}, f = 1.0\text{ MHz}$, see fig. 5 | | - | 670 | - | pF |
| Output Capacitance | C_{oss} | | | - | 250 | - | |
| Reverse Transfer Capacitance | C_{rss} | | | - | 60 | - | |
| Total Gate Charge | Q_g | $V_{GS} = 10\text{ V}$ | $I_D = 14\text{ A}, V_{DS} = 80\text{ V}$, see fig. 6 and 13 ^b | - | - | 26 | nC |
| Gate-Source Charge | Q_{gs} | | | - | - | 5.5 | |
| Gate-Drain Charge | Q_{gd} | | | - | - | 11 | |
| Turn-On Delay Time | $t_{d(on)}$ | $V_{DD} = 50\text{ V}, I_D = 14\text{ A}, R_g = 12\text{ }\Omega, R_D = 3.6\text{ }\Omega$, see fig. 10 ^b | | - | 10 | - | ns |
| Rise Time | t_r | | | - | 34 | - | |
| Turn-Off Delay Time | $t_{d(off)}$ | | | - | 23 | - | |
| Fall Time | t_f | | | - | 24 | - | |
| Internal Drain Inductance | L_D | Between lead, 6 mm (0.25") from package and center of die contact  | | - | 4.5 | - | nH |
| Internal Source Inductance | L_S | | | - | 7.5 | - | |
| Drain-Source Body Diode Characteristics | | | | | | | |
| Continuous Source-Drain Diode Current | I_S | MOSFET symbol showing the integral reverse p - n junction diode  | | - | - | 14 | A |
| Pulsed Diode Forward Current ^a | I_{SM} | | | - | - | 56 | |
| Body Diode Voltage | V_{SD} | $T_J = 25\text{ }^\circ\text{C}, I_S = 14\text{ A}, V_{GS} = 0\text{ V}^b$ | | - | - | 2.5 | V |
| Body Diode Reverse Recovery Time | t_{rr} | $T_J = 25\text{ }^\circ\text{C}, I_F = 14\text{ A}, dI/dt = 100\text{ A}/\mu\text{s}^b$ | | - | 150 | 280 | ns |
| Body Diode Reverse Recovery Charge | Q_{rr} | | | - | 0.85 | 1.7 | μC |
| Forward Turn-On Time | t_{on} | Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D) | | | | | |

Notes

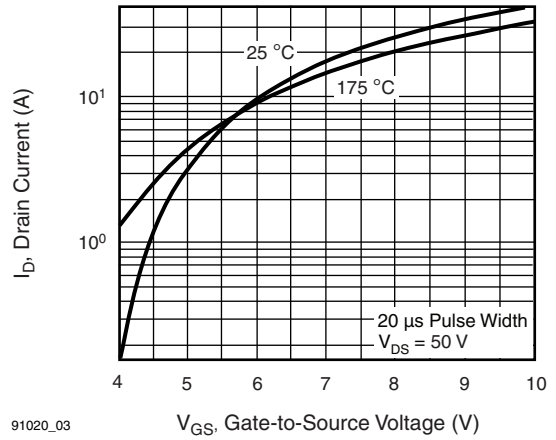
- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



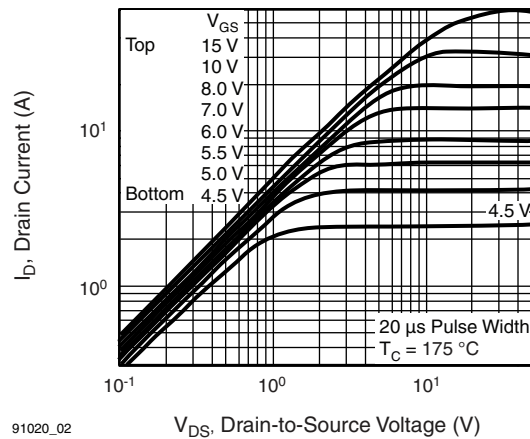
91020_01

Fig. 1 - Typical Output Characteristics, $T_C = 25\text{ °C}$



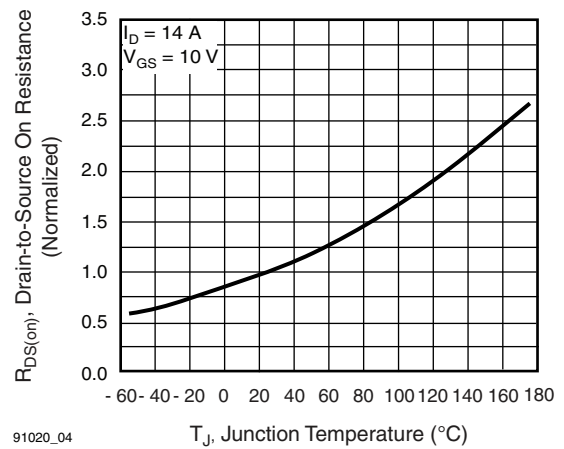
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Fig. 3 - Typical Transfer Characteristics



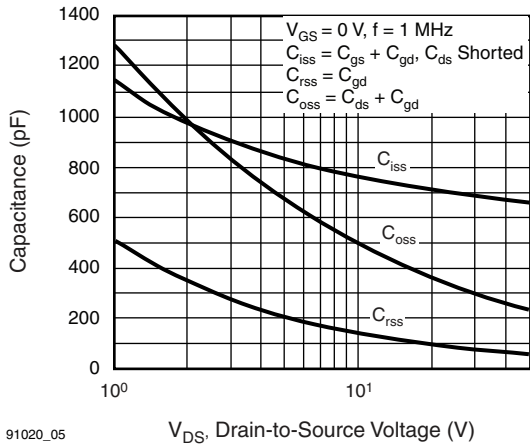
91020_02

Fig. 2 - Typical Output Characteristics, $T_C = 175\text{ °C}$



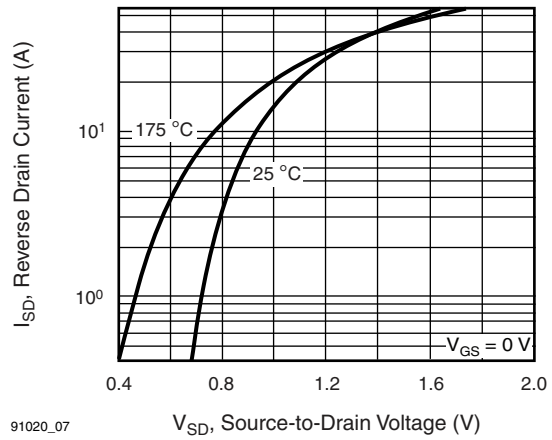
91020_04

Fig. 4 - Normalized On-Resistance vs. Temperature



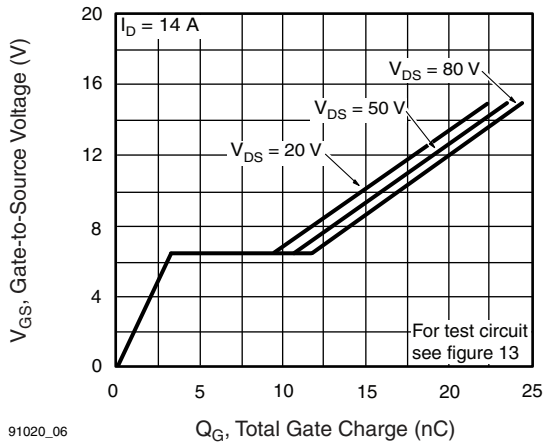
91020_05

Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage



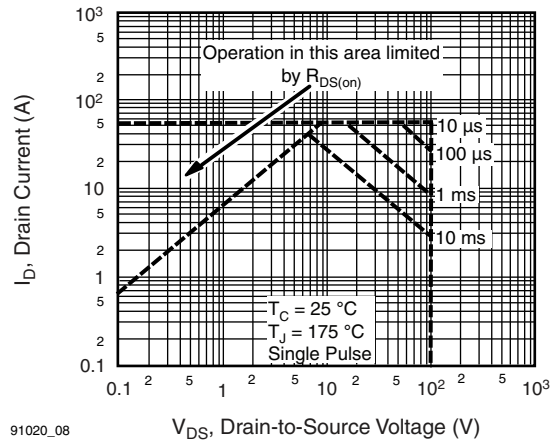
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Fig. 7 - Typical Source-Drain Diode Forward Voltage



91020_06

Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage



91020_08

Fig. 8 - Maximum Safe Operating Area

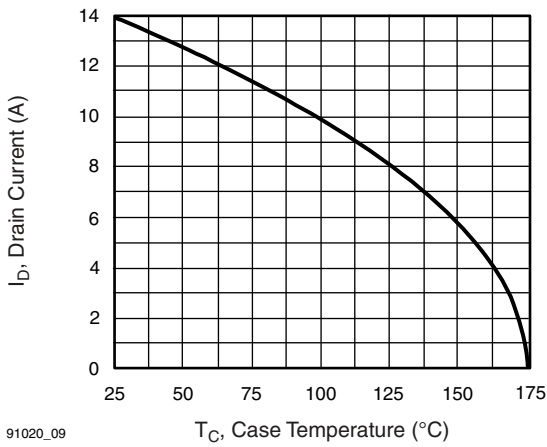


Fig. 9 - Maximum Drain Current vs. Case Temperature

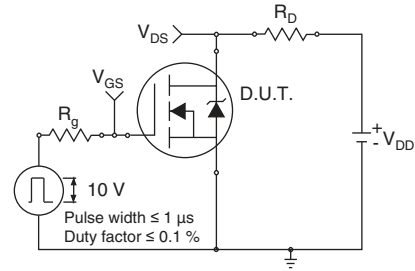


Fig. 10a - Switching Time Test Circuit



Fig. 10b - Switching Time Waveforms

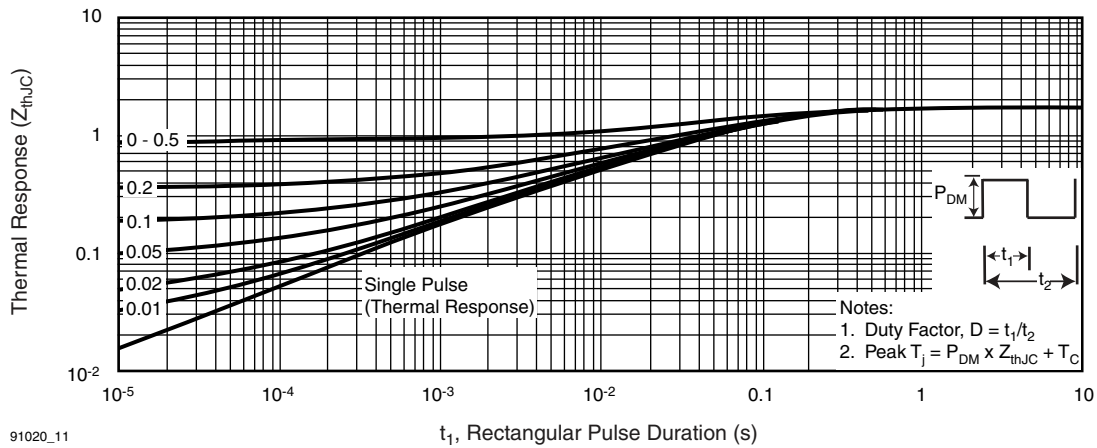


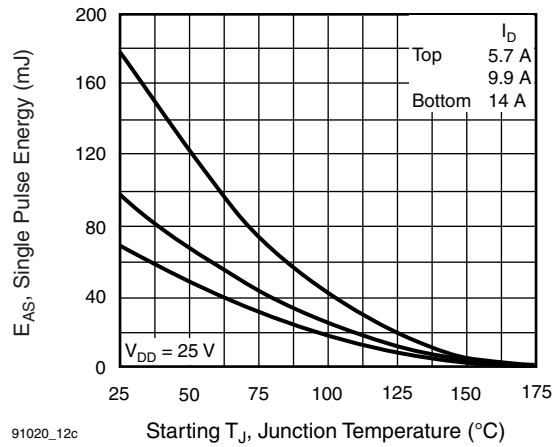
Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case



Fig. 12a - Unclamped Inductive Test Circuit



Fig. 12b - Unclamped Inductive Waveforms



91020_12c

Fig. 12c - Maximum Avalanche Energy vs. Drain Current

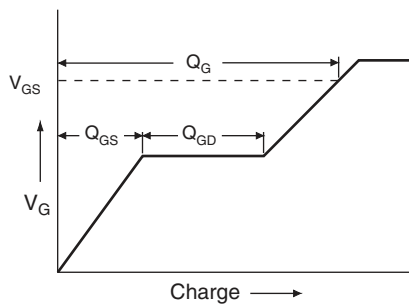


Fig. 13a - Basic Gate Charge Waveform

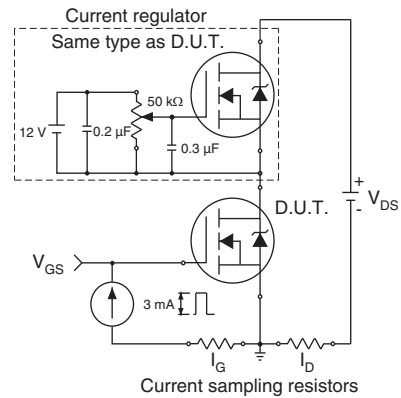
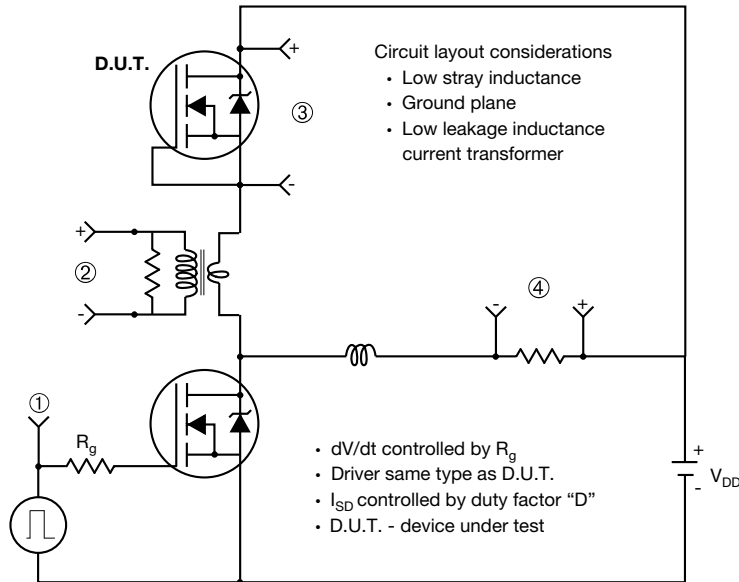


Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit



Note

a. $V_{GS} = 5 V$ for logic level devices

Fig. 14 - For N-Channel

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TO-263AB (HIGH VOLTAGE)



| DIM. | MILLIMETERS | | INCHES | |
|------|-------------|------|--------|-------|
| | MIN. | MAX. | MIN. | MAX. |
| A | 4.06 | 4.83 | 0.160 | 0.190 |
| A1 | 0.00 | 0.25 | 0.000 | 0.010 |
| b | 0.51 | 0.99 | 0.020 | 0.039 |
| b1 | 0.51 | 0.89 | 0.020 | 0.035 |
| b2 | 1.14 | 1.78 | 0.045 | 0.070 |
| b3 | 1.14 | 1.73 | 0.045 | 0.068 |
| c | 0.38 | 0.74 | 0.015 | 0.029 |
| c1 | 0.38 | 0.58 | 0.015 | 0.023 |
| c2 | 1.14 | 1.65 | 0.045 | 0.065 |
| D | 8.38 | 9.65 | 0.330 | 0.380 |

| DIM. | MILLIMETERS | | INCHES | |
|------|-------------|-------|-----------|-------|
| | MIN. | MAX. | MIN. | MAX. |
| D1 | 6.86 | - | 0.270 | - |
| E | 9.65 | 10.67 | 0.380 | 0.420 |
| E1 | 6.22 | - | 0.245 | - |
| e | 2.54 BSC | | 0.100 BSC | |
| H | 14.61 | 15.88 | 0.575 | 0.625 |
| L | 1.78 | 2.79 | 0.070 | 0.110 |
| L1 | - | 1.65 | - | 0.066 |
| L2 | - | 1.78 | - | 0.070 |
| L3 | 0.25 BSC | | 0.010 BSC | |
| L4 | 4.78 | 5.28 | 0.188 | 0.208 |

ECN: S-82110-Rev. A, 15-Sep-08
DWG: 5970

Notes

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimensions are shown in millimeters (inches).
3. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outmost extremes of the plastic body at datum A.
4. Thermal PAD contour optional within dimension E, L1, D1 and E1.
5. Dimension b1 and c1 apply to base metal only.
6. Datum A and B to be determined at datum plane H.
7. Outline conforms to JEDEC outline to TO-263AB.



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