8. DESIGN RECOMMENDATIONS

8.1. Design Note on Debug Port

- Pin# C6, C4 serve as WLAN and BT debug port, respectively. So test points for these two signals should be reserved for debugging purpose.
- Pin# C11 (WLAN_IRQ) needs to be pulled high via 10Kohm and use Pin# D11, C7 (WL_RS232_RX, WL_RS232_TX) as hardware interface to communicate with system platform and TI RTTT test utility for WLAN RF performance test, debug and manufacturing application.

8.2. Module Layout Recommendations

Follow these module layout recommendations:

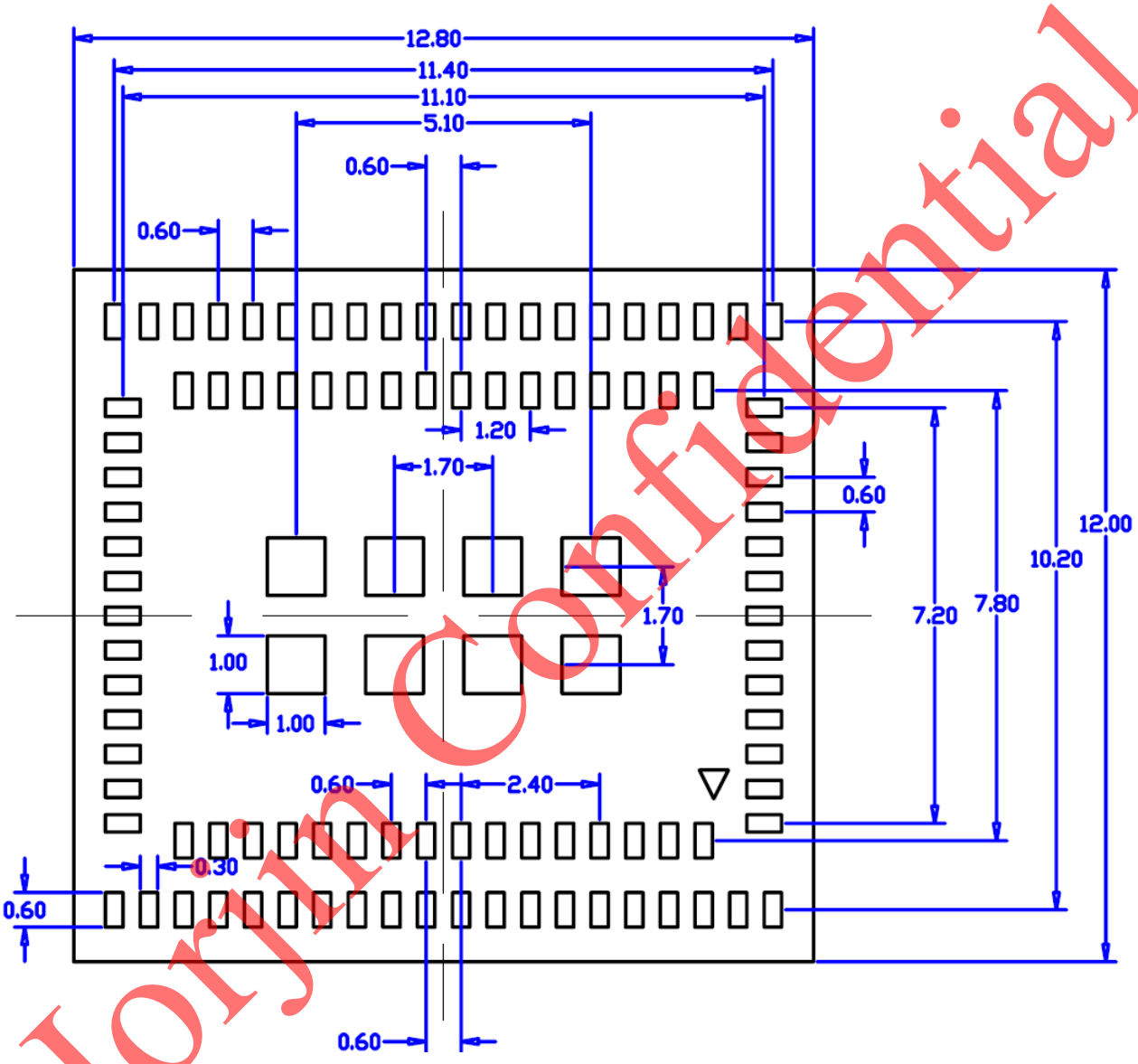
- Digital Signals Layout
  - SDIO signals traces (CMD, D0, D1, D2 and D3) should be routed in parallel to each other and as short as possible. **(Less than 12cm) Besides, every trace length must be the same as the others.**
  - Enough space above 1.5 time trace width or ground shielding between trace and trace will be benefit to make sure signal quality, especially for SDIO_CLK trace. Remember to keep them away from the other digital or analog signal traces. Adding ground shielding around these bus is recommended.
  - Route trace of SDIO_CLK at Top layer without vias.
  - SDIO Clock, Audio Clock (PCM_AUD_CLK), these digital clock signals are a source of noise. Keep the traces of these signals as short as possible. Whenever possible, maintain a clearance around them.
  - BT_AUD signals should be rounted in the same group and it's better to rout them at the same layer or confirm them referring to the same reference plane.
- RF Trace & Antenna
  - Keep 50ohm trace impedance.
  - Move all the high-speed traces and components far away from the antenna.
  - Check antenna vendor for the layout guideline and clearance.
- Power Trace

- Power trace for VBAT should be 20mil wide. 1.8V trace should be 15mil wide, at least.
- Isolate different power traces with Ground plane

- Ground
  - Having a complete Ground and more GND vias under module in layer1 for system stable and thermal dissipation.
  - Have a complete Ground pour in layer 2 for thermal dissipation.
  - Increase the GND pour in the 1st layer, move all the traces from the 1st layer to the inner layers if possible.
  - Move GND vias close to the pad.

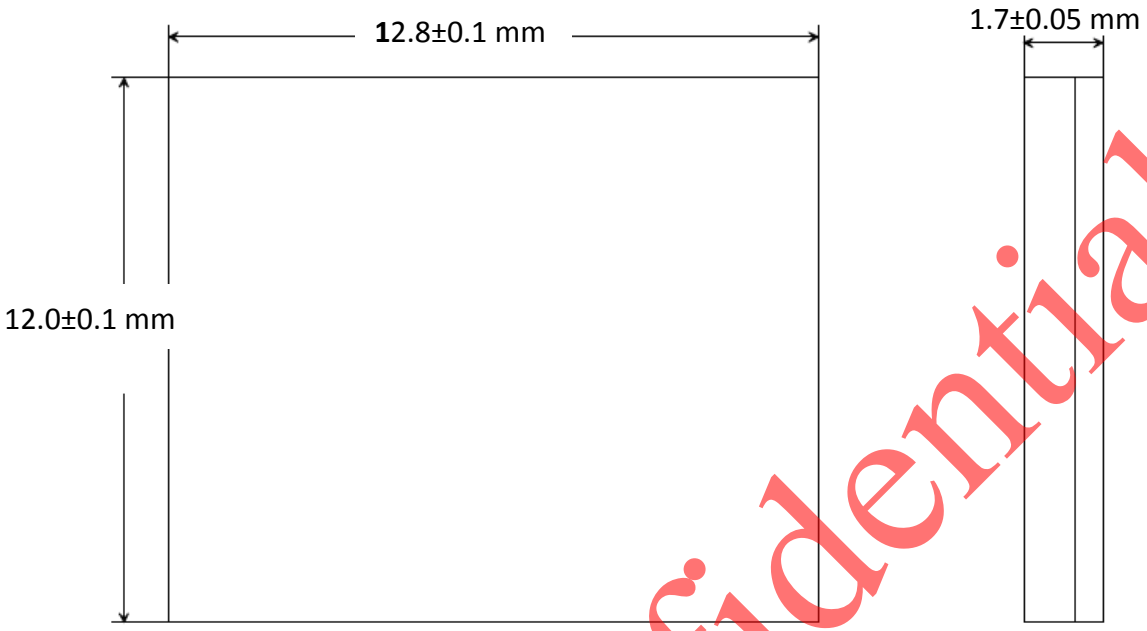
9. PACKAGE INFORMATION

9.1. Recommended Pad Design

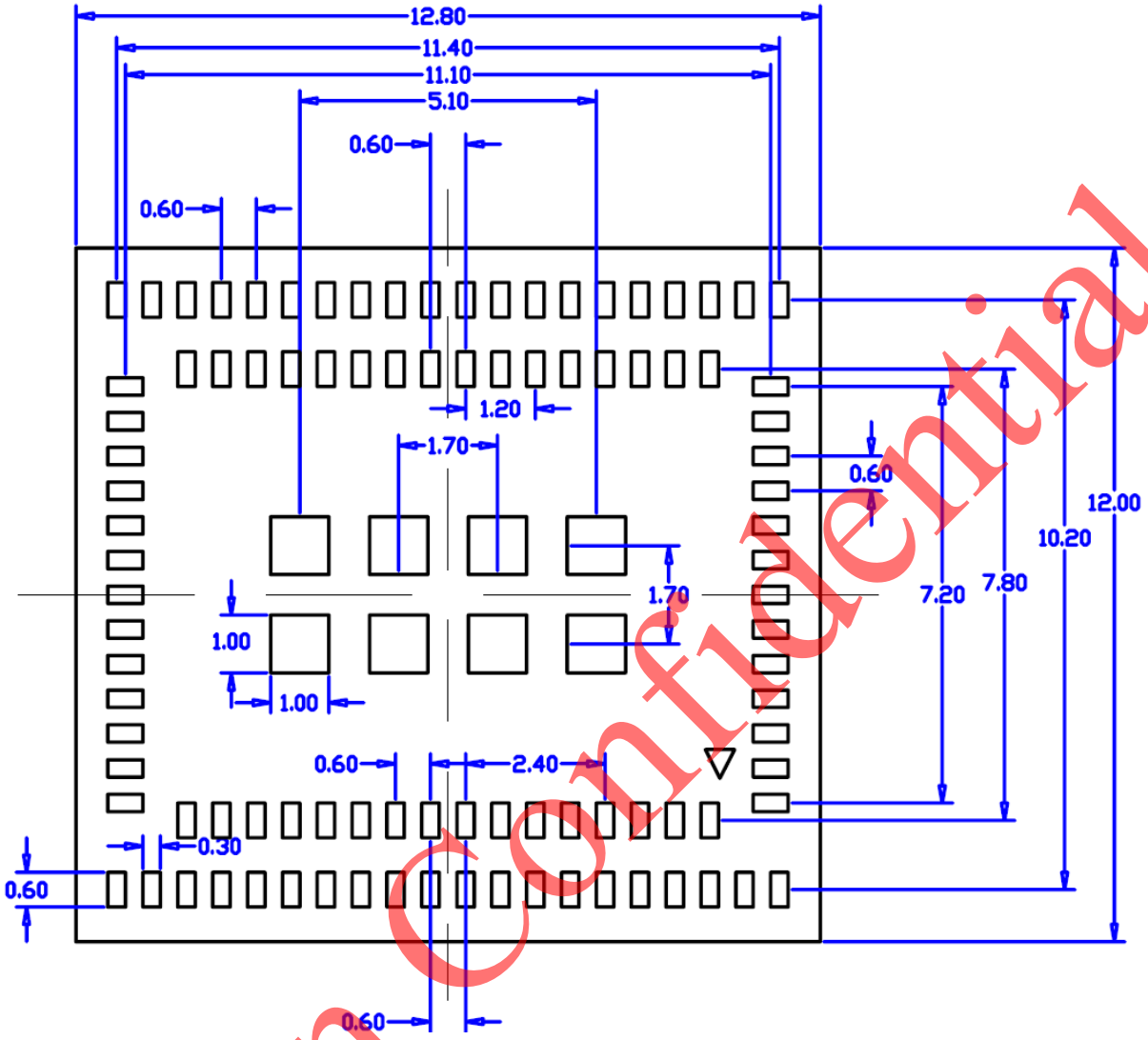


Note: Pad tolerance as ±30um

9.2. Module Mechanical Outline



Top and Side View



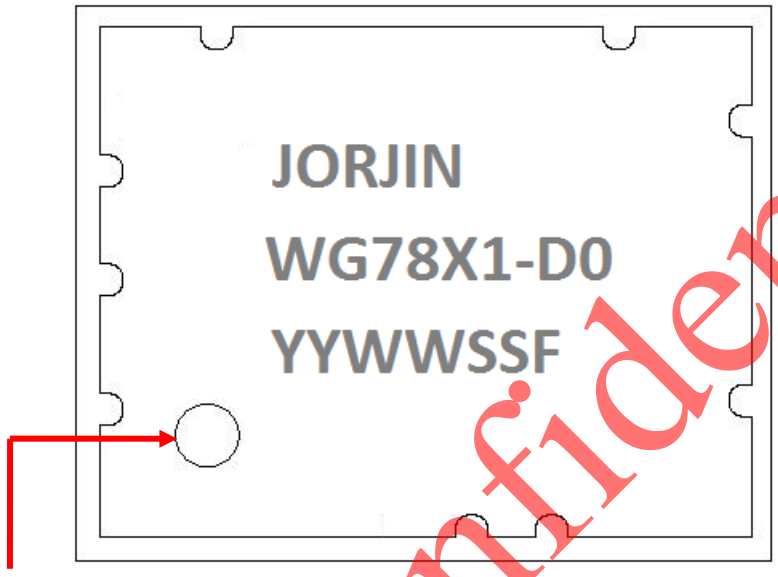
Pad dimensions

**We recommend adopting the same dimensions listed above for building PCB footprint.

9.3. Ordering Information

Part number:	WG7831-D0 WG7801-D0

9.4. Package Marking



PIN-1 Marking

Date Code: **YYWWSSF**

YY = Digit of the year, ex: 2011=11

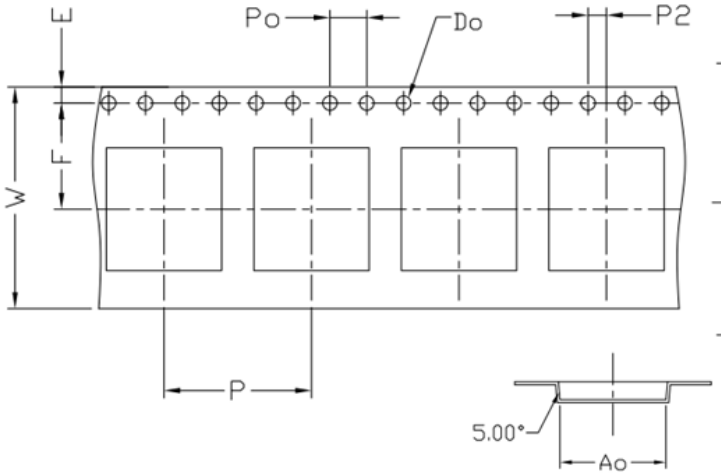
WW = Week (01~33)

SS = Serial number from 01 ~99 match to manufacture's lot number

F = Reserve for internal use

9.5PACKAGING

Tape Specification

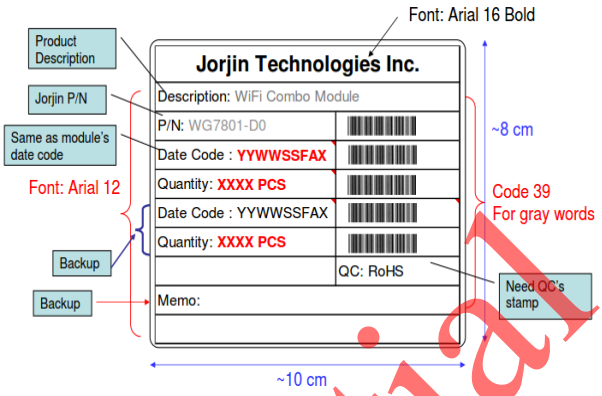


ITEM	DIM	ALTERNATE
W	24.00 +0.30 −0.30	
E	1.75 +0.10 −0.10	
F	11.50 +0.10 −0.10	
P	16.00 +0.10 −0.10	
Po	4.00 +0.10 −0.10	
P2	2.00 +0.10 −0.10	
Do	Ø1.50 +0.10 −0.00	
T	0.35 +0.05 −0.05	
Ao	12.50 +0.10 −0.10	
Bo	13.30 +0.10 −0.10	
Ko	2.10 +0.10 −0.10	

<Reel-1.8K PCS per reel>

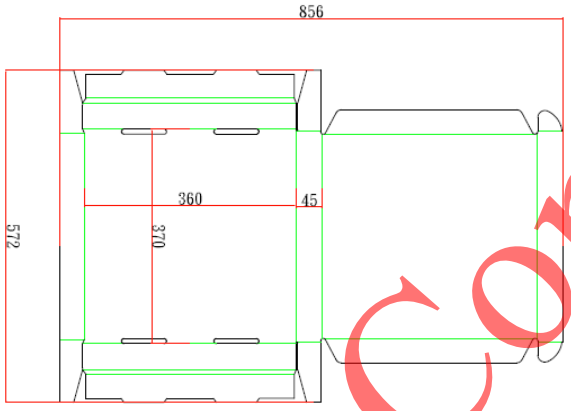
<pizza box-1 reel per pizza box>

<Carton-5 pizza box per carton>



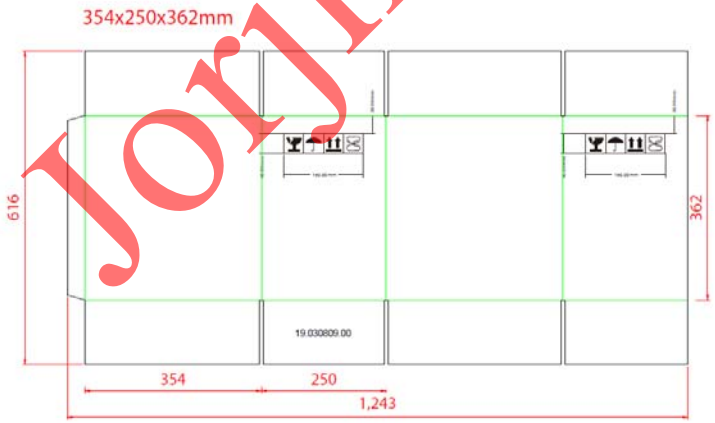
Product label

Pizza Box Specification:



佐鎂, B浪 370x360x45mm

Carton Specification:



10. SMT AND BAKING RECOMMENDATION

10.1. Baking Recommendation

- Baking condition：
  - Follow MSL Level 4 to do baking process.
  - After bag is opened, devices that will be subjected to reflow solder or other high temperature process must be

a) Mounted within 72 hours of factory conditions <30°C/60% RH, or

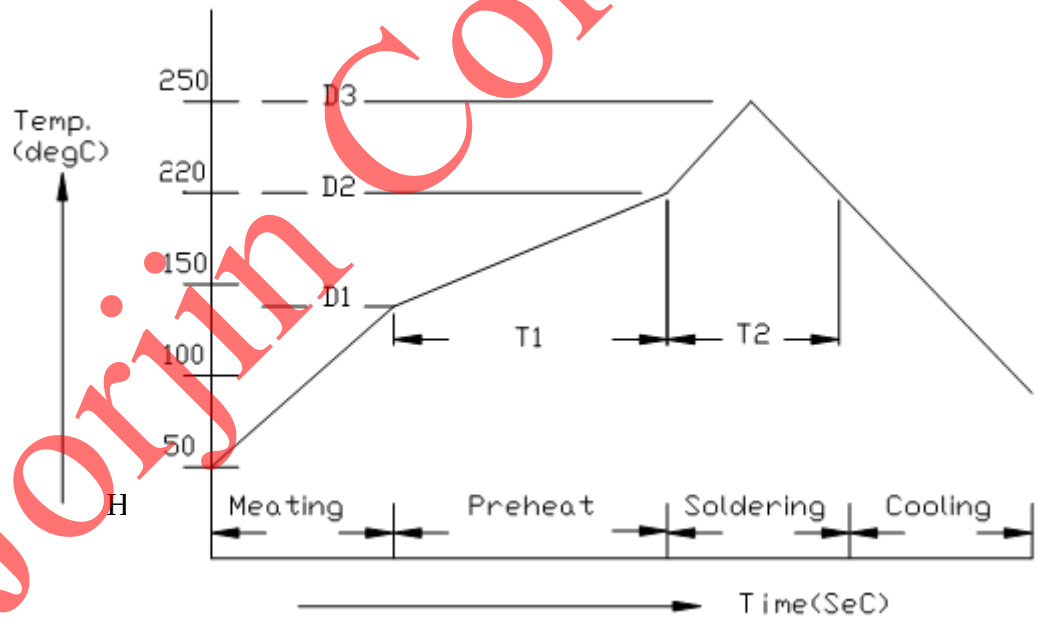
b) Stored at <10% RH.

  - Devices require bake, before mounting, if Humidity Indicator Card reads >10%

If baking is required, Devices may be baked for 8 hrs. at 125 °C.

10.2. SMT Recommendation

- Recommended Reflow profile：



No.	Item	Temperature (°C)	Time (sec)
1	Pre-heat	D1: 140 ~ D2: 200	T1: 80 ~ 120
2	Soldering	D2: = 220	T2: 60 +/- 10
3	Peak-Temp.	D3: 250 °C max	

Note: (1) Reflow soldering is recommended two times maximum.

(2) Add Nitrogen while Reflow process： SMT solder ability will be better.

- **Stencil thickness**： 0.1~ 0.13 mm (Recommended)
- **Soldering paste (without Pb)**： Recommended SENJU N705-GRN3360-K2-V can get better soldering effects.

11. HISTORY CHANGE

Revision	Date	Description
D 0.1	2013/06/11	Initial Released
D 0.2	2013/11/06	Add specifications
D 0.3	2014/03/11	Update specification