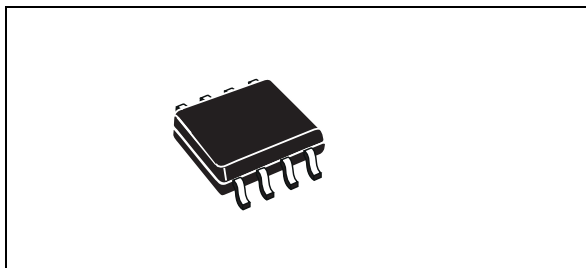


High voltage high and low-side driver

Datasheet - preliminary data



Features

- High voltage rail up to 600 V
- dV/dt immunity ± 50 V/ns in full temperature range
- Driver current capability:
 - 290 mA source
 - 430 mA sink
- Switching times 75/35 ns rise/fall with 1 nF load
- 3.3 V, 5 V TTL/CMOS inputs with hysteresis
- Integrated bootstrap diode
- Compact and simplified layout
- Bill of material reduction
- Effective fault protection
- Flexible, easy and fast design

Applications

- Motor driver for home appliances
- Factory automation
- Industrial drives and fans

Description

The L6395 is a high voltage device manufactured with BCD "OFF-LINE" technology. It is a single-chip high and low-side gate driver for N-channel power MOSFETs or IGBTs.

The high-side (floating) section is designed to stand a voltage rail up to 600 V. The logic inputs are CMOS/TTL compatible down to 3.3 V for easy interfacing microcontroller/DSP.

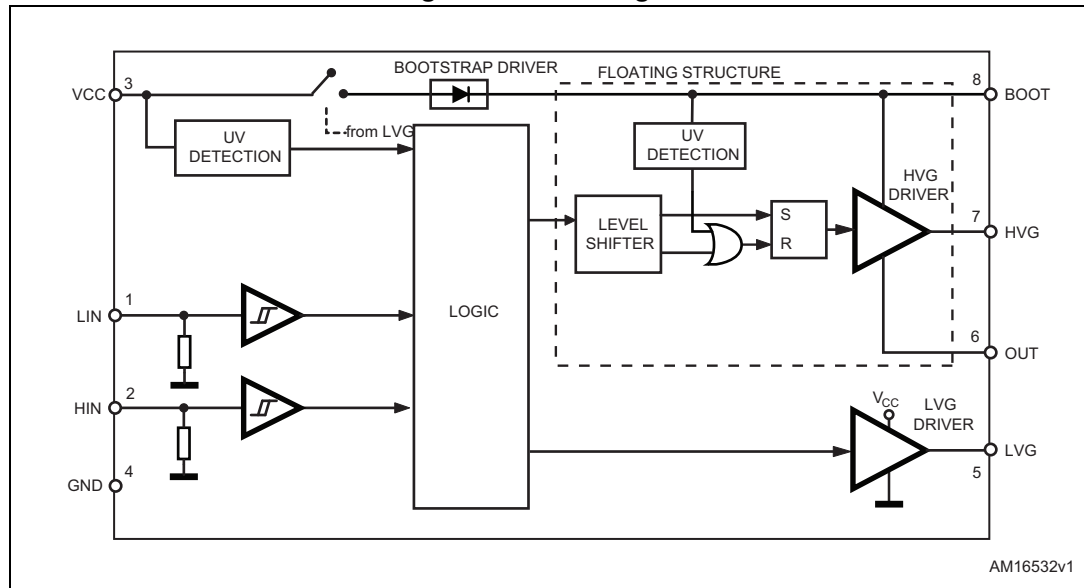
Table 1. Device summary

Order codes	Package	Packaging
L6395D	SO-8	Tube
L6395DTR	SO-8	Tape and reel

Contents

1	Block diagram	3
2	Pin connection	4
3	Truth table	5
4	Electrical data	6
4.1	Absolute maximum ratings	6
4.2	Thermal data	6
4.3	Recommended operating conditions	6
5	Electrical characteristics	7
5.1	AC operation	7
5.2	DC operation	8
6	Typical application diagram	10
7	Bootstrap driver	11
7.1	C _{BOOT} selection and charging	11
8	Package mechanical data	13
9	Revision history	15

1 Block diagram

Figure 1. Block diagram

2 Pin connection

Figure 2. Pin connection

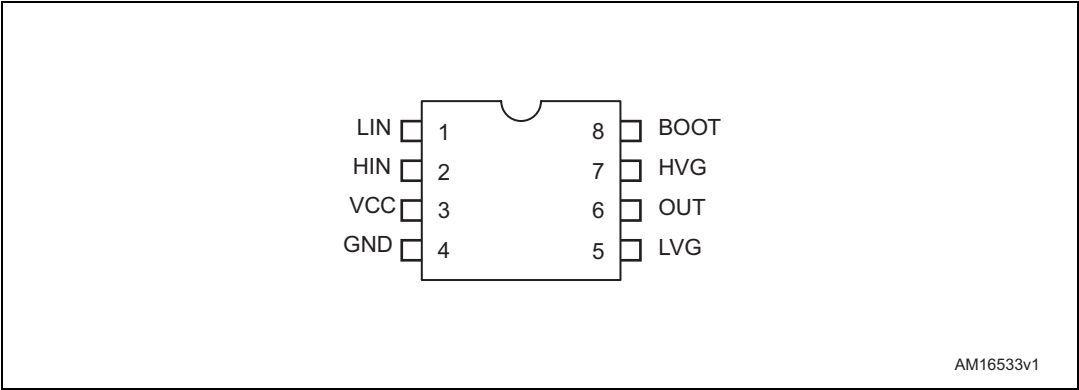


Table 2. Pin description

Pin	Pin name	Type	Function
1	LIN	I	Low-side driver logic input (active high)
2	HIN	I	High-side driver logic input (active high)
3	VCC	P	Lower section supply voltage
4	GND	P	Ground
5	LVG ⁽¹⁾	O	Low-side driver output
6	OUT	P	High-side (floating) common voltage
7	HVG ⁽¹⁾	O	High-side driver output
8	BOOT	P	Bootstrapped supply voltage

1. The circuit guarantees less than 1 V on the LVG and HVG pins (@ $I_{\text{sink}} = 10 \text{ mA}$), with $V_{\text{CC}} > 3 \text{ V}$. In this manner, the “bleeder”, resistor connected between the gate and the source of the external MOSFET normally used to hold the pin low, is omitted.

3 Truth table

Table 3. Truth table

Input		Output	
LIN	HIN	LVG	HVG
L	L	L	L
L	H	L	H
H	L	H	L
H	H	H	H

4 Electrical data

4.1 Absolute maximum ratings

Table 4. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		Min.	Max.	
V_{CC}	Supply voltage	- 0.3	21	V
V_{OUT}	Output voltage	$V_{BOOT} - 21$	$V_{BOOT} + 0.3$	V
V_{BOOT}	Bootstrap voltage	- 0.3	620	V
V_{hvg}	High-side gate output voltage	$V_{OUT} - 0.3$	$V_{BOOT} + 0.3$	V
V_{lvg}	Low-side gate output voltage	- 0.3	$V_{CC} + 0.3$	V
V_i	Logic input voltage	- 0.3	15	V
dV_{OUT}/dt	Allowed output slew rate		50	V/ns
P_{tot}	Total power dissipation ($T_A = 25\text{ °C}$)		800	mW
T_J	Junction temperature		150	°C
T_{stg}	Storage temperature	-50	150	°C

4.2 Thermal data

Table 5. Thermal data

Symbol	Parameter	SO-8	Unit
$R_{th(JA)}$	Thermal resistance junction-to-ambient	150	°C/W

4.3 Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Pin	Parameter	Test condition	Value		Unit
				Min.	Max.	
V_{CC}	3	Supply voltage		10	20	V
$V_{BO}^{(1)}$	8-6	Floating supply voltage		9.4	20	V
V_{OUT}	6	Output voltage ⁽¹⁾		-11 ⁽²⁾	580	V
f_{SW}		Switching frequency	HVG, LVG load $C_L = 1\text{ nF}$		800	kHz
T_J		Junction temperature		-40	125	°C

1. $V_{BO} = V_{BOOT} - V_{OUT}$

2. LVG off. $V_{CC} = 10\text{ V}$. Logic is operational if $V_{boot} > 5\text{ V}$

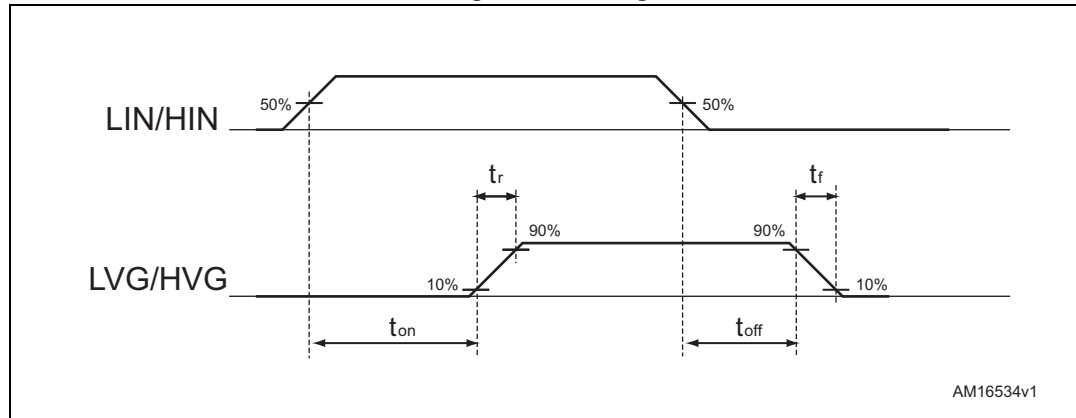
5 Electrical characteristics

5.1 AC operation

Table 7. AC operation electrical characteristics ($V_{CC} = 15\text{ V}$; $T_j = +25\text{ }^{\circ}\text{C}$)

Symbol	Pin	Parameter	Test condition	Value			Unit
				Min.	Typ.	Max.	
t_{on}	1,2 vs 5,7	High/low-side driver turn-on propagation delay	$V_{OUT} = 0\text{ V}$ $V_{BOOT} = V_{CC}$ $C_L = 1\text{ nF}$ $V_{IN} = 0\text{ to }3.3\text{ V}$ see Figure 3	50	125	200	ns
t_{off}	1,2 vs 5,7	High/low-side driver turn-off propagation delay	$V_{OUT} = 0\text{ V}$ $V_{BOOT} = V_{CC}$ $C_L = 1\text{ nF}$ $V_{IN} = 3.3\text{ V to }0$ see Figure 3	50	125	200	ns
t_r	5, 7	Rise time	$C_L = 1\text{ nF}$		75	120	ns
t_f	5, 7	Fall time	$C_L = 1\text{ nF}$		35	70	ns

Figure 3. Timing



5.2 DC operation

($V_{CC} = 15\text{ V}$; $T_j = +25\text{ °C}$)

Table 8. DC operation electrical characteristics

Symbol	Pin	Parameter	Test condition	Value			Unit
				Min.	Typ.	Max.	
Low supply voltage section							
V _{CC_hys}	3	V _{CC} UV hysteresis		0.6	0.7	0.8	V
V _{CC_thON}	3	V _{CC} UV turn ON threshold		9	9.5	10	V
V _{CC_thOFF}	3	V _{CC} UV turn OFF threshold		8.3	8.8	9.3	V
I _{qccu}	3	Undervoltage quiescent supply current	V _{CC} = 7 V LIN = 5V; HIN = GND;	40	90	150	μA
I _{qcc}	3	Quiescent current	V _{CC} = 15 V LIN = 5 V; HIN = GND;	100	220	350	μA
Bootstrapped supply voltage section ⁽¹⁾							
V _{BO_hys}	8	V _{BO} UV hysteresis		0.5	0.6	0.7	V
V _{BO_thON}	8	V _{BO} UV turn ON threshold		7.9	8.6	9.4	V
V _{BO_thOFF}	8	V _{BO} UV turn OFF threshold		7.3	8	8.7	V
I _{QBOU}	8	Undervoltage V _{BO} quiescent current	V _{BO} = 7 V LIN = GND; HIN = 5 V;	10	30	60	μA
I _{QBO}	8	V _{BO} quiescent current	V _{BO} = 15 V LIN = GND; HIN = 5 V;		190	220	μA
I _{LK}	8	High voltage leakage current	V _{hvg} = V _{OUT} = V _{BOOT} = 600V			10	μA
R _{DS(on)}		Bootstrap driver on-resistance ⁽²⁾	LVG on		120		Ω
Driving buffer section							
I _{so}	5, 7	High/low-side source short-circuit current	V _{IN} = V _{ih} (t _p < 10 μs)	200	290		mA
I _{si}	5, 7	High/low-side sink short-circuit current	V _{IN} = V _{il} (t _p < 10 μs)	250	430		mA
Logic inputs							
V _{il}	1, 2	Low level logic threshold voltage		0.8		1.1	V
V _{ih}	1, 2	High level logic threshold voltage		1.9		2.25	V
I _{HINh}	2	HIN logic “1” input bias current	HIN = 15 V	10	40	100	μA

Table 8. DC operation electrical characteristics (continued)

Symbol	Pin	Parameter	Test condition	Value			Unit
				Min.	Typ.	Max.	
I_{HINI}	2	HIN logic "0" input bias current	HIN = 0 V			1	μA
I_{LINh}	1	LIN logic "1" input bias current	LIN = 15 V	10	40	100	μA
I_{LINl}	1	LIN logic "0" input bias current	LIN = 0 V			1	μA

1. $V_{BO} = V_{BOOT} - V_{OUT}$

2. $R_{DS(on)}$ is tested in the following way: $R_{DS(on)} = [(V_{CC} - V_{CBOOT1}) - (V_{CC} - V_{CBOOT2})] / [I_1(V_{CC}, V_{CBOOT1}) - I_2(V_{CC}, V_{CBOOT2})]$ where I_1 is pin 8 current when $V_{CBOOT} = V_{CBOOT1}$, I_2 when $V_{CBOOT} = V_{CBOOT2}$.

6 Typical application diagram

Figure 4. Application diagram

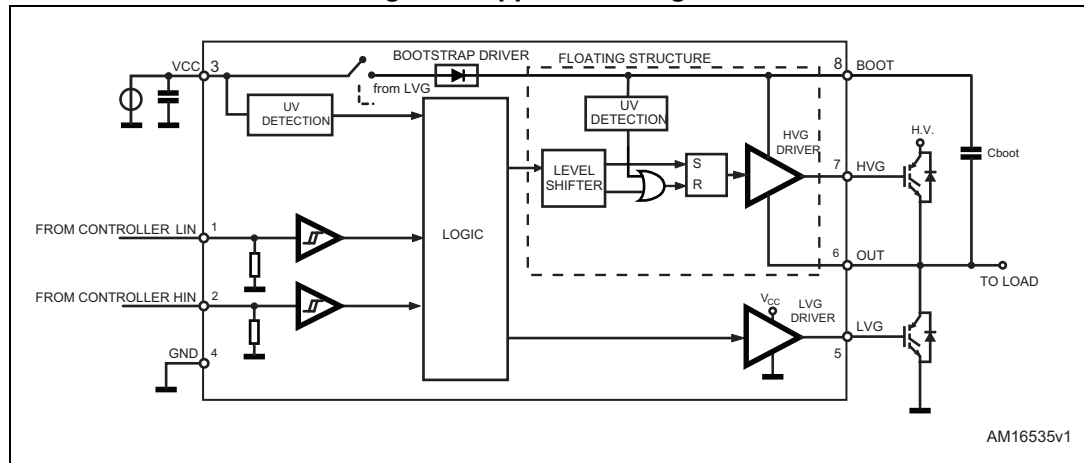
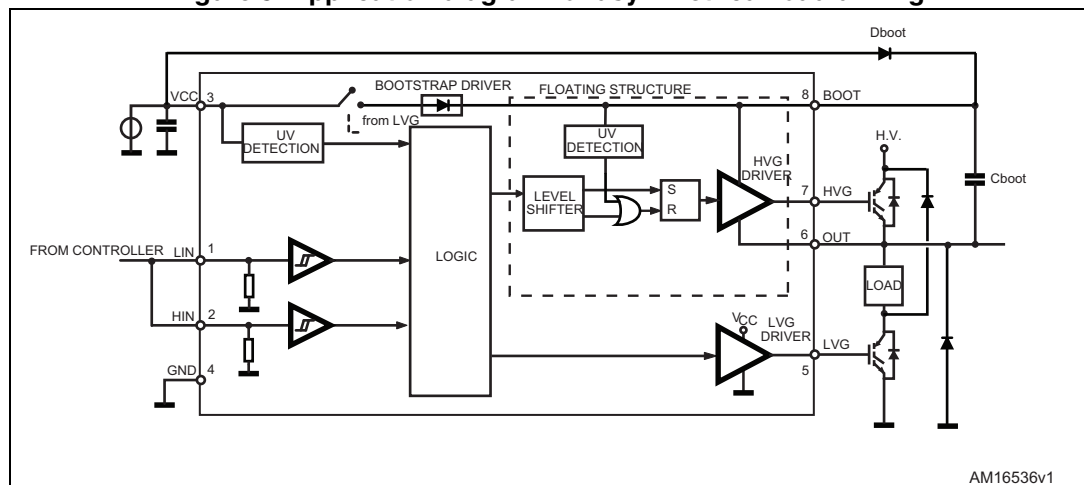


Figure 5. Application diagram for asymmetrical load driving



7 Bootstrap driver

A bootstrap circuitry is needed to supply the high-voltage section. This function is normally accomplished using a high-voltage fast recovery diode ([Figure 6](#)). In the L6395 a patented integrated structure replaces the external diode. It is implemented using a high voltage DMOS, driven synchronously with the low-side driver (LVG), with diode in series, as shown in [Figure 7](#). An internal charge pump provides the DMOS driving voltage.

7.1 C_{BOOT} selection and charging

To select the proper C_{BOOT} value the external MOS can be seen as an equivalent capacitor. This capacitor C_{EXT} is related to the MOS total gate charge:

Equation 1

$$C_{EXT} = \frac{Q_{gate}}{V_{gate}}$$

The ratio between the capacitors C_{EXT} and C_{BOOT} is proportional to the cyclical voltage loss.

It must be:

Equation 2

$$C_{BOOT} \gg C_{EXT}$$

E.g.: if Q_{gate} is 30 nC and V_{gate} is 10 V, C_{EXT} is 3 nF. With C_{BOOT} = 100 nF the drop is 300 mV.

If HVG needs to be supplied for an extended period, the C_{BOOT} selection has to take into account also the leakage and quiescent losses.

E.g.: HVG steady-state consumption is lower than 220 μA, so if HVG T_{ON} is 5 ms, C_{BOOT} must supply 1.1 μC to C_{EXT}. This charge on a 1 μF capacitor means a voltage drop of 1.1 V.

The internal bootstrap driver offers some important advantages: the external fast recovery diode can be avoided (it usually has a high leakage current).

This structure can work only if V_{OUT} is close to GND (or lower) and, at the same time, the LVG is on. The charging time (T_{charge}) of the C_{BOOT} is the time in which both conditions are fulfilled and it has to be long enough to charge the capacitor.

The bootstrap driver introduces a voltage drop due to the DMOS R_{DS(on)} (typical value: 120 Ω). At low switching frequency, this drop can be neglected but, operating at high switching frequency, it should be taken into account.

The following equation is useful to compute the drop on the bootstrap DMOS:

Equation 3

$$V_{drop} = I_{charge} \cdot R_{DS(on)} \rightarrow V_{drop} = \frac{Q_{gate}}{T_{charge}} \cdot R_{DS(on)}$$

where Q_{gate} is the gate charge of the external power MOSFET, $R_{\text{DS(on)}}$ is the on-resistance of the bootstrap DMOS and T_{charge} is the charging time of the bootstrap capacitor.

For example: using a power MOSFET with a total gate charge of 30 nC, the drop on the bootstrap DMOS is about 1 V, if the T_{charge} is 5 μs .

Equation 4

$$V_{\text{drop}} = \frac{30 \text{ nC}}{5 \mu\text{s}} \cdot 120 \Omega \approx 0.7 \text{ V}$$

V_{drop} must be taken into account when the voltage drop on C_{BOOT} is calculated: whether this drop is too high, or the circuit topology does not allow a sufficient charging time, an external diode can be used.

Figure 6. Bootstrap driver with high voltage fast recovery diode

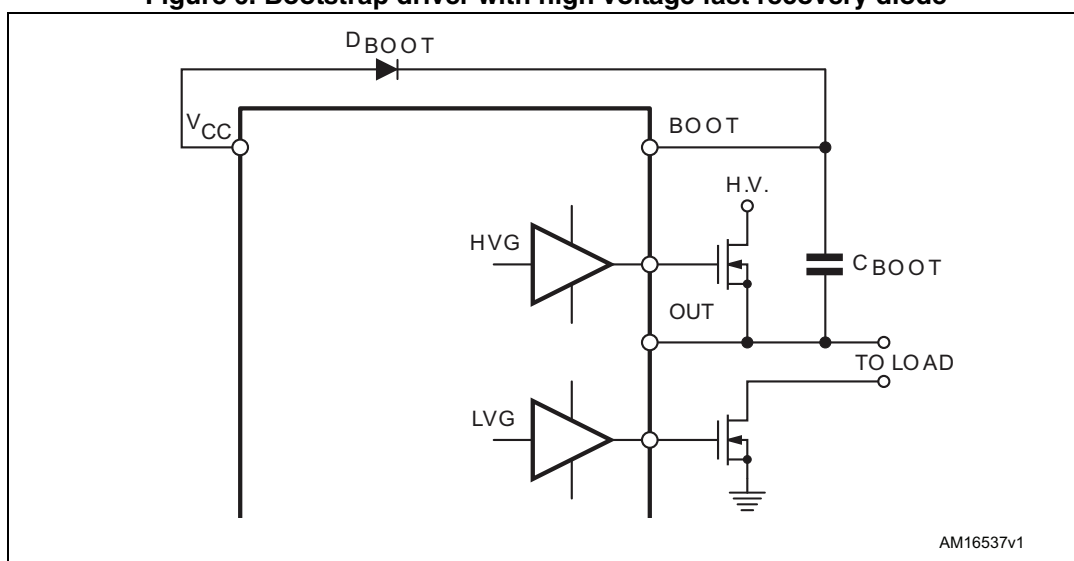
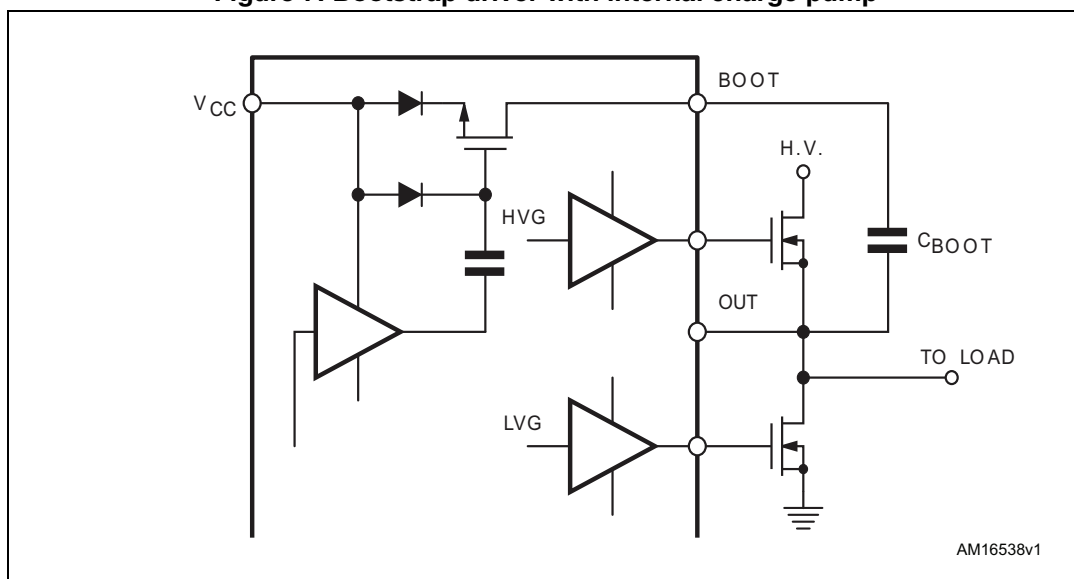


Figure 7. Bootstrap driver with internal charge pump



8 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Table 9. SO-8 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			1.75
A1	0.10		0.25
A2	1.25		
b	0.31		0.51
b1	0.28		0.48
c	0.10		0.25
c1	0.10		0.23
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e		1.27	
h	0.25		0.50
L	0.40		1.27
L1		1.04	
L2		0.25	
k	0°		8°
ccc			0.10

Figure 8. SO-8 package drawing

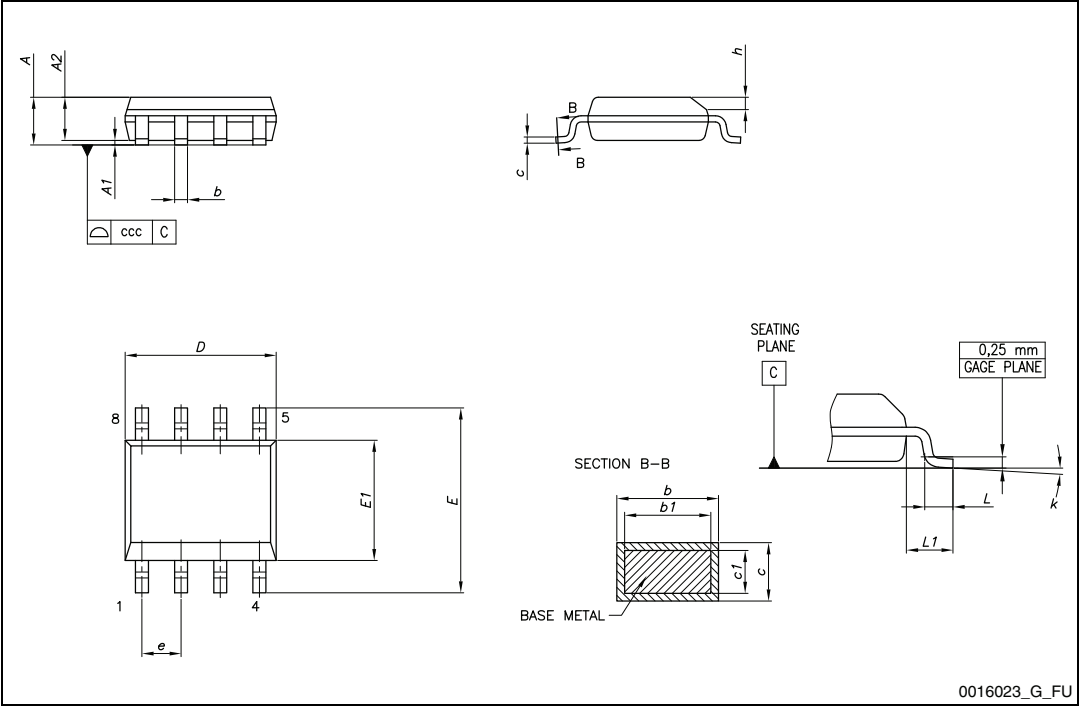
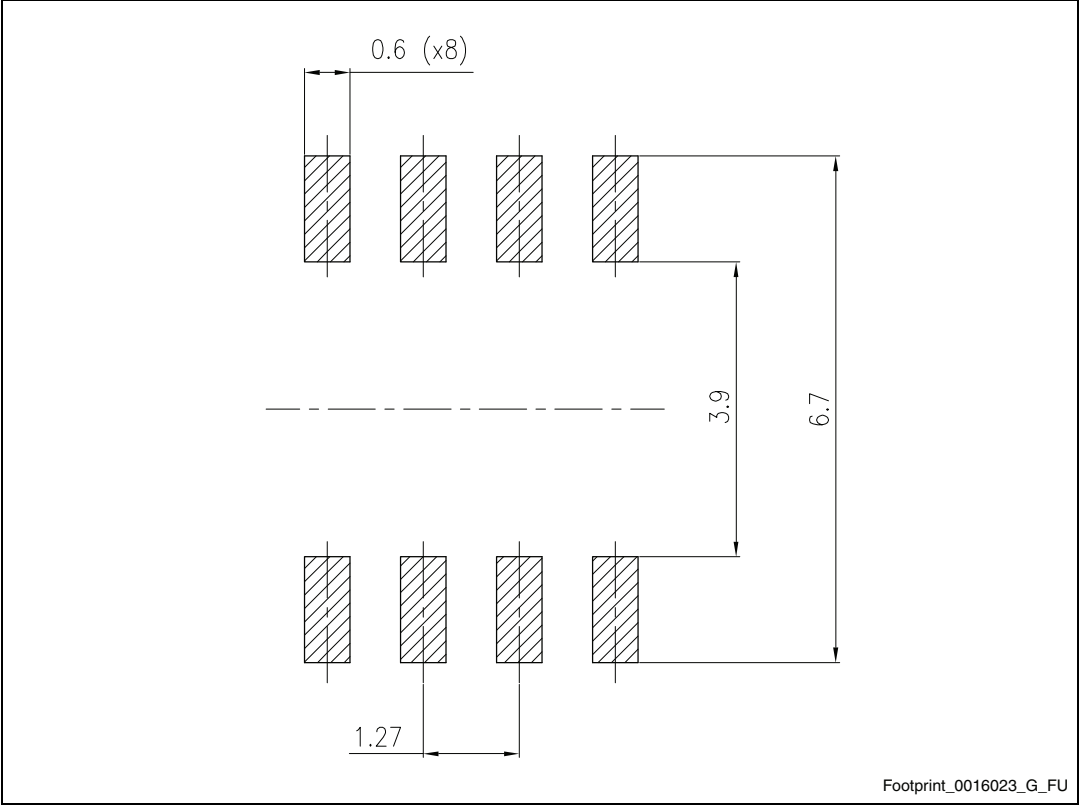


Figure 9. SO-8 footprint



9 Revision history

Table 10. Document revision history

Date	Revision	Changes
20-Mar-2013	1	Initial release.

Please Read Carefully:

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST's terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

UNLESS OTHERWISE SET FORTH IN ST'S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

ST PRODUCTS ARE NOT AUTHORIZED FOR USE IN WEAPONS. NOR ARE ST PRODUCTS DESIGNED OR AUTHORIZED FOR USE IN: (A) SAFETY CRITICAL APPLICATIONS SUCH AS LIFE SUPPORTING, ACTIVE IMPLANTED DEVICES OR SYSTEMS WITH PRODUCT FUNCTIONAL SAFETY REQUIREMENTS; (B) AERONAUTIC APPLICATIONS; (C) AUTOMOTIVE APPLICATIONS OR ENVIRONMENTS, AND/OR (D) AEROSPACE APPLICATIONS OR ENVIRONMENTS. WHERE ST PRODUCTS ARE NOT DESIGNED FOR SUCH USE, THE PURCHASER SHALL USE PRODUCTS AT PURCHASER'S SOLE RISK, EVEN IF ST HAS BEEN INFORMED IN WRITING OF SUCH USAGE, UNLESS A PRODUCT IS EXPRESSLY DESIGNATED BY ST AS BEING INTENDED FOR "AUTOMOTIVE, AUTOMOTIVE SAFETY OR MEDICAL" INDUSTRY DOMAINS ACCORDING TO ST PRODUCT DESIGN SPECIFICATIONS. PRODUCTS FORMALLY ESCC, QML OR JAN QUALIFIED ARE DEEMED SUITABLE FOR USE IN AEROSPACE BY THE CORRESPONDING GOVERNMENTAL AGENCY.

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

© 2013 STMicroelectronics - All rights reserved

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Philippines - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com