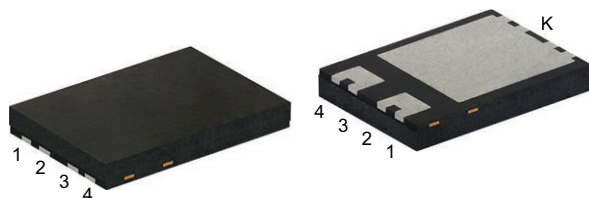
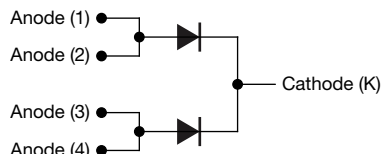


Ultrafast Rectifier, 2 x 7.5 A FRED Pt®


DFN6546A


RoHS
COMPLIANT
HALOGEN
FREE

FEATURES

- Very low profile - typical height of 0.88 mm
- Ideal for automated placement
- Wettable flanks allows easy inspection with AOI (automated optical inspection). No X-ray necessary
- Low forward voltage drop, low power losses
- Low leakage current
- Meets MSL level 1, per J-STD-020, LF maximum peak of 260 °C
- AEC-Q101 qualified
- For PFC, CRM snubber operation
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

TYPICAL APPLICATIONS

Designed for high-performance automotive applications including High-frequency rectifiers, DC/DC converters, freewheeling diodes, load dump protection, clamping and snubber circuits, reverse and series polarity protection, Engine Control Unit (ECUs) and LED lighting systems.

Suitable for low power auxiliary circuitry and medium power applications.

MECHANICAL DATA

Case: DFN6546A

Molding compound meets UL 94 V-0 flammability rating

Terminals: matte tin plated leads, solderable per J-STD-002, meets JESD 201 class 2 whisker test

Polarity: color band denotes cathode end

LINKS TO ADDITIONAL RESOURCES



PRIMARY CHARACTERISTICS

$I_{F(AV)}$	2 x 7.5 A
V_R	200 V
V_F at I_F	0.75 V
t_{rr} (typ.)	15 ns
I_{FSM}	124 A
T_J max.	175 °C
Package	DFN6546A
Circuit configuration	Common cathode

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Peak repetitive reverse voltage, per leg	V_{RRM}		200	V
Average rectified forward current, per leg	$I_{F(AV)}$	$T_M = 152\text{ °C}$, $D = 0.50$	7.5	A
Non-repetitive peak surge current, per leg	I_{FSM}	$T_J = 25\text{ °C}$, 10 ms sine pulse	124	
Operating junction and storage temperatures	T_J , T_{Stg}		-55 to +175	°C

ELECTRICAL SPECIFICATIONS ($T_J = 25\text{ °C}$ unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Breakdown voltage, blocking voltage, per leg	V_{BR} , V_R	$I_R = 100\text{ }\mu\text{A}$	200	-	-	V
Forward voltage, per leg	V_F	$I_F = 7.5\text{ A}$	-	0.9	1.1	
		$I_F = 7.5\text{ A}$, $T_J = 150\text{ °C}$	-	0.75	0.85	
Reverse leakage current, per leg	I_R	$V_R = V_R$ rated	-	-	1	μA
		$T_J = 150\text{ °C}$, $V_R = V_R$ rated	-	-	150	
Junction capacitance, per leg	C_T	$V_R = 200\text{ V}$	-	25	-	pF

**DYNAMIC RECOVERY CHARACTERISTICS** ($T_J = 25\text{ }^{\circ}\text{C}$ unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Reverse recovery time, per leg	t_{rr}	$I_F = 0.5\text{ A}$, $I_R = 1\text{ A}$, $I_{rr} = 0.25\text{ A}$	-	15	25	ns
		$T_J = 25\text{ }^{\circ}\text{C}$	-	12	-	
		$T_J = 125\text{ }^{\circ}\text{C}$	-	21	-	
Peak recovery current, per leg	I_{RRM}	$T_J = 25\text{ }^{\circ}\text{C}$	-	3.9	-	A
		$T_J = 125\text{ }^{\circ}\text{C}$	-	7.2	-	
Reverse recovery charge, per leg	Q_{rr}	$T_J = 25\text{ }^{\circ}\text{C}$	-	25	-	nC
		$T_J = 125\text{ }^{\circ}\text{C}$	-	77	-	

THERMAL - MECHANICAL SPECIFICATIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Maximum junction and storage temperature range	T_J, T_{Stg}		-55	-	175	$^{\circ}\text{C}$
Thermal resistance, junction to mount, per leg	$R_{thJM}^{(1)}$		-	-	3.4	$^{\circ}\text{C/W}$
Weight			-	0.086	-	9
Marking device		Case style DFN6546A	15CH2			

Note

(1) Thermal resistance junction to mount follows JEDEC® 51-14 transient dual interface test method (TDIM)

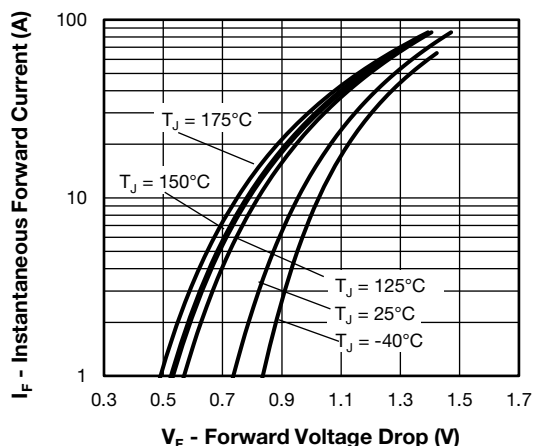


Fig. 1 - Typical Forward Voltage Drop Characteristics, per Leg

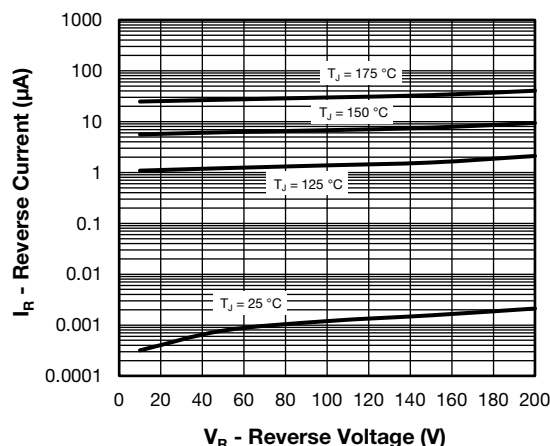


Fig. 2 - Typical Values of Reverse Current vs. Reverse Voltage, per Leg

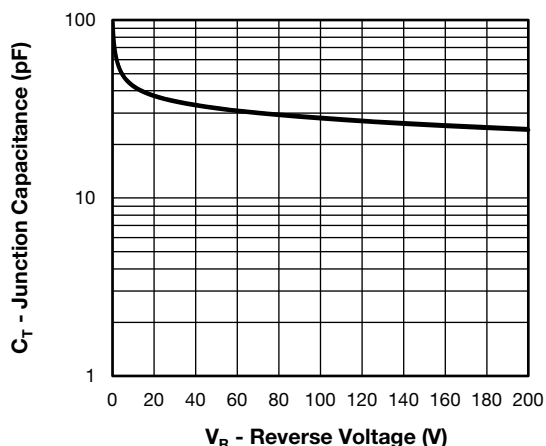


Fig. 3 - Typical Junction Capacitance vs. Reverse Voltage, per Leg

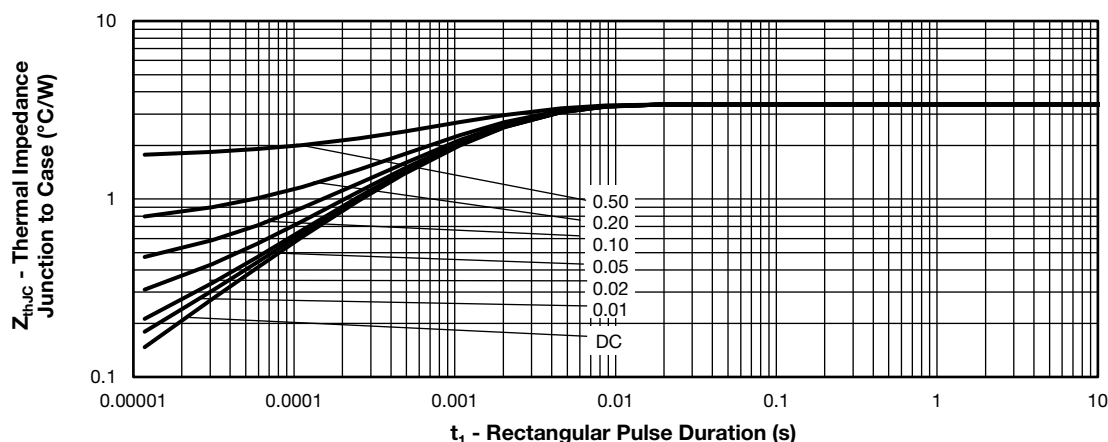


Fig. 4 - Maximum Transient Thermal Impedance, Junction to Mount, per Leg

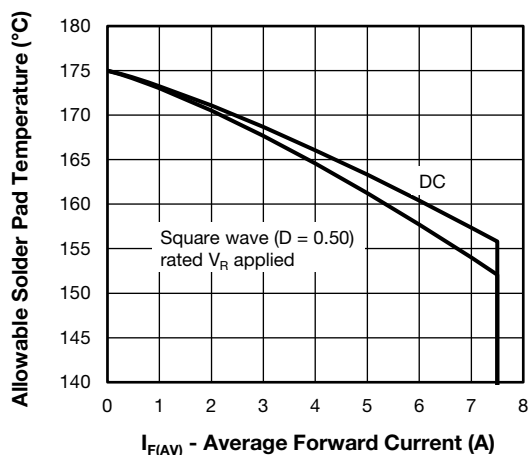


Fig. 5 - Maximum Allowable Mount Temperature vs. Average Forward Current, per Leg

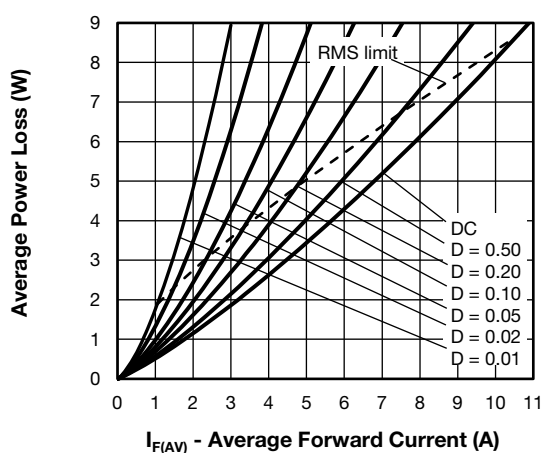


Fig. 6 - Forward Power Loss Characteristics, per Leg

Note

Formula used: $T_M = T_J - (P_d + P_{dREV}) \times R_{thJM}$;
 P_d = forward power loss = $I_{F(AV)} \times V_{FM}$ at $(I_{F(AV)}/D)$ (see fig. 5);
 P_{dREV} = inverse power loss = $V_{R1} \times I_R (1 - D)$; I_R at V_{R1} = rated V_R

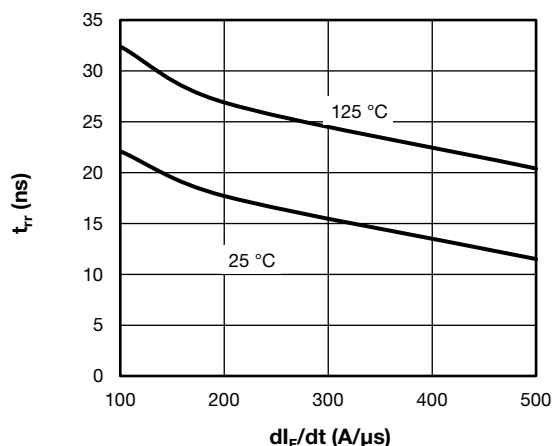
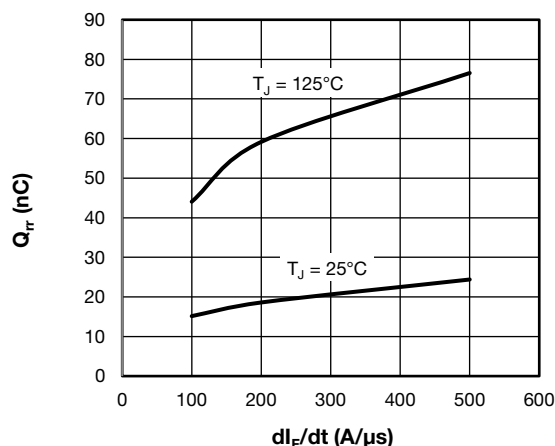
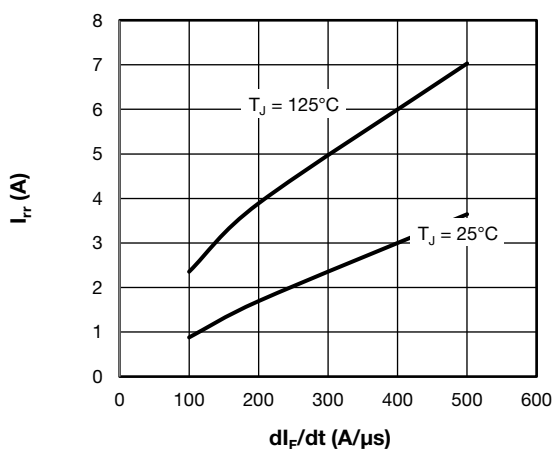
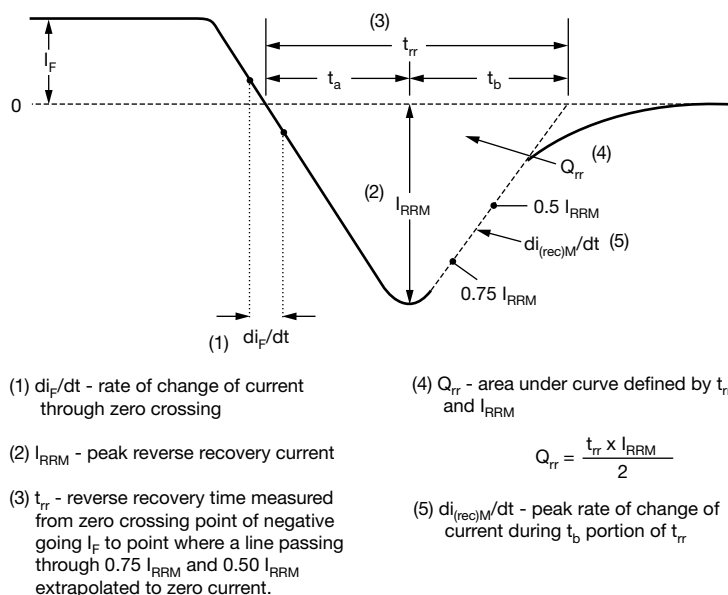

Fig. 7 - Typical Reverse Recovery Time vs. di_F/dt , per Leg

Fig. 8 - Typical Stored Charge vs. di_F/dt , per Leg

Fig. 9 - I_{rr} vs. di/dt , per Leg


Fig. 10 - Reverse Recovery Waveform and Definitions

ORDERING INFORMATION TABLE

Device code

VS-	15	C	R	H	02	H	M3
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1 2 3 4 5 6 7 8

- 1 - Vishay Semiconductors product
- 2 - Current rating (15 = 15 A)
- 3 - Circuit configuration:
C = common cathode
- 4 - R = DFN6546A package
- 5 - Process type,
H = ultrafast recovery
- 6 - Voltage code (02 = 200 V)
- 7 - H = AEC-Q101 qualified
- 8 - M3 = halogen-free, RoHS-compliant, and terminations lead (Pb)-free

ORDERING INFORMATION (Example)

PREFERRED P/N	PREFERRED PACKAGE CODE	BASE QUANTITY	PACKAGING DESCRIPTION
VS-15CRH02HM3/I	I	6000	13" diameter plastic tape and reel

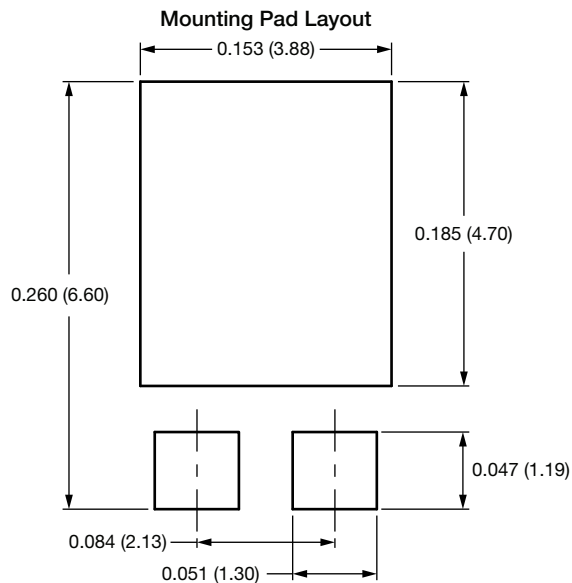
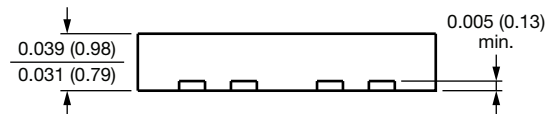
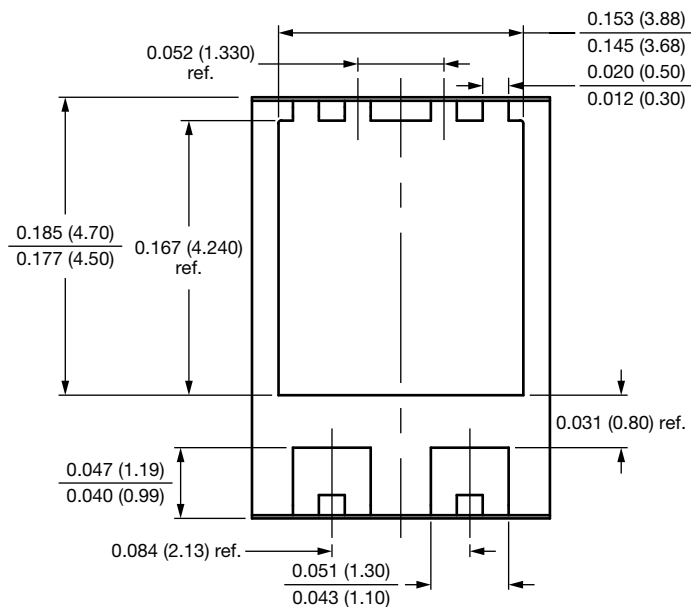
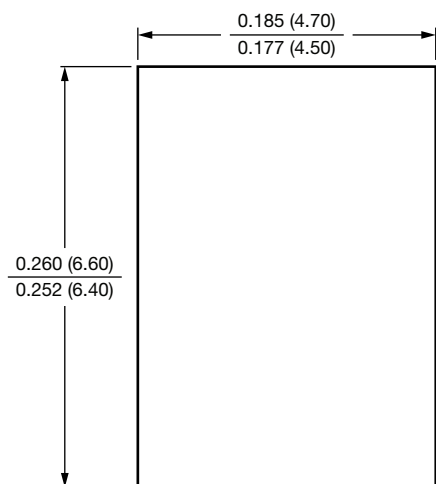
LINKS TO RELATED DOCUMENTS

Dimensions	www.vishay.com/doc?97347
Part marking information	www.vishay.com/doc?97348
Packaging information	www.vishay.com/doc?98691



DFN6546A, FRED Pt®

DIMENSIONS in inches (millimeters)





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