

Evaluating the ADM2582E/ADM2587E

FEATURES

- Power and signal isolated RS-485/RS422 transceiver**
- Convenient connections for power and signal through screw terminal blocks**
- Configurable as half-duplex or full-duplex**
- 5 V or 3.3 V operation**
- Easily configurable through jumper connections**
- Test points for measuring all signals**
- Layout optimized for emissions according to the AN-0971 Application Note**
- Passes the EN55022(2001) Class B emissions standard**

GENERAL DESCRIPTION

The [ADM2582E/ADM2587E](#) evaluation board can be used for easy evaluation of the ADM2582E and ADM2587E power and signal isolated RS-485 transceivers. Screw terminal blocks give convenient connections for the power and signal connections.

The board can be easily configured by jumper connections. The board is configurable as half-duplex or full-duplex and has a 120 Ω termination resistor fitted on the receiver input. The evaluation board can be used with both the ADM2582E 16 Mbps part and the ADM2587E 500 kbps part. The driver and receiver can be enabled and disabled by jumper connections. Test points are included on the power and signal lines on both sides of the isolation barrier.

RADIATED EMISSIONS

The ADM2582E/ADM2587E evaluation board is designed to reduce emissions generated by the high frequency switching elements used by the *isoPower* technology to transfer power through its transformer. Guidelines mentioned in the [AN-0971 Application Note](#) were used to generate the layout. The emissions of the evaluation board were measured by an independent test facility and passed the EN55022(2001) Class B emissions standard.

EVALUATION BOARD

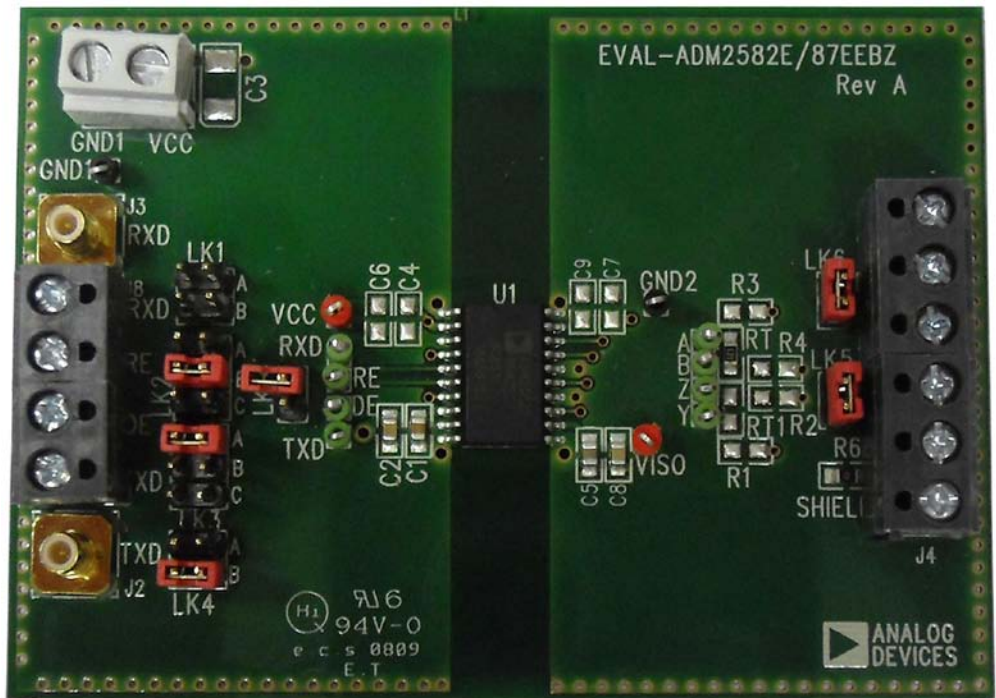


Figure 1.

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REVISION HISTORY

11/09—Revision 0: Initial Version

EVALUATION BOARD SCHEMATICS

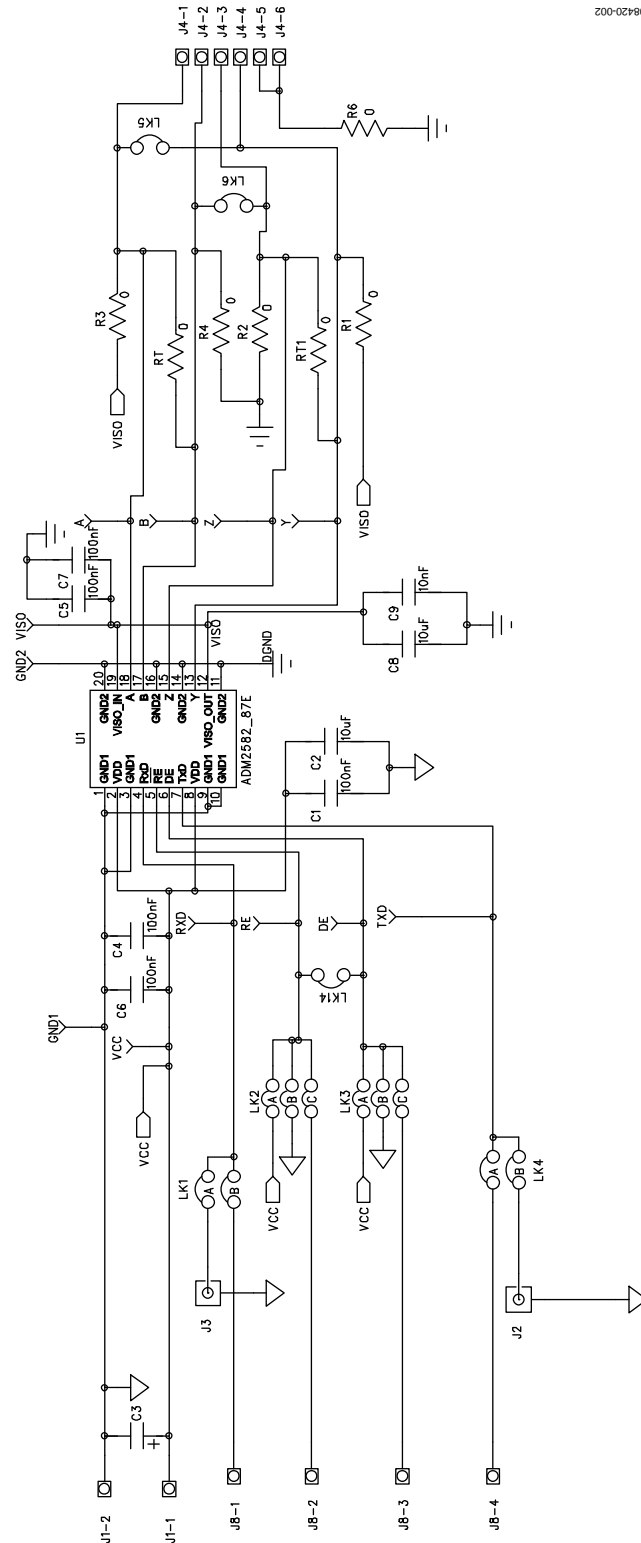


Figure 2. Schematic of the ADM2582E/ADM2587E Evaluation Board

ASSEMBLY DRAWINGS AND BOARD LAYOUT

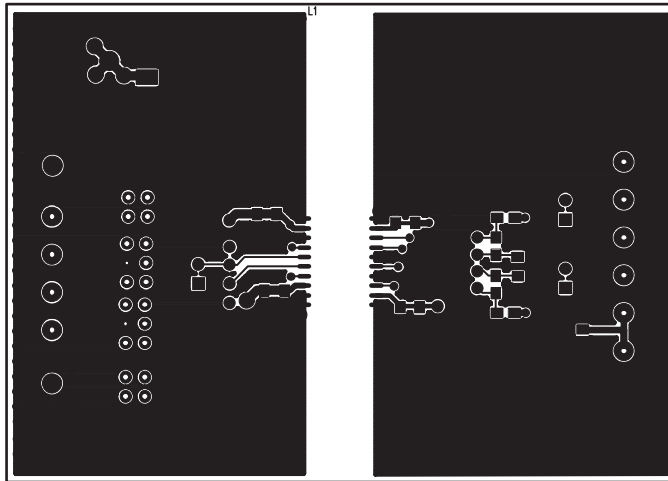


Figure 3. Top Layer

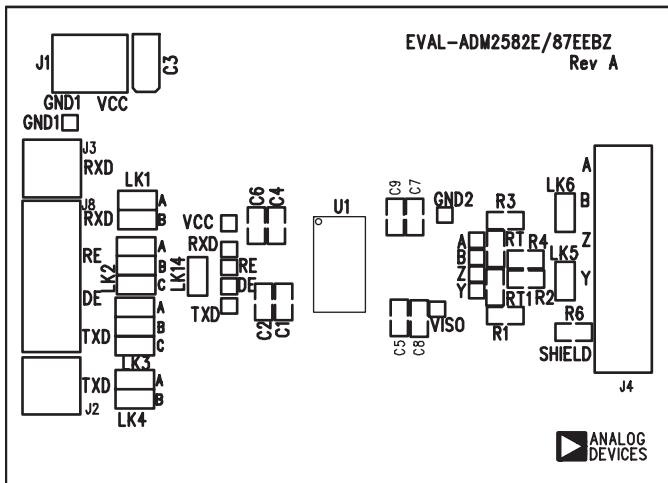


Figure 4. Silkscreen

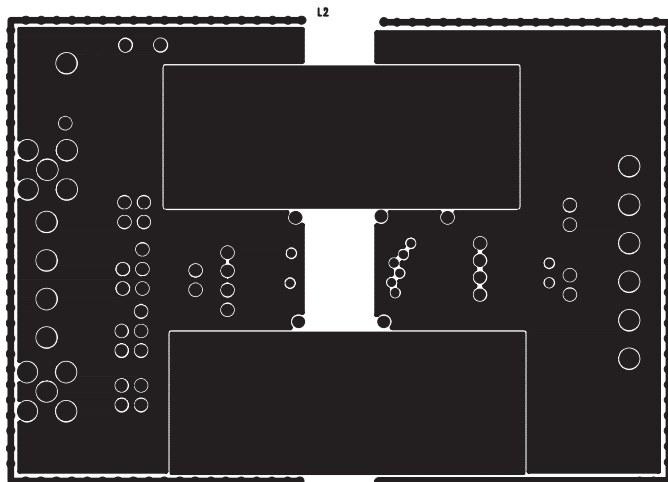


Figure 5. Internal Layer 2

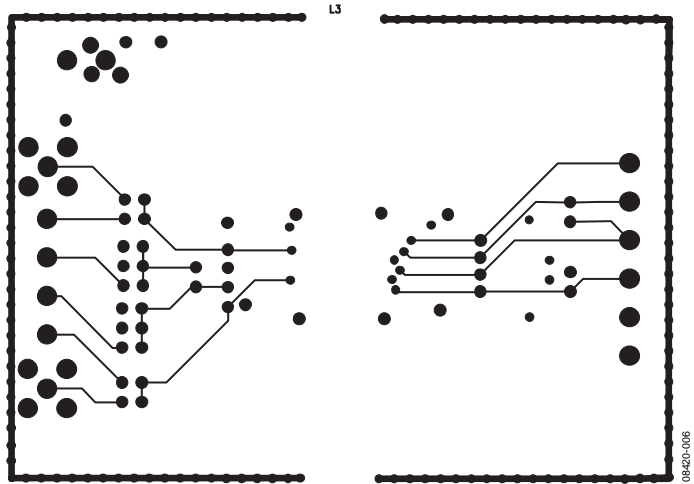


Figure 6. Internal Layer 3

08420-006

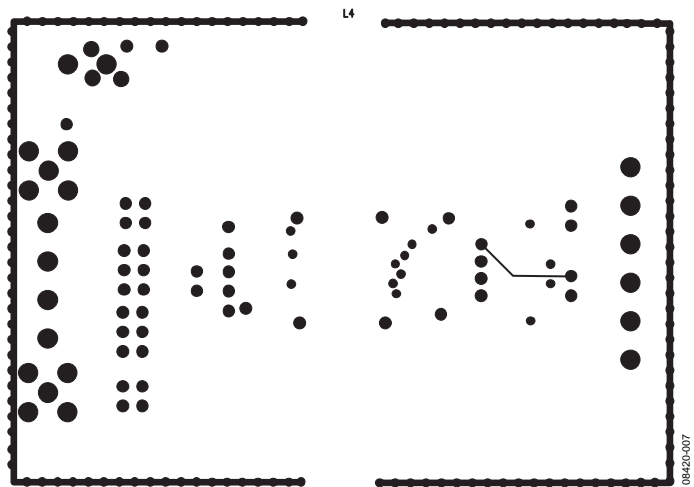


Figure 7. Internal Layer 4

08420-007

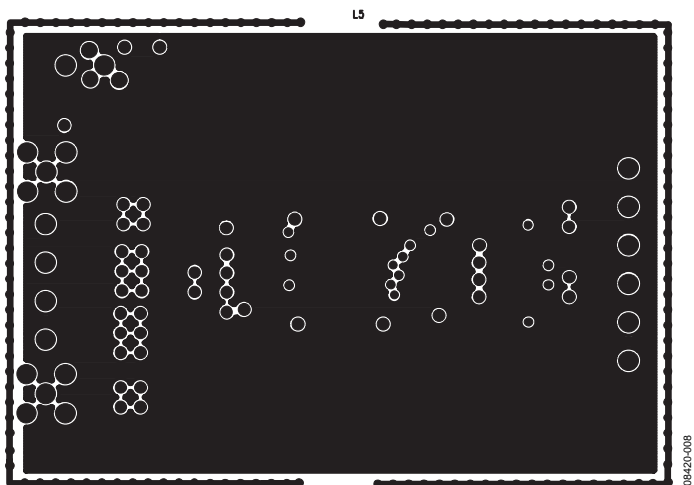


Figure 8. Internal Layer 5

08420-008

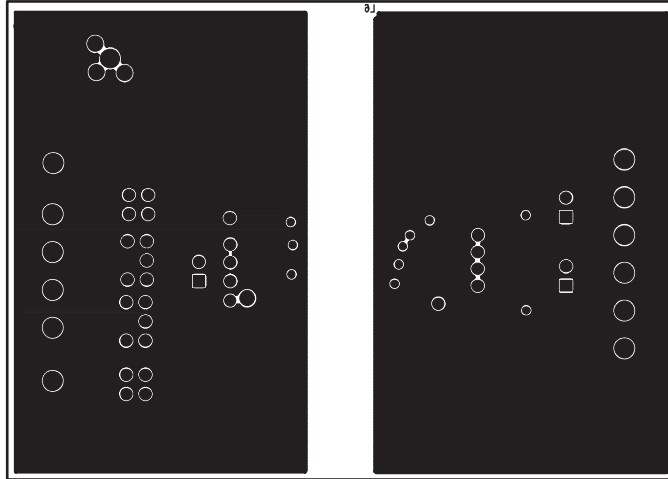





















Figure 9. Bottom Solder Layer

HARDWARE CONFIGURATION

EVALUATION BOARD JUMPER SETTINGS

Table 1.

Link	Connection	Description	Image
LK1	A	Connects the receiver output (RxD) of the ADM2582E/ADM2587E to the J3 connector.	 A ○ ○ B
LK1	B	Connects the receiver output (RxD) of the ADM2582E/ADM2587E to the J8-1 terminal block connector.	 ○ ○ A  ○ ○ B
LK2	A	Connects the receiver enable input (\overline{RE}) of the ADM2582E/ADM2587E to V_{CC} . This disables the receiver.	 ○ ○ A ○ ○ B ○ ○ C
LK2	B	Connects the receiver enable input (\overline{RE}) of the ADM2582E/ADM2587E to GND_1 . This enables the receiver.	 ○ ○ A  ○ ○ B ○ ○ C
LK2	C	Connects the receiver enable input (\overline{RE}) of the ADM2582E/ADM2587E to the J8-2 terminal block connector.	 ○ ○ A ○ ○ B  ○ ○ C
LK3	A	Connects the driver enable input (DE) of the ADM2582E/ADM2587E to V_{CC} . This enables the driver.	 ○ ○ A ○ ○ B ○ ○ C
LK3	B	Connects the driver enable input (DE) of the ADM2582E/ADM2587E to GND_1 . This disables the driver.	 ○ ○ A  ○ ○ B ○ ○ C
LK3	C	Connects the driver enable input (DE) of the ADM2582E/ADM2587E to the J8-3 terminal block connector.	 ○ ○ A ○ ○ B  ○ ○ C
LK4	A	Connects the receiver output (RxD) of the ADM2582E/ADM2587E to the J8-4 connector.	 ○ ○ A ○ ○ B
LK4	B	Connects the receiver output (RxD) of the ADM2582E/ADM2587E to the J2 terminal block connector.	 ○ ○ A  ○ ○ B
LK5	Connected	Connects the ADM2582E/ADM2587E Receiver Input B to Driver Output Z. When LK5 and LK6 are both connected, the evaluation board is connected in a half-duplex configuration.	 ○ ○ LK5
LK5	Open	When LK5 and LK6 are both open, the evaluation board is connected in a full-duplex configuration.	○ ○ LK5
LK6	Connected	Connects the ADM2582E/ADM2587E Receiver Input A to Driver Output Y. When LK5 and LK6 are both connected, the evaluation board is connected in a half-duplex configuration.	 ○ ○ LK6
LK6	Open	When LK5 and LK6 are both open, the evaluation board is connected in a full-duplex configuration.	○ ○ LK6
LK14	Connected	Connects the driver enable input (DE) of the ADM2582E/ADM2587E to the receiver enable input (\overline{RE}) of the ADM2582E/ADM2587E . This ensures that, when the driver is enabled, the receiver is disabled or that, when the driver is disabled, the receiver is enabled.	 ○ ○ LK14
LK14	Open	Disconnects the driver enable input (DE) of the ADM2582E/ADM2587E from the receiver input enable (\overline{RE}) of the ADM2582E/ADM2587E .	○ ○ LK14

DECOUPLING AND RESERVOIR CAPACITORS

On the logic side of the board, the C4 and C6 capacitors should be 10 μ F and 100 nF ceramic capacitors, and the C2 and C1 capacitors should be 100 nF and 10 nF ceramic capacitors. On the bus side of the board, the C5 and C8 capacitors should be 100 nF and 10 μ F, and the C9 and C7 capacitors should be 10 nF and 100 nF.

BOARD INTERNAL LAYER THICKNESS

The [ADM2582E/ADM2587E](#) evaluation board consists of six internal layers. The spacing between the internal board layers was chosen to maximize the stitching capacitance on the board.

Table 2.

Layers	Thickness (mm) of Space Between Layers
1 to 2	0.1016
2 to 3	0.2032
3 to 4	0.2032
4 to 5	0.2032
5 to 6	0.1016

ESD CAUTION



ESD (electrostatic discharge) sensitive device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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