CY62148ESL MoBL®

4-Mbit (512 K × 8) Static RAM

Features

- Higher speed up to 55 ns
- Wide voltage range: 2.2 V to 3.6 V and 4.5 V to 5.5 V
- Ultra low standby power
  - Typical standby current: 1 µA
  - Maximum standby current: 7 µA
- Ultra low active power
  - Typical active current: 2 mA at f = 1 MHz
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ features
- Automatic power-down when deselected
- Complementary metal oxide semiconductor (CMOS) for optimum speed and power
- Available in Pb-free 32-pin shrunk thin small outline package (STSOP) package

Functional Description

The CY62148ESL is a high performance CMOS static RAM organized as 512 K words by 8-bits. This device features advanced circuit design to provide ultra low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications. The device also has an automatic power-down feature that significantly reduces power consumption. Placing the device in standby mode reduces power consumption by more than 99 percent when deselected ($\overline{CE}$ HIGH). The eight input and output pins (I/O_0 through I/O_7) are placed in a high impedance state when the device is deselected ($\overline{CE}$ HIGH), the outputs are disabled ($\overline{OE}$ HIGH), or during a write operation ($\overline{CE}$ LOW and $\overline{WE}$ LOW).

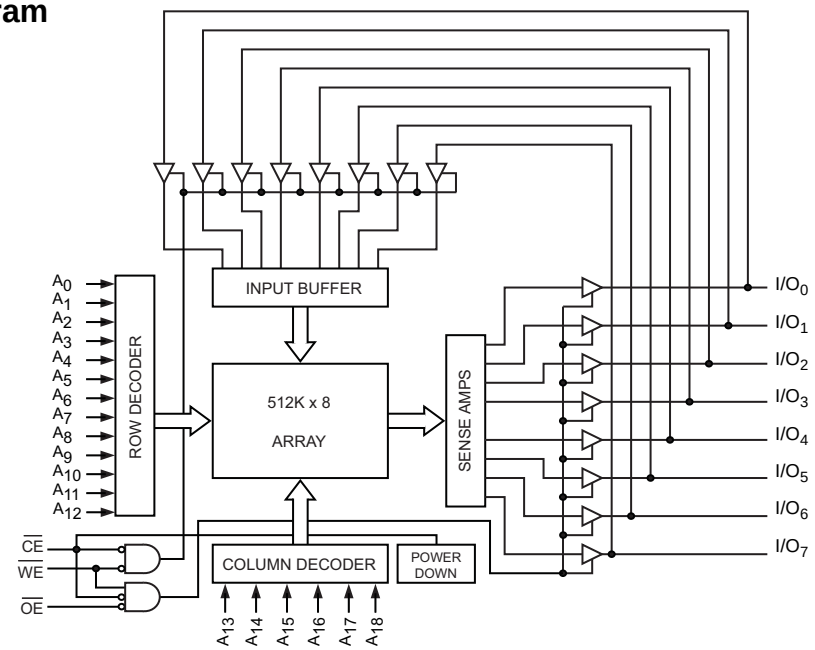
To write to the device, take Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs LOW. Data on the eight I/O pins (I/O_0 through I/O_7) is then written into the location specified on the address pins (A_0 through A_{18}).

To read from the device, take Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) LOW while forcing Write Enable ($\overline{WE}$) HIGH. Under these conditions, the contents of the memory location specified by the address pins appear on the I/O pins.

The CY62148ESL device is suitable for interfacing with processors that have TTL I/P levels. It is not suitable for processors that require CMOS I/P levels. Please see Electrical Characteristics on page 4 for more details and suggested alternatives.

For a complete list of related resources, click here.

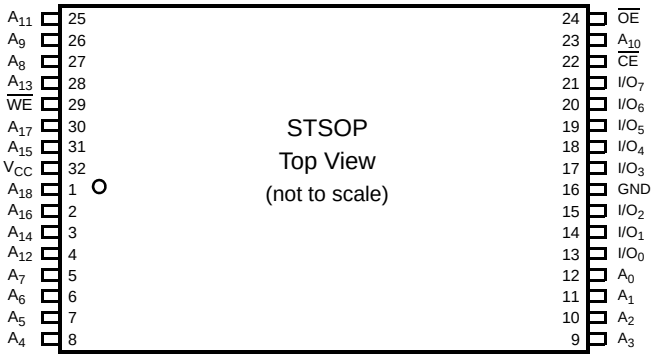
Logic Block Diagram



Contents

Pin Configuration

Figure 1. 32-pin STSOP (Top View) pinout



Product Portfolio

Product	Range	V_{CC} Range (V) [1]	Speed (ns)	Power Dissipation					
				Operating I_{CC}, (mA)				Standby, I_{SB2} (µA)	
				f = 1 MHz		f = f_{max}			
				Typ [2]	Max	Typ [2]	Max	Typ [2]	Max
CY62148ESL	Industrial / Automotive-A	2.2 V to 3.6 V and 4.5 V to 5.5 V	55	2	2.5	15	20	1	7

Notes
1. Data sheet specifications are not guaranteed for V_{CC} in the range of 3.6 V to 4.5 V.
2. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, T_A = 25 °C.

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature .....–65 °C to +150 °C

Ambient temperature with power applied ...55 °C to +125 °C

Supply voltage to ground potential .....–0.5 V to 6.0 V

DC voltage applied to outputs in high Z state [3, 4] .....–0.5 V to 6.0 V

DC input voltage [3, 4] .....–0.5 V to 6.0 V

Output current into outputs (low) .....20 mA

Static discharge voltage (MIL-STD-883, Method 3015) .....> 2001 V

Latch-up current .....> 200 mA

Operating Range

Device	Range	Ambient Temperature	V_{CC}[5]
CY62148ESL	Industrial / Automotive-A	–40 °C to +85 °C	2.2 V to 3.6 V, and 4.5 V to 5.5 V

Electrical Characteristics

Over the operating range

Parameter	Description	Test Conditions		55 ns (Industrial/Automotive-A)			Unit
				Min	Typ [6]	Max	
V_{OH}	Output HIGH voltage	$2.2 \le V_{CC} \le 2.7$	I_{OH} = –0.1 mA	2.0	–	–	V
		$2.7 \le V_{CC} \le 3.6$	I_{OH} = –1.0 mA	2.4	–	–	
		$4.5 \le V_{CC} \le 5.5$	I_{OH} = –1.0 mA	2.4	–	–	
		$4.5 \le V_{CC} \le 5.5$	I_{OH} = –0.1 mA	–	–	3.4 [7]	
V_{OL}	Output LOW voltage	$2.2 \le V_{CC} \le 2.7$	I_{OL} = 0.1 mA	–	–	0.4	V
		$2.7 \le V_{CC} \le 3.6$	I_{OL} = 2.1 mA	–	–	0.4	
		$4.5 \le V_{CC} \le 5.5$	I_{OL} = 2.1 mA	–	–	0.4	
V_{IH}	Input HIGH voltage	$2.2 \le V_{CC} \le 2.7$		1.8	–	V_{CC} + 0.3	V
		$2.7 \le V_{CC} \le 3.6$		2.2	–	V_{CC} + 0.3	
		$4.5 \le V_{CC} \le 5.5$		2.2	–	V_{CC} + 0.5	
V_{IL} [8]	Input LOW voltage	$2.2 \le V_{CC} \le 2.7$		–0.3	–	0.4	V
		$2.7 \le V_{CC} \le 3.6$		–0.3	–	0.6	
		$4.5 \le V_{CC} \le 5.5$		–0.5	–	0.6	
I_{IX}	Input leakage current	$GND \le V_{IN} \le V_{CC}$		–1	–	+1	µA
I_{OZ}	Output leakage current	$GND \le V_O \le V_{CC}$, output disabled		–1	–	+1	µA
I_{CC}	V_{CC} operating supply current	f = f_{max} = $1/t_{RC}$	V_{CC} = V_{CCmax} I_{OUT} = 0 mA, CMOS levels	–	15	20	mA
		f = 1 MHz		–	2	2.5	
I_{SB1}[9]	Automatic CE power-down current – CMOS inputs	$\overline{CE} \ge V_{CC}$ – 0.2 V, $V_{IN} \ge V_{CC}$ – 0.2 V or $V_{IN} \le$ 0.2 V, f = f_{max} (address and data only), f = 0 ($\overline{OE}$ and $\overline{WE}$), V_{CC} = $V_{CC(max)}$		–	1	7	µA
				–			
I_{SB2}[9]	Automatic CE power-down current – CMOS inputs	$\overline{CE} \ge V_{CC}$ – 0.2 V, $V_{IN} \ge V_{CC}$ – 0.2 V or $V_{IN} \le$ 0.2 V, f = 0, V_{CC} = $V_{CC(max)}$		–	1	7	µA
				–			

Notes

3. $V_{IL(min)}$ = –2.0 V for pulse durations less than 20 ns.
4. $V_{IH(max)}$ = V_{CC} + 0.75 V for pulse durations less than 20 ns.
5. Full device AC operation assumes a minimum of 100 µs ramp time from 0 to $V_{CC(min)}$ and 200 µs wait time after V_{CC} stabilization.
6. Typical values are included for reference and are not guaranteed or tested. Typical values are measured at V_{CC} = $V_{CC(typ)}$, T_A = 25 °C.
7. Please note that the maximum VOH limit does not exceed minimum CMOS VIH of 3.5 V. If you are interfacing this SRAM with 5 V legacy processors that require a minimum VIH of 3.5 V, please refer to Application Note AN6081 for technical details and options you may consider
8. Under DC conditions the device meets a V_{IL} of 0.8 V (for V_{CC} range of 2.7 V to 3.6 V and 4.5 V to 5.5 V) and 0.6 V (for V_{CC} range of 2.2 V to 2.7 V). However, in dynamic conditions Input LOW voltage applied to the device must not be higher than 0.6 V and 0.4 V for the above ranges.
9. Chip enable ($\overline{CE}$) must be HIGH at CMOS level to meet the I_{SB1} / I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.

Capacitance

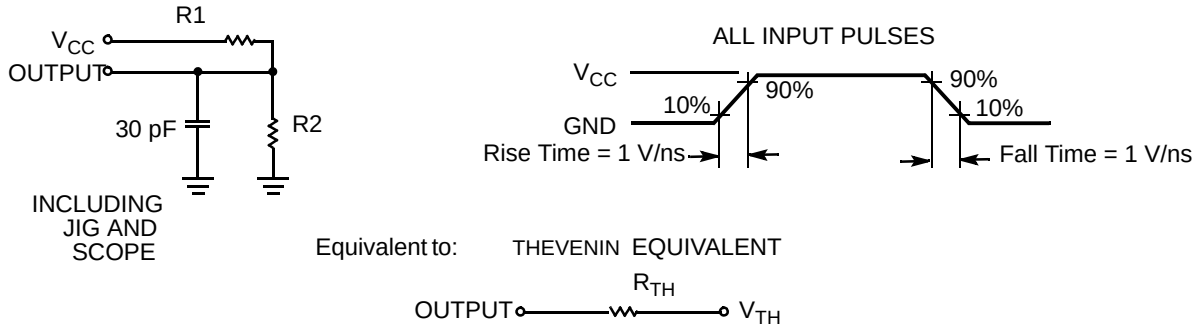
Parameter [10]	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{CC} = $V_{CC(Typ)}$	10	pF
C_{OUT}	Output capacitance		10	pF

Thermal Resistance

Parameter [10]	Description	Test Conditions	32-pin STSOP	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 inch, two-layer printed circuit board	49.02	°C/W
Θ_{JC}	Thermal resistance (junction to case)		14.07	°C/W

AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms



Parameter	2.5 V	3.0 V	5.0 V	Unit
R1	16667	1103	1800	Ω
R2	15385	1554	990	Ω
R_{TH}	8000	645	639	Ω
V_{TH}	1.20	1.75	1.77	V

Note
10. Tested initially and after any design or process changes that may affect these parameters.

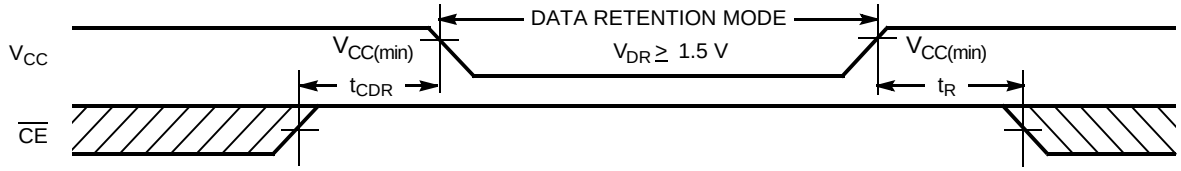
Data Retention Characteristics

Over the operating range

Parameter	Description	Conditions		Min	Typ [11]	Max	Unit
V_{DR}	V_{CC} for data retention			1.5	–	–	V
I_{CCDR} [12]	Data retention current	$\overline{CE} \geq V_{CC} - 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V, $V_{CC} = 1.5$ V	Industrial / Automotive-A	–	1	7	µA
t_{CDR}	Chip deselect to data retention time			0	–	–	ns
t_R [13]	Operation recovery time			55	–	–	ns

Data Retention Waveform

Figure 3. Data Retention Waveform



Notes
11. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, $T_A = 25$ °C.
12. Chip enable ($\overline{CE}$) must be HIGH at CMOS level to meet the I_{SB1} / I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.
13. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)} \geq 100$ µs or stable at $V_{CC(min)} \geq 100$ µs.

Switching Characteristics

Over the operating range

Parameter [14, 15]	Description	55 ns (Industrial / Automotive-A)		Unit
		Min	Max	
Read Cycle				
t_{RC}	Read cycle time	55	–	ns
t_{AA}	Address to data valid	–	55	ns
t_{OHA}	Data hold from address change	10	–	ns
t_{ACE}	$\overline{CE}$ LOW to data valid	–	55	ns
t_{DOE}	$\overline{OE}$ LOW to data valid	–	25	ns
t_{LZOE}	$\overline{OE}$ LOW to low Z [16]	5	–	ns
t_{HZOE}	$\overline{OE}$ HIGH to high Z [16, 17]	–	20	ns
t_{LZCE}	$\overline{CE}$ LOW to low Z [16]	10	–	ns
t_{HZCE}	$\overline{CE}$ HIGH to high Z [16, 17]	–	20	ns
t_{PU}	$\overline{CE}$ LOW to power-up	0	–	ns
t_{PD}	$\overline{CE}$ HIGH to power-up	–	55	ns
Write Cycle [18, 19]				
t_{WC}	Write cycle time	55	–	ns
t_{SCE}	$\overline{CE}$ LOW to write end	40	–	ns
t_{AW}	Address setup to write end	40	–	ns
t_{HA}	Address hold from write end	0	–	ns
t_{SA}	Address setup to write start	0	–	ns
t_{PWE}	$\overline{WE}$ pulse width	40	–	ns
t_{SD}	Data setup to write end	25	–	ns
t_{HD}	Data hold from write end	0	–	ns
t_{HZWE}	$\overline{WE}$ LOW to high Z [16, 17]	–	20	ns
t_{LZWE}	$\overline{WE}$ HIGH to low Z [16]	10	–	ns

Notes

14. In an earlier revision of this device, under a specific application condition, READ and WRITE operations were limited to switching of the chip enable signal as described in the Application Note AN66311. However, the issue has been fixed and in production now, and hence, this Application Notes is no longer applicable. It is available for download on our website as it contains information on the date code of the parts, beyond which the fix has been in production.
15. Test conditions for all parameters other than tri-state parameters assume signal transition time of 3 ns or less (1 V/ns), timing reference levels of $V_{CC(typ)}/2$, input pulse levels of 0 to $V_{CC(typ)}$, and output loading of the specified I_{OL}/I_{OH} as shown in Figure 2 on page 5.
16. At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any device.
17. t_{HZOE}, t_{HZCE}, and t_{HZWE} transitions are measured when the output enter a high impedance state.
18. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}$ = V_{IL}. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.
19. The minimum write cycle pulse width for Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) should be equal to the sum of t_{SD} and t_{HZWE}.

Switching Waveforms

Figure 4. Read Cycle No. 1 (Address Transition Controlled) [20, 21]

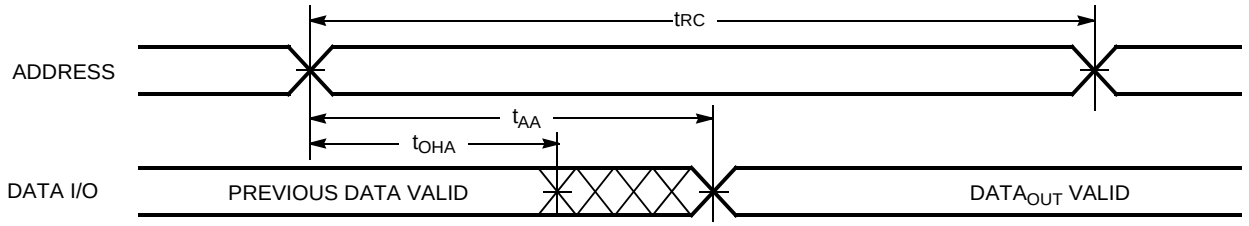
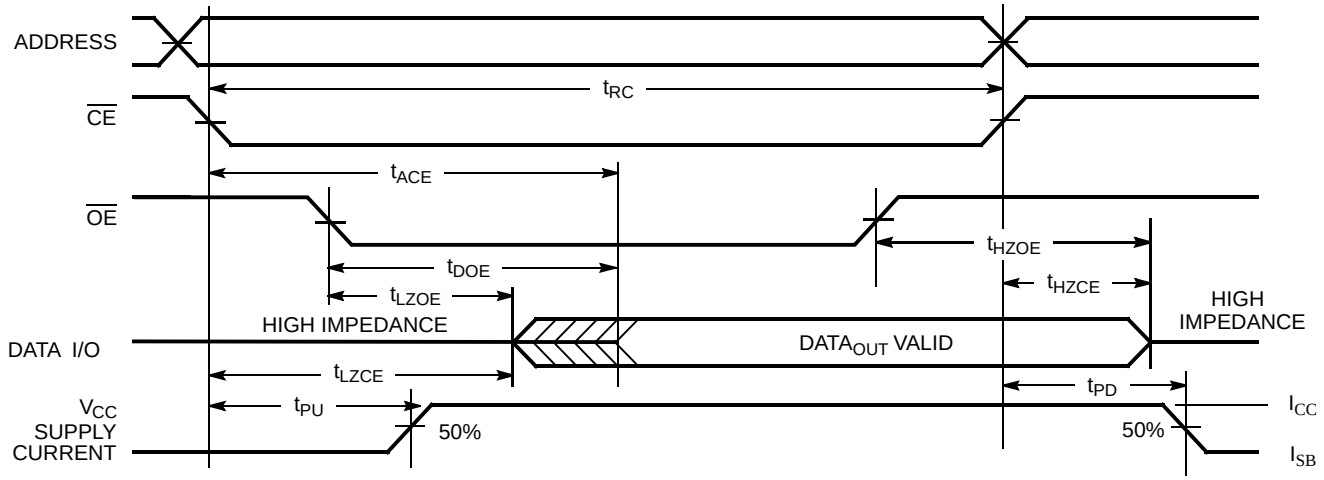


Figure 5. Read Cycle No. 2 ($\overline{OE}$ Controlled) [21, 22]



Notes
20. Device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}.
21. $\overline{WE}$ is HIGH for read cycles.
22. Address valid before or similar to $\overline{CE}$ transition LOW.
23. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.
24. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in high impedance state.
25. During this period, the I/Os are in output state. Do not apply input signals.

Switching Waveforms (continued)

Figure 6. Write Cycle No. 1 (CE Controlled) [26, 27]

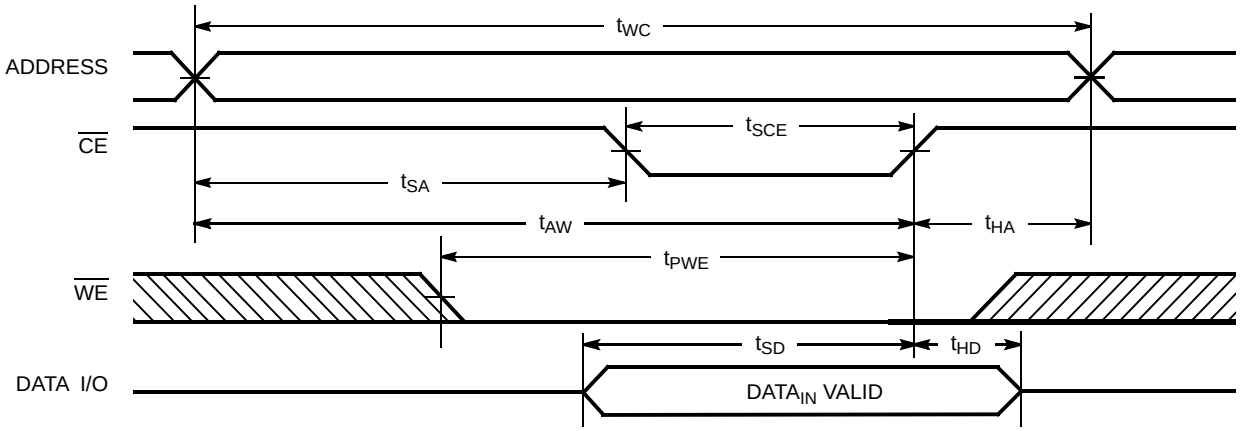
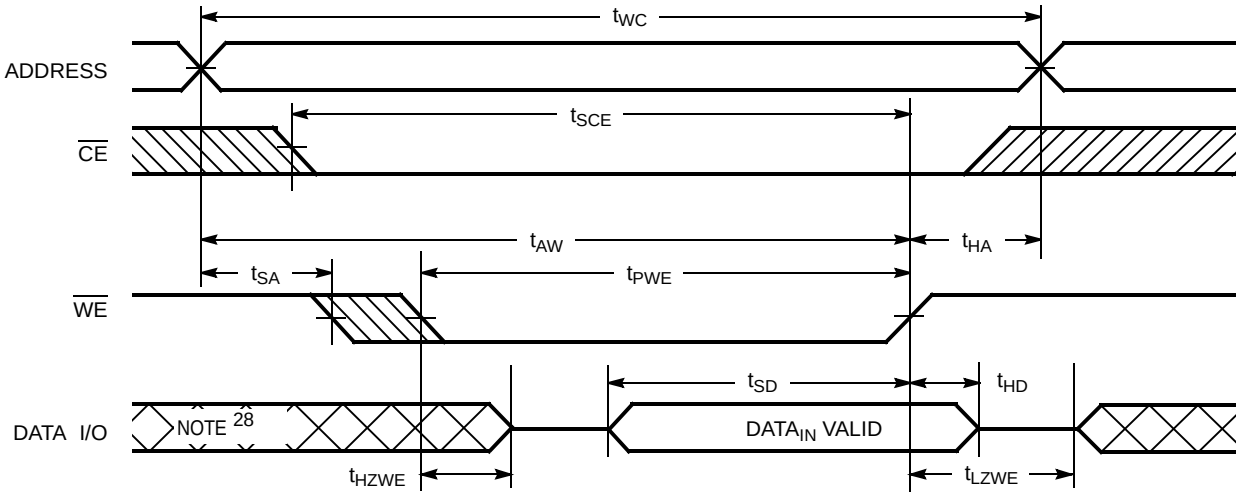


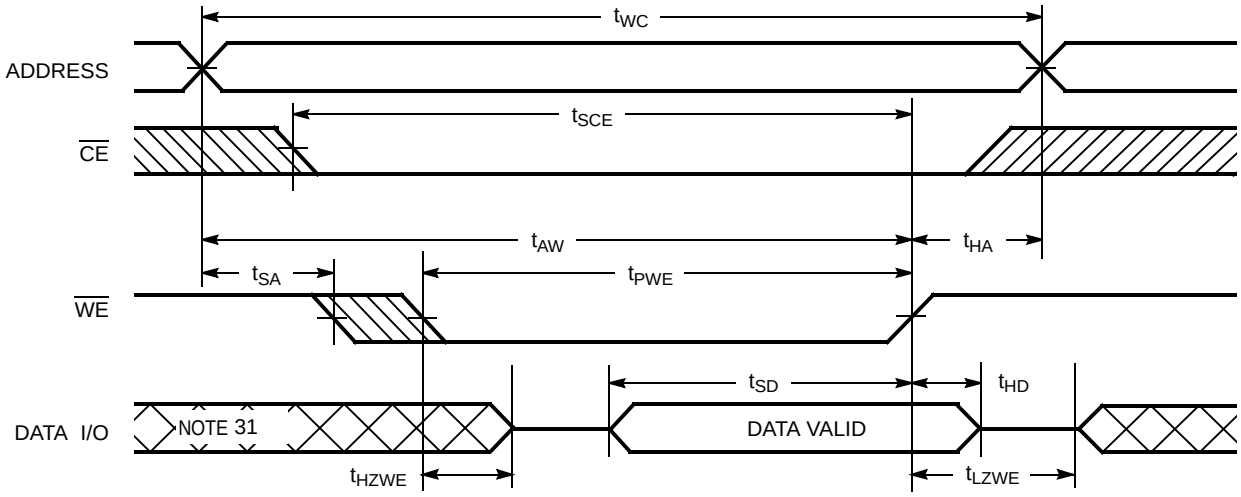
Figure 7. Write Cycle No. 2 (WE Controlled) [27]



Notes
26. Data I/O is high impedance if $\overline{OE} = V_{IH}$.
27. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in high impedance state.
28. During this period, the I/Os are in output state. Do not apply input signals.

Switching Waveforms (continued)

Figure 8. Write Cycle No. 3 (WE Controlled, OE LOW) [29, 30]



Notes
29. If CE goes HIGH simultaneously with WE HIGH, the output remains in high impedance state.
30. The minimum write cycle pulse width should be equal to the sum of t_{SD} and t_{HZWE}.
31. During this period, the I/Os are in output state. Do not apply input signals.

Truth Table

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	I/O	Mode	Power
H [32]	X	X	High Z	Deselect/power-down	Standby (I_{SB})
L	H	L	Data out	Read	Active (I_{CC})
L	H	H	High Z	Output disabled	Active (I_{CC})
L	L	X	Data in	Write	Active (I_{CC})

Note
32. Chip enable ($\overline{CE}$) must be HIGH at CMOS level to meet the I_{SB1}/ I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.

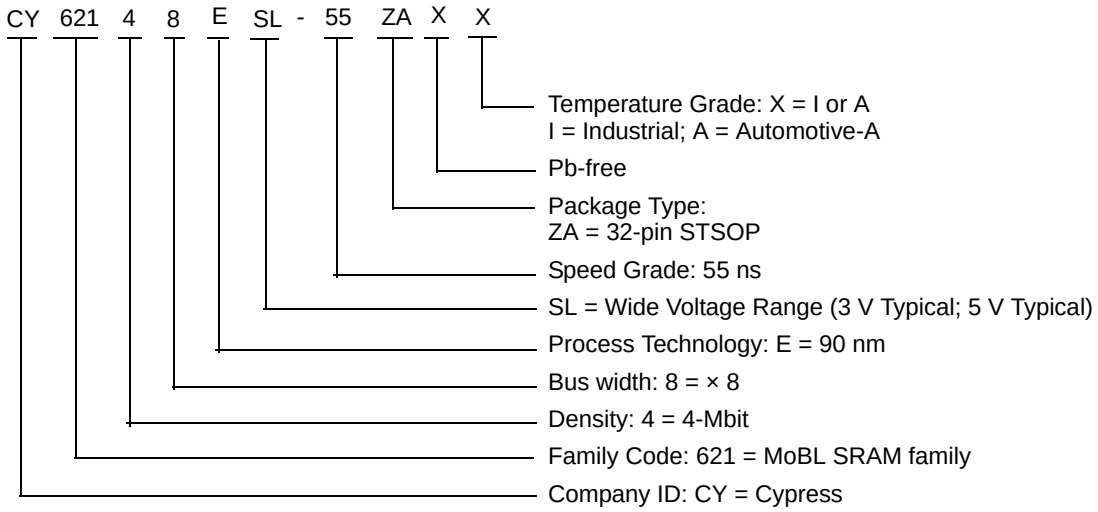
Ordering Information

Table 1 lists the CY62148ESL MoBL® key package features and ordering codes. The table contains only the parts that are currently available. If you do not see what you are looking for, contact your local sales representative. For more information, visit the Cypress website at www.cypress.com and refer to the product summary page at http://www.cypress.com/products.

Table 1. Key features and Ordering Information

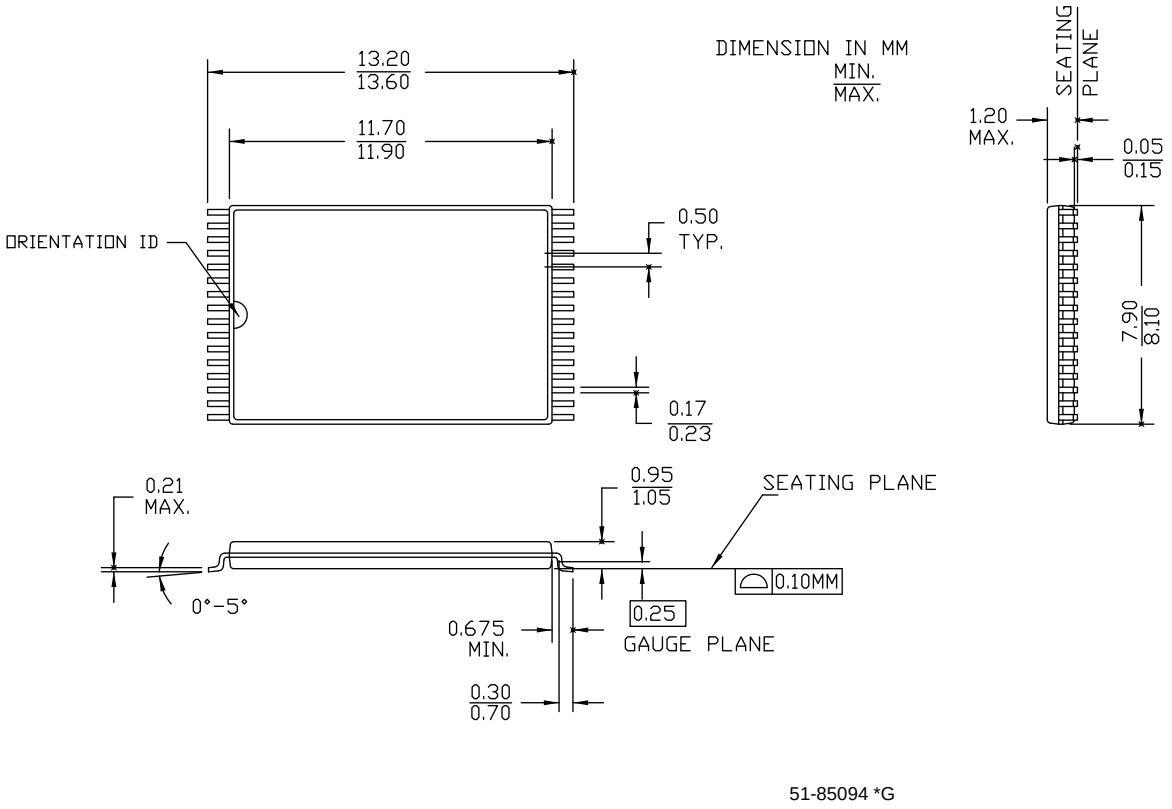
Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
55	CY62148ESL-55ZAXI	51-85094	32-pin STSOP (Pb-free)	Industrial
	CY62148ESL-55ZAXA	51-85094	32-pin STSOP (Pb-free)	Automotive-A

Ordering Code Definitions



Package Diagram

Figure 9. 32-pin STSOP (8 × 13.4 × 1.2 mm) ZA32 Package Outline, 51-85094



51-85094 *G

Acronyms

Acronym	Description
$\overline{BHE}$	Byte High Enable
$\overline{BLE}$	Byte Low Enable
$\overline{CE}$	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input/Output
$\overline{OE}$	Output Enable
SRAM	Static Random Access Memory
TSOP	Thin Small Outline Package
$\overline{WE}$	Write Enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
µA	microampere
mA	milliampere
ns	nanosecond
Ω	ohm
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY62148ESL MoBL®, 4-Mbit (512 K × 8) Static RAM Document Number: 001-50045				
Rev.	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	2612938	VKN / PYRS	01/21/09	New data sheet.
*A	2800124	VKN	11/06/2009	Updated Product Portfolio (Included Automotive-A information). Updated Operating Range (Included Automotive-A information). Updated Ordering Information (Updated part numbers (Included Automotive-A information)).
*B	2947039	VKN	06/10/2010	Updated Electrical Characteristics (Added Note 9 and referred the same note in I_{SB2} parameter). Updated Truth Table (Added Note 32 and referred the same note in $\overline{CE}$ column). Updated Package Diagram.
*C	3006318	AJU	08/23/2010	Updated Electrical Characteristics (Updated Note 9 and referred the same note in I_{SB1} parameter). Updated Data Retention Characteristics (Added Note 12 and referred the same note in I_{CCDR} parameter). Added Ordering Code Definitions. Added Acronyms and Units of Measure. Updated in new template.
*D	3296704	RAME	06/29/2011	Updated Functional Description (Removed “For best practice recommendations, refer to the Cypress application note AN1064, SRAM System Guidelines.”). Updated Ordering Code Definitions. Updated Package Diagram to latest revision.
*E	3515577	TAVA	02/03/2012	Updated Switching Waveforms.
*F	3548240	TAVA	03/12/2012	Updated Electrical Characteristics (Updated Note 8 (Removed “Refer to AN13470 for details.”).
*G	3897076	MEMJ	02/06/2013	Updated Switching Waveforms: Removed figure “Write Cycle No. 1 ($\overline{WE}$ Controlled, $\overline{OE}$ HIGH During Write)”. Updated title of Figure 7.
*H	4039358	MEMJ	07/01/2013	Updated Functional Description. Updated Electrical Characteristics: Added one more Test Condition “$4.5 \le V_{CC} \le 5.5$” for V_{OH} parameter and added maximum value corresponding to that Test Condition. Added Note 7 and referred the same note in maximum value for V_{OH} parameter corresponding to Test Condition “$4.5 \le V_{CC} \le 5.5$”. Updated to new template.
*I	4099182	VINI	08/19/2013	Updated Switching Characteristics: Added Note 14 and referred the same note in “Parameter” column.
*J	4779516	MEMJ	05/28/2015	Updated Functional Description: Added “For a complete list of related resources, click here.” at the end. Updated AC Test Loads and Waveforms: Updated Figure 2. Updated Switching Characteristics: Added Note 19 and referred the same note in “Write Cycle”. Updated Switching Waveforms: Added Figure 8. Added Note 29, 30, 31 and referred the same note in Figure 8. Updated Package Diagram: spec 51-85094 – Changed revision from *F to *G. Updated to new template.

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