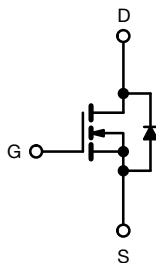
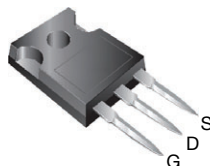


## E Series Power MOSFET

**TO-247AC**


N-Channel MOSFET

### FEATURES

- 4<sup>th</sup> generation E series technology
- Low figure-of-merit (FOM)  $R_{on} \times Q_g$
- Low effective capacitance ( $C_{o(er)}$ )
- Reduced switching and conduction losses
- Avalanche energy rated (UIS)
- Kelvin connection for reduced gate noise
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**

### APPLICATIONS

- Server and telecom power supplies
- Switch mode power supplies (SMPS)
- Power factor correction power supplies (PFC)
- Lighting
  - High-intensity discharge (HID)
  - Fluorescent ballast lighting
- Industrial
  - Welding
  - Induction heating
  - Motor drives
  - Battery chargers
  - Solar (PV inverters)

### PRODUCT SUMMARY

$V_{DS}$ (V) at $T_J$ max.	700	
$R_{DS(on)}$ typ. ( $\Omega$ ) at 25 °C	$V_{GS} = 10$ V	0.087
$Q_g$ max. (nC)	62	
$Q_{gs}$ (nC)	16	
$Q_{gd}$ (nC)	15	
Configuration	Single	

### ORDERING INFORMATION

Package	TO-247AC
Lead (Pb)-free and halogen-free	SiHG100N65E-GE3

### ABSOLUTE MAXIMUM RATINGS ( $T_C = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	$V_{DS}$	650	V
Gate-source voltage	$V_{GS}$	$\pm 30$	
Continuous drain current ( $T_J = 150$ °C)	$V_{GS}$ at 10 V	$T_C = 25$ °C	A
		$T_C = 100$ °C	
Pulsed drain current <sup>a</sup>	$I_{DM}$	63	W/°C
Linear derating factor		1.47	
Single pulse avalanche energy <sup>b</sup>	$E_{AS}$	127	mJ
Maximum power dissipation	$P_D$	208	W
Operating junction and storage temperature range	$T_J, T_{stg}$	-55 to +150	°C
Drain-source voltage slope	$dv/dt$	100	V/ns
Reverse diode $dv/dt$ <sup>c</sup>		11	


#### Notes

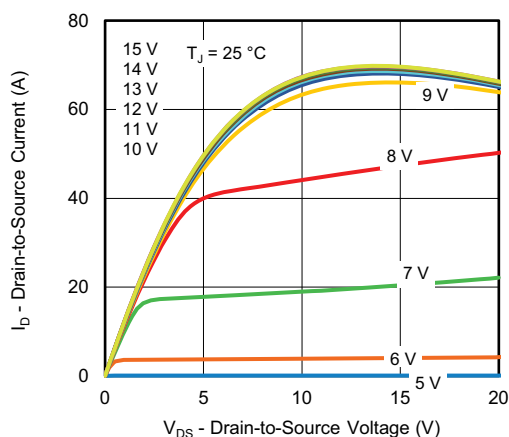
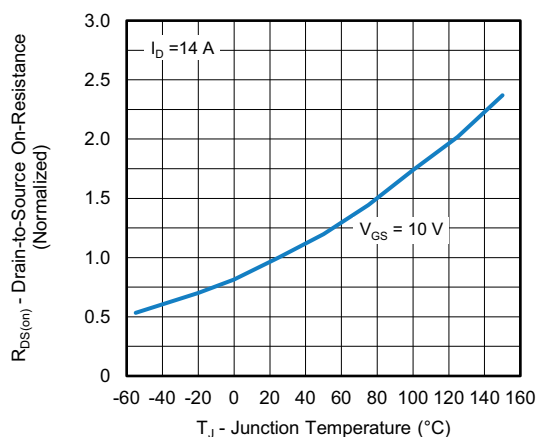
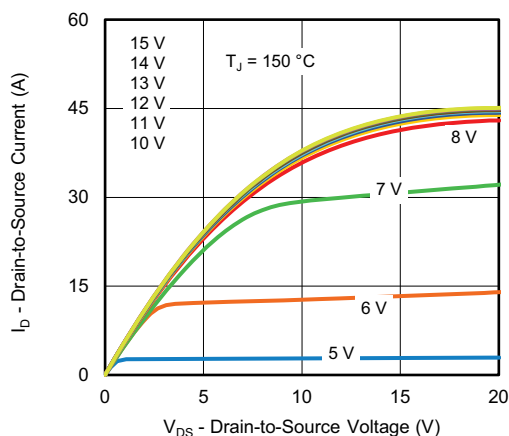
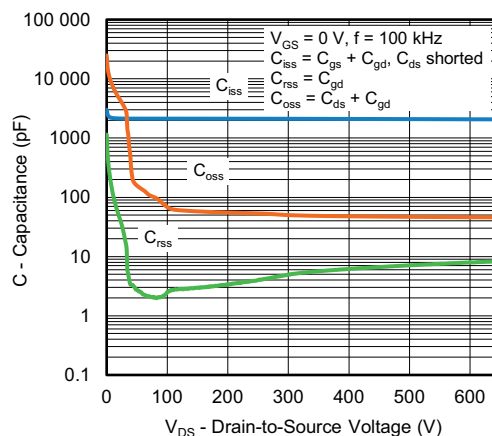
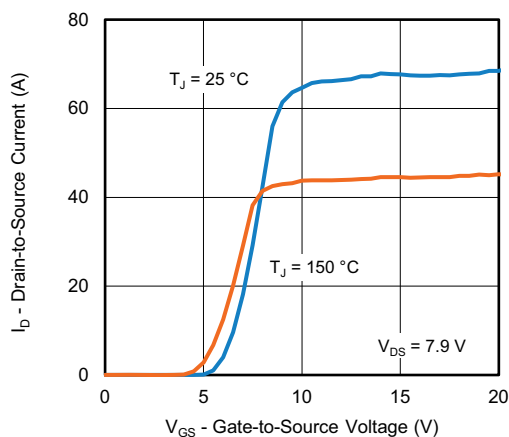
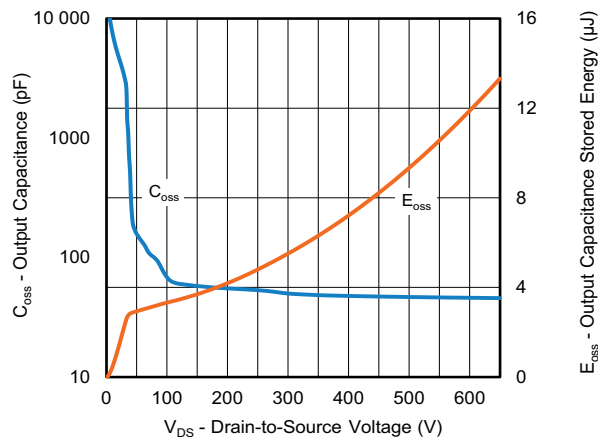
- Repetitive rating; pulse width limited by maximum junction temperature
- $V_{DD} = 140$  V, starting  $T_J = 25$  °C,  $L = 28.2$  mH,  $R_g = 25$   $\Omega$ ,  $I_{AS} = 3.0$  A
- $I_{SD} \leq I_D$ ,  $di/dt = 100$  A/ $\mu$ s, starting  $T_J = 25$  °C

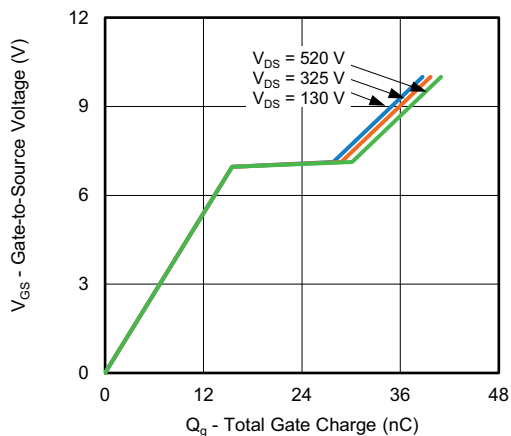
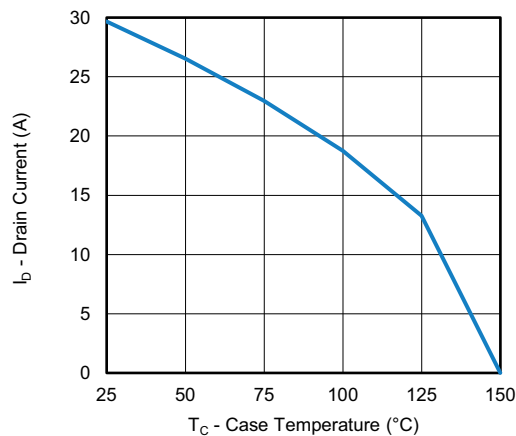
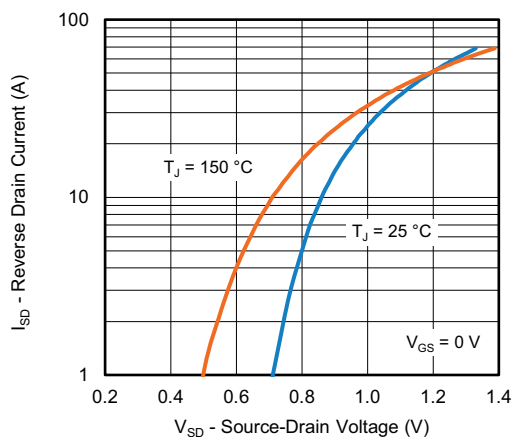
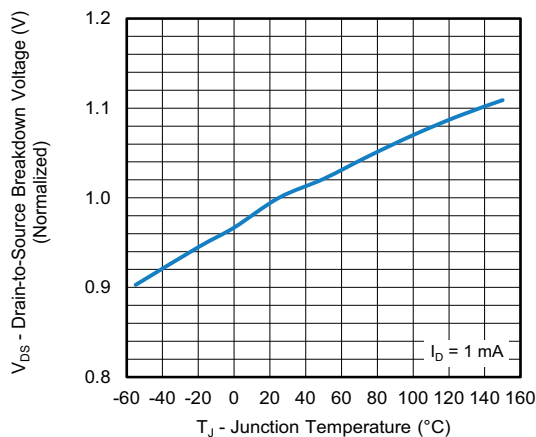
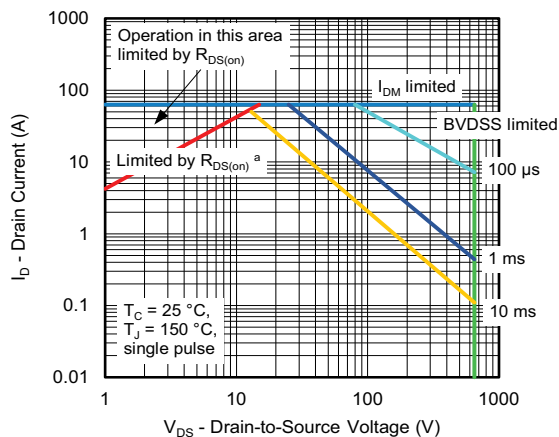
**THERMAL RESISTANCE RATINGS**

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum junction-to-ambient	$R_{thJA}$	-	40	°C/W
Maximum junction-to-case (drain)	$R_{thJC}$	-	0.6	

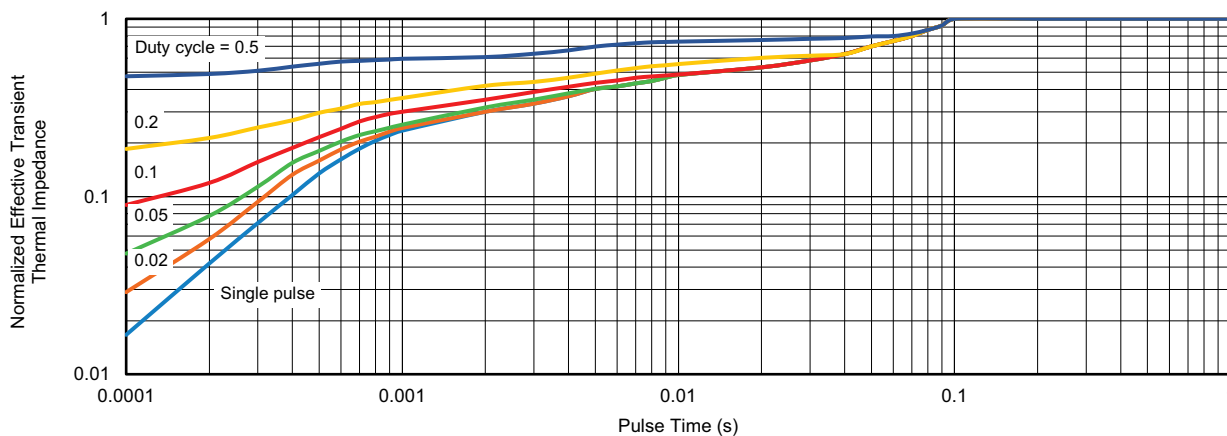
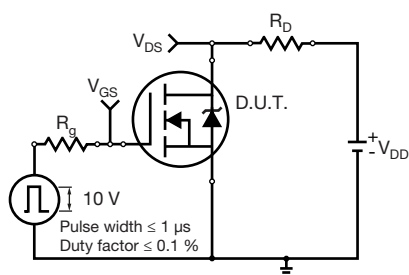
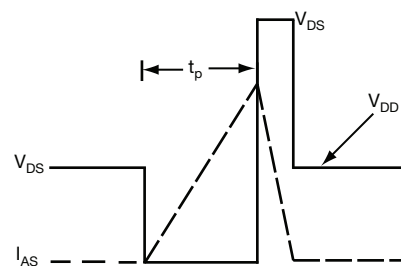
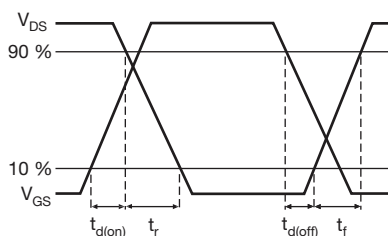
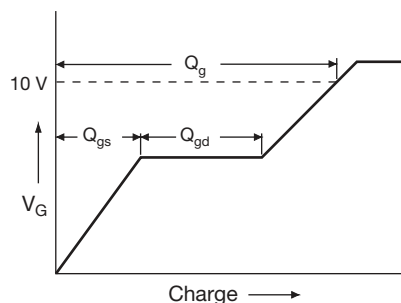
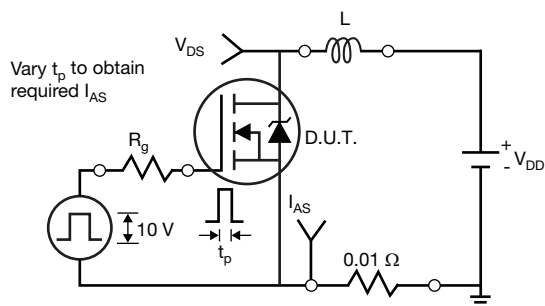
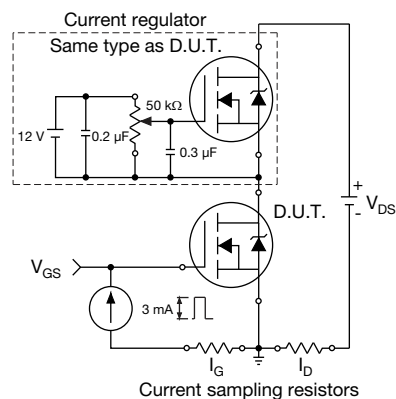
**SPECIFICATIONS** ( $T_J = 25\text{ °C}$ , unless otherwise noted)

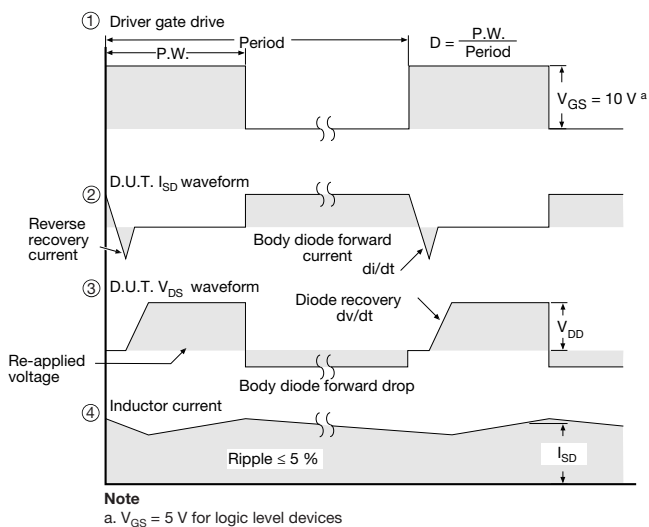
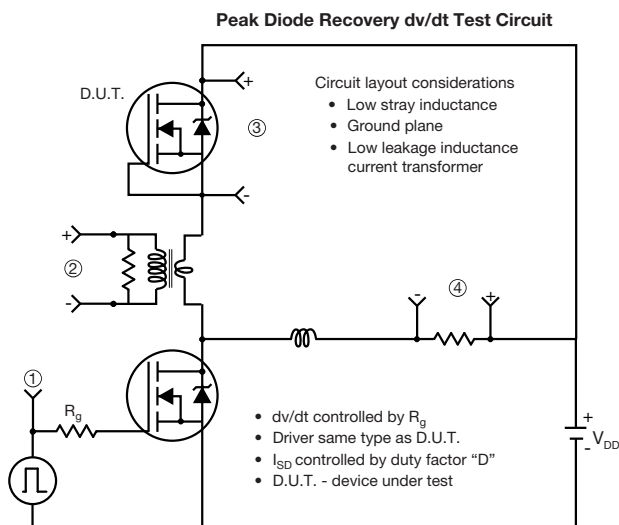
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-source breakdown voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA		650	-	-	V
V <sub>DS</sub> temperature coefficient	ΔV <sub>DS</sub> /T <sub>J</sub>	Reference to 25 °C, I <sub>D</sub> = 1 mA		-	0.68	-	V/°C
Gate-source threshold voltage (N)	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA		3.0	-	5.0	V
Gate-source leakage	I <sub>GSS</sub>	V <sub>GS</sub> = ± 20 V		-	-	± 100	nA
		V <sub>GS</sub> = ± 30 V		-	-	± 1	μA
Zero gate voltage drain current	I <sub>DSS</sub>	V <sub>DS</sub> = 650 V, V <sub>GS</sub> = 0 V		-	-	1	μA
		V <sub>DS</sub> = 520 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 125 °C		-	-	10	
Drain-source on-state resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 12 A	-	0.087	0.100	Ω
Forward transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 8 V, I <sub>D</sub> = 14 A		-	12	-	S
Dynamic							
Input capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 100 V, f = 1 MHz		-	2137	-	pF
Output capacitance	C <sub>Oss</sub>			-	89	-	
Reverse transfer capacitance	C <sub>rss</sub>			-	2	-	
Effective output capacitance, energy related <sup>a</sup>	C <sub>O(er)</sub>	V <sub>DS</sub> = 0 V to 400 V, V <sub>GS</sub> = 0 V		-	90	-	
Effective output capacitance, time related <sup>b</sup>	C <sub>O(tr)</sub>			-	633	-	
Total gate charge	Q <sub>g</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 14 A, V <sub>DS</sub> = 520 V	-	41	62	nC
Gate-source charge	Q <sub>gs</sub>			-	16	-	
Gate-drain charge	Q <sub>gd</sub>			-	15	-	
Turn-on delay time	t <sub>d(on)</sub>	V <sub>DD</sub> = 520 V, I <sub>D</sub> = 14 A, V <sub>GS</sub> = 10 V, R <sub>g</sub> = 9.1 Ω		-	28	56	ns
Rise time	t <sub>r</sub>			-	68	136	
Turn-off delay time	t <sub>d(off)</sub>			-	50	100	
Fall time	t <sub>f</sub>			-	32	64	
Gate input resistance	R <sub>g</sub>	f = 1 MHz, Open Drain		0.5	1.1	2.2	Ω
Drain-Source Body Diode Characteristics							
Continuous source-drain diode current	I <sub>S</sub>	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	30	A
Pulsed diode forward current	I <sub>SM</sub>			-	-	63	
Diode forward voltage	V <sub>SD</sub>	T <sub>J</sub> = 25 °C, I <sub>S</sub> = 14 A, V <sub>GS</sub> = 0 V		-	-	1.2	V
Reverse recovery time	t <sub>rr</sub>	T <sub>J</sub> = 25 °C, I <sub>F</sub> = I <sub>S</sub> = 14A, di/dt = 100 A/μs, V <sub>R</sub> = 25 V		-	362	724	ns
Reverse recovery charge	Q <sub>rr</sub>			-	5.0	10	μC
Reverse recovery current	I <sub>RRM</sub>			-	22	-	A

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

**Fig. 1 - Typical Output Characteristics**

**Fig. 4 - Normalized On-Resistance vs. Temperature**

**Fig. 2 - Typical Output Characteristics**

**Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage**

**Fig. 3 - Typical Transfer Characteristics**

**Fig. 6 -  $C_{oss}$  and  $E_{oss}$  vs.  $V_{DS}$**


**Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage**

**Fig. 10 - Maximum Drain Current vs. Case Temperature**

**Fig. 8 - Typical Source-Drain Diode Forward Voltage**

**Fig. 11 - Temperature vs. Drain-to-Source Voltage**

**Fig. 9 - Maximum Safe Operating Area**
**Note**

a.  $V_{GS} >$  minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified

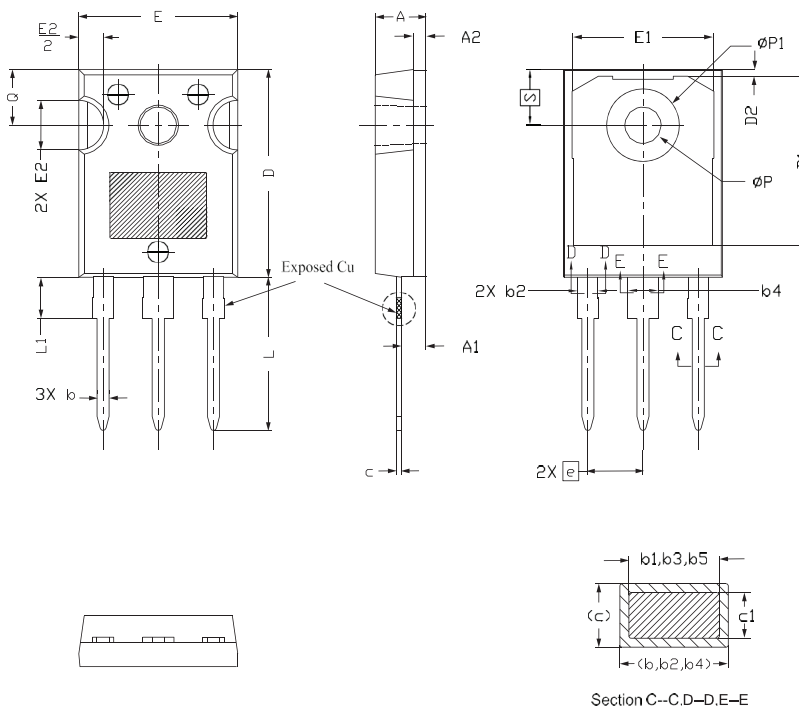

**Fig. 12 - Normalized Transient Thermal Impedance, Junction-to-Case**

**Fig. 13 - Switching Time Test Circuit**

**Fig. 16 - Unclamped Inductive Waveforms**

**Fig. 14 - Switching Time Waveforms**

**Fig. 17 - Basic Gate Charge Waveform**

**Fig. 15 - Unclamped Inductive Test Circuit**

**Fig. 18 - Gate Charge Test Circuit**



**Fig. 19 - For N-Channel**

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## TO-247AC (High Voltage)

**VERSION 1: FACILITY CODE = 9**

Section C--C.D--D.E--E

	MILLIMETERS			
DIM.	MIN.	NOM.	MAX.	NOTES
A	4.83	5.02	5.21	
A1	2.29	2.41	2.55	
A2	1.17	1.27	1.37	
b	1.12	1.20	1.33	
b1	1.12	1.20	1.28	
b2	1.91	2.00	2.39	6
b3	1.91	2.00	2.34	
b4	2.87	3.00	3.22	6, 8
b5	2.87	3.00	3.18	
c	0.40	0.50	0.60	6
c1	0.40	0.50	0.56	
D	20.40	20.55	20.70	4

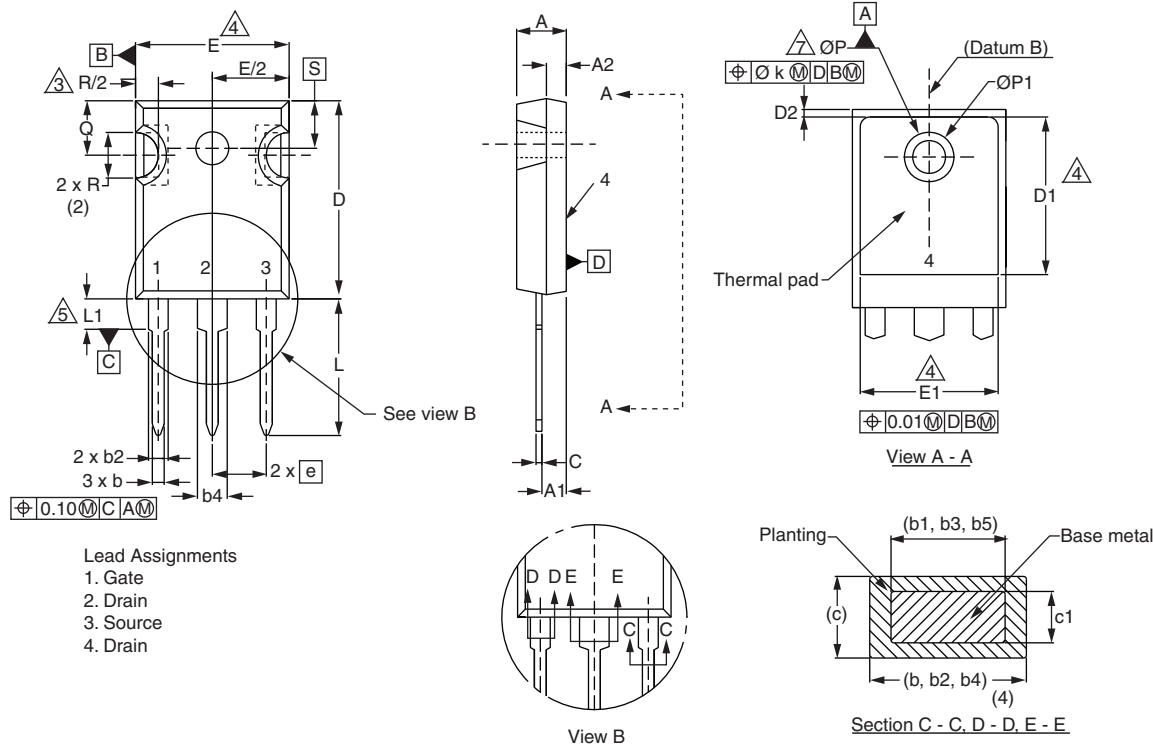
## Notes

- (1) Package reference: JEDEC® TO247, variation AC
- (2) All dimensions are in mm
- (3) Slot required, notch may be rounded
- (4) Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm per side. These dimensions are measured at the outermost extremes of the plastic body
- (5) Thermal pad contour optional with dimensions D1 and E1
- (6) Lead finish uncontrolled in L1
- (7) Ø P to have a maximum draft angle of 1.5° to the top of the part with a maximum hole diameter of 3.91 mm
- (8) Dimension b2 and b4 does not include dambar protrusion. Allowable dambar protrusion shall be 0.1 mm total in excess of b2 and b4 dimension at maximum material condition

	MILLIMETERS			
DIM.	MIN.	NOM.	MAX.	NOTES
D1	16.46	16.76	17.06	5
D2	0.56	0.66	0.76	
E	15.50	15.70	15.87	4
E1	13.46	14.02	14.16	5
E2	4.52	4.91	5.49	3
e	5.46 BSC			
L	14.90	15.15	15.40	
L1	3.96	4.06	4.16	6
Ø P	3.56	3.61	3.65	7
Ø P1	7.19 ref.			
Q	5.31	5.50	5.69	
S	5.51 BSC			



### VERSION 2: FACILITY CODE = Y



DIM.	MILLIMETERS		NOTES
	MIN.	MAX.	
A	4.58	5.31	
A1	2.21	2.59	
A2	1.17	2.49	
b	0.99	1.40	
b1	0.99	1.35	
b2	1.53	2.39	
b3	1.65	2.37	
b4	2.42	3.43	
b5	2.59	3.38	
c	0.38	0.86	
c1	0.38	0.76	
D	19.71	20.82	
D1	13.08	-	

DIM.	MILLIMETERS		NOTES
	MIN.	MAX.	
D2	0.51	1.30	
E	15.29	15.87	
E1	13.72	-	
e	5.46 BSC		
Ø k	0.254		
L	14.20	16.25	
L1	3.71	4.29	
Ø P	3.51	3.66	
Ø P1	-	7.39	
Q	5.31	5.69	
R	4.52	5.49	
S	5.51 BSC		

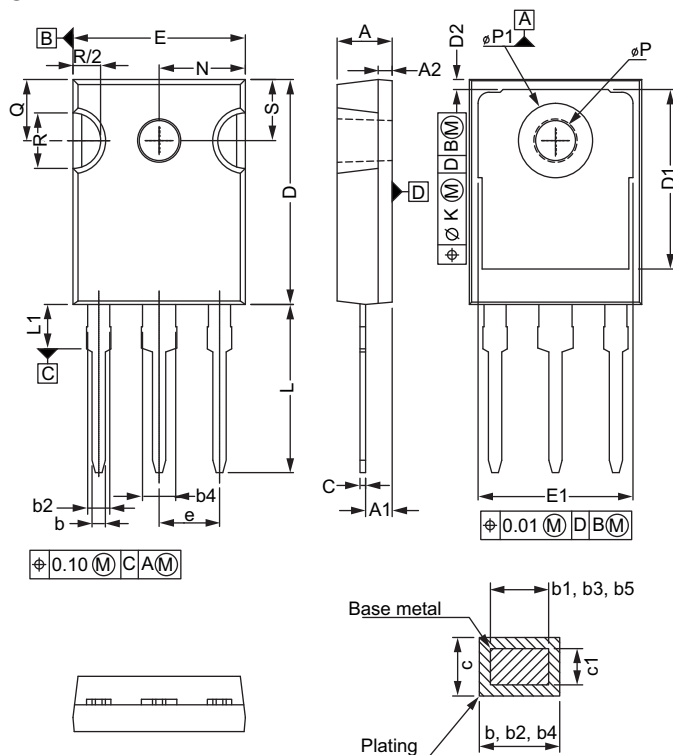
#### Notes

- (1) Dimensioning and tolerancing per ASME Y14.5M-1994
- (2) Contour of slot optional
- (3) Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body
- (4) Thermal pad contour optional with dimensions D1 and E1
- (5) Lead finish uncontrolled in L1
- (6) Ø P to have a maximum draft angle of 1.5 to the top of the part with a maximum hole diameter of 3.91 mm (0.154")
- (7) Outline conforms to JEDEC outline TO-247 with exception of dimension c





## VERSION 3: FACILITY CODE = N



MILLIMETERS		
DIM.	MIN.	MAX.
A	4.65	5.31
A1	2.21	2.59
A2	1.17	1.37
b	0.99	1.40
b1	0.99	1.35
b2	1.65	2.39
b3	1.65	2.34
b4	2.59	3.43
b5	2.59	3.38
c	0.38	0.89
c1	0.38	0.84
D	19.71	20.70
D1	13.08	-

MILLIMETERS		
DIM.	MIN.	MAX.
D2	0.51	1.35
E	15.29	15.87
E1	13.46	-
e	5.46 BSC	
k	0.254	
L	14.20	16.10
L1	3.71	4.29
N	7.62 BSC	
P	3.56	3.66
P1	-	7.39
Q	5.31	5.69
R	4.52	5.49
S	5.51 BSC	

ECN: E22-0452-Rev. G, 31-Oct-2022  
DWG: 5971

### Notes

- (1) Dimensioning and tolerancing per ASME Y14.5M-1994
- (2) Contour of slot optional
- (3) Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body
- (4) Thermal pad contour optional with dimensions D1 and E1
- (5) Lead finish uncontrolled in L1
- (6) Ø P to have a maximum draft angle of 1.5 to the top of the part with a maximum hole diameter of 3.91 mm (0.154")



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