

N-Channel 30 V (D-S) MOSFET

PRODUCT SUMMARY

V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)	Q_g (Typ.)
30	0.0039 at $V_{GS} = 10$ V	107 ^d	67
	0.0045 at $V_{GS} = 4.5$ V	103 ^d	

FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET[®] Power MOSFET
- 100 % R_g and UIS Tested
- Compliant to RoHS Directive 2002/95/EC

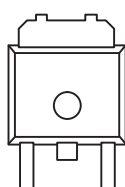


RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

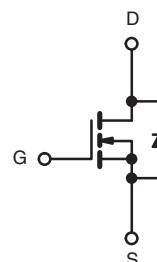
- DC/DC Converters
- Synchronous Buck Low Side

TO-252



Top View

Drain Connected to Tab



N-Channel MOSFET

Ordering Information: SUD42N03-3m9P-GE3 (Lead (Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current	I_D	$T_C = 25$ °C (Silicon Limited)	107 ^d
		$T_C = 70$ °C (Silicon Limited)	85 ^d
		$T_C = 25$ °C (Package Limited)	42
Pulsed Drain Current ($t = 300$ μ s)	I_{DM}	120	A
Avalanche Current	I_{AS}	45	
Single Avalanche Energy ^a	E_{AS}	101	
Maximum Power Dissipation ^a	P_D	$T_C = 25$ °C	73.5 ^b
		$T_A = 25$ °C ^c	2.5
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 150	°C

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Limit	Unit
Junction-to-Ambient (PCB Mount) ^c	R_{thJA}	50	°C/W
Junction-to-Case (Drain)	R_{thJC}	1.7	

Notes:

a. Duty cycle ≤ 1 %.

b. See SOA curve for voltage derating.

c. When mounted on 1" square PCB (FR-4 material).

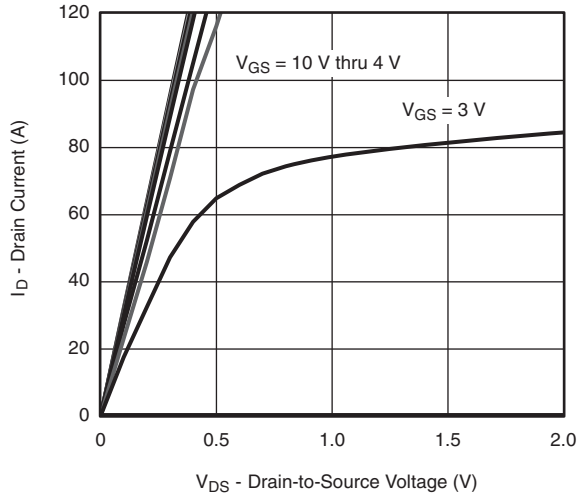
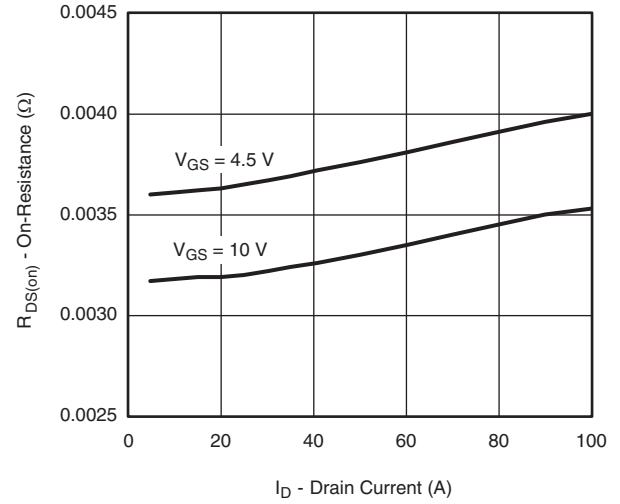
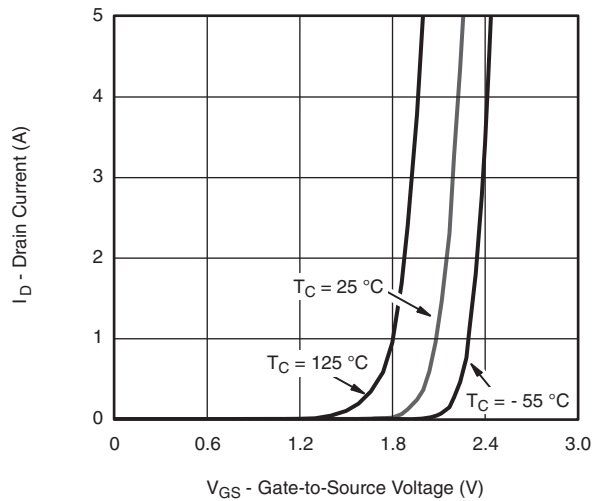
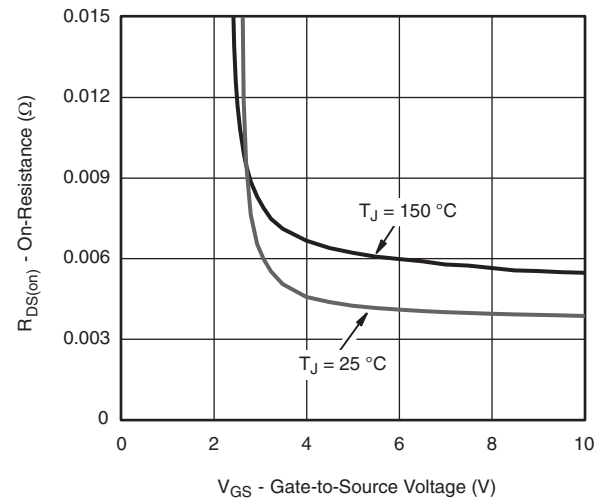
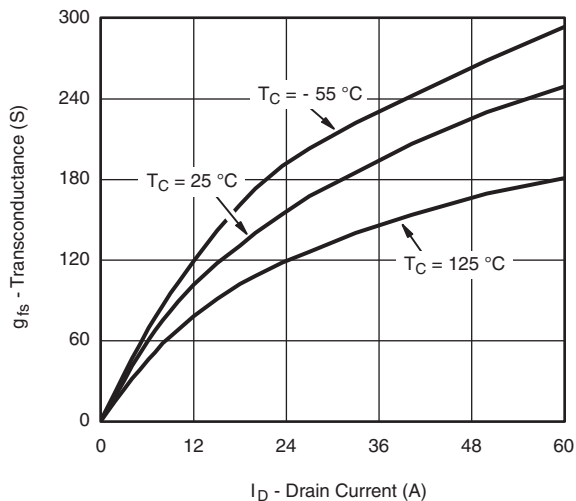
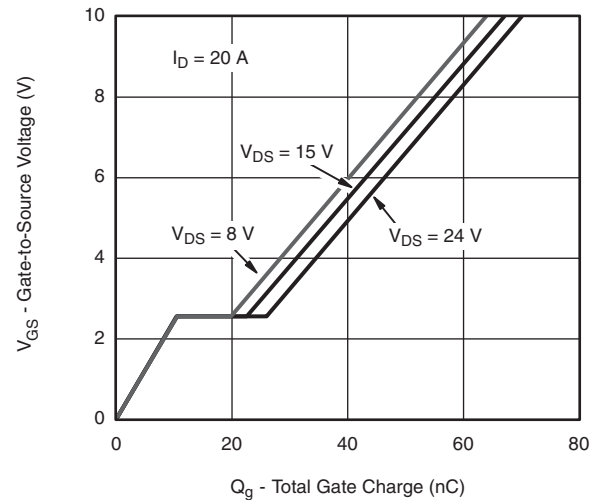
d. Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 42 A.

SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{DS}	V _{DS} = 0 V, I _D = 250 μA	30			V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	1		2.5	
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V			± 250	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 30 V, V _{GS} = 0 V			1	μA
		V _{DS} = 30 V, V _{GS} = 0 V, T _J = 125 °C			50	
		V _{DS} = 30 V, V _{GS} = 0 V, T _J = 150 °C			250	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≥ 10 V, V _{GS} = 10 V	50			A
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = 10 V, I _D = 22 A		0.0032	0.0039	Ω
		V _{GS} = 4.5 V, I _D = 20 A		0.0037	0.0045	
Forward Transconductance ^a	g _{fs}	V _{DS} = 15 V, I _D = 20 A		110		S
Dynamic ^b						
Input Capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = 15 V, f = 1 MHz		3535		pF
Output Capacitance	C _{oss}			680		
Reverse Transfer Capacitance	C _{rss}			400		
Total Gate Charge ^c	Q _g	V _{DS} = 15 V, V _{GS} = 10 V, I _D = 20 A		67	100	nC
Gate-Source Charge ^c	Q _{gs}			10.5		
Gate-Drain Charge ^c	Q _{gd}			12.2		
Gate Resistance	R _g	f = 1 MHz	0.3	1.4	2.8	Ω
Turn-On Delay Time ^c	t _{d(on)}	V _{DD} = 15 V, R _L = 1.5 Ω I _D ≅ 10 A, V _{GEN} = 10 V, R _g = 1 Ω		11	20	ns
Rise Time ^c	t _r			10	20	
Turn-Off Delay Time ^c	t _{d(off)}			35	53	
Fall Time ^c	t _f			10	20	
Drain-Source Body Diode Ratings and Characteristics ^b T _C = 25 °C						
Continuous Current	I _S				42	A
Pulsed Current	I _{SM}				120	
Forward Voltage ^a	V _{SD}	I _F = 10 A, V _{GS} = 0 V		0.83	1.5	V
Reverse Recovery Time	t _{rr}	I _F = 10 A, dI/dt = 100 A/μs		41	62	ns
Peak Reverse Recovery Current	I _{RM(REC)}			2	3	A
Reverse Recovery Charge	Q _{rr}				40	60

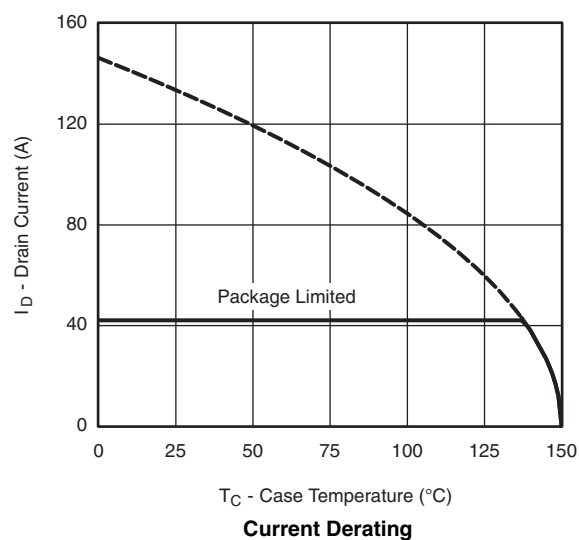
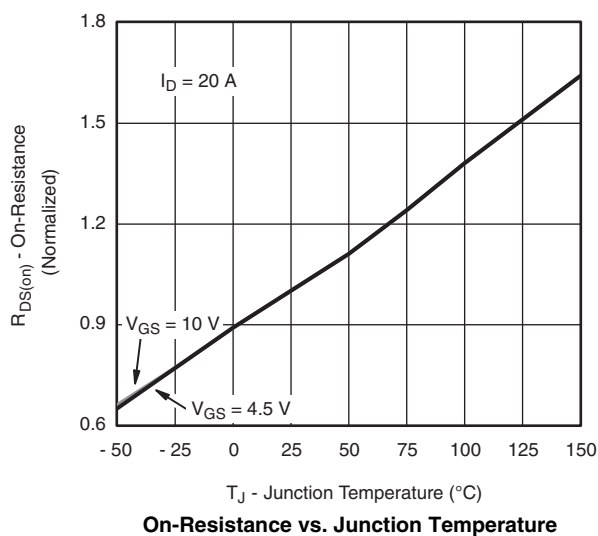
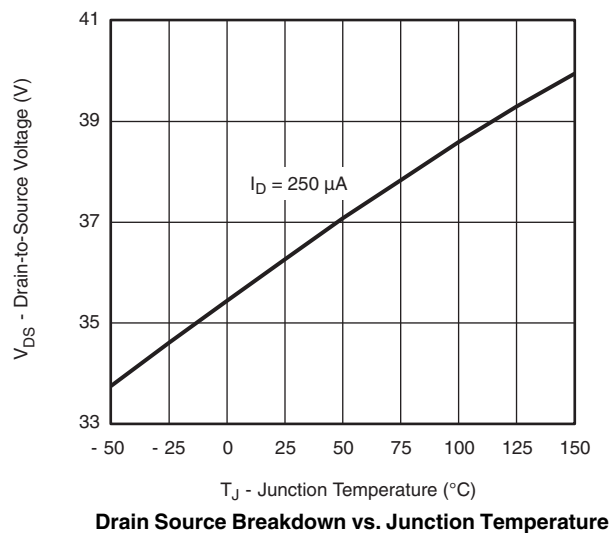
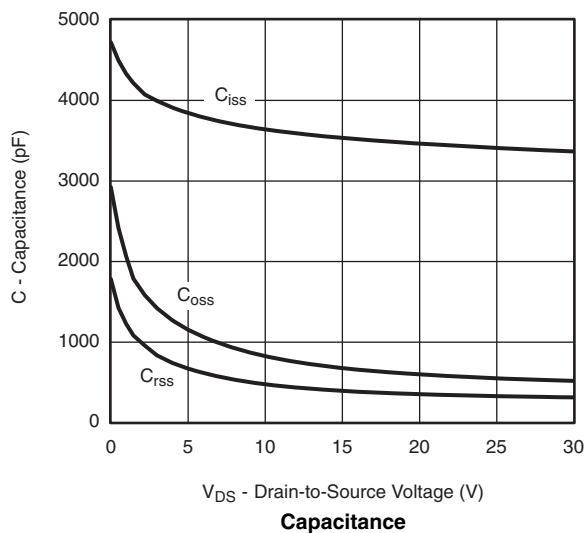
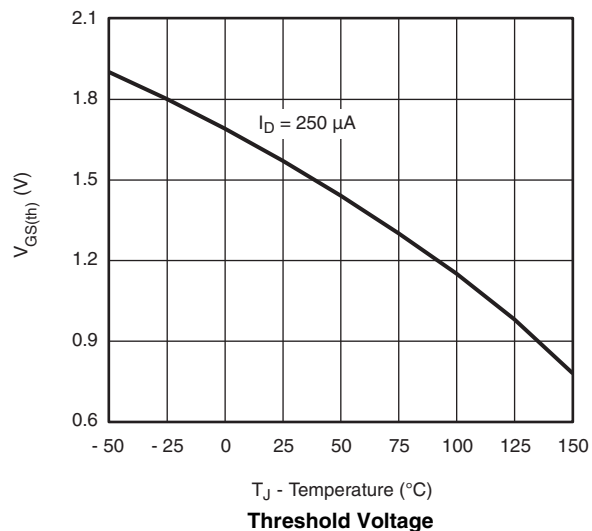
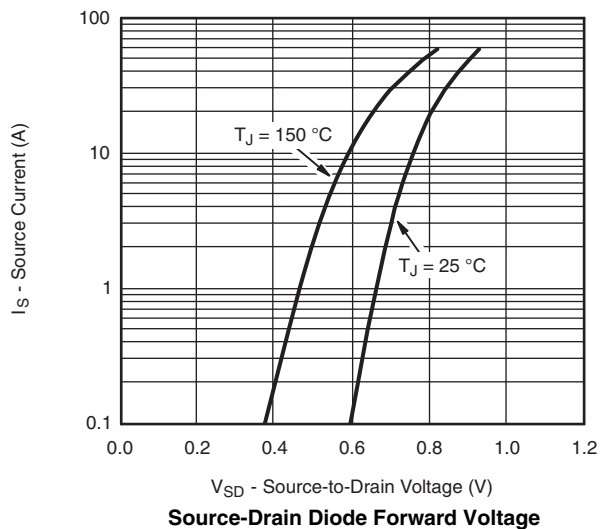
Notes:

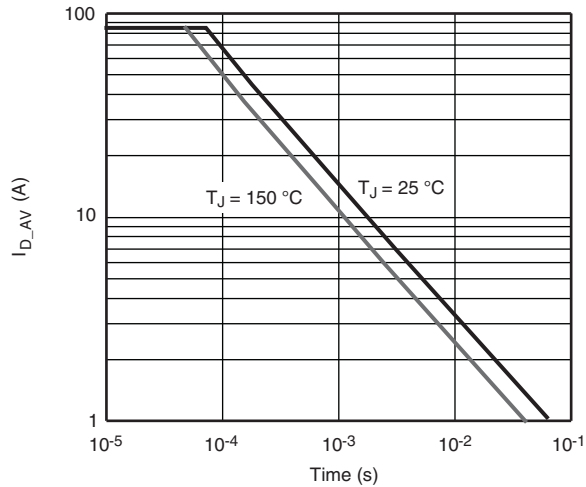
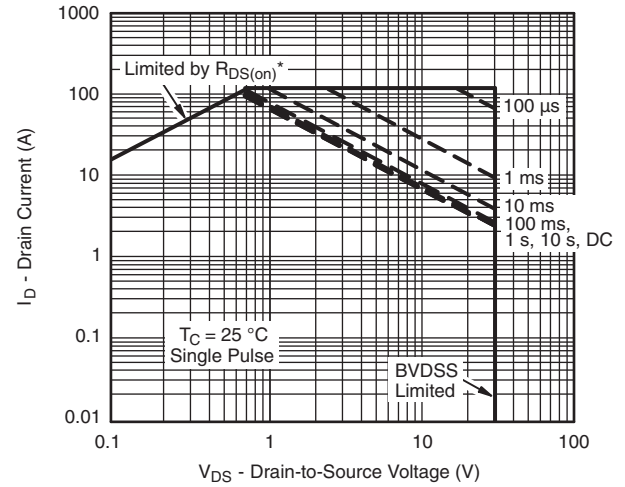
- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
b. Guaranteed by design, not subject to production testing.
c. Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

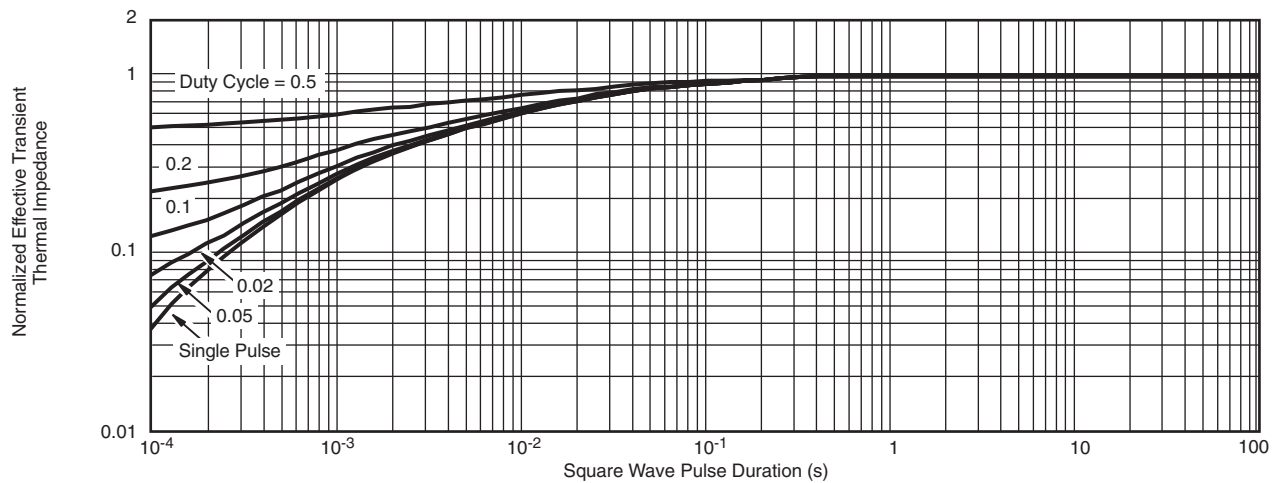
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Output Characteristics

On-Resistance vs. Drain Current

Transfer Characteristics

On-Resistance vs. Gate-to-Source Voltage

Transconductance

Gate Charge

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Single Pulse Avalanche Current Capability vs. Time


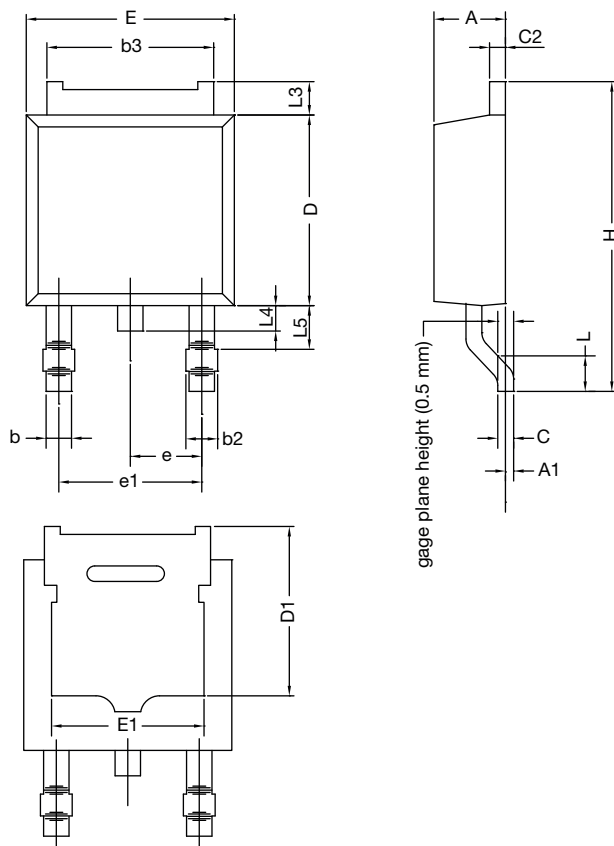
* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified
Safe Operating Area


Normalized Thermal Transient Impedance, Junction-to-Case

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TO-252AA Case Outline

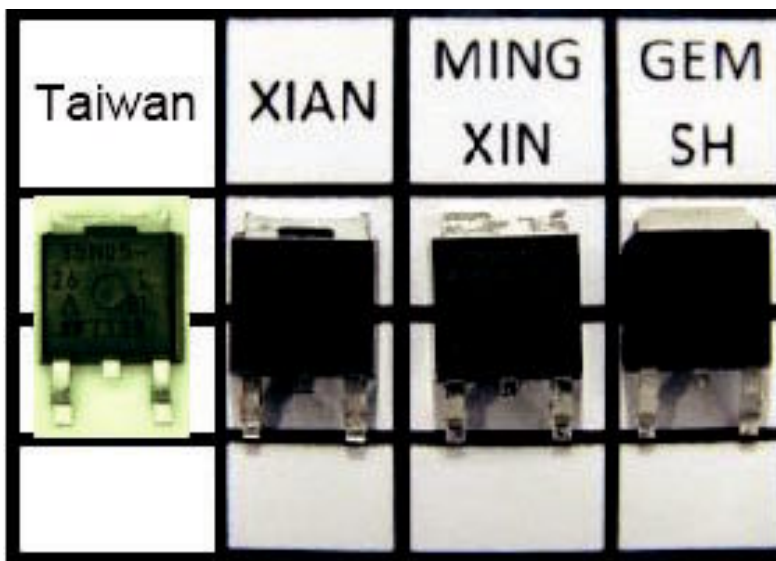


DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	2.18	2.38	0.086	0.094
A1	-	0.127	-	0.005
b	0.64	0.88	0.025	0.035
b2	0.76	1.14	0.030	0.045
b3	4.95	5.46	0.195	0.215
C	0.46	0.61	0.018	0.024
C2	0.46	0.89	0.018	0.035
D	5.97	6.22	0.235	0.245
D1	4.10	-	0.161	-
E	6.35	6.73	0.250	0.265
E1	4.32	-	0.170	-
H	9.40	10.41	0.370	0.410
e	2.28 BSC		0.090 BSC	
e1	4.56 BSC		0.180 BSC	
L	1.40	1.78	0.055	0.070
L3	0.89	1.27	0.035	0.050
L4	-	1.02	-	0.040
L5	1.01	1.52	0.040	0.060

ECN: T13-0359-Rev. O, 03-Jun-13
DWG: 5347

Notes

- Dimension L3 is for reference only.
- Xi'an, Mingxin, and GEM SH actual photo.



RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)



Recommended Minimum Pads
Dimensions in Inches/(mm)

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