High Sound Quality Audio D/A Converters

32-bit, 1536 kHz Sampling Stereo Audio D/A Converter

BD34302EKV

ROHM Musical Device
MUS-IC

General Description

BD34302EKV is a D/A converter for high-quality audio that incorporates ROHM's unique sound quality design technology. The newly developed DWA improves THD performance and provides higher resolution and more natural sound quality with HD (High Definition) monaural mode. In addition, an automatic mode switching function makes it possible to easily switch between PCM/DSD and between different sampling frequencies.

Features

- MUS-IC™ Series
- SNR 130 dB (Typ), THD+N -115 dB (Typ)*(Note 1)*
- Sampling Frequency 32 kHz to 1536 kHz*(Note 2)*
- 2 Types of Digital FIR Filters *(Note 1)*
- DSD 2.8 MHz, 5.6 MHz, 11.2 MHz and 22.5 MHz
- Supports Stereo Mode (2ch), Monaural Mode (1ch), and HD (High Definition) Monaural Mode (1ch)
- 2 Types of DWA Algorithms
- Automatic Mode Switching
- Selectable 4 Device Addresses (38h/3Ah/3Ch/3Eh)

Applications

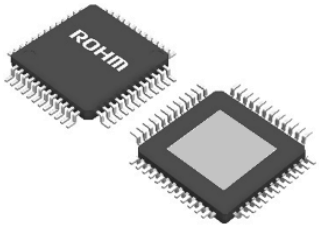
- CD/SACD Player
- Digital Audio Player (DAP)
- USB-DAC and Others

Key Specifications

- Supply Voltage Range of AVCC*(Note 3)*: 4.5 V to 5.5 V
- Supply Voltage Range of DVDD: 1.4 V to 1.6 V
- Supply Voltage Range of DVDDIO: 3.0 V to 3.6 V
- SNR*(Note 1)*: 130 dB (Typ)
- THD+N*(Note 1)*: -115 dB (Typ)
- Dynamic Range*(Note 1)*: 130 dB (Typ)
- Operation Temperature Range: -40 °C to +85 °C

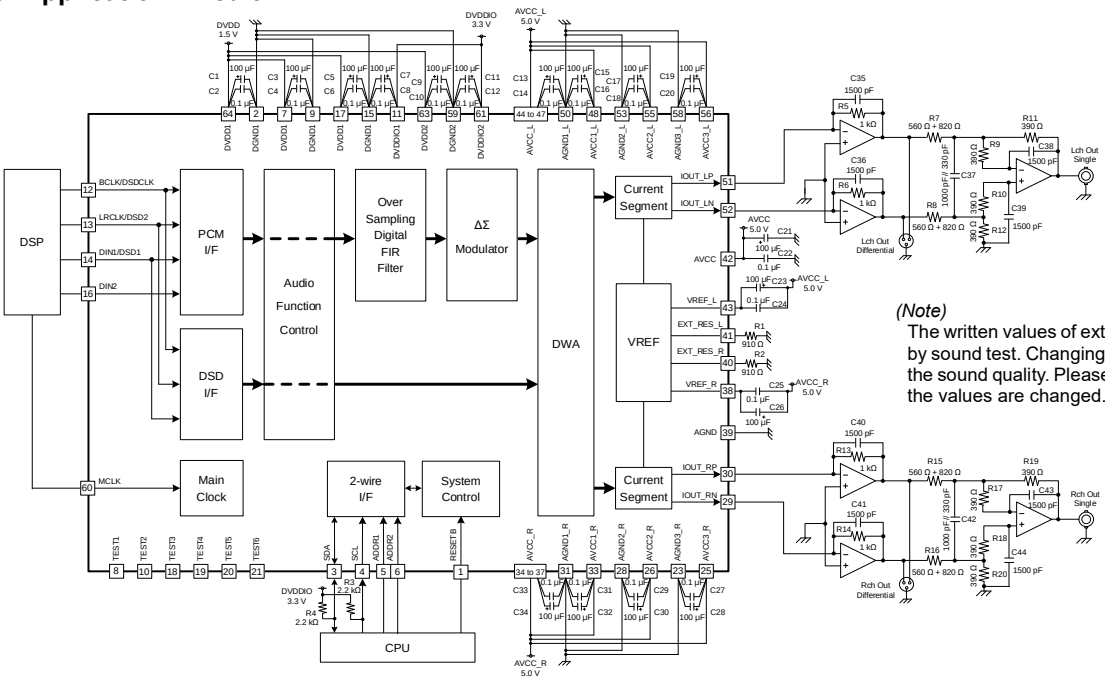
Package

	W (Typ) x D (Typ) x H (Max)
HTQFP64BV	12.0 mm x 12.0 mm x 1.0 mm



(Note 1) PCM mode
(Note 2) Double data transfer
(Note 3) AVCC, AVCC_R and AVCC_L in Typical Application Circuit

Typical Application Circuit



(Note)
The written values of external parts are checked by sound test. Changing these values can affect the sound quality. Please check the sound when the values are changed.

Figure 1. Typical Application Circuit

MUS-IC™ is a trademark or a registered trademark of ROHM Co., Ltd.

Contents

MUS-IC™

MUS-IC™ stands for ROHM Musical Device MUS-IC. MUS-IC™ series are products designed for high-end audio.

Pin Configuration

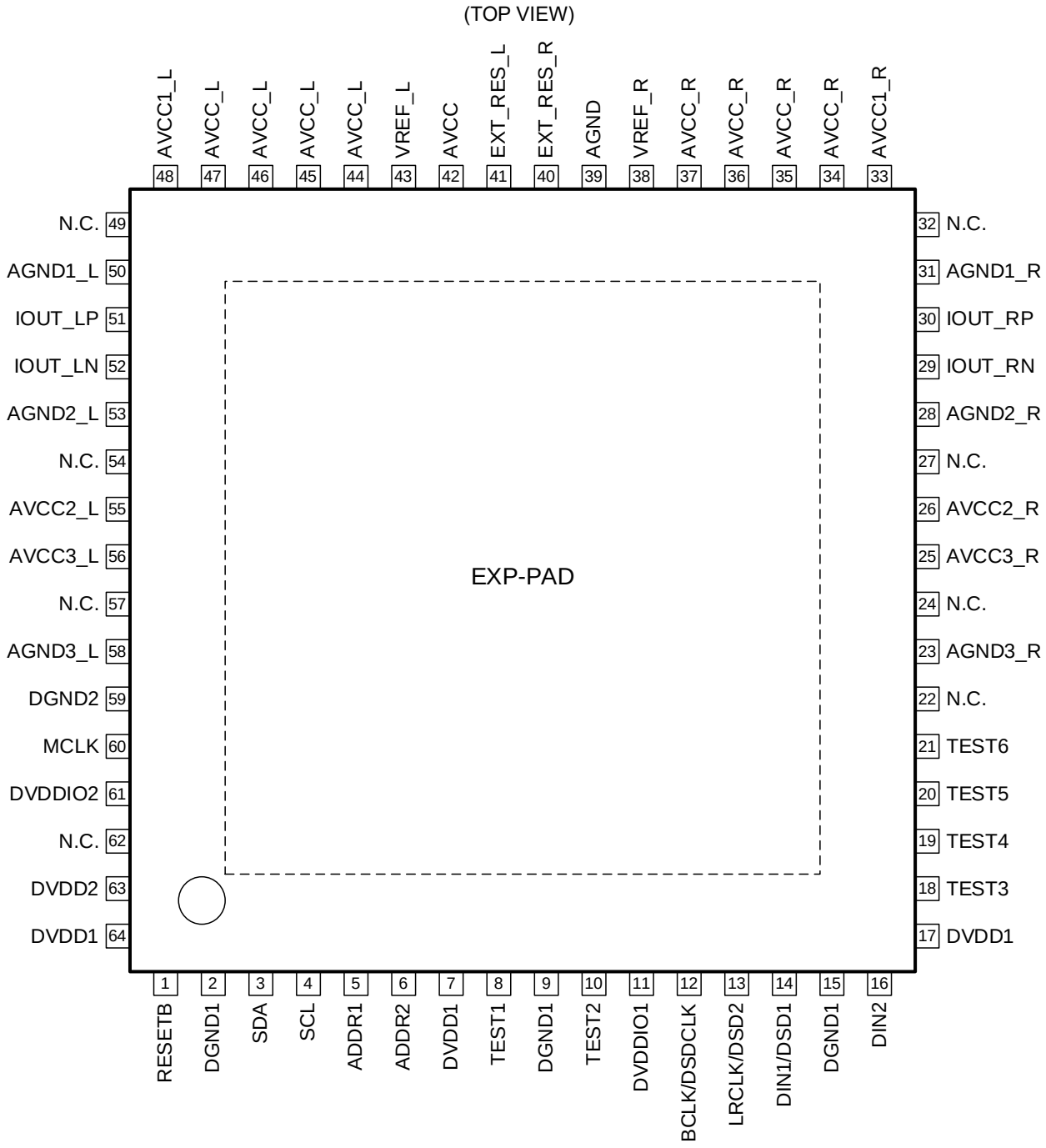


Figure 2. Pin Configuration

Caution:

Open the N.C. pins and the TEST pins (TEST1 to TEST6).
The EXP-PAD should be connected to AGND.

Pin Descriptions

Pin No.	Pin Name	D/A(Note 1)	I/O(Note 2)	Function
1	RESETB	D	I	Reset (L: Reset)
2	DGND1	D	-	Digital ground
3	SDA	D	I/O	2-wire I/F data(Note 3)
4	SCL	D	I	2-wire I/F clock
5	ADDR1	D	I	2-wire I/F device address selector1 (38h/3Ah/3Ch/3Eh)
6	ADDR2	D	I	2-wire I/F device address selector2 (38h/3Ah/3Ch/3Eh)
7	DVDD1	D	-	Digital core power supply (1.5 V)
8	TEST1	D	I	The TEST pin(Note 4)
9	DGND1	D	-	Digital ground
10	TEST2	D	I	The TEST pin(Note 4)
11	DVDDIO1	D	-	Digital I/O power supply (3.3 V)
12	BCLK/DSDCLK	D	I	PCM I/F bit clock / DSD clock
13	LRCLK/DSD2	D	I	PCM I/F LR clock / DSD2 data
14	DIN1/DSD1	D	I	PCM I/F serial data / DSD1 data
15	DGND1	D	-	Digital ground
16	DIN2	D	I	PCM I/F serial data(Note 5)
17	DVDD1	D	-	Digital core power supply (1.5 V)
18	TEST3	D	I	The TEST pin(Note 4)
19	TEST4	D	I	The TEST pin(Note 4)
20	TEST5	D	I	The TEST pin(Note 4)
21	TEST6	D	I	The TEST pin(Note 4)
22	N.C.	-	-	No connection(Note 4)
23	AGND3_R	A	-	Rch analog ground
24	N.C.	-	-	No connection(Note 4)
25	AVCC3_R	A	-	Rch analog power supply (5.0 V)
26	AVCC2_R	A	-	Rch analog power supply (5.0 V)
27	N.C.	-	-	No connection(Note 4)
28	AGND2_R	A	-	Rch analog ground
29	IOUT_RN	A	O	Rch negative output
30	IOUT_RP	A	O	Rch positive output
31	AGND1_R	A	-	Rch analog ground
32	N.C.	-	-	No connection(Note 4)

(Note 1) D/A means D: Digital pin, A: Analog pin.
(Note 2) I/O means I: Input, O: Output.
(Note 3) In 2-wire I/F operation, this pin becomes open-drain output.
(Note 4) N.C. pins and TEST pins (TEST1 to TEST6) should be left open.
(Note 5) If double data transfer (fs = 1536 kHz) is not used, DIN2 pin should be left open.

Pin Descriptions - continued

Pin No.	Pin Name	D/A(Note 1)	I/O(Note 2)	Function
33	AVCC1_R	A	-	Rch analog power supply (5.0 V)
34	AVCC_R	A	-	Rch analog power supply for Current Segment (5.0 V)
35	AVCC_R	A	-	Rch analog power supply for Current Segment (5.0 V)
36	AVCC_R	A	-	Rch analog power supply for Current Segment (5.0 V)
37	AVCC_R	A	-	Rch analog power supply for Current Segment (5.0 V)
38	VREF_R	A	O	Rch external capacitor (Recommended: 0.1 µF + 100 µF)
39	AGND	A	-	Analog ground
40	EXT_RES_R	A	O	Rch external register (Recommended: 910 Ω)
41	EXT_RES_L	A	O	Lch external register (Recommended: 910 Ω)
42	AVCC	A	-	Analog power supply (5.0 V)
43	VREF_L	A	O	Lch external capacitor (Recommended: 0.1 µF + 100 µF)
44	AVCC_L	A	-	Lch analog power supply for Current Segment (5.0 V)
45	AVCC_L	A	-	Lch analog power supply for Current Segment (5.0 V)
46	AVCC_L	A	-	Lch analog power supply for Current Segment (5.0 V)
47	AVCC_L	A	-	Lch analog power supply for Current Segment (5.0 V)
48	AVCC1_L	A	-	Lch analog power supply (5.0 V)
49	N.C.	-	-	No connection(Note 4)
50	AGND1_L	A	-	Lch analog ground
51	IOUT_LP	A	O	Lch positive output
52	IOUT_LN	A	O	Lch negative output
53	AGND2_L	A	-	Lch analog ground
54	N.C.	-	-	No connection(Note 4)
55	AVCC2_L	A	-	Lch analog power supply (5.0 V)
56	AVCC3_L	A	-	Lch analog power supply (5.0 V)
57	N.C.	-	-	No connection(Note 4)
58	AGND3_L	A	-	Lch analog ground
59	DGND2	D	-	Digital ground for MCLK
60	MCLK	D	I	Main clock
61	DVDDIO2	D	-	Digital I/O power supply for MCLK (3.3 V)
62	N.C.	-	-	No connection(Note 4)
63	DVDD2	D	-	Digital power supply for MCLK (1.5 V)
64	DVDD1	D	-	Digital core power supply (1.5 V)
-	EXP_PAD	-	-	Connect the EXP-PAD to AGND.

(Note 1) D/A means D: Digital pin, A: Analog pin.
(Note 2) I/O means I: Input, O: Output.
(Note 4) N.C. pins and TEST pins (TEST1 to TEST6) should be left open.

Block Diagram

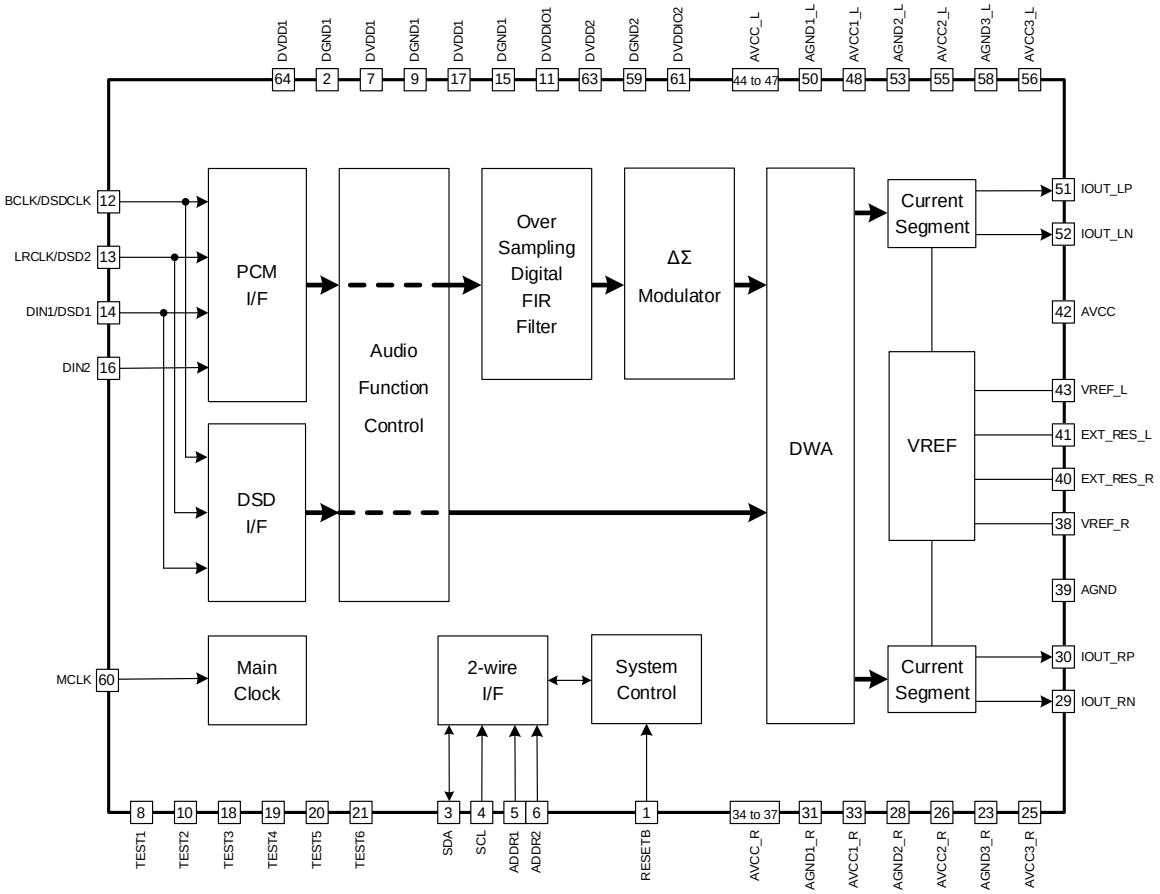


Figure 3. Block Diagram

Table 1. Description of Blocks

Block	Description
PCM I/F	Digital audio interface for PCM audio format 2ch stereo Supports 32 kHz to 1536 kHz input sampling frequency Supports 16-bit to 32-bit input data length BCLK = 64 fs
DSD I/F	Digital audio interface for DSD audio format 2ch stereo Supports 2.8 MHz, 5.6 MHz, 11.2 MHz, 22.5 MHz
Main Clock	Clock control
2-wire I/F	2-wire Interface block for register settings Supports 400 kHz data transmission speed 4 device addresses (38h/3Ah/3Ch/3Eh) selectable
System Control	System control by register setting
Audio Function Control	Digital audio format control LR swap → stereo/monaural → polarity inversion
Over Sampling Digital FIR Filter	Over sampling digital FIR filter Sharp roll-off / slow roll-off filter selectable
ΔΣ Modulator	ΔΣ modulator
DWA	DWA (Data Weighted Averaging) circuit 2 DWA algorithms selectable
Current Segment	Current segment
VREF	Voltage reference

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply Voltage	AVCC	7.0	V
	DVDDIO	7.0	
	DVDD	2.1	
Input Voltage	Vin	-0.3 to DVDDIO + 0.3	V
Storage Temperature Range	Tstg	-55 to +150	°C
Maximum Junction Temperature	Tjmax	150	°C

Caution 1: *Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.*

Caution 2: *Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.*

Thermal Resistance*(Note 1)*

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s*(Note 3)*	2s2p*(Note 4)*	
HTQFP64BV				
Junction to Ambient	θ_{JA}	64.5	16.1	°C/W
Junction to Top Characterization Parameter*(Note 2)*	Ψ_{JT}	3	2	°C/W

(Note 1) Based on JESD51-2A (Still-Air).
(Note 2) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.
(Note 3) Using a PCB board based on JESD51-3.
(Note 4) Using a PCB board based on JESD51-5,7.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3 mm x 76.2 mm x 1.57 mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70 µm

Layer Number of Measurement Board	Material	Board Size	Thermal Via*(Note 5)*	
			Pitch	Diameter
4 Layers	FR-4	114.3 mm x 76.2 mm x 1.6 mmt	1.20 mm	Φ0.30 mm

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70 µm	74.2 mm x 74.2 mm	35 µm	74.2mm x 74.2 mm	70 µm

(Note 5) This thermal via connect with the copper pattern of layers 1, 2 and 4. The placement and dimensions obey a land pattern.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Operating Supply Voltage	AVCC	4.5	5.0	5.5	V
	DVDDIO	3.0	3.3	3.6	
	DVDD	1.4	1.5	1.6	
Operating Temperature	Topr	-40	+25	+85	°C

Caution: *Operating supply voltage and operating temperature are the ranges in which the IC is available for basic operation. (Basic operation means that the IC operates without emitting unexpected noise or stopping signal.) Characteristics and rating are not warranted in the whole operating supply voltage and operating temperature.*

Electrical Characteristics

Unless otherwise specified Ta = 25 °C, AVCC = 5.0 V, DVDDIO = 3.3 V, DVDD = 1.5 V, Input signal frequency = 1 kHz, 20-kHz AES17 LPF, Differential output (XLR) measurement, PCM Mode, 24-bit I^2S, fs = 44.1 kHz, MCLK = 22.5792 MHz, Clock 1 (04h) = 02h, Clock 2 (06h) = 01h, FIR Filter 1 (30h) = 01h, FIR Filter 2 (31h) = 80h, Delta Sigma (40h) = 00h, DWA (68h) = 00h

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
Power Supply Current						
AVCC Current	I_{AVCC}	-	30.5	45.0	mA	AVCC_L + AVCC_R + AVCC -∞ dBFS (PCM, No Signal)
DVDDIO Current	I_{DVDDIO}	-	7	70	µA	-∞ dBFS (PCM, No Signal)
DVDD Current 1	I_{DVDD1}	-	7	14	mA	-∞ dBFS (PCM, No Signal)
DVDD Current 2	I_{DVDD2}	-	10	20	mA	0 dBFS, fs = 44.1 kHz
DVDD Current 3	I_{DVDD3}	-	16	32	mA	0 dBFS, fs = 96 kHz, (04h) = 00h, (30h) = 02h, (31h) = 01h, (40h) = 11h, MCLK = 24.5760 MHz
DVDD Current 4	I_{DVDD4}	-	14	28	mA	0 dBFS, fs = 192 kHz, (04h) = 00h, (30h) = 04h, (31h) = 02h, (40h) = 11h, MCLK = 24.5760 MHz
DVDD Current 5	I_{DVDD5}	-	8	16	mA	0 dBFS, fs = 384 kHz, (04h) = 00h, (30h) = 08h, (31h) = 00h, (40h) = 11h, MCLK = 24.5760 MHz
DVDD Current 6	I_{DVDD6}	-	20	40	mA	0 dBFS, fs = 44.1 kHz, (04h) = 00h, (30h) = 01h, (31h) = 00h, (40h) = 11h
PCM AC Characteristics						
SNR	SNR_{P1}	126	130	-	dB	20-kHz AES17 LPF + A-weight, DWA1*(Note 1)*
	SNR_{P2}	-	123	-	dB	20-kHz AES17 LPF + A-weight, DWA2*(Note 2)*
THD+N	THD_{P1}	-	-115	-100	dB	20-kHz AES17 LPF, -3 dBFS, DWA1*(Note 1)*
	THD_{P2}	-	-117	-	dB	20-kHz AES17 LPF, -3 dBFS, DWA2*(Note 2)*
Dynamic Range	DR_P	126	130	-	dB	20-kHz AES17 LPF + A-weight, -60 dBFS
Channel Gain Mismatch	GM_P	-0.5	0	+0.5	dB	20-kHz AES17 LPF, 0 dBFS
Output Center Current	I_{CN_P}	4.6	5.3	6.0	mA	-∞ dBFS (No Signal), Bias Current Single Output
Peak Output Current	I_{PP_P}	8.5	9.8	11.1	mApp	0 dBFS, Current Amplitude
Sampling Frequency	fs	32.0	44.1	1536.0	kHz	-
Bit Length	Bit	16	-	32	Bit	-

(Note 1) DWA1: using DWA algorithm 1 (Delta Sigma (40h) = 00h, DWA (68h) = 00h)
(Note 2) DWA2: using DWA algorithm 2 (Delta Sigma (40h) = 02h, DWA (68h) = 02h)

Electrical Characteristics - continued

Unless otherwise specified Ta = 25 °C, AVCC = 5.0 V, DVDDIO = 3.3 V, DVDD = 1.5 V, Input Signal Frequency = 1 kHz, 20-kHz AES17 LPF, Differential output (XLR) measurement, DSD Mode, f_{DSD} = 5.6448 MHz, MCLK = 22.5792 MHz, Clock 1 (04h) = 00h, Clock 2 (06h) = 01h, DSD Filter (16h) = 01h, Delta Sigma (40h) = 02h, DWA (68h) = 00h

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
DSD AC Characteristics						
SNR	SNR_D	115	125	-	dB	20-kHz AES17 LPF + A-weight *(Note 1)*
THD+N	THD_D	-	-113	-103	dB	20-kHz AES17LPF, 0 dBFS
Dynamic Range	DR_D	107	120	-	dB	20-kHz AES17LPF + A-weight, -60 dBFS
Output Center Current	I_{CN_D}	4.6	5.3	6.0	mA	-∞ dBFS (No signal), Bias Current Single Output
Peak Output Current	I_{PP_D1}	4.6	5.3	6.0	mApp	0 dBFS, Current Amplitude, LEVEL1 *(Note 2)*
	I_{PP_D2}	9.2	10.6	12.0	mApp	0 dBFS, Current Amplitude, LEVEL2 *(Note 3)*
DSD Clock	f_{DSD}	2.8224	-	22.5792	MHz	-

(Note 1) The silent input pattern of DSD data is a repetition of 5Ah.
(Note 2) LEVEL1: using normal output level (0 dB) (DSD Filter(16h) = 01h, DWA (68h) = 00h)
(Note 3) LEVEL2: using double output level (+6 dB) (DSD Filter (16h) = 09h, DWA (68h) = 80h)

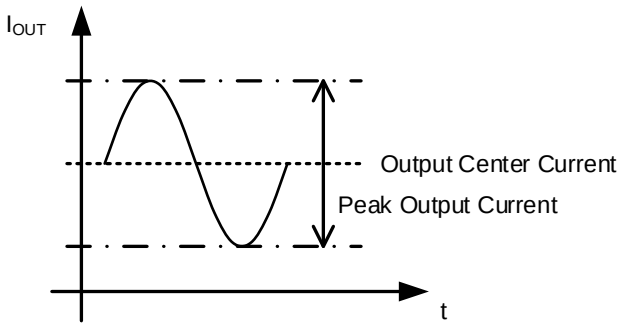


Figure 4. Peak Output Current

Measurement Circuit

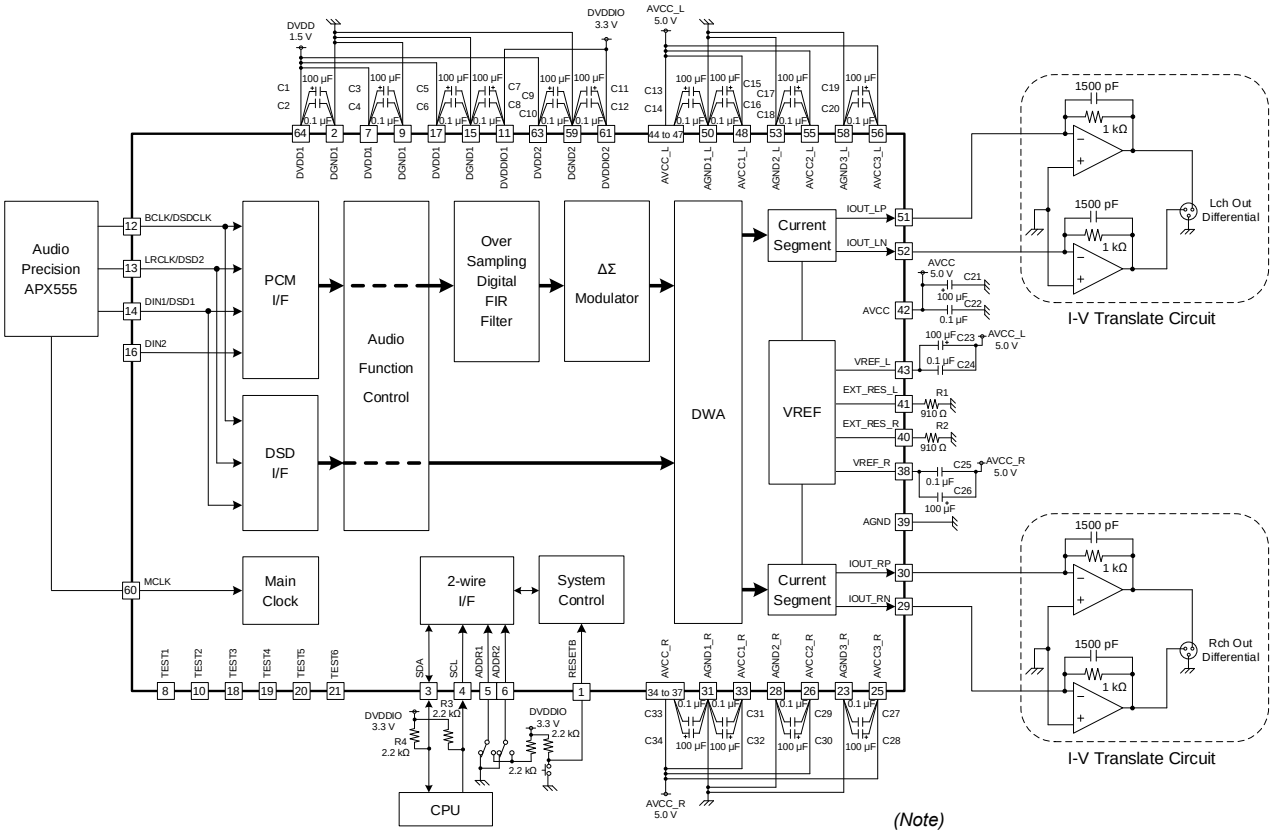


Figure 5. Measurement Circuit

(Note)
The written values of external parts are checked by sound test. Changing these values can affect the sound quality. Please check the sound when the values are changed.

DC Characteristics

Unless otherwise specified Ta = 25 °C, AVCC = 5.0 V, DVDDIO = 3.3 V, DVDD = 1.5 V

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
High Level Input Voltage	V_{IH}	0.8 x DVDDIO	-	-	V	RESETB, MCLK, BCLK/DSDCLK, LRCLK/DSD2, DIN1/DSD1, DIN2, ADDR1, ADDR2, SCL, SDA pin
Low Level Input Voltage	V_{IL}	-	-	0.2 x DVDDIO	V	
Input Leakage Current	I_{IN1}	-10	-	+10	µA	RESETB, MCLK, BCLK/DSDCLK, LRCLK/DSD2, DIN1/DSD1, SCL, SDA pin
	I_{IN2}	-500	-	+500	µA	DIN2, ADDR1, ADDR2 pin
Low Level Output Voltage	V_{OL}	-	-	0.4	V	SDA pin, I_O: 3 mA

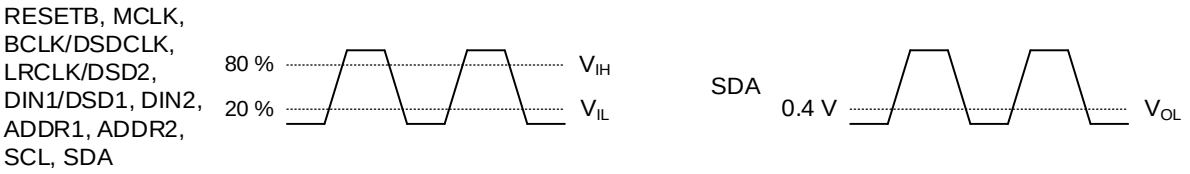


Figure 6. High/Low Level Specifications

AC Characteristics

1. MCLK, RESETB

Unless otherwise specified Ta = 25 °C, AVCC = 5.0 V, DVDDIO = 3.3 V, DVDD = 1.5 V

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
MCLK Frequency	f_{MCLK}	2.8224	-	49.1520	MHz	-
MCLK “H” Length	t_{MCH}	8.1	-	-	ns	-
MCLK “L” Length	t_{MCL}	8.1	-	-	ns	-
MCLK Duty	$DUTY_M$	40	50	60	%	$t_{MCH} / (t_{MCH} + t_{MCL})$
RESETB Pulse Width	t_{RST}	1	-	-	µs	-

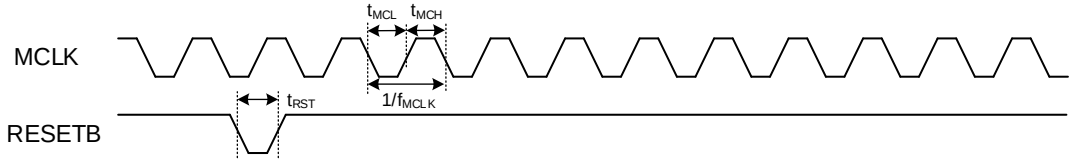


Figure 7. Timing Specifications of MCLK

AC Characteristics - continued

2. PCM I/F

Unless otherwise specified Ta = 25 °C, AVCC = 5.0 V, DVDDIO = 3.3 V, DVDD = 1.5 V

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
LRCLK Frequency	f_{LRC}	32	-	768	kHz	f_{LRC} = fs
LRCLK Hold Time	t_{LRH}	8.1	-	-	ns	-
LRCLK Setup Time	t_{LRSU}	8.1	-	-	ns	-
LRCLK Duty	$DUTY_L$	40	50	60	%	-
BCLK Frequency	f_{BC}	2.048	-	49.152	MHz	f_{BC} = 64 f_{LRC}
BCLK “H” Length	t_{BCH}	8.1	-	-	ns	-
BCLK “L” Length	t_{BCL}	8.1	-	-	ns	-
BCLK Duty	$DUTY_B$	40	50	60	%	t_{BCH} / (t_{BCH} + t_{BCL})
DIN1/DIN2 Setup Time	t_{DINS}	8.1	-	-	ns	-
DIN1/DIN2 Hold Time	t_{DINH}	8.1	-	-	ns	-

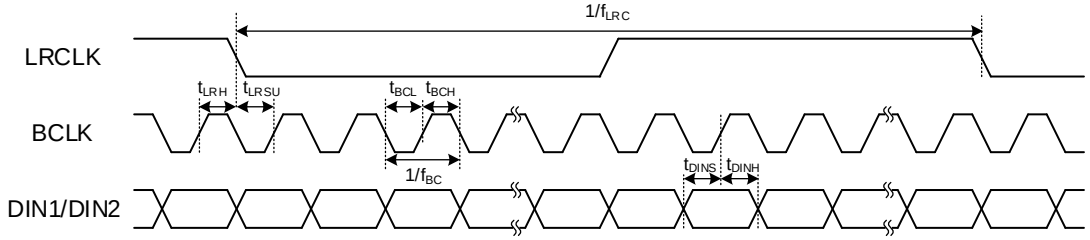


Figure 8. Timing Specifications of I²S

3. DSD I/F

Unless otherwise specified Ta = 25 °C, AVCC = 5.0 V, DVDDIO = 3.3 V, DVDD = 1.5 V

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
DSDCLK Frequency	f_{DSD}	2.8224	-	22.5792	MHz	-
DSDCLK Duty	$DUTY_D$	40	50	60	%	t_{DCH} / (t_{DCH} + t_{DCL})
DSDCLK “H” Length	t_{DCH}	17.7	-	-	ns	-
DSDCLK “L” Length	t_{DCL}	17.7	-	-	ns	-
DSD Data Setup Time	t_{DSDS}	17.7	-	-	ns	-
DSD Data Hold Time	t_{DSDH}	17.7	-	-	ns	-

DSD1 data and DSD2 data are output from Lch and Rch respectively.

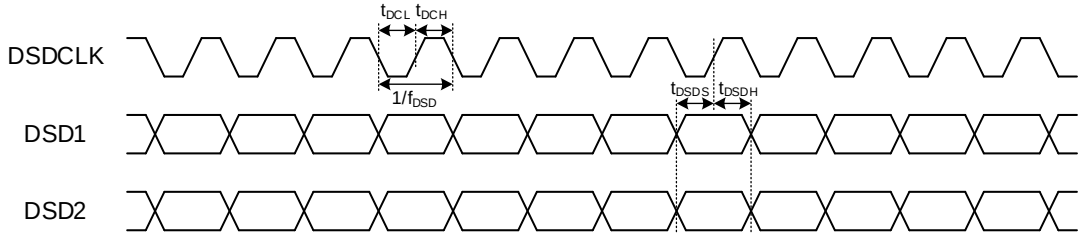


Figure 9. Timing Specifications of DSD

AC Characteristics - continued

4. 2-wire I/F

Unless otherwise specified Ta = 25 °C, AVCC = 5.0 V, DVDDIO = 3.3 V, DVDD = 1.5 V

Parameter	Symbol	Limit		Unit
		Min	Max	
SCL Clock Frequency	f_{SCL}	-	400	kHz
Bus Free Time between a STOP and START Condition	t_{BUF}	0.8	-	µs
Hold Time (Repeated) START Condition	t_{HD_STA}	0.4	-	µs
LOW Period of the SCL Clock	t_{LOW}	0.8	-	µs
HIGH Period of the SCL Cock	t_{HIGH}	0.4	-	µs
Setup Time for a Repeated START Condition	t_{SU_STA}	0.4	-	µs
Data Hold Time	t_{HD_DAT}	0	-	µs
Data Setup Time	t_{SU_DAT}	0.1	-	µs
Setup Time for STOP Condition	t_{SU_STO}	0.4	-	µs

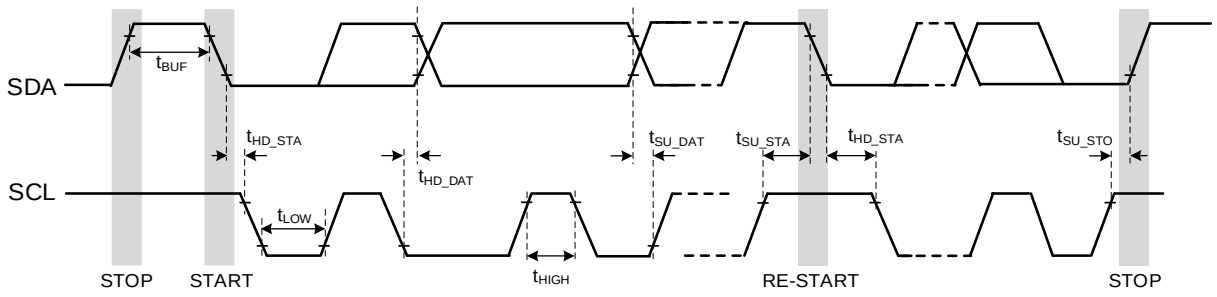


Figure 10. Timing Specifications of 2-wire I/F

Typical Performance Curves (Reference Data)

Unless otherwise specified Ta = 25 °C, AVCC = 5.0 V, DVDDIO = 3.3 V, DVDD = 1.5 V, Input signal frequency = 1 kHz, 20-kHz AES17 LPF, Differential output (XLR) measurement, PCM Mode, 24-bit I^2S, fs = 44.1 kHz, MCLK = 22.5792 MHz, Clock 1 (04h) = 02h, Clock 2 (06h) = 01h, FIR Filter 1 (30h) = 01h, FIR Filter 2 (31h) = 80h, Delta Sigma (40h) = 00h, DWA (68h) = 00h

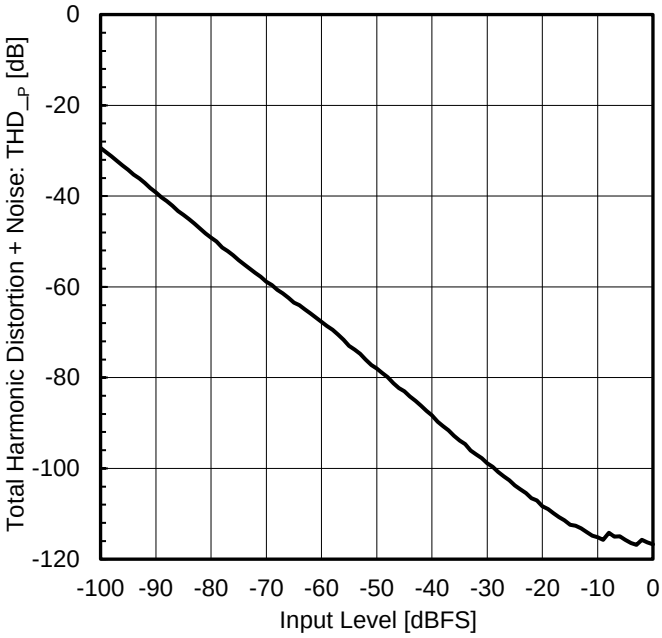


Figure 11. THD+N vs Input Level
(External LPF AUX-0025 (Audio Precision))

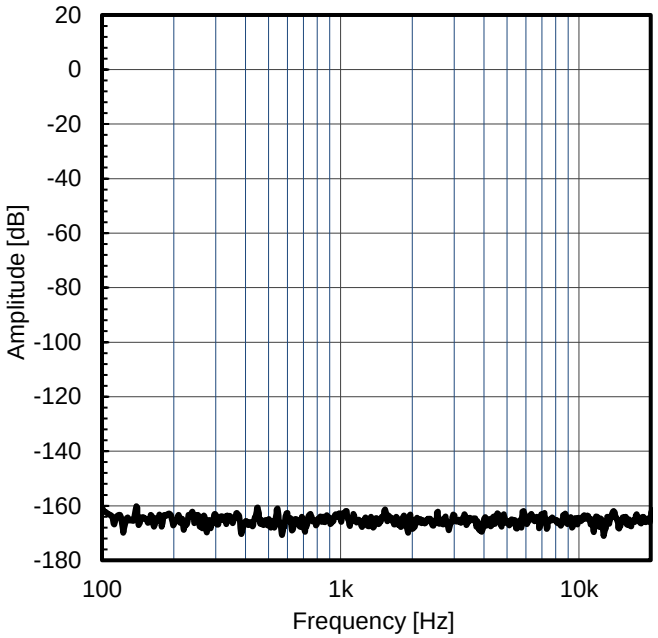


Figure 12. Amplitude vs Frequency
(Input Level = -∞ dBFS)

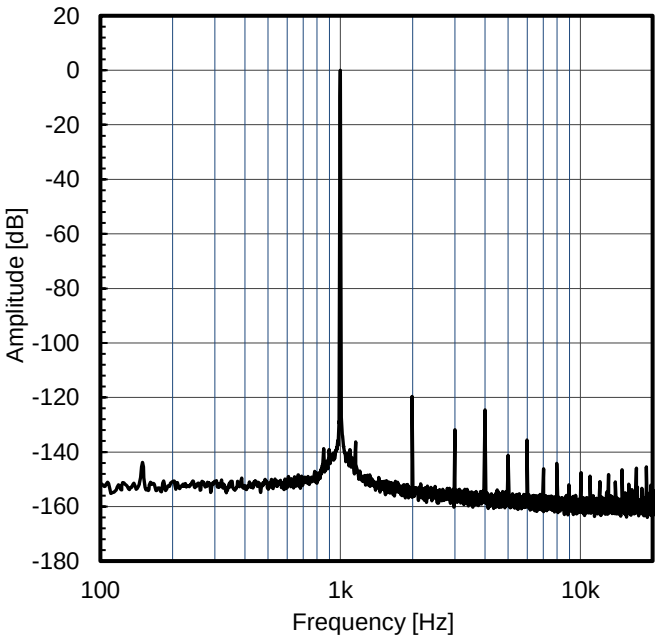


Figure 13. Amplitude vs Frequency
(Input Level = -3 dBFS)

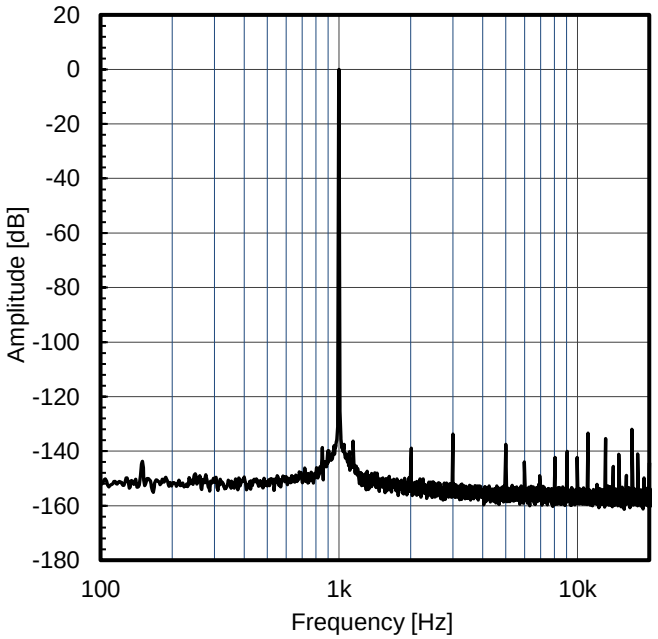


Figure 14. Amplitude vs Frequency
(Input Level = -3 dBFS,
Delta Sigma (40h) = 02h, DWA (68h) = 02h)

2-wire I/F

Format

Device address and 1 byte of register address are sent in data write-in and data read-out. The format of 2-wire I/F Target mode is shown below.

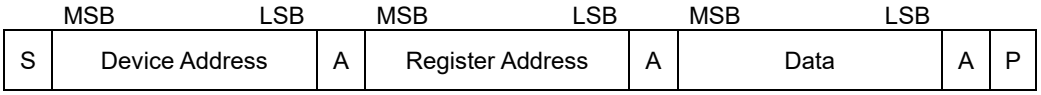


Figure 15. 2-wire I/F Transmission Format

S:	START Condition
Device Address:	Device Address of 8-bit data (MSB first)
A:	Acknowledge. Acknowledge bit is added to send and receive data every bite. When the correct data is sent and received, acknowledge is “L”. In the case of “H”, there is no acknowledge.
Register Address:	Register Address of 8-bit data (MSB first)
Data:	Write-in or Read-out data of 8-bit (MSB first)
P:	STOP Condition

START and STOP Conditions

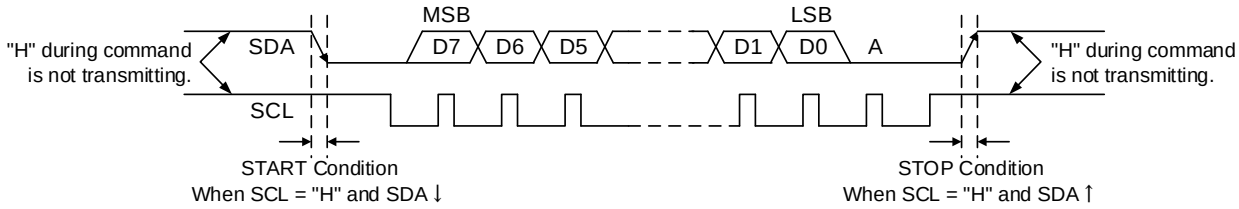


Figure 16. START and STOP Specifications

Device Address

The data format of the device address is shown below. Four device address can be selected by setting the ADDR1 and ADDR2 pins. The R/W bit sets the write (R/W = 0) or read (R/W = 1) mode.

MSB							LSB
D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	1	ADDR2	ADDR1	R/W

Figure 17. Device Address Data Format

The pins setting of Device Address are shown below.

Table 2. Pin Setting of Device Address

Pin Setting		Device Address	
ADDR2	ADDR1	Write-in (R/W = 0)	Read-out (R/W = 1)
L	L	38h	39h
L	H	3Ah	3Bh
H	L	3Ch	3Dh
H	H	3Eh	3Fh

2-wire I/F - continued

Write Operation

In case of write-in, the device address and register address are sent, and then the write data is sent. Auto incremental function allows consecutive data transmission. In case of forwarding data, repeat Step 6 to 7 of below table so that address will automatically be +1. When the register address reaches FFh, it does not increase and repeats FFh. In the example shown below, N consecutive registers from register address 20h are written.

S	Device Address	A	Register Address	A	Data 1	A	…	A	Data N	A	P
Ex	38h		20h		01h				EFh		

: from Controller to Target
: from Target to Controller
S : START Condition
P : STOP Condition
A : Acknowledge

Figure 18. Data Write-in Format

Table 3. Write Operation Sequence

Step	Bit	Controller	Target	Note
1	-	START Condition	-	-
2	8	Device Address	-	38h, 3Ah, 3Ch or 3Eh
3	1	-	Acknowledge	-
4	8	Register Address	-	Register Address 8-bit
5	1	-	Acknowledge	-
6	8	Write-in Data	-	Write Data 8-bit
7	1	-	Acknowledge	-
8	-	STOP Condition	-	-

Read Operation

In case of read-out, device address and register address are sent. Then, device address is sent again, and data is read. Acknowledge should not be returned after finishing the command. Auto incremental function allows consecutive data transmission. In case of forwarding consecutive data, repeat Step 9 to 10 of below table so that address will automatically be +1. When the register address reaches FFh, it does not increase and repeats FFh. In the example shown below, N consecutive registers from register address 30h are read.

S	Device Address	A	Register Address	A
Ex	38h		30h	

S	Device Address	A	Data 1	A	Data 2	A	…	A	Data N	Ā	P
Ex	39h										

: from Controller to Target
: from Target to Controller
S : START Condition
P : STOP Condition
A : Acknowledge
Ā : No Acknowledge

Figure 19. Data Read-out Format

Table 4. Read Operation Sequence

Step	Bit	Controller	Target	Note
1	-	START Condition	-	-
2	7	Device Address	-	38h, 3Ah, 3Ch or 3Eh
3	1	-	Acknowledge	-
4	8	Register Address	-	-
5	1	-	Acknowledge	-
6	1	START Condition	-	-
7	8	Device Address	-	39h, 3Bh, 3Dh or 3Fh
8	1	-	Acknowledge	-
9	8	-	Read-out Data	-
10	1	Acknowledge	-	-
11	-	STOP Condition	-	-

Register Map

Do not change the setting which 0 or 1 is assigned in register map. Otherwise, normal operation is not guaranteed.

Address	Register Name	R/W	Initial	D7	D6	D5	D4	D3	D2	D1	D0
00h	Software Reset	R/W	00h	0	0	0	0	0	0	0	SoftRst_X
01h	Chip Version	R	02h	ChipVer = 02h							
02h	Digital Power	R/W	00h	0	0	0	0	0	0	0	DigPon
03h	Analog Power	R/W	00h	0	0	0	0	0	0	0	AnaPon
04h	Clock 1	R/W	00h	0	0	0	MclkFreq	0	0	MclkDiv[1:0]	
05h	(Reserved)	R/W	00h	0	0	0	0	0	0	0	0
06h	Clock 2	R/W	00h	0	0	0	0	0	0	0	PhaseAdj
07h	(Reserved)	R/W	04h	0	0	0	0	0	1	0	0
↓	(Reserved)	R/W	00h	0	0	0	0	0	0	0	0
0Fh	(Reserved)	R/W	00h	0	0	0	0	0	0	0	0
10h	Audio I/F 1	R/W	0Bh	DsdOn	0	0	DsdMute Mode	Fmt[1:0]		WLen[1:0]	
11h	Audio I/F 2	R/W	00h	0	0	0	0	0	0	0	DoubleDin
12h	Audio I/F 3	R/W	00h	HdMono	0	0	0	0	0	MonoSel[1:0]	
13h	Audio I/F 4	R/W	00h	0	0	0	DsdLrSwap	0	0	0	PcmLrSwap
14h	Audio Output Polarity	R/W	00h	0	0	0	0	0	0	OutPol2	OutPol1
15h	DSD Full Scale Detection	R/W	00h	0	0	0	0	0	0	0	DsdFullDet_X
16h	DSD Filter	R/W	02h	0	0	0	0	DsdLvl	DsdFilter[2:0]		
17h	Audio Input Polarity	R/W	00h	0	0	0	0	0	0	InPol2	InPol1
18h	(Reserved)	R/W	00h	0	0	0	0	0	0	0	0
↓	(Reserved)	R/W	00h	0	0	0	0	0	0	0	0
1Fh	(Reserved)	R/W	00h	0	0	0	0	0	0	0	0
20h	PCM Volume Transition Time	R/W	48h	0	1	0	0	PcmVolTranTime[3:0]			
21h	PCM Volume 1	R/W	00h	PcmVol1[7:0]							
22h	PCM Volume 2	R/W	00h	PcmVol2[7:0]							
23h	DSD Volume Transition Time	R/W	08h	0	0	0	0	DsdVolTranTime[3:0]			
24h	DSD Volume 1	R/W	00h	DsdVol1[7:0]							
25h	DSD Volume 2	R/W	00h	DsdVol2[7:0]							
26h	(Reserved)	R/W	00h	0	0	0	0	0	0	0	0
↓	(Reserved)	R/W	00h	0	0	0	0	0	0	0	0
28h	(Reserved)	R/W	00h	0	0	0	0	0	0	0	0
29h	PCM Mute Transition Time	R/W	08h	0	0	0	0	PcmMuteTranTime[3:0]			
2Ah	Mute	R/W	00h	0	0	0	0	0	0	Mute2_X	Mute1_X
2Bh	(Reserved)	R/W	00h	0	0	0	0	0	0	0	0
↓	(Reserved)	R/W	00h	0	0	0	0	0	0	0	0
2Eh	(Reserved)	R/W	00h	0	0	0	0	0	0	0	0
2Fh	RAM Clear	R/W	00h	RamClr	0	0	0	0	0	0	0
30h	FIR Filter 1	R/W	00h	0	0	0	0	FirAlgo[3:0]			
31h	FIR Filter 2	R/W	00h	HpcMode	0	0	0	0	FirCoef[2:0]		
32h	(Reserved)	R/W	00h	0	0	0	0	0	0	0	0
33h	De-Emphasis 1	R/W	00h	0	0	0	0	0	0	DempFs[1:0]	
34h	De-Emphasis 2	R/W	00h	0	0	0	0	0	0	0	Demp
35h	(Reserved)	R/W	00h	0	0	0	0	0	0	0	0
↓	(Reserved)	R/W	00h	0	0	0	0	0	0	0	0
40h	Delta Sigma	R/W	00h	0	0	DsSetting[1:0]		0	0	DsOsr[1:0]	
41h	Setting 1	R/W	00h	Setting1[7:0]							
42h	Setting 2	R/W	00h	Setting2[7:0]							
43h	Setting 3	R/W	00h	Setting3[7:0]							
44h	(Reserved)	R/W	00h	0	0	0	0	0	0	0	0
↓	(Reserved)	R/W	00h	0	0	0	0	0	0	0	0
47h	(Reserved)	R/W	00h	0	0	0	0	0	0	0	0
48h	Setting 4	R/W	00h	Setting4[7:0]							
49h	(Reserved)	R/W	00h	0	0	0	0	0	0	0	0
↓	(Reserved)	R/W	00h	0	0	0	0	0	0	0	0
4Fh	(Reserved)	R/W	00h	0	0	0	0	0	0	0	0

Register Map - continued

Do not change the setting which 0 or 1 is assigned in register map. Otherwise, normal operation is not guaranteed.

Address	Register Name	R/W	Initial	D7	D6	D5	D4	D3	D2	D1	D0
50h	(Reserved)	R/W	00h	0	0	0	0	0	0	0	0
51h	Setting 5	R/W	00h	Setting5[7:0]							
52h	Setting 6	R/W	00h	Setting6[7:0]							
53h	(Reserved)	R/W	00h	0	0	0	0	0	0	0	0
↓	(Reserved)	R/W	00h	0	0	0	0	0	0	0	0
5Fh	(Reserved)	R/W	00h	0	0	0	0	0	0	0	0
60h	PCM Segment Control 1	R/W	00h	PcmSeg1[7:0]							
61h	PCM Segment Control 2	R/W	00h	PcmSeg2[7:0]							
62h	DSD Segment Control 1	R/W	00h	DsdSeg1[7:0]							
63h	DSD Segment Control 2	R/W	00h	DsdSeg2[7:0]							
64h	(Reserved)	R/W	00h	0	0	0	0	0	0	0	0
↓	(Reserved)	R/W	00h	0	0	0	0	0	0	0	0
67h	(Reserved)	R/W	00h	0	0	0	0	0	0	0	0
68h	DWA	R/W	00h	DsdDwa	0	DsdDwa Algo	0	0	0	PcmDwa Algo	0
69h	Setting 7	R/W	00h	Setting7[7:0]							
6Ah	(Reserved)	R/W	00h	0	0	0	0	0	0	0	0
↓	(Reserved)	R/W	00h	0	0	0	0	0	0	0	0
6Fh	(Reserved)	R/W	00h	0	0	0	0	0	0	0	0
70h	Mode Detect 1	R/W	00h	DsSetting1	0	DsOsr1[1:0]		HpcMode1	0	MclkDiv1[1:0]	
71h	Mode Detect 2	R/W	00h	DsSetting2	0	DsOsr2[1:0]		HpcMode2	0	MclkDiv2[1:0]	
72h	Mode Detect 3	R/W	00h	DsSetting3	0	DsOsr3[1:0]		HpcMode3	0	MclkDiv3[1:0]	
73h	Mode Detect 4	R/W	00h	DsSetting4	0	DsOsr4[1:0]		HpcMode4	0	MclkDiv4[1:0]	
74h	Mode Detect 5	R/W	00h	DsSetting5	0	DsOsr5[1:0]		HpcMode5	0	MclkDiv5[1:0]	
75h	Mode Detect 6	R/W	00h	DsSetting6	0	DsOsr6[1:0]		HpcMode6	0	MclkDiv6[1:0]	
76h	Mode Detect 7	R/W	00h	0	0	0	0	DsdLvl1	DsdFilter1[2:0]		
77h	Mode Detect 8	R/W	00h	0	0	0	0	DsdLvl2	DsdFilter2[2:0]		
78h	Mode Detect 9	R/W	00h	0	0	0	0	DsdLvl3	DsdFilter3[2:0]		
79h	Mode Detect 10	R/W	00h	0	0	0	0	DsdLvl4	DsdFilter4[2:0]		
7Ah	(Reserved)	R/W	00h	0	0	0	0	0	0	0	0
7Bh	Mode Detect Control	R/W	00h	0	0	0	0	0	0	DsdDetOn	PcmDetOn
7Ch	Mode Detect Status	R	00h	0	0	0	0	ModeDetStat[3:0]			
7Dh	(Reserved)	R/W	00h	0	0	0	0	0	0	0	0
↓	(Reserved)	R/W	00h	0	0	0	0	0	0	0	0
FFh	(Reserved)	R/W	00h	0	0	0	0	0	0	0	0

Register Description

1. Address 00h (Software Reset)

Address	Register Name	R/W	Initial	D7	D6	D5	D4	D3	D2	D1	D0
00h	Software Reset	R/W	00h	0	0	0	0	0	0	0	SoftRst_X

SoftRst_X: Software Reset Control
- 0 Software reset (All registers are not initialized) (default)
- 1 Normal operation

2. Address 01h (Chip Version)

Address	Register Name	R/W	Initial	D7	D6	D5	D4	D3	D2	D1	D0
01h	Chip Version	R	02h	ChipVer = 02h							

ChipVer: Chip Version Register (Read only)

3. Address 02h (Digital Power)

Address	Register Name	R/W	Initial	D7	D6	D5	D4	D3	D2	D1	D0
02h	Digital Power	R/W	00h	0	0	0	0	0	0	0	DigPon

DigPon: Digital Power Control
- 0 Power off and stop clock (default)
- 1 Power on and provide clock

4. Address 03h (Analog Power)

Address	Register Name	R/W	Initial	D7	D6	D5	D4	D3	D2	D1	D0
03h	Analog Power	R/W	00h	0	0	0	0	0	0	0	AnaPon

AnaPon: Analog Power Control
- 0 Power off (Current output off) (default)
- 1 Power on (Current output on)

5. Address 04h (Clock 1)

Address	Register Name	R/W	Initial	D7	D6	D5	D4	D3	D2	D1	D0
04h	Clock 1	R/W	00h	0	0	0	MclkFreq	0	0	MclkDiv[1:0]	

MclkFreq: MCLK Frequency
- 0 22.5792 MHz or 24.5760 MHz (default)
- 1 45.1584 MHz or 49.1520 MHz

MclkDiv[1:0]: MCLK Division Ratio Selection for Internal Clock
- 00 1 time (default)
- 01 2/3 times
- 10 1/2 times
- 11 1/3 times

There are some functions that cannot be used due to this setting. Please refer to the “System Clock” section for more details on the available register combinations.

Register Description - continued

6. Address 06h (Clock 2)

Address	Register Name	R/W	Initial	D7	D6	D5	D4	D3	D2	D1	D0
06h	Clock 2	R/W	00h	0	0	0	0	0	0	0	PhaseAdj

PhaseAdj: Phase Adjustment Control for Internal Clock
- 0 Phase adjustment disabled (default) Sound quality may be improved.
- 1 Phase adjustment enabled Audio characteristics may be improved.

(Note) When this function is enabled, follow the restriction below. Other settings are not guaranteed.
- In PCM mode, the over sampling rate of ΔΣ modulator DsOsr (40h[1:0]) = 10 cannot be used.
- In DSD mode, the MCLK frequency should be twice that of DSDCLK.

Refer to the "System Clock" section for the setting of MCLK frequency.

7. Address 10h (Audio I/F 1)

Address	Register Name	R/W	Initial	D7	D6	D5	D4	D3	D2	D1	D0
10h	Audio I/F 1	R/W	0Bh	DsdOn	0	0	DsdMute Mode	Fmt[1:0]		WLen[1:0]	

DsdOn: DSD Mode Selection
- 0 PCM mode (default)
- 1 DSD mode

DsdMuteMode: DSD Mute Enable (For DSD mode)
- 0 DSD mute enabled (default) On/off control by Mute (2Ah[1:0]) register is enabled.
- 1 DSD mute disabled

Fmt[1:0]: Audio Data Input Format (For PCM mode)
- 00 Right Justified
- 01 Left Justified
- 10 I^2S (default)
- 11 Prohibition

WLen[1:0]: Audio Data Input Bit Length (For PCM mode)
- 00 16-bit
- 01 20-bit
- 10 24-bit
- 11 32-bit (default)

Right Justified

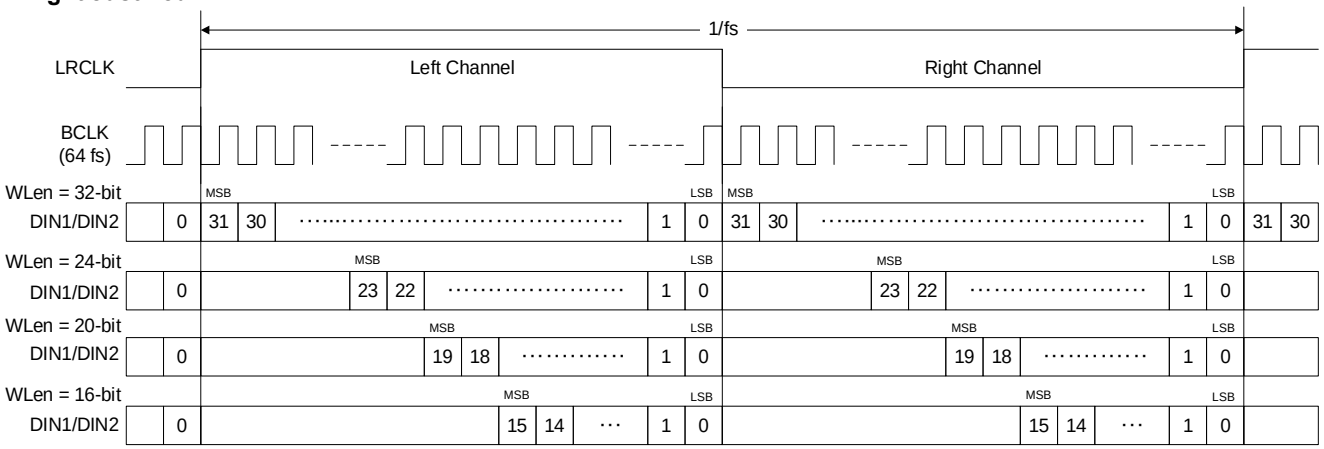


Figure 20. Audio Data Input Format: Right Justified

Address 10h (Audio I/F 1) - continued

Left Justified

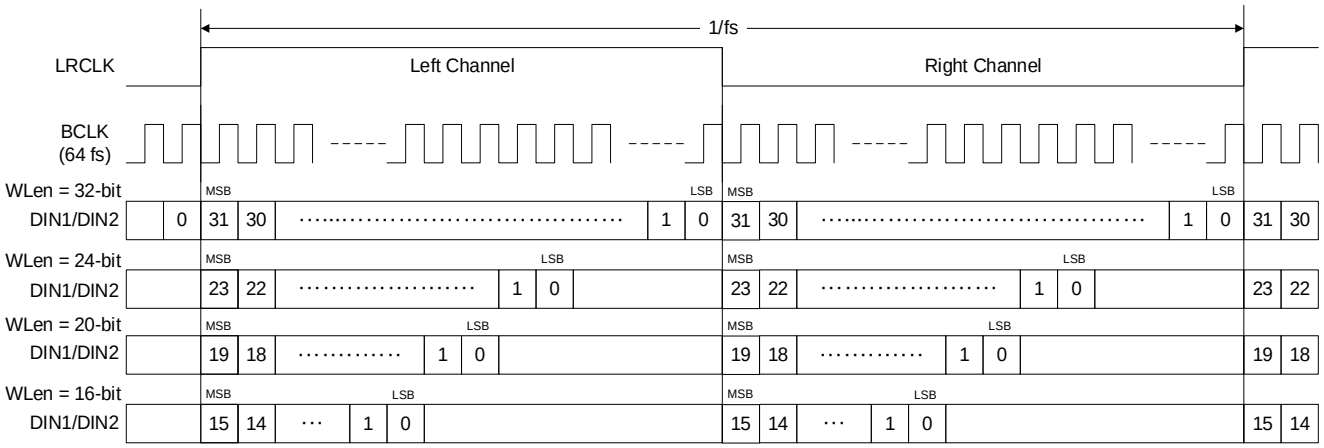


Figure 21. Audio Data Input Format: Left Justified

I²S

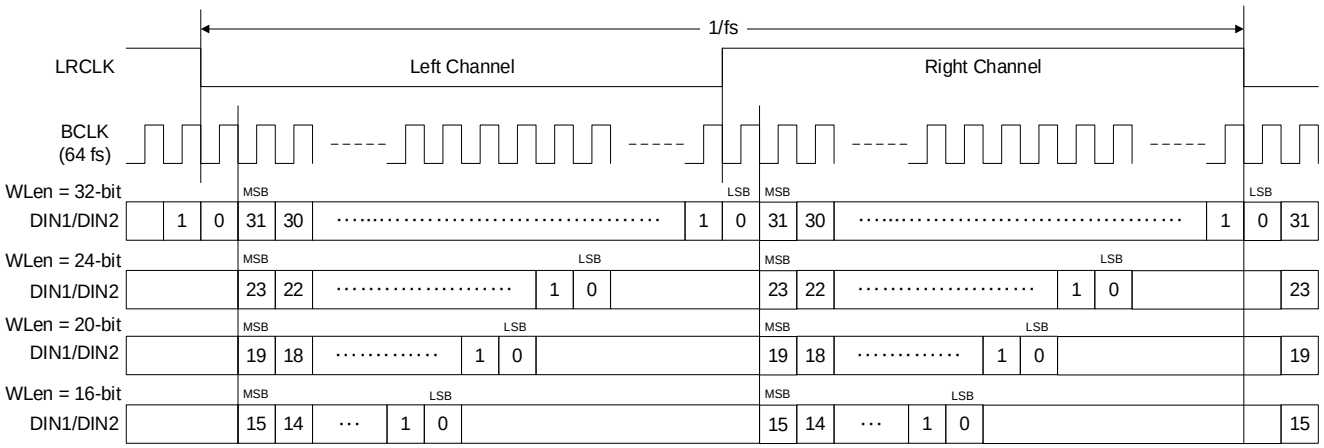


Figure 22. Audio Data Input Format: I²S

8. Address 11h (Audio I/F 2)

Address	Register Name	R/W	Initial	D7	D6	D5	D4	D3	D2	D1	D0
11h	Audio I/F 2	R/W	00h	0	0	0	0	0	0	0	Double Din

DoubleDin: Double Data Transfer Mode (For PCM mode)

0 Single date transfer (default) fs = 32 kHz to 768 kHz

1 Double data transfer fs = 1536 kHz

Use double data transfer for fs = 1536 kHz and single data transfer for fs = 32 kHz to 768 kHz. If double data transfer is not used, the DIN2 pin should be left open. The data input format for double data transfer is shown in the figure below.

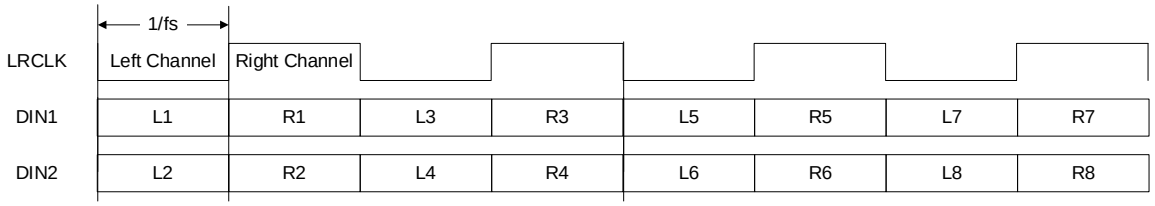


Figure 23. Double Data Transfer Format (For I²S)

Register Description - continued

9. Address 12h (Audio I/F 3)

Address	Register Name	R/W	Initial	D7	D6	D5	D4	D3	D2	D1	D0
12h	Audio I/F 3	R/W	00h	HdMono	0	0	0	0	0	MonoSel[1:0]	

MonoSel[1:0]: Monaural Mode Selection

Table 5. Stereo/Monaural Mode Settings for PCM Mode

MonoSel[1:0]	Mode	Lch Output	Rch Output	
00	Stereo Mode	Lch Input	Rch Input	(default)
01	Mixing Mode	(Lch Input + Rch Input)/2		
10	Monaural Mode Lch	Lch Input		
11	Monaural Mode Rch	Rch Input		

Table 6. Stereo/Monaural Mode Settings for DSD Mode

MonoSel[1:0]	Mode	Lch Output	Rch Output	
00	Stereo Mode	Lch Input	Rch Input	(default)
01	Stereo Mode	Lch Input	Rch Input	
10	Monaural Mode Lch	Lch Input		
11	Monaural Mode Rch	Rch Input		

HdMono: High Definition Monaural Mode Control

0 Monaural mode (default)
1 HD (High Definition) Monaural mode

When using HD (High Definition) monaural mode, the resolution of the current segment output can be improved, resulting in more natural sound quality. Audio characteristics may also be improved. For details on the application circuits in each mode, refer to the “Application Examples” section.

10. Address 13h (Audio I/F 4)

Address	Register Name	R/W	Initial	D7	D6	D5	D4	D3	D2	D1	D0
13h	Audio I/F 4	R/W	00h	0	0	0	Dsd LrSwap	0	0	0	Pcm LrSwap

PcmLrSwap: PCM Audio Data Swap Control (For PCM mode)

DsdLrSwap: DSD Audio Data Swap Control (For DSD mode)

Swap can be set separately in PCM and DSD modes.

Table 7. LR Swap Setting

PcmLrSwap DsdLrSwap	Lch Output	Rch Output	
0	Lch Input	Rch Input	(default)
1	Rch Input	Lch Input	

Register Description - continued

11. Address 14h (Audio Output Polarity)

Address	Register Name	R/W	Initial	D7	D6	D5	D4	D3	D2	D1	D0
14h	Audio Output Polarity	R/W	00h	0	0	0	0	0	0	OutPol2	OutPol1

OutPol1: Polarity Inversion Control for Lch
- 0 Normal (default)
- 1 Polarity inversion

OutPol2: Polarity Inversion Control for Rch
- 0 Normal (default)
- 1 Polarity inversion

12. Address 15h (DSD Full Scale Detection)

Address	Register Name	R/W	Initial	D7	D6	D5	D4	D3	D2	D1	D0
15h	DSD Full Scale Detection	R/W	00h	0	0	0	0	0	0	0	DsdFull Det_X

DsdFullDet_X: DSD Full Scale Detection (For DSD mode)
- 0 DSD full scale detection function on (default)
- 1 DSD full scale detection function off

If either DSD data inputs (DSD1/DSD2) has the same value for 128 consecutive clocks, it is judged to be full-scale data and the Lch/Rch outputs are immediately muted at the same time. Then, when zero data is detected while muted, muting will be released. The transition time at mute release is set to DsdVolTranTime (23h[3:0]).
(Note) When using the automatic mode switching function, DSD full scale detection function must be on.

13. Address 16h (DSD Filter)

Address	Register Name	R/W	Initial	D7	D6	D5	D4	D3	D2	D1	D0
16h	DSD Filter	R/W	02h	0	0	0	0	DsdLvl	DsdFilter[2:0]		

DsdFilter[2:0]: DSD Filter Selection (For DSD mode)

Table 8. Cut Off Frequency of DSD Filter

DsdFilter [2:0]	Cut Off Frequency				
	DSD 2.8 MHz	DSD 5.6 MHz	DSD 11.2 MHz	DSD 22.5 MHz	
0h	13 kHz	26 kHz	52 kHz	104 kHz	
1h	26 kHz	52 kHz	104 kHz	208 kHz	
2h	52 kHz	104 kHz	208 kHz	416 kHz	(default)
3h	Prohibition				
4h	19 kHz	39 kHz	78 kHz	157 kHz	
5h	39 kHz	78 kHz	157 kHz	314 kHz	
6h	78 kHz	157 kHz	314 kHz	628 kHz	
7h	Prohibition				

DsdLvl: DSD Output Level Control (For DSD mode)
- 0 Normal output level (0 dB) (default)
- 1 Double output level (+6 dB)

By setting the output level to double, the output level in DSD mode is doubled (+6 dB) compared to normal.
When using a double output level, the electrical characteristics of the DSD are not guaranteed.
(Note) If you want to use the double output level, be sure to set the DWA function to on (DsdDwa (68h[7]) = 1).

Register Description - continued

14. Address 17h (Audio Input Polarity)

Address	Register Name	R/W	Initial	D7	D6	D5	D4	D3	D2	D1	D0
17h	Audio Input Polarity	R/W	00h	0	0	0	0	0	0	InPol2	InPol1

InPol1: Polarity Inversion Control for Lch
0 Normal (default)
1 Polarity inversion

InPol2: Polarity Inversion Control for Rch
0 Normal (default)
1 Polarity inversion

15. Address 20h (PCM Volume Transition Time)

Address	Register Name	R/W	Initial	D7	D6	D5	D4	D3	D2	D1	D0
20h	PCM Volume Transition Time	R/W	48h	0	1	0	0	PcmVolTranTime[3:0]			

PcmVolTranTime[3:0]: PCM Volume Transition Time Selection (For PCM mode)

The table below shows the volume transition time when the gain is switched from 0 dB to -∞ dB. The volume transition time depends on the difference in the gain to be switched. For example, the volume transition time when the gain is switched from 0 dB to -6 dB is half the time in the table below.

Table 9. Volume Transition Time in PCM Mode

PcmVol TranTime [3:0]	Transition Time (ms)							
	32 kHz	44.1 kHz	48 kHz	96 kHz	192 kHz	384 kHz	768 kHz 1536 kHz	
0h	0							
1h to 7h	Prohibition							
8h	32.0	23.2	21.3	10.7	5.33	2.67	1.33	(default)
9h	64.0	46.4	42.7	21.3	10.7	5.33	2.67	
Ah	128	92.9	85.3	42.7	21.3	10.7	5.33	
Bh	256	186	171	85.3	42.7	21.3	10.7	
Ch	512	372	341	171	85.3	42.7	21.3	
Dh	1024	743	683	341	171	85.3	42.7	
Eh	2048	1486	1365	683	341	171	85.3	
Fh	4096	2972	2731	1365	683	341	171	

(For automatic mode switching)
When using the automatic mode switching, only the 8h to Bh setting can be used, and the operation of other settings cannot be guaranteed. The same transition time is automatically applied at fs = 48 kHz to 768 kHz.

Table 10. Volume Transition Time in PCM Mode (Automatic Mode Switching)

PcmVol TranTime [3:0]	Transition Time (ms)							
	32 kHz	44.1 kHz	48 kHz	96 kHz	192 kHz	384 kHz	768 kHz	
8h	32.0	23.2	21.3					(default)
9h	64.0	46.4	42.7					
Ah	128	92.9	85.3					
Bh	256	186	171					
Others	Prohibition							

Register Description - continued

16. Address 21h, 22h (PCM Volume 1, PCM Volume 2)

Address	Register Name	R/W	Initial	D7	D6	D5	D4	D3	D2	D1	D0
21h	PCM Volume 1	R/W	00h	PcmVol1[7:0]							
22h	PCM Volume 2	R/W	00h	PcmVol2[7:0]							

PcmVol1[7:0]: PCM Digital Volume (Attenuation Level) Setting for Lch (For PCM mode)
0 dB (00h default) to -127.0 dB (FEh), -∞ dB (FFh)
0.5 dB step
In Monaural mode, both Lch and Rch are controlled by PcmVol1[7:0].

PcmVol2[7:0]: PCM Digital Volume (Attenuation Level) Setting for Rch (For PCM mode)
0 dB (00h default) to -127.0 dB (FEh) , -∞ dB (FFh)
0.5 dB step
In Monaural mode, PcmVol2[7:0] is not used.

Table 11. PCM Volume (Attenuation Level) Setting

Setting	Gain (dB)	Setting	Gain (dB)	Setting	Gain (dB)	Setting	Gain (dB)	Setting	Gain (dB)	Setting	Gain (dB)	Setting	Gain (dB)	Setting	Gain (dB)
00h	0.0	20h	-16.0	40h	-32.0	60h	-48.0	80h	-64.0	A0h	-80.0	C0h	-96.0	E0h	-112.0
01h	-0.5	21h	-16.5	41h	-32.5	61h	-48.5	81h	-64.5	A1h	-80.5	C1h	-96.5	E1h	-112.5
02h	-1.0	22h	-17.0	42h	-33.0	62h	-49.0	82h	-65.0	A2h	-81.0	C2h	-97.0	E2h	-113.0
03h	-1.5	23h	-17.5	43h	-33.5	63h	-49.5	83h	-65.5	A3h	-81.5	C3h	-97.5	E3h	-113.5
04h	-2.0	24h	-18.0	44h	-34.0	64h	-50.0	84h	-66.0	A4h	-82.0	C4h	-98.0	E4h	-114.0
05h	-2.5	25h	-18.5	45h	-34.5	65h	-50.5	85h	-66.5	A5h	-82.5	C5h	-98.5	E5h	-114.5
06h	-3.0	26h	-19.0	46h	-35.0	66h	-51.0	86h	-67.0	A6h	-83.0	C6h	-99.0	E6h	-115.0
07h	-3.5	27h	-19.5	47h	-35.5	67h	-51.5	87h	-67.5	A7h	-83.5	C7h	-99.5	E7h	-115.5
08h	-4.0	28h	-20.0	48h	-36.0	68h	-52.0	88h	-68.0	A8h	-84.0	C8h	-100.0	E8h	-116.0
09h	-4.5	29h	-20.5	49h	-36.5	69h	-52.5	89h	-68.5	A9h	-84.5	C9h	-100.5	E9h	-116.5
0Ah	-5.0	2Ah	-21.0	4Ah	-37.0	6Ah	-53.0	8Ah	-69.0	AAh	-85.0	CAh	-101.0	EAh	-117.0
0Bh	-5.5	2Bh	-21.5	4Bh	-37.5	6Bh	-53.5	8Bh	-69.5	ABh	-85.5	CBh	-101.5	EBh	-117.5
0Ch	-6.0	2Ch	-22.0	4Ch	-38.0	6Ch	-54.0	8Ch	-70.0	ACh	-86.0	CCh	-102.0	ECh	-118.0
0Dh	-6.5	2Dh	-22.5	4Dh	-38.5	6Dh	-54.5	8Dh	-70.5	ADh	-86.5	CDh	-102.5	EDh	-118.5
0Eh	-7.0	2Eh	-23.0	4Eh	-39.0	6Eh	-55.0	8Eh	-71.0	AEh	-87.0	CEh	-103.0	EEh	-119.0
0Fh	-7.5	2Fh	-23.5	4Fh	-39.5	6Fh	-55.5	8Fh	-71.5	AFh	-87.5	CFh	-103.5	EFh	-119.5
10h	-8.0	30h	-24.0	50h	-40.0	70h	-56.0	90h	-72.0	B0h	-88.0	D0h	-104.0	F0h	-120.0
11h	-8.5	31h	-24.5	51h	-40.5	71h	-56.5	91h	-72.5	B1h	-88.5	D1h	-104.5	F1h	-120.5
12h	-9.0	32h	-25.0	52h	-41.0	72h	-57.0	92h	-73.0	B2h	-89.0	D2h	-105.0	F2h	-121.0
13h	-9.5	33h	-25.5	53h	-41.5	73h	-57.5	93h	-73.5	B3h	-89.5	D3h	-105.5	F3h	-121.5
14h	-10.0	34h	-26.0	54h	-42.0	74h	-58.0	94h	-74.0	B4h	-90.0	D4h	-106.0	F4h	-122.0
15h	-10.5	35h	-26.5	55h	-42.5	75h	-58.5	95h	-74.5	B5h	-90.5	D5h	-106.5	F5h	-122.5
16h	-11.0	36h	-27.0	56h	-43.0	76h	-59.0	96h	-75.0	B6h	-91.0	D6h	-107.0	F6h	-123.0
17h	-11.5	37h	-27.5	57h	-43.5	77h	-59.5	97h	-75.5	B7h	-91.5	D7h	-107.5	F7h	-123.5
18h	-12.0	38h	-28.0	58h	-44.0	78h	-60.0	98h	-76.0	B8h	-92.0	D8h	-108.0	F8h	-124.0
19h	-12.5	39h	-28.5	59h	-44.5	79h	-60.5	99h	-76.5	B9h	-92.5	D9h	-108.5	F9h	-124.5
1Ah	-13.0	3Ah	-29.0	5Ah	-45.0	7Ah	-61.0	9Ah	-77.0	BAh	-93.0	DAh	-109.0	FAh	-125.0
1Bh	-13.5	3Bh	-29.5	5Bh	-45.5	7Bh	-61.5	9Bh	-77.5	BBh	-93.5	DBh	-109.5	FBh	-125.5
1Ch	-14.0	3Ch	-30.0	5Ch	-46.0	7Ch	-62.0	9Ch	-78.0	BCh	-94.0	DCh	-110.0	FCh	-126.0
1Dh	-14.5	3Dh	-30.5	5Dh	-46.5	7Dh	-62.5	9Dh	-78.5	BDh	-94.5	DDh	-110.5	FDh	-126.5
1Eh	-15.0	3Eh	-31.0	5Eh	-47.0	7Eh	-63.0	9Eh	-79.0	BEh	-95.0	DEh	-111.0	FEh	-127.0
1Fh	-15.5	3Fh	-31.5	5Fh	-47.5	7Fh	-63.5	9Fh	-79.5	BFh	-95.5	DFh	-111.5	FFh	-∞

Example of Volume Switching (fs = 44.1 kHz)
In case of setting PcmVolTranTime (20h[3:0]) = 23.2 ms (8h), PcmVol1 (21h[7:0]) = -∞ dB (FFh), 0 dB (00h)

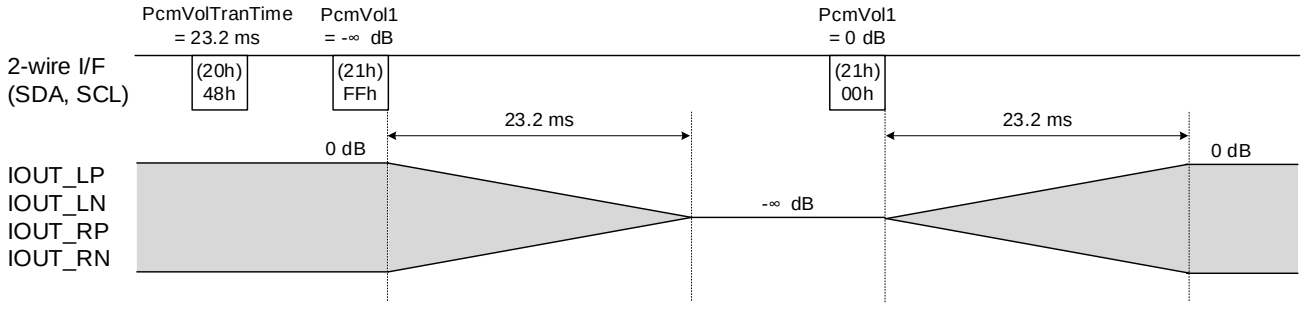


Figure 24. Example of Volume Switching

Register Description - continued

17. Address 23h (DSD Volume Transition Time)

Address	Register Name	R/W	Initial	D7	D6	D5	D4	D3	D2	D1	D0
23h	DSD Volume Transition Time	R/W	08h	0	0	0	0	DsdVolTranTime[3:0]			

DsdVolTranTime[3:0]: DSD Volume Transition Time Selection (For DSD mode)

The table below shows the volume transition time when switching from 0 dB to -∞ dB. The volume transition time depends on the difference in the gain to be switched. For example, when switching from 0 dB to -6 dB, the volume transition time is half the time shown in the table below.

Table 12. Volume Transition Time in DSD Mode

DsdVol TranTime [3:0]	Transition Time (ms)				
	2.8224 MHz	5.6448 MHz	11.2896 MHz	22.5792 MHz	
0h	0				
1h to 7h	Prohibition				
8h	17.41	8.71	4.35	2.18	(default)
9h	34.83	17.41	8.71	4.35	
Ah	69.66	34.83	17.41	8.71	
Bh	139.32	69.66	34.83	17.41	
Ch	278.64	139.32	69.66	34.83	
Dh	557.28	278.64	139.32	69.66	
Eh	1114.56	557.28	278.64	139.32	
Fh	2229.12	1114.56	557.28	278.64	

(For automatic mode switching)
When using automatic mode switching, only the 8h to Ch setting can be used, and the operation of other settings cannot be guaranteed. The same transition time is automatically applied at 2.8224 MHz to 22.5792 MHz.

Table 13. Volume Transition Time in DSD Mode (Automatic Mode Switching)

DsdVol TranTime [3:0]	Transition Time (ms)				
	2.8224 MHz	5.6448 MHz	11.2896 MHz	22.5792 MHz	
8h	17.41				(default)
9h	34.83				
Ah	69.66				
Bh	139.32				
Ch	278.64				
Others	Prohibition				

In DSD mode, the volume and mute transition time are the same, and the DsdVolTranTime (23h[3:0]) setting is applied. On the other hand, in PCM mode, the volume and mute transition time can be set separately, PcmVolTranTime (20h[3:0]) is applied to the volume transition time and PcmMuteTranTime (29h[3:0]) is applied to the mute transition time.

Register Description - continued

18. Address 24h, 25h (DSD Volume 1, DSD Volume 2)

Address	Register Name	R/W	Initial	D7	D6	D5	D4	D3	D2	D1	D0
24h	DSD Volume 1	R/W	00h	DsdVol1[7:0]							
25h	DSD Volume 2	R/W	00h	DsdVol2[7:0]							

The output level is set to 0 dB when DsdVol1[7:0] = 00h / DsdVol2[7:0] = 00h.

DsdVol1[7:0]: DSD Digital Volume (Attenuation Level) Setting for Lch (For DSD mode)
0 dB (00h default) to -39.6 dB (5Fh), -∞ dB (60h to FFh)
In monaural mode, the volume setting of DsdVol1[7:0] is used for both Lch and Rch.

DsdVol2[7:0]: DSD Digital Volume (Attenuation Level) Setting for Rch (For DSD mode)
0 dB (00h default) to -39.6 dB (5Fh), -∞ dB (60h to FFh)
In monaural mode, DsdVol2[7:0] volume setting is not used.

Table 14. DSD Volume (Attenuation Level) Setting (Normal Output Level)

Setting	Gain (dB)	Setting	Gain (dB)	Setting	Gain (dB)	Setting	Gain (dB)	Setting	Gain (dB)	Setting	Gain (dB)	Setting	Gain (dB)
00h	0.0	10h	-1.6	20h	-3.5	30h	-6.0	40h	-9.5	50h	-15.6	60h	-∞
01h	-0.1	11h	-1.7	21h	-3.7	31h	-6.2	41h	-9.8	51h	-16.1	↓	-∞
02h	-0.2	12h	-1.8	22h	-3.8	32h	-6.4	42h	-10.1	52h	-16.7	FFh	-∞
03h	-0.3	13h	-1.9	23h	-3.9	33h	-6.6	43h	-10.4	53h	-17.4		
04h	-0.4	14h	-2.0	24h	-4.1	34h	-6.8	44h	-10.7	54h	-18.1		
05h	-0.5	15h	-2.1	25h	-4.2	35h	-7.0	45h	-11.0	55h	-18.8		
06h	-0.6	16h	-2.3	26h	-4.4	36h	-7.2	46h	-11.3	56h	-19.6		
07h	-0.7	17h	-2.4	27h	-4.5	37h	-7.4	47h	-11.7	57h	-20.6		
08h	-0.8	18h	-2.5	28h	-4.7	38h	-7.6	48h	-12.0	58h	-21.6		
09h	-0.9	19h	-2.6	29h	-4.8	39h	-7.8	49h	-12.4	59h	-22.7		
0Ah	-1.0	1Ah	-2.7	2Ah	-5.0	3Ah	-8.0	4Ah	-12.8	5Ah	-24.1		
0Bh	-1.1	1Bh	-2.9	2Bh	-5.2	3Bh	-8.3	4Bh	-13.2	5Bh	-25.7		
0Ch	-1.2	1Ch	-3.0	2Ch	-5.3	3Ch	-8.5	4Ch	-13.6	5Ch	-27.6		
0Dh	-1.3	1Dh	-3.1	2Dh	-5.5	3Dh	-8.8	4Dh	-14.1	5Dh	-30.1		
0Eh	-1.4	1Eh	-3.3	2Eh	-5.7	3Eh	-9.0	4Eh	-14.5	5Eh	-33.6		
0Fh	-1.5	1Fh	-3.4	2Fh	-5.8	3Fh	-9.3	4Fh	-15.0	5Fh	-39.6		

Register Description - continued

19. Address 29h (PCM Mute Transition Time)

Address	Register Name	R/W	Initial	D7	D6	D5	D4	D3	D2	D1	D0
29h	PCM Mute Transition Time	R/W	08h	0	0	0	0	PcmMuteTranTime[3:0]			

PcmMuteTranTime[3:0]: PCM Mute Transition Time Selection (For PCM mode)

The table below shows the transition time when muting from 0 dB to -∞ dB. If the setting time is short, pop noise may occur. Please evaluate it carefully before determining the setting value.

Table 15. Mute Transition Time in PCM Mode

PcmMute TranTime [3:0]	Transition Time (ms)							
	32 kHz	44.1 kHz	48 kHz	96 kHz	192 kHz	384 kHz	768 kHz 1536 kHz	
0h	0							
1h to 7h	Prohibition							
8h	32.0	23.2	21.3	10.7	5.33	2.67	1.33	(default)
9h	64.0	46.4	42.7	21.3	10.7	5.33	2.67	
Ah	128	92.9	85.3	42.7	21.3	10.7	5.33	
Bh	256	186	171	85.3	42.7	21.3	10.7	
Ch	512	372	341	171	85.3	42.7	21.3	
Dh	1024	743	683	341	171	85.3	42.7	
Eh	2048	1486	1365	683	341	171	85.3	
Fh	4096	2972	2731	1365	683	341	171	

(For automatic mode switching)
When using automatic mode switching, only the 8h to Bh setting can be used, and the operation of other settings cannot be guaranteed. The same transition time is automatically applied at fs = 48 kHz to 768 kHz.

Table 16. Mute Transition Time in PCM Mode (Automatic Mode Switching)

PcmMute TranTime [3:0]	Transition Time (ms)							
	32 kHz	44.1 kHz	48 kHz	96 kHz	192 kHz	384 kHz	768 kHz	
8h	32.0	23.2	21.3					(default)
9h	64.0	46.4	42.7					
Ah	128	92.9	85.3					
Bh	256	186	171					
Others	Prohibition							

Register Description - continued

20. Address 2Ah (Mute)

Address	Register Name	R/W	Initial	D7	D6	D5	D4	D3	D2	D1	D0
2Ah	Mute	R/W	00h	0	0	0	0	0	0	Mute2_X	Mute1_X

Mute1_X: Digital Mute Control for Lch
0 Mute on (default)
1 Mute off

Mute2_X: Digital Mute Control for Rch
0 Mute on (default)
1 Mute off

In PCM mode, the Lch and Rch mute on/off control must be at the same timing. Therefore, set Mute (2Ah[1:0]) = 00 when mute is on and Mute (2Ah[1:0]) = 11 when mute is off. In DSD mode, Lch and Rch can be controlled at different timings.

Example of Mute switching (fs = 44.1 kHz)
In case of setting PcmMuteTranTime (29h[3:0]) = 23.2 ms (8h), Mute (2Ah[1:0])= Off (3h), On (0h)

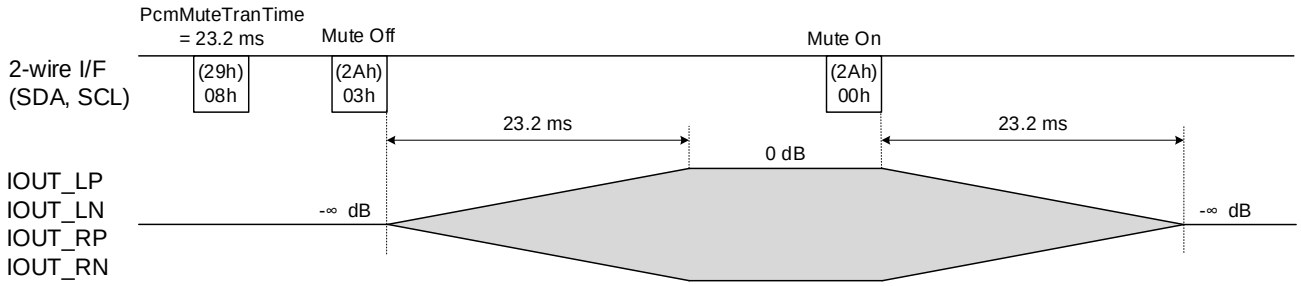


Figure 25. Example of Mute On/Off

21. Address 2Fh (RAM Clear)

Address	Register Name	R/W	Initial	D7	D6	D5	D4	D3	D2	D1	D0
2Fh	RAM Clear	R/W	00h	RamClr	0	0	0	0	0	0	0

RamClr: RAM Clear and Initialization Control (For PCM mode)
0 RAM clear off (default)
1 RAM clear on

If you change the clock or filter settings, be sure to turn RAM clear on and off. For more information, refer to the "Mode Switching Sequence" section.

Register Description - continued

22. Address 30h, 31h (FIR Filter 1, FIR Filter 2)

Address	Register Name	R/W	Initial	D7	D6	D5	D4	D3	D2	D1	D0
30h	FIR Filter 1	R/W	00h	0	0	0	0	FirAlgo[3:0]			
31h	FIR Filter 2	R/W	00h	HpcMode	0	0	0	0	FirCoef[2:0]		

FirAlgo[3:0]: FIR Calculation Algorithm Selection (For PCM mode)

FirCoef[2:0]: FIR Coefficient Selection (For PCM mode)

Follow the table below to configure the FIR filter. For the frequency characteristics of each filter, refer to the "Frequency Response of FIR Filter" section. If you change the filter settings, be sure to perform a mode switching sequence. When the RAM is cleared in the mode switching sequence, the filter settings are reflected. For more information, refer to the "Mode Switching Sequence" section.

Table 17. FIR Filter Setting

FirAlgo[3:0]	FirCoef[2:0]	fs (kHz)	Filter Setting	
0h	0h	-	FIR Stop (-∞ dB Output)	(default)
1h	0h	32 44.1 48	Sharp Roll-Off	
	3h		Slow Roll-Off	
2h	1h	88.2 96	Sharp Roll-Off	
	4h		Slow Roll-Off	
4h	2h	176.4 192	Sharp Roll-Off	
	5h		Slow Roll-Off	
8h	0h	352.8 384	FIR Bypass	
		705.6 768		
		1411.2 1536		
Others		Prohibition		

HpcMode: High Precision Calculation Mode Control (For PCM mode)

0 High precision calculation on (default)
1 High precision calculation off

This setting allows you to adjust the sound quality and audio characteristics. Note that when high precision calculation is turned on, the DVDD operating current also increases as the amount of calculation increases. Also, if the filter setting is FIR bypass, or if the MCLK division ratio (MclkDiv (04h[1:0])) = 10 or 11, this function is cannot be used and should be set to off. For more information on the register settings that can be configured, refer to the "System Clock" section.

Address 30h, 31h (FIR Filter 1, FIR Filter 2) - continued

Frequency Response of FIR Filter

Sharp Roll-Off Filter

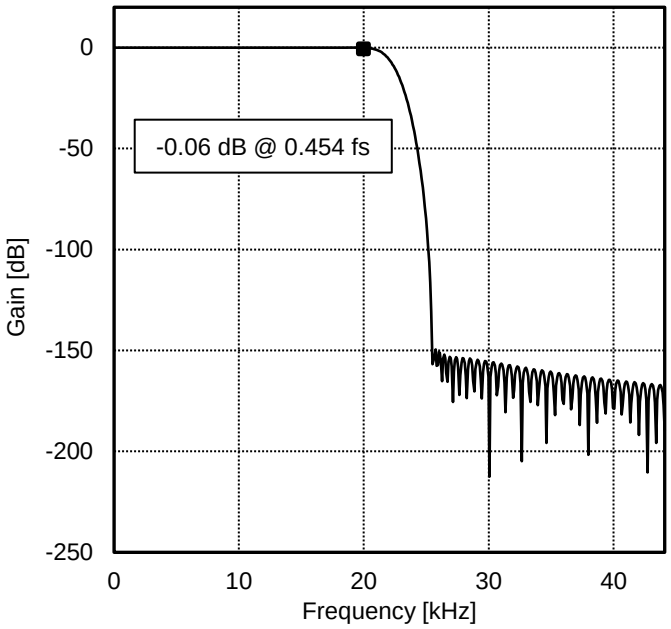


Figure 26. Gain vs Frequency
(fs = 44.1 kHz, Group Delay = 36/fs)

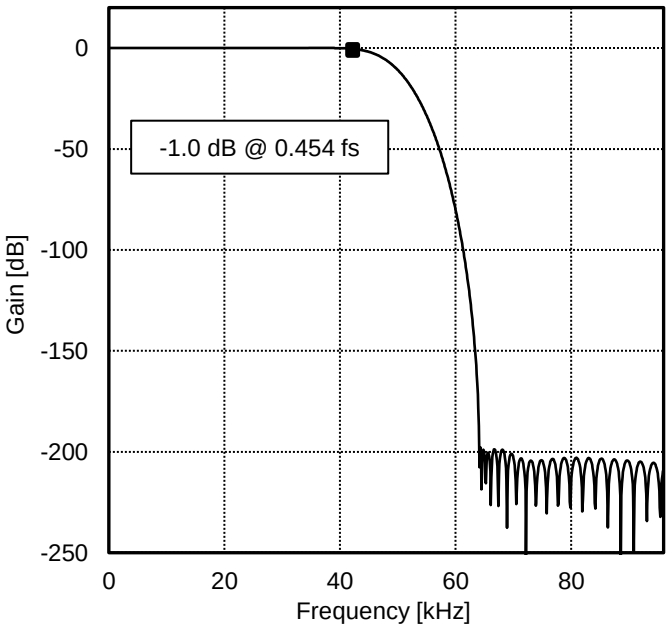


Figure 27. Gain vs Frequency
(fs = 96 kHz, Group Delay = 24/fs)

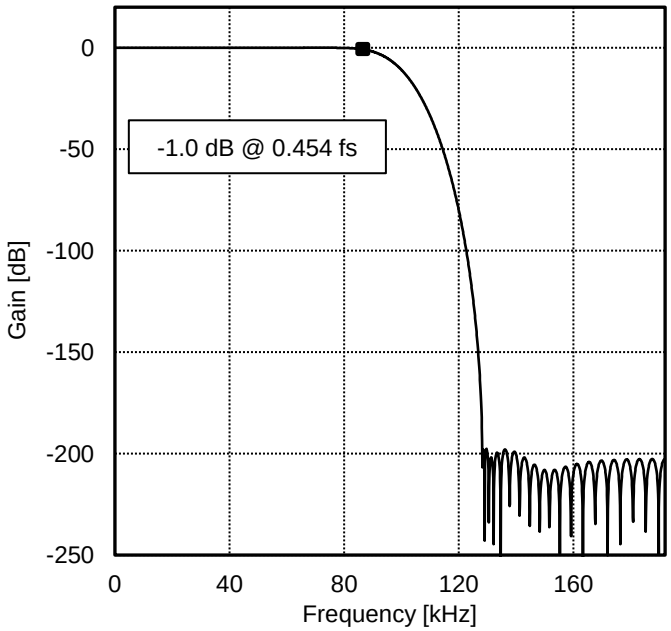


Figure 28. Gain vs Frequency
(fs = 192 kHz, Group Delay = 24/fs)

Address 30h, 31h (FIR Filter 1, FIR Filter 2) - continued

Frequency Response of FIR Filter

Slow Roll-Off Filter

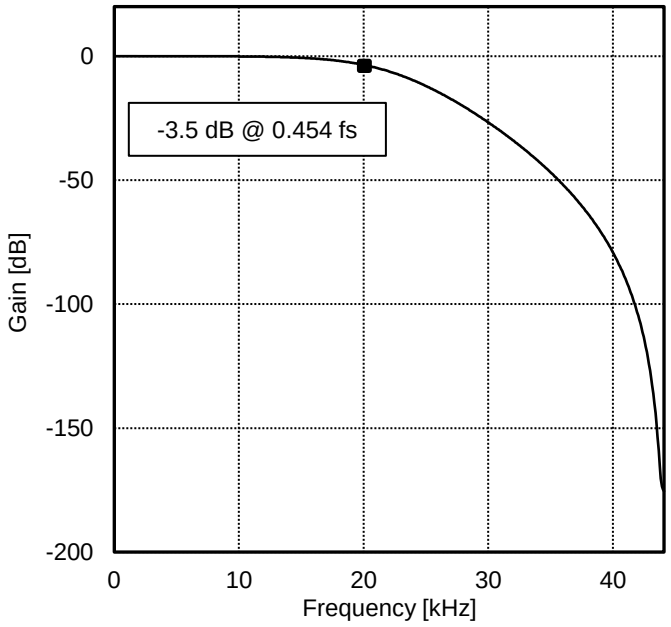


Figure 29. Gain vs Frequency
(fs = 44.1 kHz, Group Delay = 36/fs)

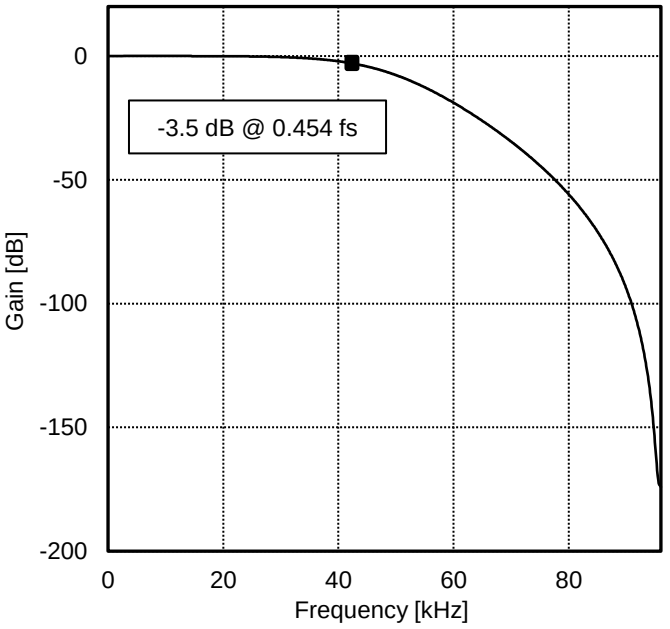


Figure 30. Gain vs Frequency
(fs = 96 kHz, Group Delay= 20/fs)

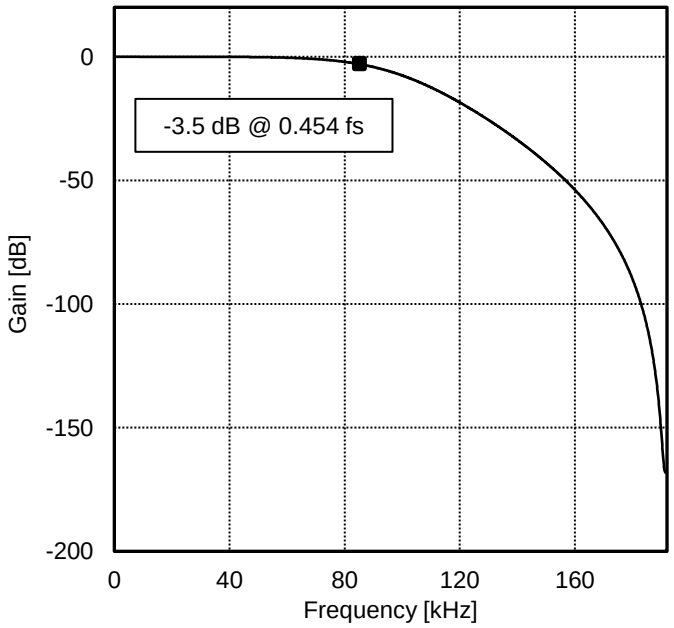


Figure 31. Gain vs Frequency
(fs = 192 kHz, Group Delay = 20/fs)

Register Description - continued

23. Address 33h, 34h (De-Emphasis 1, De-Emphasis 2)

Address	Register Name	R/W	Initial	D7	D6	D5	D4	D3	D2	D1	D0
33h	De-Emphasis 1	R/W	00h	0	0	0	0	0	0	DempFs[1:0]	
34h	De-Emphasis 2	R/W	00h	0	0	0	0	0	0	0	Demp

DempFs[1:0]: Sampling Frequency Selection for De-Emphasis (For PCM mode)
This register is available when De-Emphasis is enabled by Demp setting.
00 Through (De-Emphasis is disabled) (default)
01 fs = 32 kHz
10 fs = 44.1 kHz
11 fs = 48 kHz

The frequency responses are shown in the "Frequency Response of De-Emphasis Filter" section.

Demp: De-Emphasis Control for Lch/Rch (For PCM mode)
0 De-Emphasis disabled (default)
1 De-Emphasis enabled

Address 33h, 34h (De-Emphasis 1, De-Emphasis 2) - continued

Frequency Response of De-Emphasis Filter

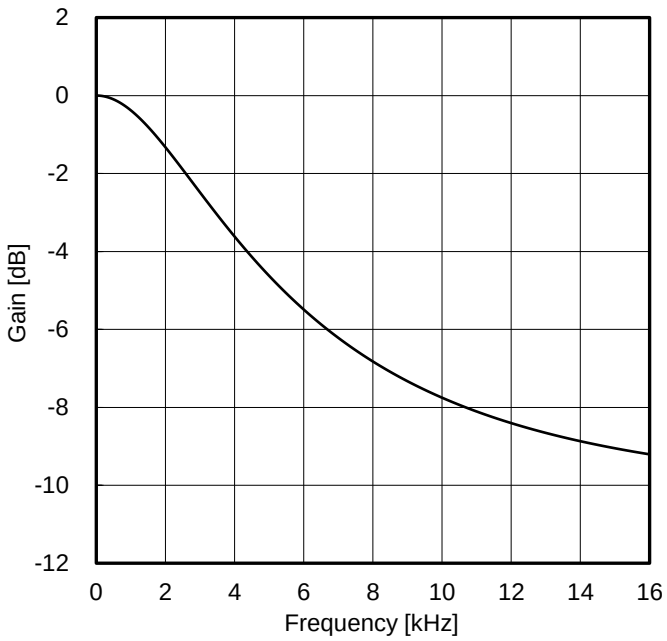


Figure 32. Gain vs Frequency
(fs = 32 kHz)

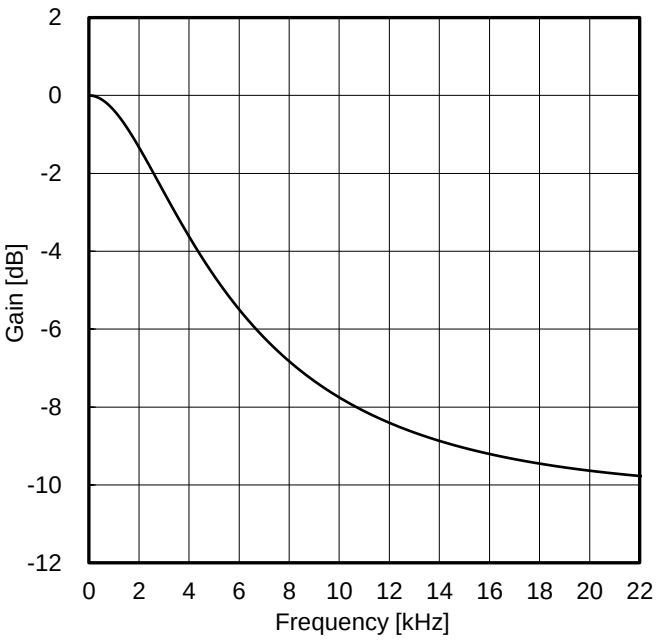


Figure 33. Gain vs Frequency
(fs = 44.1 kHz)

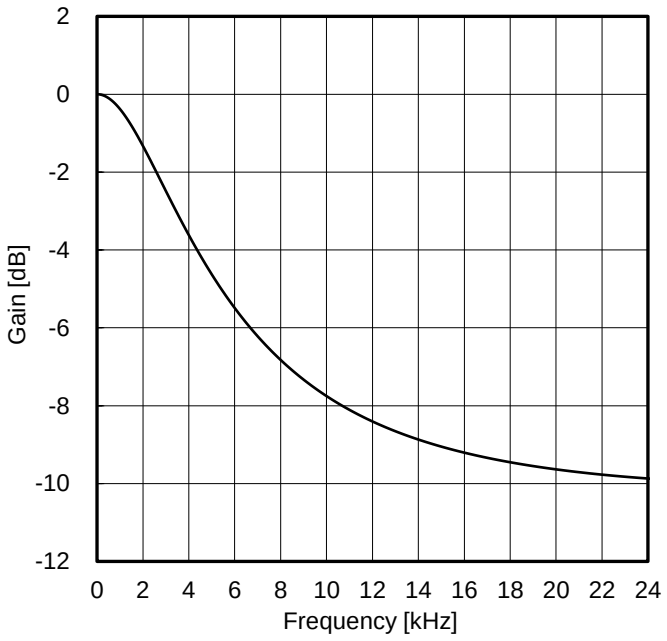


Figure 34. Gain vs Frequency
(fs = 48 kHz)

Register Description - continued

24. Address 40h (Delta Sigma)

Address	Register Name	R/W	Initial	D7	D6	D5	D4	D3	D2	D1	D0
40h	Delta Sigma	R/W	00h	0	0	DsSetting[1:0]		0	0	DsOsr[1:0]	

DsSetting[1:0]: ΔΣ Modulator Setting

DsOsr[1:0]: Over Sampling Rate Selection for ΔΣ Modulator

(PCM mode)
The over sampling rate of ΔΣ Modulator can be changed. The sound quality and audio characteristics are adjustable by this setting. This register must be changed according to the MCLK division ratio setting (MclkDiv (04h[1:0])).
Please refer to the "System Clock" section for more details on the available register combinations.

Table 18. Over Sampling Rate Setting of ΔΣ Modulator

DsSetting[1:0]	DsOsr[1:0]	Over Sampling Rate	
00	00	x 8	(default)
	01	x 16	
	10	x 32*(Note 2)*	
	11	Prohibition	
01	00	x 16	
	01	x 32*(Note 2)*	
	10	x 64*(Note 2)*	
	11	Prohibition	
10*(Note 1)*	00	x 4	
	01	x 8	
	10	x 16*(Note 2)*	
	11	Prohibition	
11	Prohibition		

(Note 1) Used only during double data transfer (fs = 1536 kHz).
(Note 2) When using DWA algorithm 2 (PcmDwaAlgo (68h[1]) = 1), only these settings can be used, Other settings are prohibited.

(DSD mode)
In DSD mode, over sampling rate of ΔΣ modulator cannot be changed. Always set DsSetting[1:0] = 00 and DsOsr[1:0] = 10.

Register Description - continued

25. Address 41h, 42h, 43h, 48h (Setting 1, Setting 2, Setting 3, Setting 4)

Address	Register Name	R/W	Initial	D7	D6	D5	D4	D3	D2	D1	D0
41h	Setting 1	R/W	00h	Setting1[7:0]							
42h	Setting 2	R/W	00h	Setting2[7:0]							
43h	Setting 3	R/W	00h	Setting3[7:0]							
48h	Setting 4	R/W	00h	Setting4[7:0]							

Setting1[7:0]: Set 00h
Setting2[7:0]: Set 34h
Setting3[7:0]: Set B8h
Setting4[7:0]: Set 0Dh

Set these registers in power-on sequence. Please refer to the "Power-On Sequence" section for more details.

26. Address 51h, 52h (Setting 5, Setting 6)

Address	Register Name	R/W	Initial	D7	D6	D5	D4	D3	D2	D1	D0
51h	Setting 5	R/W	00h	Setting5[7:0]							
52h	Setting 6	R/W	00h	Setting6[7:0]							

Setting5[7:0]: Set 10h
Setting6[7:0]: Set 08h

Set these registers in power-on sequence. Please refer to the "Power-On Sequence" section for more details.

Register Description - continued

27. Address 60h to 63h (PCM Segment 1 to 2, DSD Segment Control 1 to 2)

Address	Register Name	R/W	Initial	D7	D6	D5	D4	D3	D2	D1	D0
60h	PCM Segment Control 1	R/W	00h	PcmSeg1[7:0]							
61h	PCM Segment Control 2	R/W	00h	PcmSeg2[7:0]							
62h	DSD Segment Control 1	R/W	00h	DsdSeg1[7:0]							
63h	DSD Segment Control 2	R/W	00h	DsdSeg2[7:0]							

PcmSeg1[7:0]: Set the following value according to the DWA algorithm in PCM mode.
06h When DWA algorithm 1 is selected (PcmDwaAlgo (68h[1]) = 0)
07h When DWA algorithm 2 is selected (PcmDwaAlog (68h[1]) = 1)
PcmSeg2[7:0]: Set the same value as PcmSeg1.

DsdSeg1[7:0]: Set one of 0Dh/17h/1Dh.
DsdSeg2[7:0]: Set the same value as DsdSeg1.

28. Address 68h (DWA)

Address	Register Name	R/W	Initial	D7	D6	D5	D4	D3	D2	D1	D0
68h	DWA	R/W	00h	DsdDwa	0	DsdDwa Algo	0	0	0	PcmDwa Algo	0

DsdDwa: DSD DWA (Data Weighted Averaging) Control (For DSD mode)
0 DWA function is off (default)
1 DWA function is on
(Note) When using the double output level (DsdLvl (16h[3]) = 1), DWA function must be turned on. Otherwise, operation cannot be guaranteed.

DsdDwaAlog: DSD DWA (Data Weighted Averaging) Algorithm Selection (For DSD mode)
0 DWA algorithm 1 (default)
1 DWA algorithm 2
This is enabled when DWA function is turned on by DsdDwa register.

PcmDwaAlgo: PCM DWA (Data Weighted Averaging) Algorithm Selection (For PCM mode)
0 DWA Algorithm 1 (default)
1 DWA Algorithm 2
In PCM mode, DWA function is always on.
(Note) When using the DWA algorithm 2 in PCM mode, the over sampling rate of ΔΣ modulation (DsOsr (40h[1:0])) must be set to “x 32” or “x 64” (fs = 32 kHz to 384 kHz), “x 32” (fs = 768 kHz), or “x 16” (fs = 1536 kHz). Otherwise, operation cannot be guaranteed.

DWA (68h) and Segment Control (60h to 63h) registers can be set to adjust sound quality and audio characteristics. Separate DWA algorithms can be selected in PCM mode and DSD mode.

29. Address 69h (Setting 7)

Address	Register Name	R/W	Initial	D7	D6	D5	D4	D3	D2	D1	D0
69h	Setting 7	R/W	00h	Setting7[7:0]							

Setting7[7:0]: Set 01h

Set this register in power-on sequence. Please refer to the "Power-On Sequence" section for more details.

Register Description - continued

30. Address 70h to 79h (Mode Detect 1 to Mode Detect 10)

Address	Register Name	R/W	Initial	D7	D6	D5	D4	D3	D2	D1	D0
70h	Mode Detect 1 (PCM 32 kHz)	R/W	00h	DsSetting 1	0	DsOsr1[1:0]		HpcMode 1	0	MclkDiv1[1:0]	
71h	Mode Detect 2 (PCM 44.1 kHz)	R/W	00h	DsSetting 2	0	DsOsr2[1:0]		HpcMode 2	0	MclkDiv2[1:0]	
72h	Mode Detect 3 (PCM 96 kHz)	R/W	00h	DsSetting 3	0	DsOsr3[1:0]		HpcMode 3	0	MclkDiv3[1:0]	
73h	Mode Detect 4 (PCM 192 kHz)	R/W	00h	DsSetting 4	0	DsOsr4[1:0]		HpcMode 4	0	MclkDiv4[1:0]	
74h	Mode Detect 5 (PCM 384 kHz)	R/W	00h	DsSetting 5	0	DsOsr5[1:0]		HpcMode 5	0	MclkDiv5[1:0]	
75h	Mode Detect 6 (PCM 768 kHz)	R/W	00h	DsSetting 6	0	DsOsr6[1:0]		HpcMode 6	0	MclkDiv6[1:0]	
76h	Mode Detect 7 (DSD 2.8 MHz)	R/W	00h	0	0	0	0	DsdLvl1	DsdFilter1[2:0]		
77h	Mode Detect 8 (DSD 5.6 MHz)	R/W	00h	0	0	0	0	DsdLvl2	DsdFilter2[2:0]		
78h	Mode Detect 9 (DSD 11.2 MHz)	R/W	00h	0	0	0	0	DsdLvl3	DsdFilter3[2:0]		
79h	Mode Detect 10 (DSD 22.5 MHz)	R/W	00h	0	0	0	0	DsdLvl4	DsdFilter4[2:0]		

MclkDiv1[1:0] to MclkDiv6[1:0]: MCLK Division Ratio Selection for Internal Clock
These registers have the same function as MclkDiv (04h[1:0]).
Please refer to 04h[1:0] section for more details.

HpcMode1 to HpcMode6: High Precision Calculation Mode Control (For PCM mode)
These registers have the same function as HpcMode (31h[7]).
Please refer to 31h[7] section for more details.

DsOsr1[1:0] to DsOsr6[1:0]: Over Sampling Rate Selection for ΔΣ Modulator
These registers have the same function as DsOsr (40h[1:0]).
Please refer to 40h[1:0] section for more details.

DsSetting1 to DsSetting6: ΔΣ Modulator Setting
These registers have the same function as DsSetting (40h[4]).
Please refer to 40h[4] section for more details.

DsdFilter1[2:0] to DsdFilter4[2:0]: DSD Filter Selection (For DSD mode)
These registers have the same function as DsdFilter (16h[2:0])
Please refer to 16h[2:0] section for more details.

DsdLvl1 to DsdLvl4: DSD Output Level Control (For DSD mode)
These registers have the same function as DsdLvl (16h[3]).
Please refer to 16h[3] section for more details.
(Note) The same value must be set for DsdLvl1 to DsdLvl4.

These registers save the settings in each mode in advance when using the automatic mode switching function. Set Mode Detect 1 to 10 (70h to 79h) registers before turning on automatic mode switching function. The register setting corresponding to the detected mode is automatically reflected. Please refer to the "Automatic Mode Switching" section for more details.

Register Description - continued

31. Address 7Bh (Mode Detect Control)

Address	Register Name	R/W	Initial	D7	D6	D5	D4	D3	D2	D1	D0
7Bh	Mode Detect Control	R/W	00h	0	0	0	0	0	0	DsdDet On	PcmDet On

PcmDetOn: PCM Mode Detect Control (For PCM mode)
0 Automatic mode switching function off (default)
1 Automatic mode switching function on
This function supports mode switching from PCM 32 kHz to PCM 768 kHz.

DsdDetOn: DSD Mode Detect Control (For DSD mode)
0 Automatic mode switching function off (default)
1 Automatic mode switching function on
This function supports mode switching from DSD 2.8 MHz to DSD 22.5 MHz.

Automatic mode switching function can be turned on and off in PCM and DSD mode, respectively.
(Note) When either PCM mode or DSD mode is set to off, automatic mode switching between PCM mode and DSD mode is not performed. In this case, set registers manually according to the “Mode Switching Sequence”.

32. Address 7Ch (Mode Detect Status)

Address	Register Name	R/W	Initial	D7	D6	D5	D4	D3	D2	D1	D0
7Ch	Mode Detect Status	R	00h	0	0	0	0	ModeDetStat[3:0]			

ModeDetStat[3:0]: Mode Detect Status

This is a read-only register that returns the result of mode detection. The register settings corresponding to this detection result are automatically reflected. If the automatic mode switching function is turned off, 0h (not detected) is returned.

Table 19. Mode Detection Result

ModeDetStat[3:0]	Mode	Corresponding Register	
0h	Not Detected	-	(default)
1h	PCM 32 kHz	Mode Detect 1 (70h)	
2h	PCM 44.1 kHz	Mode Detect 2 (71h)	
3h	PCM 96 kHz	Mode Detect 3 (72h)	
4h	PCM 192 kHz	Mode Detect 4 (73h)	
5h	PCM 384 kHz	Mode Detect 5 (74h)	
6h	PCM 768 kHz	Mode Detect 6 (75h)	
7h	-	-	
8h	-	-	
9h	-	-	
Ah	DSD 2.8 MHz	Mode Detect 7 (76h)	
Bh	DSD 5.6 MHz	Mode Detect 8 (77h)	
Ch	DSD 11.2 MHz	Mode Detect 9 (78h)	
Dh	DSD 22.5 MHz	Mode Detect 10 (79h)	
Eh	-	-	
Fh	-	-	

System Clock

This section describes the system clock setting in PCM mode and DSD mode. When switching the system clock, it is necessary to execute the mode switching sequence. Please refer to the "Mode Switching Sequence" section for more details and refer to the "Recommended Settings" section for more details on recommended settings for each fs.

(PCM mode)

The system clocks required for PCM mode are MCLK, BCLK, and LRCLK. The system clocks must be synchronized, but not in phase. The MCLK can be input with a clock of 22.5792 MHz/24.5760 MHz or 45.1584 MHz/49.1520 MHz. Set the MCLK frequency with MclkFreq (04h[4]). When fs = 32 kHz/44.1 kHz/48 kHz, the frequency of the internal clock can be reduced by setting the MCLK division ratio register to (MclkDiv (04h[1:0]) = 10 (1/2 times) or 11 (1/3 times)). In this case, the high precision calculation (HpcMode (31h[7])) function cannot be used because the amount of computational processing is reduced. You also need to change the over sampling rate settings for the ΔΣ modulator (DsSetting (40h[5:4]), DsOsr (40h[1:0])) according to the MCLK division ratio. The table below shows the system clock frequency settings and the combinations of registers that can be set.

Table 20. System Clock Frequency Settings in PCM Mode

fs (kHz)	LRCLK (kHz)	BCLK (MHz)	MCLK (MHz)		MclkDiv (04h[1:0])		HpcMode (31h[7])		DsSetting (40h[5:4])	DsOsr (40h[1:0])	
32	32	2.0480	768 fs	24.5760	01	2/3 times	0/1	On/Off	01	00	x 6
										01	x 32
										10	x 64
					11	1/3 times	1	Off	00	00	x 8
										01	x 16
										10	x 32
44.1 48	44.1 48	2.8224 3.0720	512 fs	22.5792 24.5760	00	1 time	0/1	On/Off	01	00	x 16
										01	x 32
										10	x 64
					10	1/2 times	1	Off	00	00	x 8
										01	x 16
										10	x 32
88.2 96	88.2 96	5.6448 6.1440	256 fs	22.5792 24.5760	00	1 time	0/1	On/Off	01	00	x 16
										01	x 32
										10	x 64
176.4 192	176.4 192	11.2896 12.2880	128 fs	22.5792 24.5760	00	1 time	0/1	On/Off	01	00	x 16
										01	x 32
										10	x 64
352.8 384	352.8 384	22.5792 24.5760	64 fs	22.5792 24.5760	00	1 time	1	Off	01	00	x 16
										01	x 32
										10	x 64
705.6 768	705.6 768	45.1584 49.1520	32 fs	22.5792 24.5760	00	1 time	1	Off	00	00	x 8
										01	x 16
										10	x 32
1411.2 1536 *(Note 1)*	705.6 768	45.1584 49.1520	32 fs	22.5792 24.5760	00	1 time	1	Off	10	00	x 4
										01	x 8
										10	x 16

(Note 1) For fs = 1411.2 kHz/1536 kHz, double data transfer (DoubleDin (11h[0]) = 1)) must be used.

System Clock - continued

(DSD mode)
The system clocks required for DSD mode are MCLK and DSDCLK. The system clocks must be synchronized, but not in phase. The frequency of MCLK should be the same as or twice of DSDCLK. When the phase adjustment function for internal clock is enabled (PhaseAdj (06h[0]) = 1), the frequency of MCLK must be twice of DSDCLK. The following table shows system clock frequency settings.

Table 21. System Clock Frequency Setting in DSD Mode

DSDCLK (MHz)	MCLK (MHz)	
	PhaseAdj (06h[0])	
	0	1
2.8224	2.8224	5.6448
5.6448	5.6448	11.2896
11.2896	11.2896	22.5792
22.5792	22.5792	45.1584

Power-On Sequence

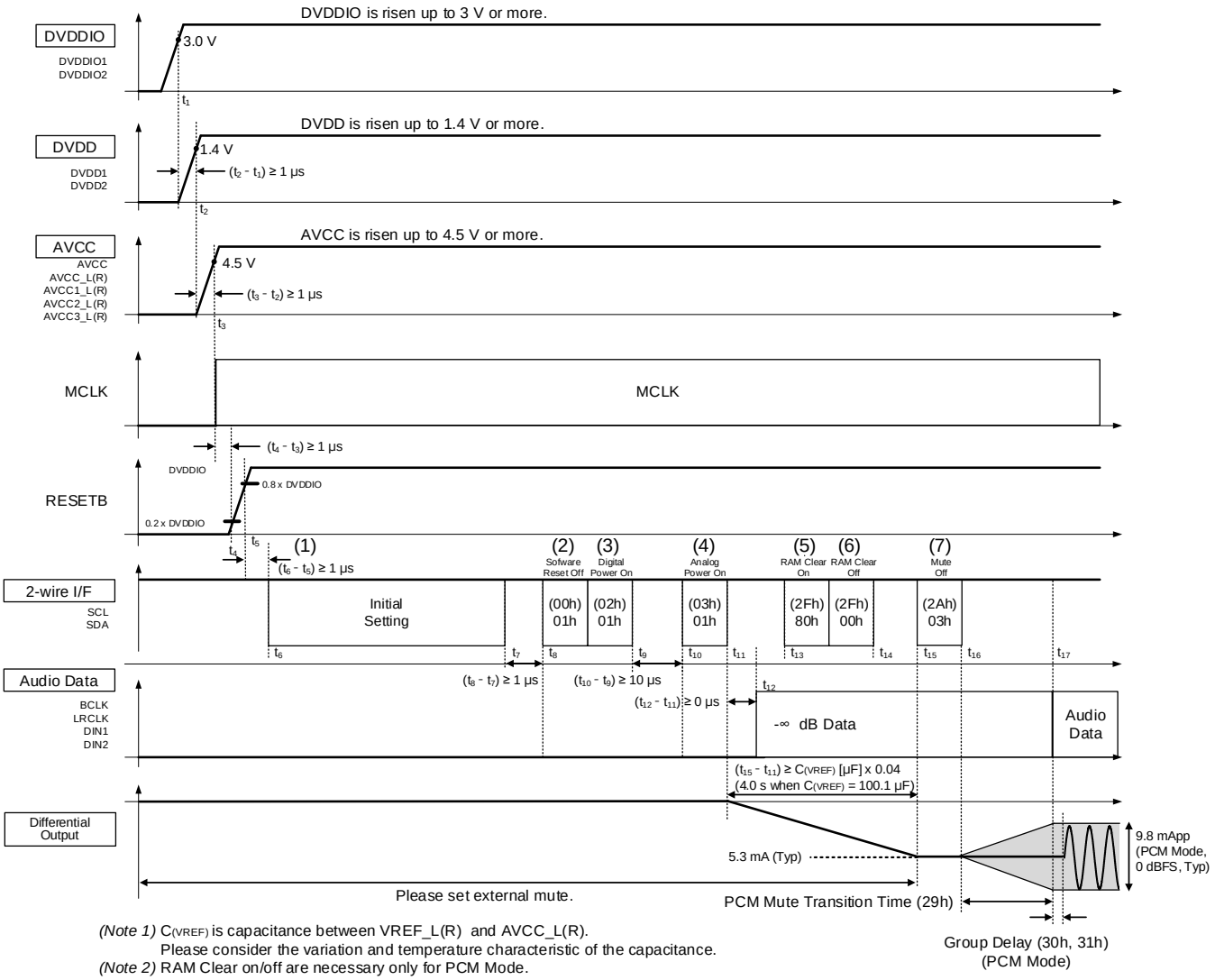
In the power-on sequence, the power supply is turned on in the order of DVDDIO, DVDD, and AVCC. After the power supply is turned on, input MCLK, release hard reset (RESETB), and set register with 2-wire I/F. When the power supply is turned on, all registers must be initialized. Please execute the power-on sequence according to the following register setting and timing charts. If the sequence is not followed, normal operation cannot be guaranteed.

Table 22. Register Settings in Power-On Sequence

Step	Operations	Register Address	Register Settings
1	Initial Setting	04h	Clock 1
		06h	Clock 2
		10h	Audio I/F 1
		11h	Audio I/F 2
		12h	Audio I/F 3
		13h	Audio I/F 4
		14h	Audio Output Polarity
		16h	DSD Filter
		17h	Audio Input Polarity
		20h	PCM Volume Transition Time
		21h	PCM Volume 1
		22h	PCM Volume 2
		23h	DSD Volume Transition Time
		24h	DSD Volume 1
		25h	DSD Volume 2
		29h	PCM Mute Transition Time
		30h	FIR Filter 1
		31h	FIR Filter 2
		33h	De-Emphasis 1
		34h	De-Emphasis 2
		40h	Delta Sigma
		41h	Setting 1 = 00h
		42h	Setting 2 = 34h
		43h	Setting 3 = B8h
		48h	Setting 4 = 0Dh
		51h	Setting 5 = 10h
		52h	Setting 6 = 08h
		60h to 63h	Segment Control
		68h	DWA
		69h	Setting 7 = 01h
		70h to 79h	Mode Detect 1 to 10
		7Bh	Mode Detect Control
2	Software Reset Off	00h	= 01h
3	Digital Power On	02h	= 01h
4	Analog Power On	03h	= 01h
5	RAM Clear On	2Fh	= 80h
6	RAM Clear Off	2Fh	= 00h
7	Mute Off	2Ah	= 03h

Power-On Sequence - continued

Timing Chart



(Note 1) $C_{(VREF)}$ is capacitance between VREF_L(R) and AVCC_L(R).
Please consider the variation and temperature characteristic of the capacitance.
(Note 2) RAM Clear on/off are necessary only for PCM Mode.

Figure 35. Power-On Sequence

Power-Off Sequence

In the power-off sequence, the power supply must be turned off after setting the registers as shown in the table below. The power supply should be turned off in the order of AVCC, DVDD, DVDDIO. Please execute the power-off sequence according to the following register settings and timing charts. If the sequence is not followed, normal operation cannot be guaranteed.

Table 23. Register Settings in Power-Off Sequence

Step	Operations	Register Address	Register Settings
1	Mute On	2Ah	= 00h
2	Analog Power Off	03h	= 00h
3	Digital Power Off	02h	= 00h

Timing Chart

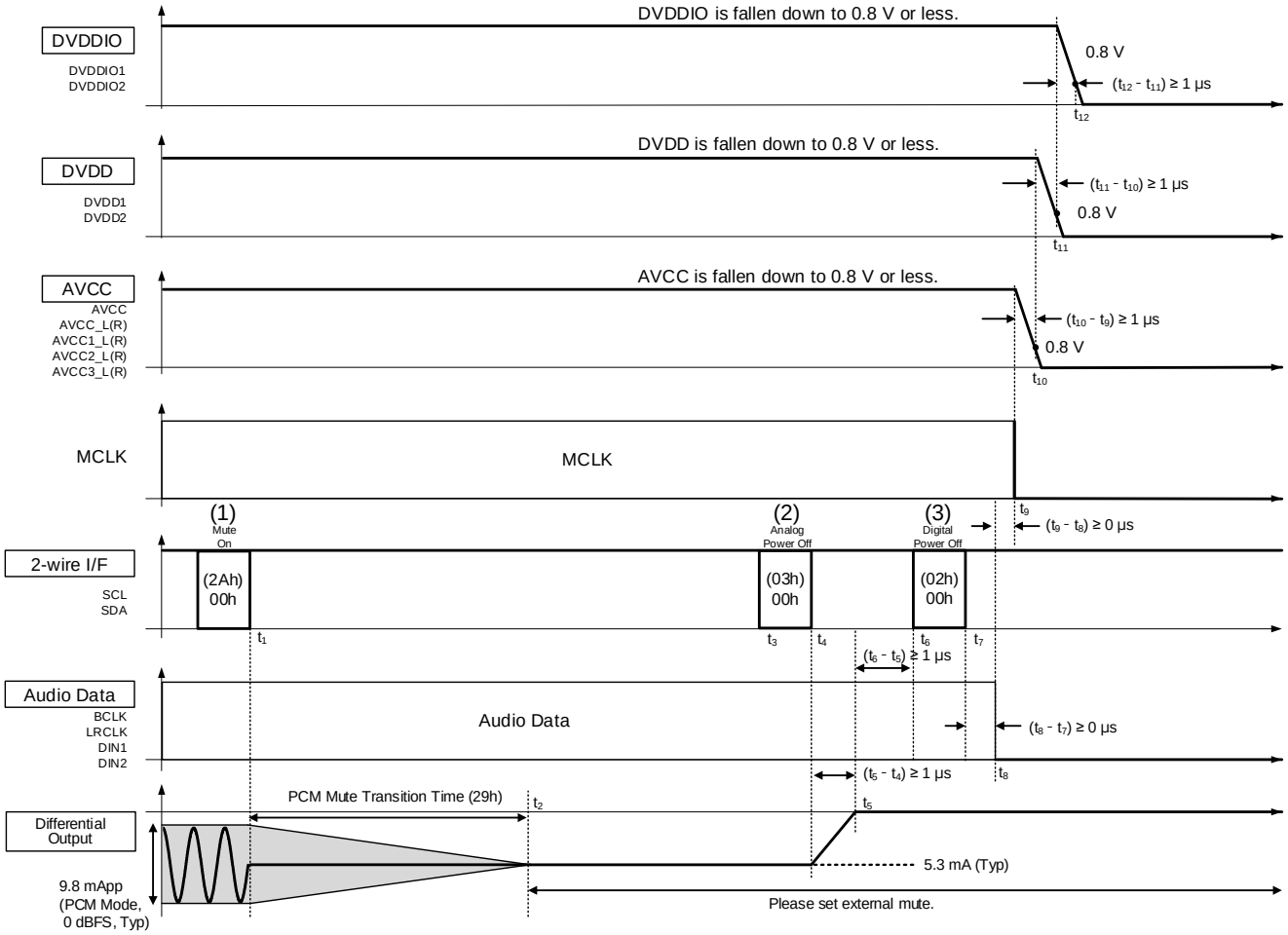


Figure 36. Power-Off Sequence

Mode Switching Sequence

Mode switching refers to switching from PCM mode to DSD mode and from DSD mode to PCM mode, as well as switching input signals (MCLK, BCLK/DSDCLK, LRCLK/DSD2, DIN1/DSD1) with changes in sampling frequency in each mode. The input signal must always be switched during the software reset period (SoftRst_X (00h[0]) = 0) of the mode switching sequence. Follow the register setting example and timing chart to execute the mode switching sequence. Also, refer to the "Recommended Settings" section for recommended register settings.

Table 24. Register Settings in Mode Switching Sequence

Step	Operation	Register Address	Register Setting	PCM Mode	DSD Mode
1	Mute On	2Ah	= 00h	Yes	Yes
2	Digital Power Off	02h	= 00h	Yes	Yes
3	Software Reset On	00h	= 00h	Yes	Yes
4	Mode Switching	04h	Clock 1	Yes	Yes
		06h	Clock 2	Yes	Yes
		10h	Audio I/F 1	Yes	Yes
		16h	DSD Filter	-	Yes
		30h	FIR Filter 1	Yes	-
		31h	FIR Filter 2	Yes	-
		40h	Delta Sigma	Yes	Yes
5	Software Reset Off	00h	= 01h	Yes	Yes
6	Digital Power On	02h	= 01h	Yes	Yes
7	RAM Clear On	2Fh	= 80h	Yes	-
8	RAM Clear Off	2Fh	= 00h	Yes	-
9	Mute Off	2Ah	= 03h	Yes	Yes

Note: If mode switching sequence is not done according to the following timing charts, pop noise may occur. In such cases, please set external mute in parallel.

Timing Chart

PCM Mode to DSD Mode

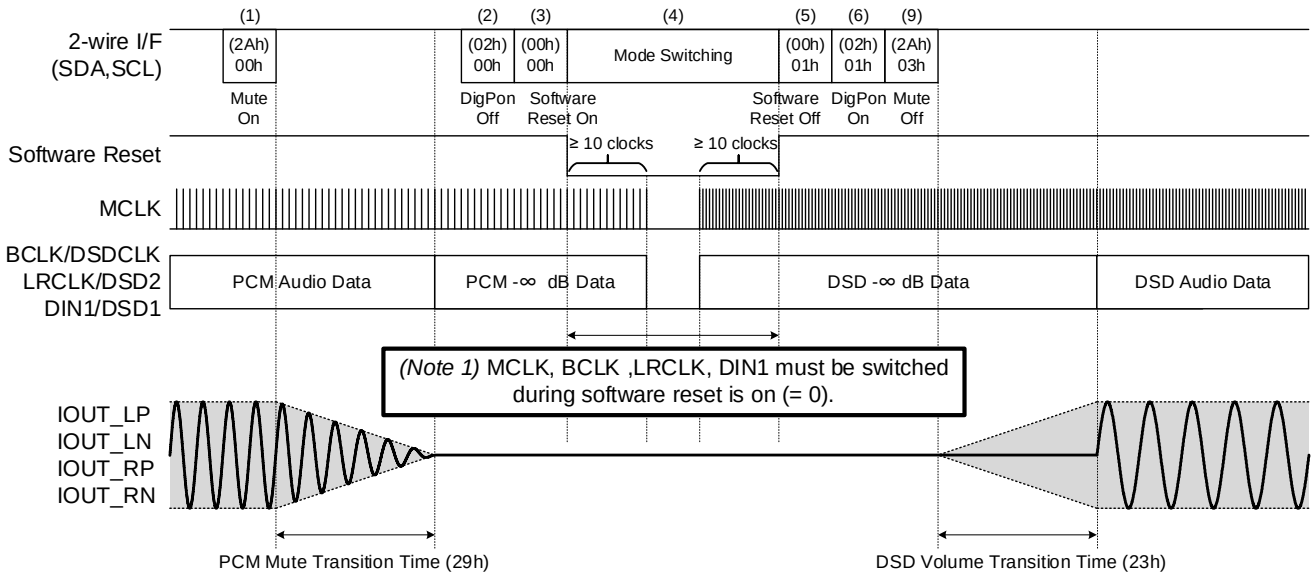


Figure 37. Sequence of Mode Switching from PCM Mode to DSD Mode

Mode Switching Sequence - continued

DSD Mode to PCM Mode

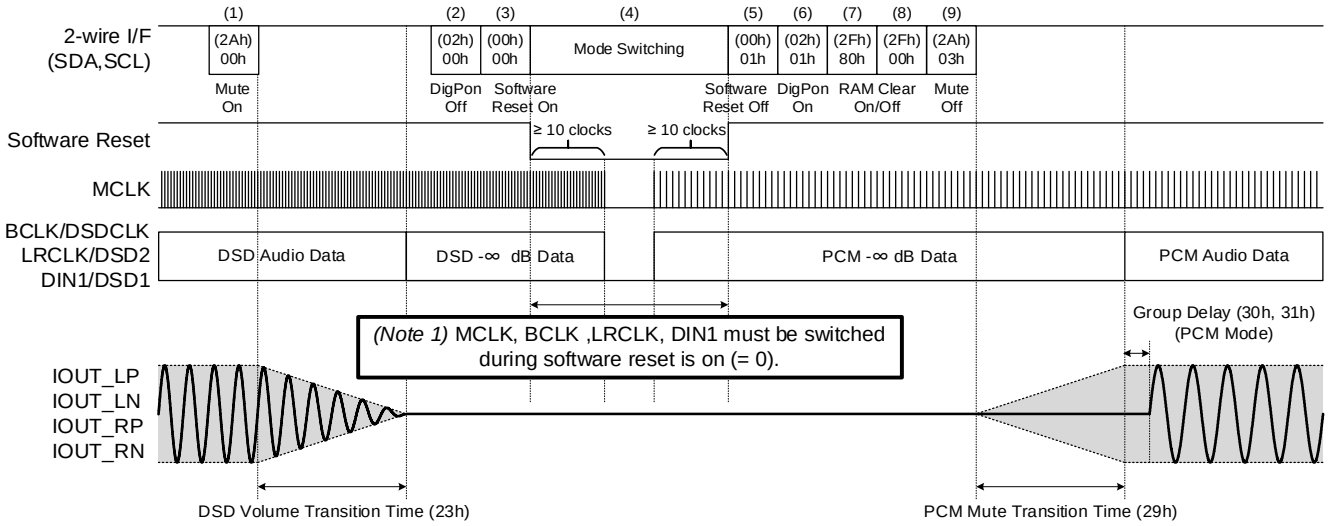


Figure 38. Sequence of Mode Switching from DSD Mode to PCM Mode

PCM Mode to PCM Mode

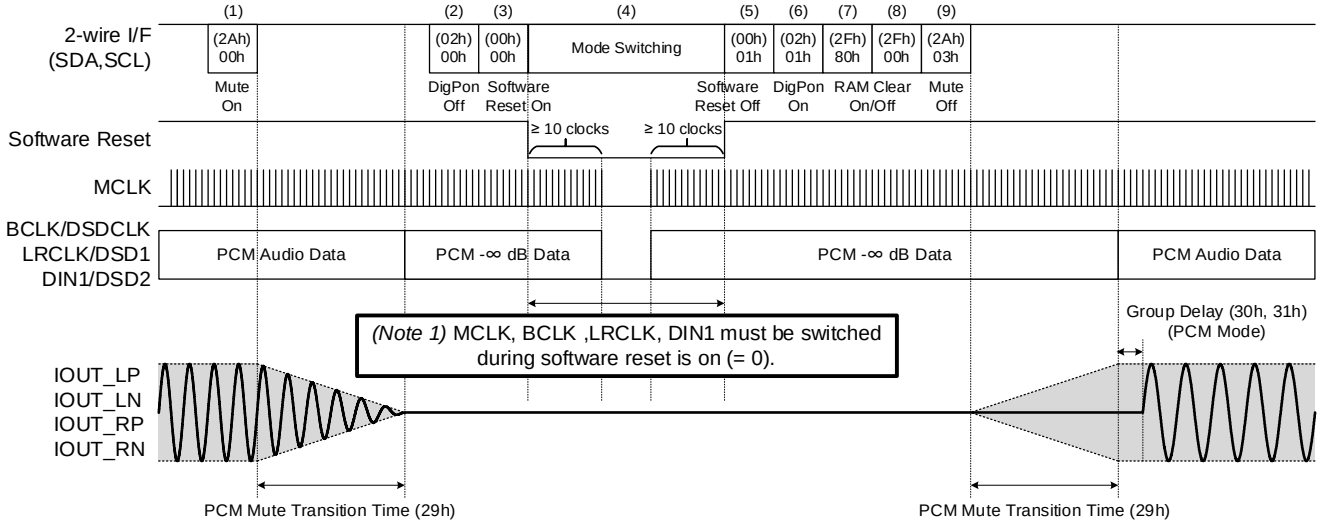


Figure 39. Sequence of Mode Switching from PCM Mode to PCM Mode

Recommended Settings

The recommended settings shown in the tables below provide a good balance between electrical characteristics and sound quality for PCM mode and DSD mode.

Table 25. Recommended Settings in PCM Mode

fs (kHz)			32	44.1 48	88.2 96	176.4 192	352.8 384	705.6 768	1411.2 1536
MCLK (MHz)			24.5760	22.5792 24.5760	22.5792 24.5760	22.5792 24.5760	22.5792 24.5760	22.5792 24.5760	22.5792 24.5760
Address	Register		Recommended Setting						
04h	Clock 1		03h	02h	00h				
06h	Clock 2		00h						
10h	Audio I/F 1		0Bh						
11h	Audio I/F 2		00h						01h
30h	FIR Filter 1		01h		02h	04h	08h		
31h	FIR Filter 2	Sharp Roll-Off	80h		01h	02h	80h		
		Slow Roll-Off	83h		04h	05h			
40h	Delta Sigma		02h		11h			01h	21h
60h, 61h	PCM Segment Control 1, 2	DWA1*(Note 1)*	06h						
		DWA2*(Note 2)*	07h						
68h	DWA	DWA1*(Note 1)*	00h						
		DWA2*(Note 2)*	02h						

(Note 1) DWA 1 = This is the recommended setting when using DWA algorithm 1 (PcmDwaAlgo (68h[1]) = 0).
(Note 2) DWA 2 = This is the recommended setting when using DWA algorithm 2 (PcmDwaAlgo (68h[1]) = 1).

Table 26. Recommended Settings in DSD Mode

DSDCLK (MHz)		2.8224	5.6448	11.2896	22.5792
MCLK (MHz)		= DSDCLK			
Address	Register	Recommended Setting			
04h	Clock 1	00h			
06h	Clock 2	00h			
10h	Audio I/F 1	8Bh			
16h	DSD Filter	02h	01h	00h	
40h	Delta Sigma	02h			
62h, 63h	DSD Segment Control 1, 2	1Dh			
68h	DWA	00h			

Sound Settings

In addition to selecting FIR filter or DSD filter, some register settings such that HPC (High Precision Calculation) mode, which is ROHM's original function, provide further adjustment of the sound quality. Changing these register settings may affect audio characteristics such as THD+N. Please evaluate the futures carefully before determining the setting value.

Table 27. Registers for Sound Setting

Register	Function
PhaseAdj (06h[0])	Phase adjustment for internal clock
HdMono (12h[7])	HD (High Definition) monaural mode
HpcMode (31h[7])	HPC (High Precision Calculation) mode
DsSetting (40h[4]), DsOsr (40h[1:0])	Over sampling rate of ΔΣ modulator
PcmSeg1 (60h[7:0]), PcmSeg2 (61h[7:0]) DsdSeg1 (62h[7:0]), DsdSeg2 (63h[7:0])	Current Segment Control
DsdDwa (68h[7]), DsdDwaAlgo (68h[5]), PcmDwaAlgo (68h[1])	DWA

Please refer to the "Register Description" for more details on each register.

Automatic Mode Switching

Automatic mode switching function detects mode switching by monitoring the input signals of BCLK/DSDCLK, LRCLK/DSD2, and DIN1/DSD1, and automatically switches to the register setting corresponding to the detected mode. By turning on this function, mode switching between PCM mode and DSD mode and between the sampling frequency (fs) in each mode are automatically performed without executing a mode switching sequence. This function supports PCM 32 kHz to 768 kHz and DSD 2.8 MHz to 22.5 MHz.

The clock frequency of MCLK should be 22.5792 MHz/24.5760 MHz or 45.1584 MHz/49.1520 MHz and its frequency must be set with MclkFreq (04h[4]) register. If this setting is incorrect, the automatic mode switching function will not work properly.

The DSD full scale detection function must be set to on, DsdFullDet_X (15h[0]) = 0. If DSD input data matches the same value for 128 consecutive clocks, the output will be muted by full scale detection. Therefore, be careful when inputting DSD data above 0 dBFS.

Regarding the FIR filter settings, auto-detected values are used for FirAlgo (30h[3:0]), but the values must be set in FirCoef (31h[2:0]). Set FirCoef (31h[2:0]) = 0h to select sharp roll-off filter and set FirCoef (31h[2:0]) = 3h to select slow roll-off filter.

De-Emphasis is not supported. De-Emphasis function must be off (Demp (34h[0]) = 0).

PCM 1536 kHz is not supported. Single data transfer must be used (DoubleDin (11h[0]) = 0).

DSD output level cannot mix normal level and double level. DsdLvl bit in the Mode Detect 7 to 10 registers must be set to the same value (76h[3] = 77h[3] = 78h[3] = 79h[3]).

For example, the table below shows the register settings when the recommended settings are used.

Table 28. Automatic Mode Switching Register Setting Example (Recommended Settings in PCM Mode)

Address	Register Name	fs (kHz)	Setting	D7	D6	D5	D4	D3	D2	D1	D0
				DsSetting (40h[4])	-	DsOsr (40h[1:0])		HpcMode (31h[7])	-	MclkDiv (04h[1:0])	
70h	Mode Detect 1 (PCM 32 kHz)	32	2Bh	0	0	1	0	1	0	1	1
71h	Mode Detect 2 (PCM 44.1 kHz)	44.1 48	2Ah	0		1	0	1		1	0
72h	Mode Detect 3 (PCM 96 kHz)	88.2 96	90h	1		0	1	0		0	0
73h	Mode Detect 4 (PCM 192 kHz)	176.4 192	90h	1		0	1	0		0	0
74h	Mode Detect 5 (PCM 384 kHz)	352.8 384	98h	1		0	1	1		0	0
75h	Mode Detect 6 (PCM 768 kHz)	705.6 768	18h	0		0	1	1		0	0

Table 29. Automatic Mode Switching Register Setting Example (Recommended Settings in DSD Mode)

Address	Register Name	DSDCLK (MHz)	Setting	D7	D6	D5	D4	D3	D2	D1	D0
				-	-	-	-	DsdLvl (16h[3])	DsdFilter (16h[2:0])		
76h	Mode Detect 7 (DSD 2.8 MHz)	2.8224	02h	0	0	0	0	0	0	1	0
77h	Mode Detect 8 (DSD 5.6 MHz)	5.6448	01h					0	0	0	1
78h	Mode Detect 9 (DSD 11.2 MHz)	11.2896	00h					0	0	0	0
79h	Mode Detect 10 (DSD 22.5 MHz)	22.5792	00h					0	0	0	0

Automatic Mode Switching - continued

When using automatic mode switching function, input -∞ dB data for a period of 2 ms or longer before switching modes. Also, after switching modes, input audio data after inputting -∞ dB data for a period of 2 ms or longer. -∞ dB data is repetitive continuous data in which the ratio of 0 and 1 is the same, such as DIN1 = 0 in PCM mode, DSD1/DSD2 = 10101010, 00110011, 01011010 in DSD mode. A pop noise may occur if -∞ dB data is not input for a period of time. After detecting the switching of the input signal, the mode shifts when the input signal is detected to be stable, and the register setting of the new mode is reflected. It remains in the previous mode until it detects a stable signal input. Also, even if the register setting does not change before and after mode switching, such as from fs = 44.1 kHz to fs = 48 kHz, -∞ dB data must be input for a period of 2 ms or longer. After inputting -∞ dB data for a period, input audio data. The current mode status can be checked by reading the ModeDetStat (7Ch[3:0]) register.

Timing Chart

PCM Mode to DSD Mode

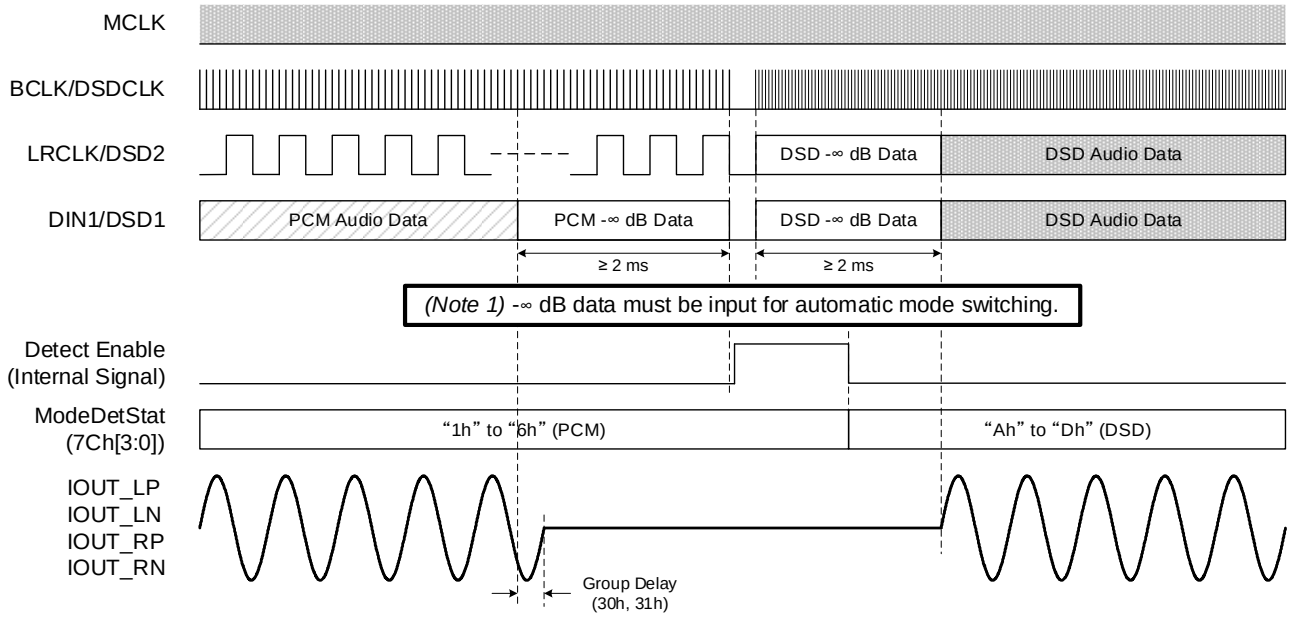


Figure 40. Sequence of Automatic Mode Switching from PCM Mode to DSD Mode

DSD Mode to PCM Mode

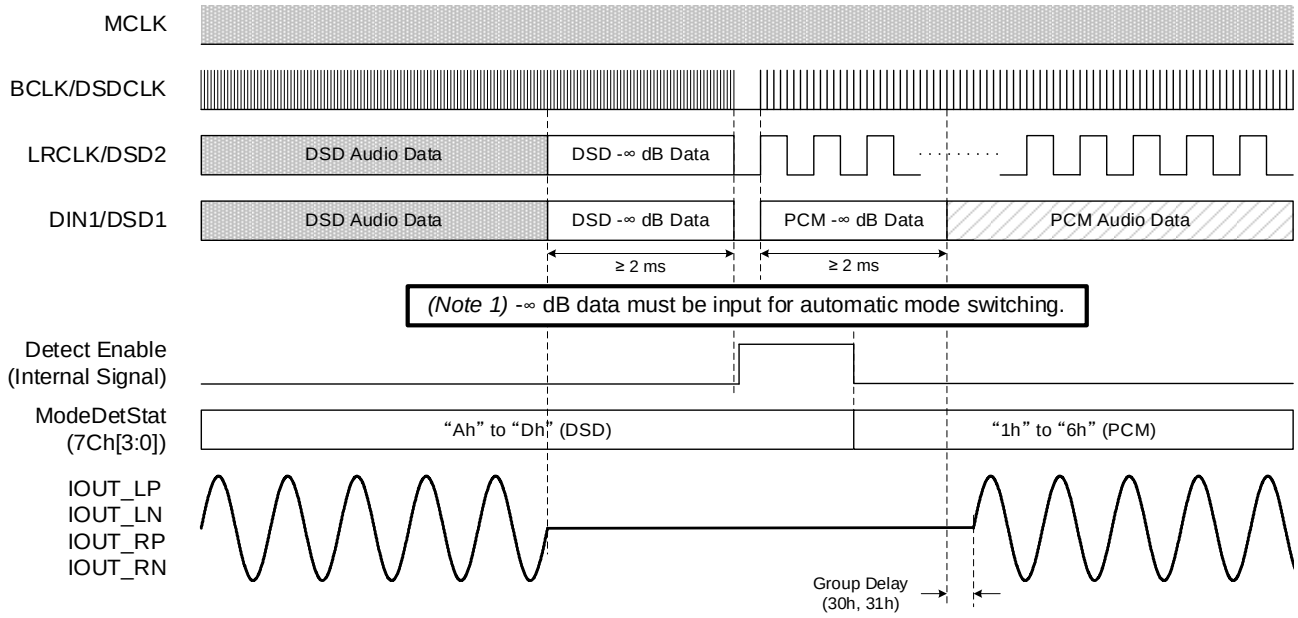


Figure 41. Sequence of Automatic Mode Switching from DSD Mode to PCM Mode

Automatic Mode Switching - continued

PCM Mode to PCM Mode

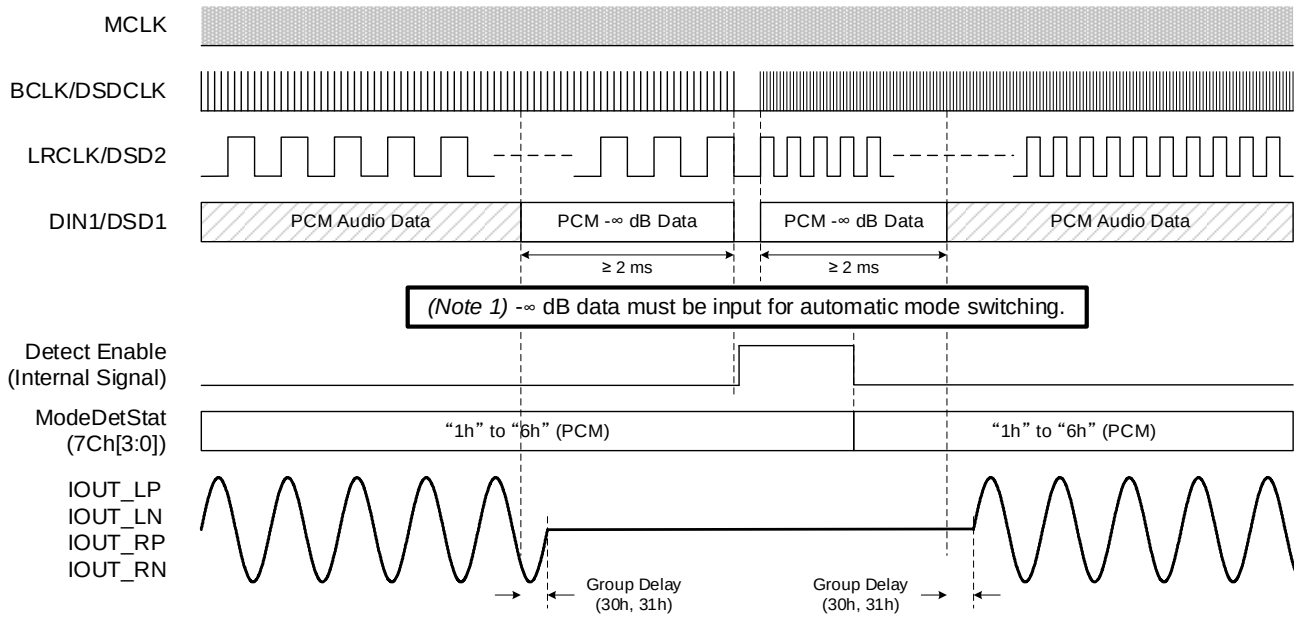


Figure 42. Sequence of Automatic Mode Switching from PCM Mode to PCM Mode

DSD Mode to DSD Mode

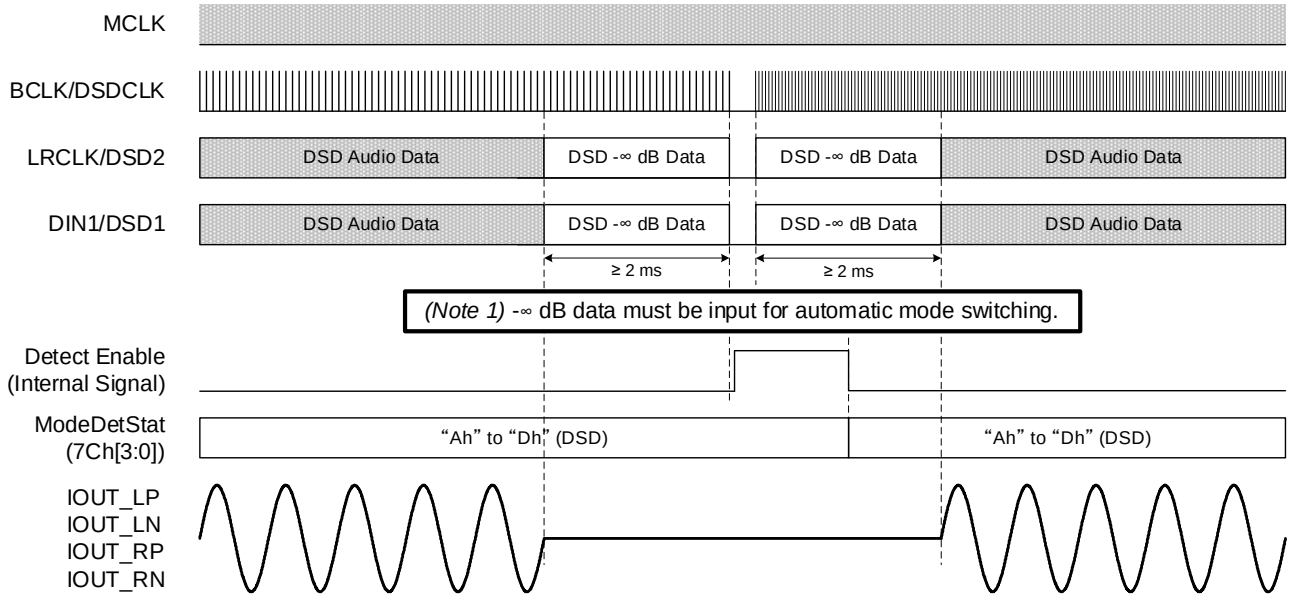


Figure 43. Sequence of Automatic Mode Switching DSD Mode to DSD Mode

Application Examples

1. Stereo 2ch

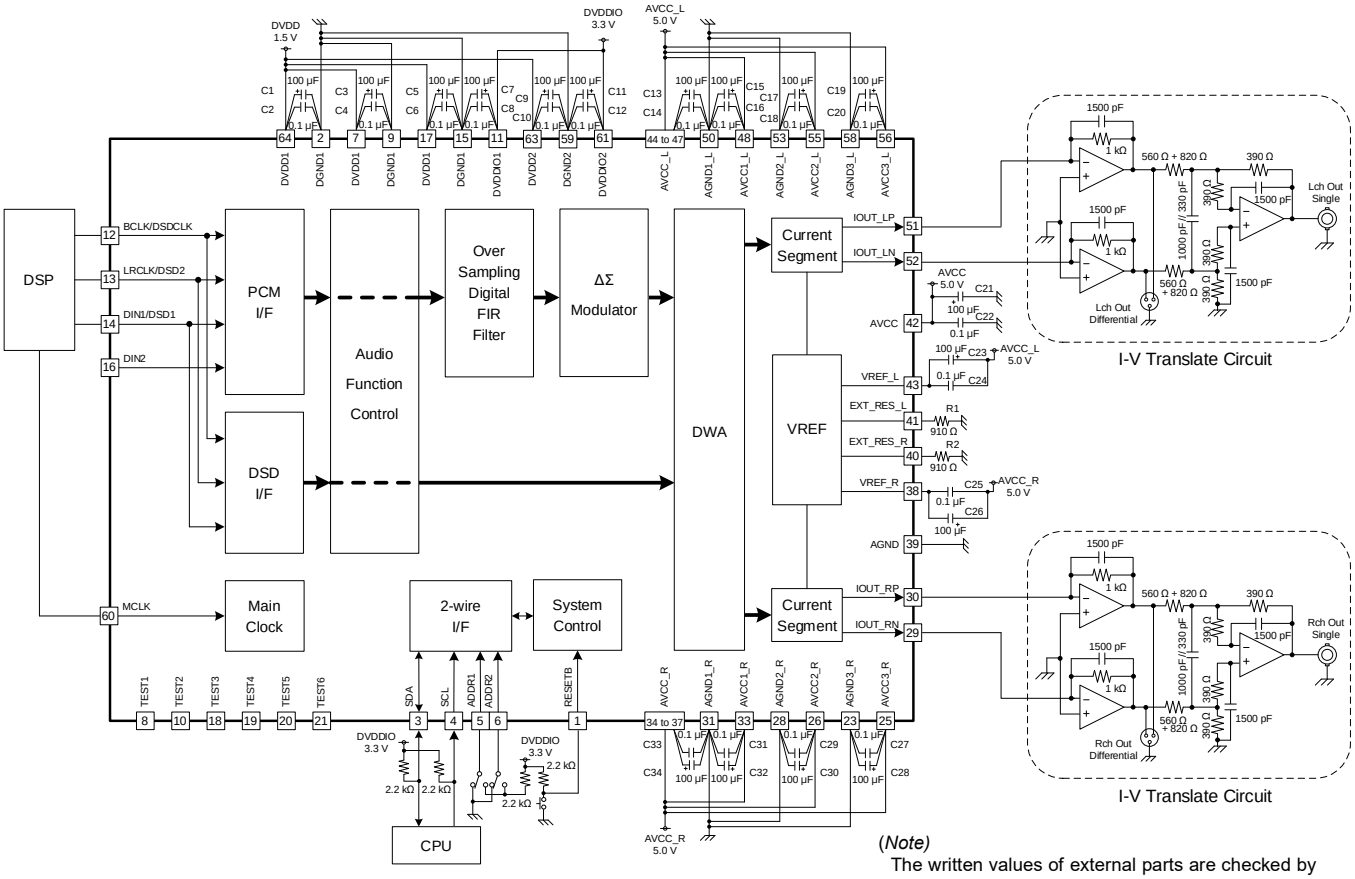


Figure 44. Application Circuit

I-V Translate Circuit (Enlarged)

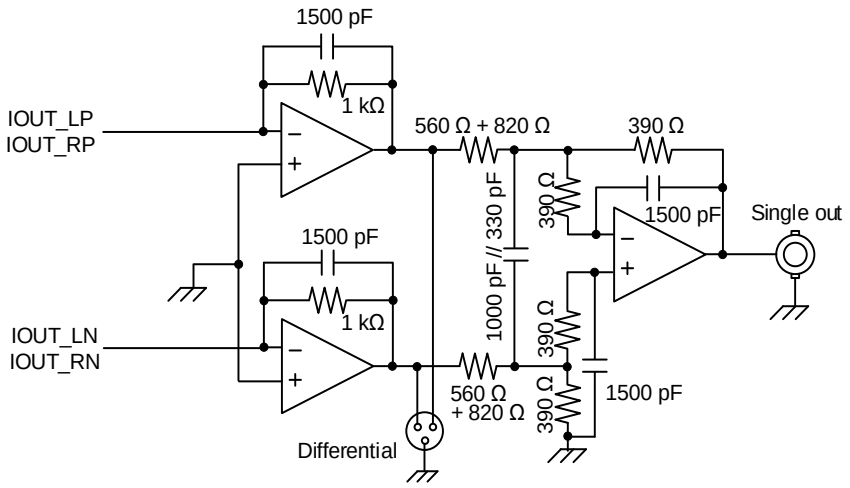
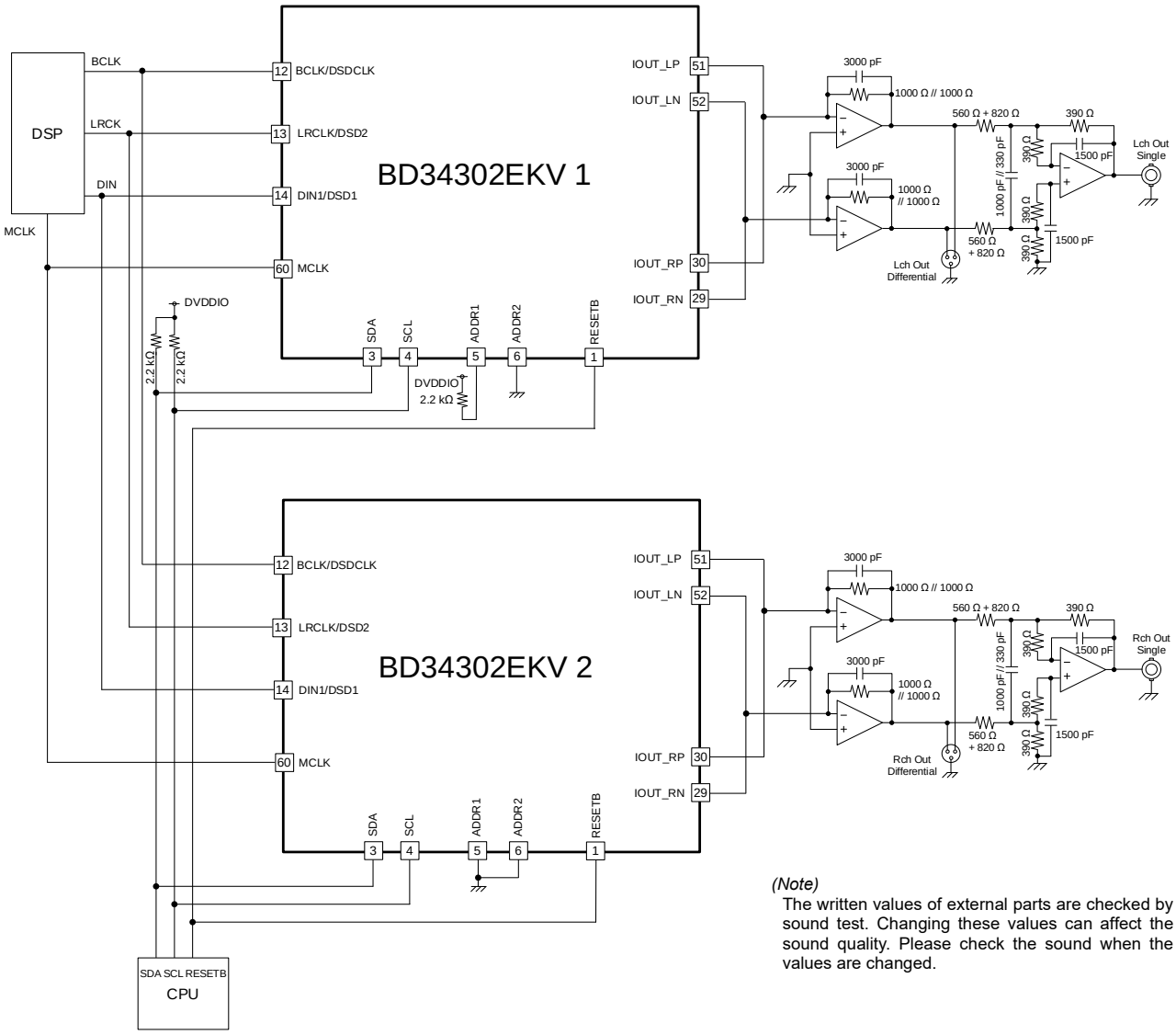


Figure 45. Application Circuit (I-V Translate Circuit)

Application Examples - continued

2. Monaural Mode x 2 – A



(Note)
The written values of external parts are checked by sound test. Changing these values can affect the sound quality. Please check the sound when the values are changed.

Figure 46. Application Circuit of Monaural Mode x 2 – A

Application Examples - continued

3. Monaural mode x 2 - B

Stereo 2ch circuit can also configure Lch/Rch differential output in monaural mode.

Table 30. Lch/Rch Differential Output Setting in Monaural Mode

Chip No.	MonoSel (12h[1:0])	OutPol2 (14h[1])	Function
1	10	1 (IOUT_R inverted)	Lch output
2	11	1 (IOUT_R inverted)	Rch output

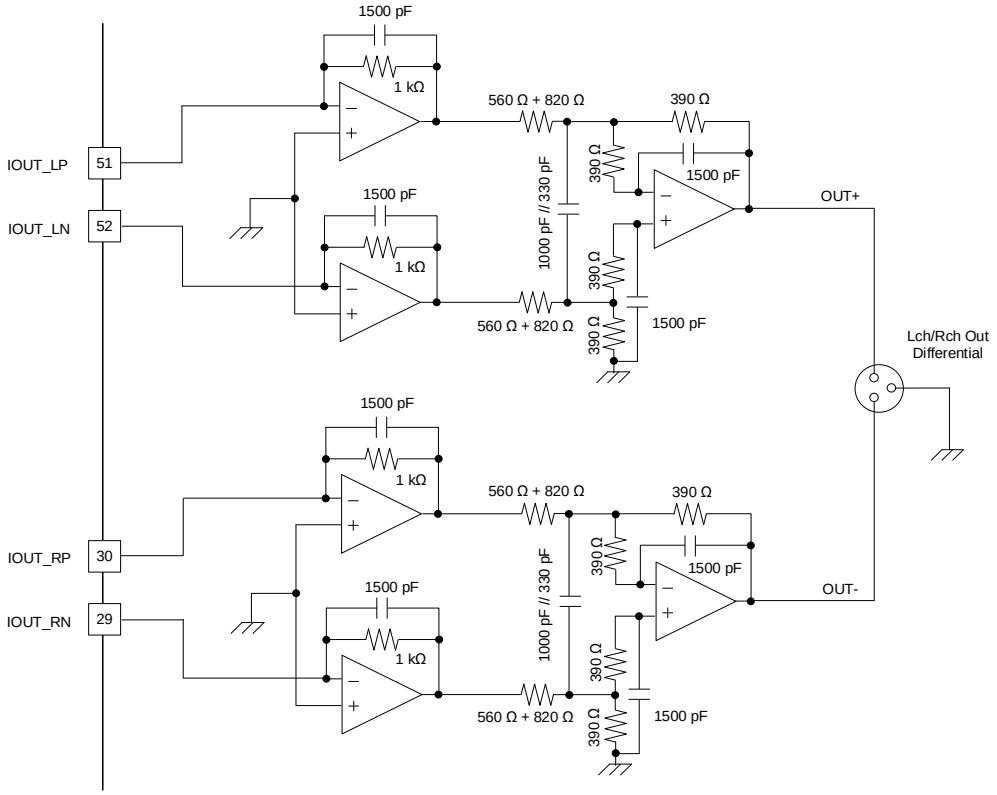
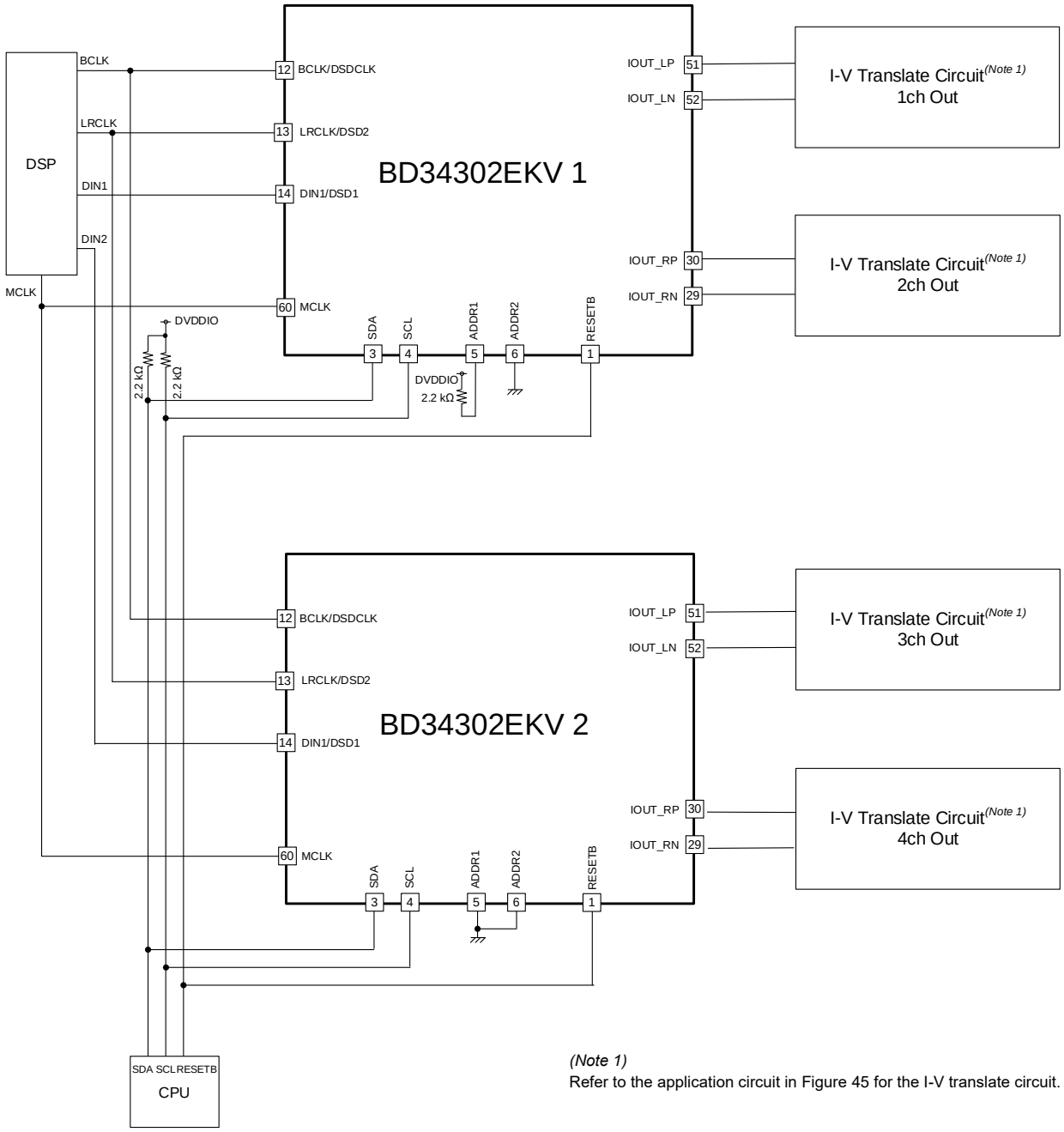


Figure 47. Application Circuit of Monaural Mode x 2 - B

Application Examples - continued

4. 2ch x 2 = 4ch

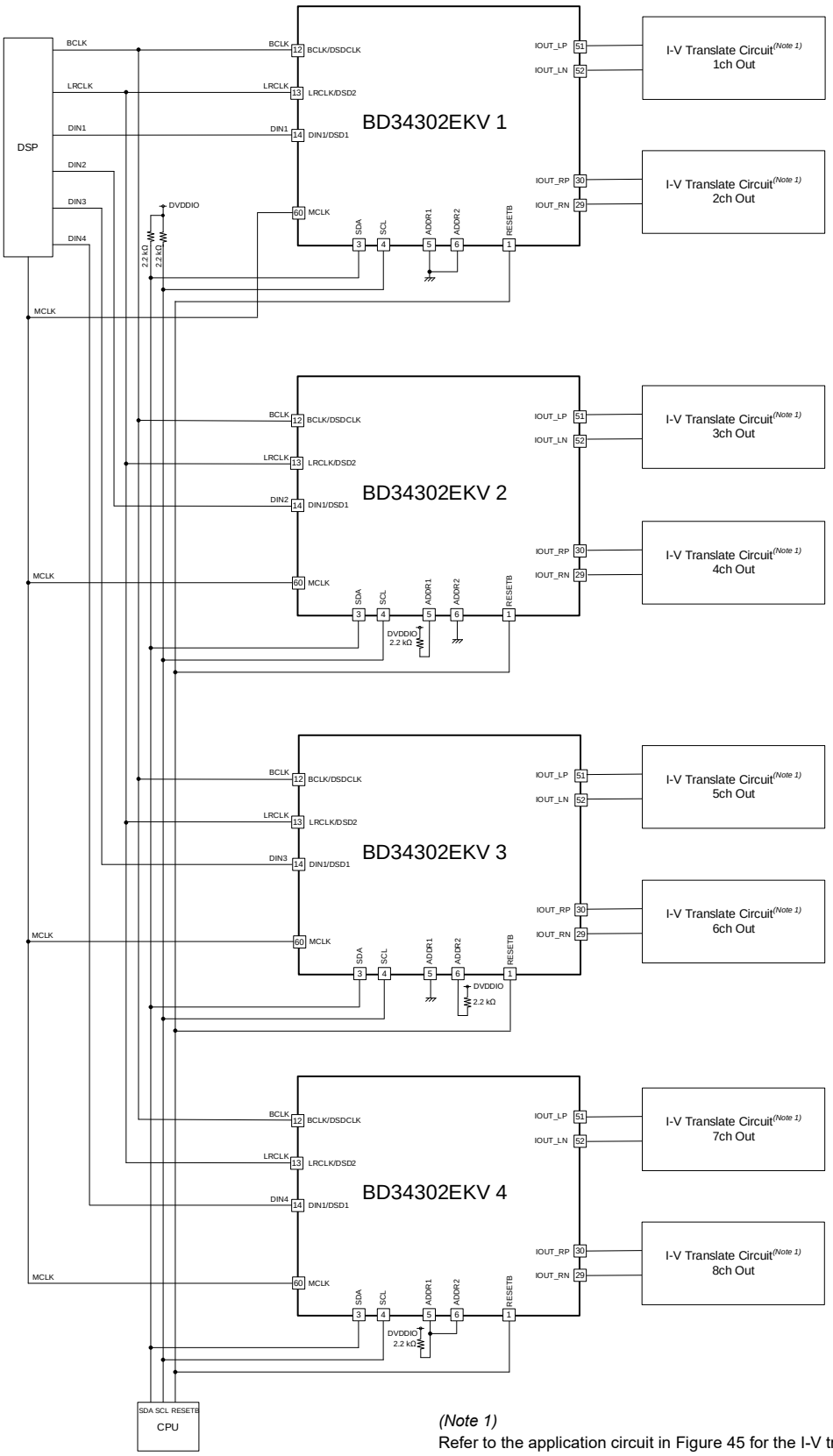


(Note 1)
Refer to the application circuit in Figure 45 for the I-V translate circuit.

Figure 48. Application Circuit of 4ch Output

Application Examples - continued

5. 2ch x 4 = 8ch

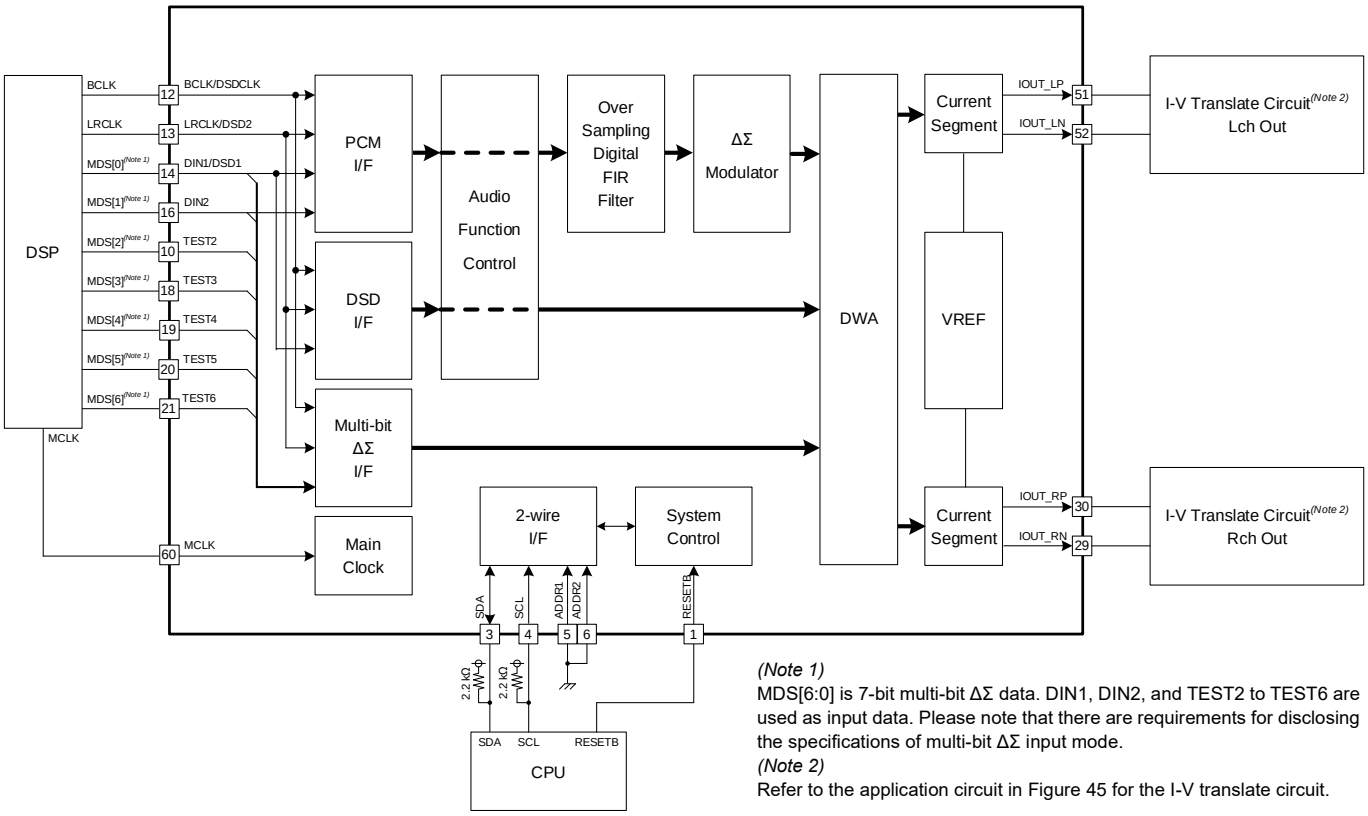


(Note 1)
Refer to the application circuit in Figure 45 for the I-V translate circuit.

Figure 49. Application Circuit of 8ch Output

Application Examples - continued

6. Multi-bit ΔΣ Data Input



(Note 1)
MDS[6:0] is 7-bit multi-bit ΔΣ data. DIN1, DIN2, and TEST2 to TEST6 are used as input data. Please note that there are requirements for disclosing the specifications of multi-bit ΔΣ input mode.
(Note 2)
Refer to the application circuit in Figure 45 for the I-V translate circuit.

Figure 50. Application Circuit of Multi-bit ΔΣ Data Input

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Recommended Operating Conditions**
   The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

8. **Inter-pin Short and Mounting Errors**
   Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

9. **Unused Input Pins**
   Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So, unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes - continued

10. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

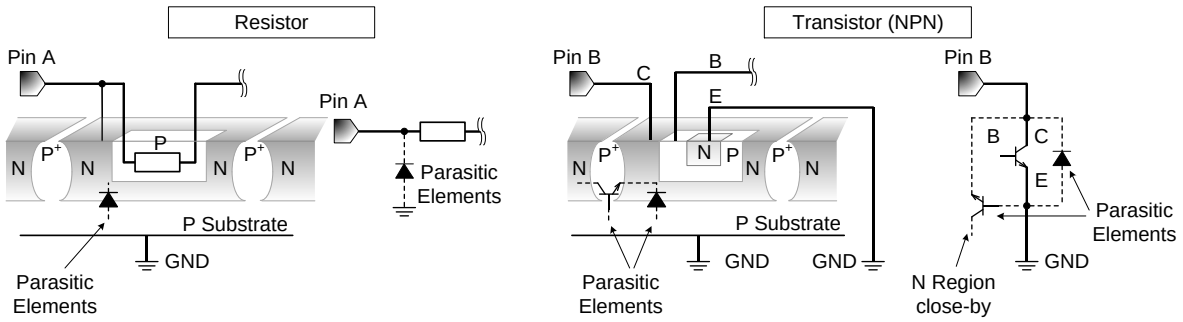


Figure 51. Example of Monolithic IC Structure

11. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

Ordering Information

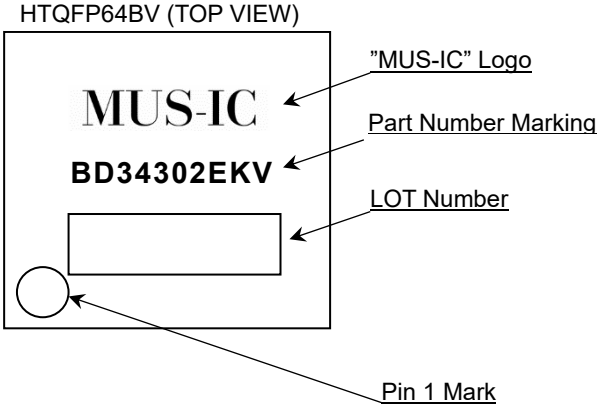
B	D	3	4	3	0	2	E	K	V	-	E 2

Package
EKV: HTQFP64BV

Packaging and forming specification
E2: Embossed tape and reel

Marking Diagram

HTQFP64BV (TOP VIEW)



”MUS-IC” Logo

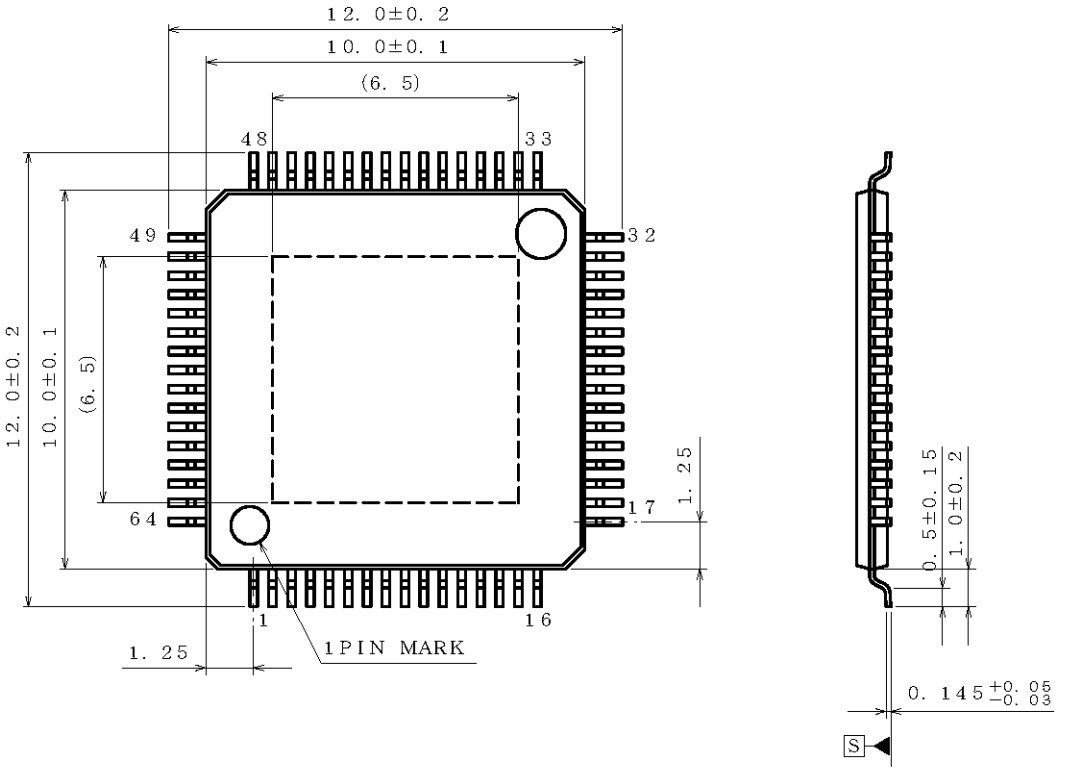
Part Number Marking

LOT Number

Pin 1 Mark

Physical Dimension and Packing Information

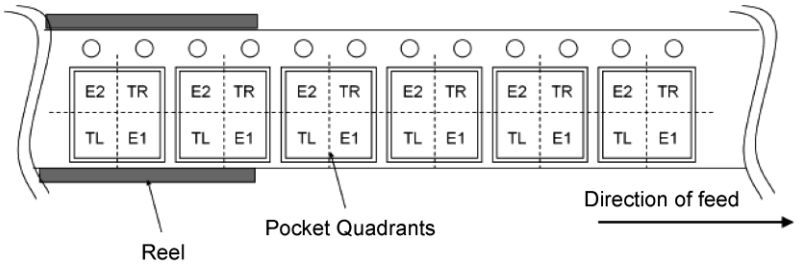
Package Name	HTQFP64BV



(UNIT : mm)
PKG : HTQFP64BV
Drawing No. EX282-5001-1

< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	1000pcs
Direction of feed	E2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand



Revision History

Date	Revision	Changes
01.Aug.2024	001	New Release
10.Dec.2024	002	P.1 Multi-bit ΔΣ Data Input Support delete P.57 (Note 1) Text change. When you consider using the multi-bit ΔΣ data input mode, please contact ROHM separately. →Please note that there are requirements for disclosing the specifications of multi-bit ΔΣ input mode.

Notice

Precaution on using ROHM Products

1. Our Products are designed and manufactured for application in ordinary electronic equipment (such as AV equipment, OA equipment, telecommunication equipment, home electronic appliances, amusement equipment, etc.). If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), transport equipment, traffic equipment, aircraft/spacecraft, nuclear power controllers, fuel controllers, car equipment including car accessories, safety devices, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
   [a] Installation of protection circuits or other protective devices to improve system safety
   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are designed and manufactured for use under standard conditions and not under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.) ; or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse, is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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A two-dimensional barcode printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

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