X67BC8513.L12-1

1 General information

1.1 Other applicable documents

For additional and supplementary information, see the following documents.

Other applicable documents

Document name	Title
MAX67	X67 system user's manual
MAEMV	Installation / EMC guide

1.2 Order data

Order number	Short description	Figure
	Bus controller modules	
X67BC8513.L12-1	X67 bus controller, 1 POWERLINK interface, X2X Link power supply 15 W, 6 digital input channels, 6 digital output channels, 24 VDC, 0.5 A, propagation delay measurement, configurable input filter, 1 analog input 0 to 20 mA, 12-bit, M12 connectors, high-density module	

Table 1: X67BC8513.L12-1 - Order data

Required accessories
See "Required cables and connectors" on page 9. For a general overview, see section "Accessories - General overview" in the X67 system user's manual.

1.3 Module description

The bus controller makes it possible to connect X2X Link I/O nodes to POWERLINK. It is also possible to operate the X2X Link cycle synchronously 1:1 or synchronous to POWERLINK using a prescaler.

Additional X2X Link I/O nodes (X67 modules or other modules based on X2X Link) can be connected using the integrated X2X Link connection. Mechanically, POWERLINK is connected via an IP67-protected standard D-coded M12 Ethernet connector.

Functions:

- POWERLINK
- Digital inputs and outputs
- Propagation delay measurement
- Analog input

POWERLINK

POWERLINK is a standard protocol for Fast Ethernet equipped with hard real-time characteristics.

Digital inputs and outputs

This module is equipped with 6 digital inputs and outputs each. In addition, the inputs and outputs of the module can be used in pairs for propagation delay measurement.

Propagation delay measurement

Propagation delay measurement of the switching delay is performed in pairs via permanently assigned input and output channels. Both normal and inverted switching edges can be used for measurement.

Analog input filter

The module is equipped with 1 analog input with configurable input filter with input ramp limiting.

2 Technical description

2.1 Technical data

Order number	X67BC8513.L12-1
Short description	
Bus controller	POWERLINK (V1/V2) controlled node
General information	
Inputs/Outputs	6 digital inputs, 6 digital outputs (not configurable), inputs with additional function, 1 analog channel
Insulation voltage between channel and bus	500 V_{eff}
Nominal voltage	24 VDC
B&R ID code	
Bus controller	0x046C
Internal I/O module	0x04A8
Sensor/Actuator power supply	0.5 A summation current
Status indicators	I/O function per channel, supply voltage, bus function
Diagnostics	
Outputs	Yes, using LED status indicator and software
I/O power supply	Yes, using LED status indicator and software
Support	
Dynamic node allocation (DNA)	Yes
Connection type	
Fieldbus	M12, D-coded
X2X Link	M12, B-coded
Inputs/Outputs	8x M12, A-coded
I/O power supply	M8, 4-pin
Power output	15 W X2X Link power supply for I/O modules
Power consumption	
Fieldbus	2.5 W
Internal I/O	0.6 W
X2X Link power supply	17.25 W at maximum power output for connected I/O modules
Certifications	
CE	Yes
UKCA	Yes
Interfaces	
Fieldbus	POWERLINK (V1/V2) controlled node
Type	Type 2 [1)]
Variant	2x M12 interface (hub), 2x female connector on module
Line length	Max. 100 m between 2 stations (segment length)
Transfer rate	100 Mbit/s
Transfer	
Physical layer	100BASE-TX
Half-duplex	Yes
Full-duplex	No
Autonegotiation	Yes
Auto-MDI/MDIX	Yes
Hub propagation delay	0.96 to 1 µs
Min. cycle time [2)]	
Fieldbus	200 µs
X2X Link	250 µs
Synchronization between bus systems possible	Yes
I/O power supply	
Nominal voltage	24 VDC
Voltage range	18 to 30 VDC
Integrated protection	Reverse polarity protection
Power consumption	
Sensor/Actuator power supply	Max. 12 W [3)]
Sensor/Actuator power supply	
Voltage	I/O power supply minus voltage drop for short-circuit protection
Voltage drop for short-circuit protection at 0.5 A	Max. 2 VDC
Summation current	Max. 0.5 A
Short-circuit proof	Yes
Digital inputs	
Input characteristics per EN 61131-2	Type 1
Input voltage	18 to 30 VDC
Input current at 24 VDC	Typ. 4 mA
Input circuit	Sink
Input resistance	Typ. 6 kΩ
Switching threshold	
Low	<5 VDC
High	>15 VDC

Table 2: X67BC8513.L12-1 - Technical data

Order number	X67BC8513.L12-1
Edge detection / Time measurement	
Counter size	16-bit
Counter frequency	
Internal	10 kHz
Pulse length	>200 µs with 200 µs pause between pulses
Signal form	Square wave pulse
Measurement type	Propagation delay measurement between output and corresponding feedback input
Analog inputs	
Input	0 to 20 mA
Input type	Differential input
Digital converter resolution	12-bit
Conversion time	200 µs
Output format	INT
Output format	
Current	0x0000 - 0x7FFF / 1 LSB = 0x0008 = 4.883 µA
Load	<300 Ω
Input protection	Protection against wiring with supply voltage
Permissible input signal	Max. ±30 mA
Output of digital value during overload	
Undershoot	0x0000
Overshoot	0x7FFF
Conversion procedure	Successive approximation
Max. error	
Gain	0.1% [4)]
Offset	0.05% [5)]
Max. gain drift	0.013 %/°C [4)]
Max. offset drift	0.02 %/°C [5)]
Common-mode rejection	
DC	>50 dB
50 Hz	>50 dB
Common-mode range	±2 V
Crosstalk between channels	>70 dB
Nonlinearity	<0.1% [5)]
Insulation voltage between input and bus	500 V_{eff}
Voltage drop at 20 mA	Typ. 4.5 V
Input filter	
Cutoff frequency	1 kHz
Slope	40 dB
Digital outputs	
Variant	Current-sourcing FET
Switching voltage	I/O power supply minus residual voltage
Nominal output current	0.5 A
Total nominal current	8 A
Output circuit	Source
Output protection	Thermal shutdown in the event of overcurrent or short circuit, integrated protection for switching inductive loads, reverse polarity protection of the output power supply
Diagnostic status	Output monitoring with 10 ms delay
Leakage current when the output is switched off	5 µA
Switching on after overload shutdown	Approx. 10 ms (depends on the module temperature)
$R_{DS(on)}$	150 mΩ
Residual voltage	<0.3 V at 0.5 A nominal current
Peak short-circuit current	<12 A
Switching delay	
0 → 1	<400 µs
1 → 0	<400 µs
Switching frequency	
Resistive load	Max. 100 Hz
Inductive load	See section "Switching inductive loads".
Braking voltage when switching off inductive loads	50 VDC
Electrical properties	
Electrical isolation	Bus isolated from POWERLINK and channel Channel not isolated from channel
Operating conditions	
Mounting orientation	
Any	Yes
Installation elevation above sea level	
0 to 2000 m	No limitation
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
Degree of protection per EN 60529	IP67

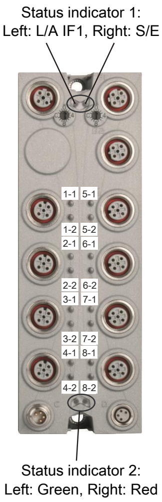
Table 2: X67BC8513.L12-1 - Technical data

Order number	X67BC8513.L12-1
Ambient conditions	
Temperature	
Operation	-25 to 60°C
Derating	-
Storage	-40 to 85°C
Transport	-40 to 85°C
Mechanical properties	
Dimensions	
Width	53 mm
Height	155 mm
Depth	42 mm
Weight	360 g
Torque for connections	
M8	Max. 0.4 Nm
M12	Max. 0.6 Nm

Table 2: X67BC8513.L12-1 - Technical data

1) For additional information, see section "Communication / POWERLINK / General information / Hardware - CN" in Automation Help.
2) The minimum cycle time specifies how far the bus cycle can be reduced without communication errors occurring.
3) The power consumption of the sensors and actuators connected to the module is not permitted to exceed 12 W.
4) Based on the current measured value.
5) Based on the entire measurement range.

2.2 LED status indicators

Figure	LED	Color	Status	Description
	**Status indicator 1:** Status indicator for POWERLINK bus controller			
	L/A IF (Link/Active)	Green	On	The link to the remote station is established.
			Blinking	The link to the remote station is established. The LED blinks if POWERLINK activity is taking place on the bus.
	S/E [1] (Status/Error)	Green/Red		LED states are described in section "Status/Error LED "S/E"" on page 6.
	I/O LEDs			
	1-1/2 to 6-1/2	Orange	Input/Output state of the corresponding channel	
	7-1/2	Not used		
	8-1	Green	On	The analog-to-digital converter is running.
			Blinking	Input signal overflow or underflow
	8-2	Not used		
	Status indicator 2: Status indicator for module functionality			
	Left	Green	Off	No power to module
			Single flash	Mode RESET
			Blinking	Mode PREOPERATIONAL
			On	Mode RUN
	Right	Red	Off	Module not supplied with power or everything OK
			On	Error or reset state
			Single flash	Warning/Error on an I/O channel. Level monitoring for digital outputs has been triggered.
			Double flash	Supply voltage not within the valid range

1) This LED is a green/red dual LED.

2.2.1 Status/Error LED "S/E"

LED "Status/Error" is a green and red dual LED. The color green (status) is superimposed on the color red (error).

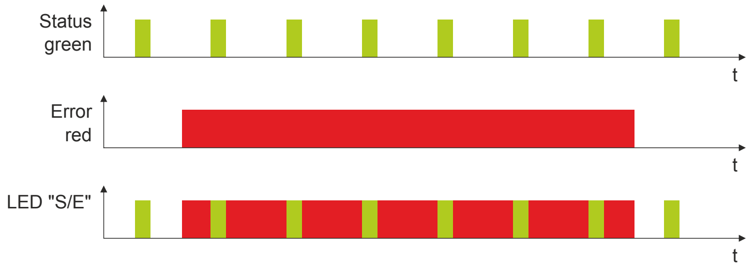
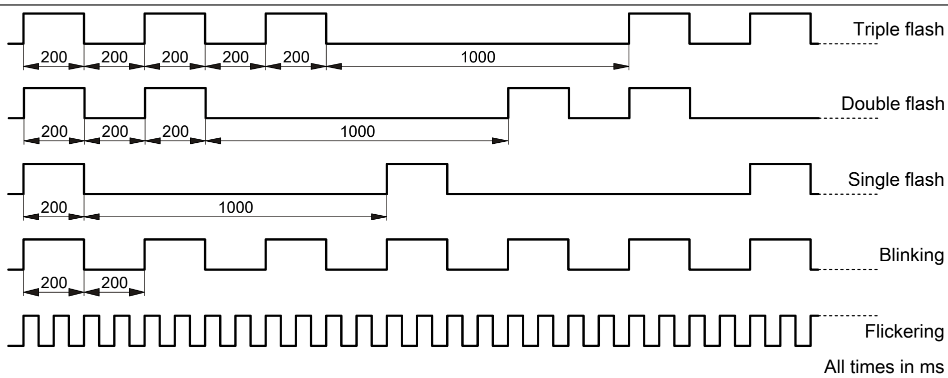
Color red - Error	Description
On	The controlled node (CN) is in an error state (failed Ethernet frames, increased number of collisions on the network, etc.). If an error occurs in the following states, the red LED is superimposed by the green flashing LED: • PRE_OPERATIONAL_1 • PRE_OPERATIONAL_2 • READY_TO_OPERATE  Note: • Several red blinking signals are displayed immediately after the device is switched on. This is not an error, however. • The LED lights up red for CNs with set physical node number 0 that have not yet been assigned a node number via dynamic node allocation (DNA).

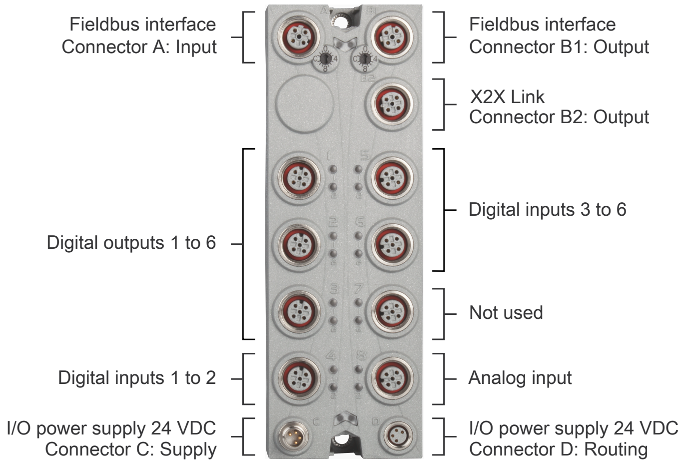
Table 3: Status/Error LED lit red: LED indicating error state

Color green - Status	Description
Off	No power supply or mode NOT_ACTIVE. The controlled node (CN) is either not supplied with power or it is in state NOT_ACTIVE. The CN waits in this state for about 5 s after a restart. Communication is not possible with the CN. If no POWERLINK communication is detected during these 5 s, the CN changes to state BASIC_ETHERNET (flickering). If POWERLINK communication is detected before this time expires, however, the CN immediately changes to state PRE_OPERATIONAL_1.
Green flickering (approx. 10 Hz)	Mode BASIC_ETHERNET. The CN has not detected any POWERLINK communication. In this state, it is possible to communicate directly with the CN (e.g. with UDP, IP). If POWERLINK communication is detected in this state, the CN changes to state PRE_OPERATIONAL_1.
Single flash (approx. 1 Hz)	Mode PRE_OPERATIONAL_1. When operating on a POWERLINK V1 manager, the CN immediately changes to state PRE_OPERATIONAL_2. When operating on a POWERLINK V2 manager, the CN waits until an SoC frame is received and then changes to state PRE_OPERATIONAL_2.
Double flash (approx. 1 Hz)	Mode PRE_OPERATIONAL_2. The CN is normally configured by the manager in this state. It is then switched to state READY_TO_OPERATE by command (POWERLINK V2) or by setting flag "Data valid" in the output data (POWERLINK V1).
Triple flash (approx. 1 Hz)	Mode READY_TO_OPERATE. In a POWERLINK V1 network, the CN switches to state OPERATIONAL automatically as soon as input data is present. In a POWERLINK V2 network, the manager switches to state OPERATIONAL by command.
On	Mode OPERATIONAL. PDO mapping is active and cyclic data is evaluated.
Blinking (approx. 2.5 Hz)	Mode STOPPED. Output data is not being output, and no input data is being provided. It is only possible to switch to or leave this state after the manager has given the appropriate command.

Table 4: Status/Error LED lit green: LED indicating operating state

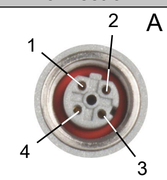
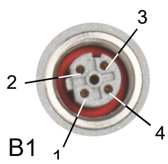


2.3 Operating and connection elements



2.3.1 POWERLINK interface

The module is connected to the network using pre-assembled cables. The connection is made using M12 circular connectors.

Connection	Pinout		
	Pin	Name	
 	1	TXD	Transmit data
	2	RXD	Receive data
	3	TXD\	Transmit data\
	4	RXD\	Receive data\
	Shield connection made via threaded insert in the module A → D-coded (female), input B1 → D-coded (female), output		

Information:

The color of the wires used in field-assembled cables for connecting to the fieldbus interface may deviate from the standard.

It is very important to ensure that the pinout is correct (see section "Accessories - POWERLINK cables" in the X67 user's manual).

2.3.1.1 Wiring guidelines for bus controllers with Ethernet cable

Some X67 system bus controllers are based on Ethernet technology. POWERLINK cables offered by B&R can be used for wiring.

Order number	Connection type
X67CA0E41.xxxx	Attachment cables - RJ45 to M12
X67CA0E61.xxxx	Connection cables - M12 to M12

The following cabling guidelines must be observed:

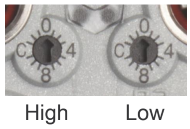
- Use Cat 5 SFTP cables.
- Observe the bend radius of the cable (see the data sheet of the cable)

Information:

Using POWERLINK cables offered by B&R (X67CA0E61.xxxx and X67CA0E41.xxxx) meets product standard EN 61131-2.

The customer must implement additional measures in the event of further requirements.

2.3.2 POWERLINK node number

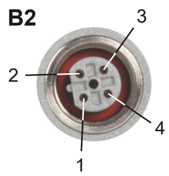


The node number for the POWERLINK node is set using the two number switches.

Switch position	Description
0x00	Only permitted when operating the POWERLINK node in DNA mode.
0x01 - 0xEF	Node number of the POWERLINK node. Operation as a controlled node (CN).
0xF0 - 0xFF	Reserved, switch position not permitted.

2.3.3 X2X Link

Additional modules are connected to the bus controller via X2X Link using pre-assembled cables. The connection is made using M12 circular connectors.

Connection	Pinout	
	Pin	Name
	1	X2X+
	2	X2X
	3	X2X⊥
	4	X2X\
	Shield connection made via threaded insert in the module B2 → B-coded (female), output	

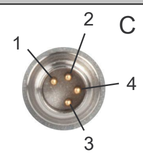
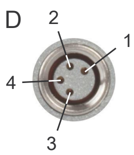
2.3.4 I/O power supply 24 VDC

The I/O power supply is connected via M8 connectors C and D. The power supply is fed via connector C (male). Connector D (female) is used to route the power supply to other modules.

The fieldbus / X2X Link power supply and I/O power supply are supplied separately via pins 1 and 2.

Information:

The maximum permissible current for the I/O power supply is 8 A (4 A per pin)!

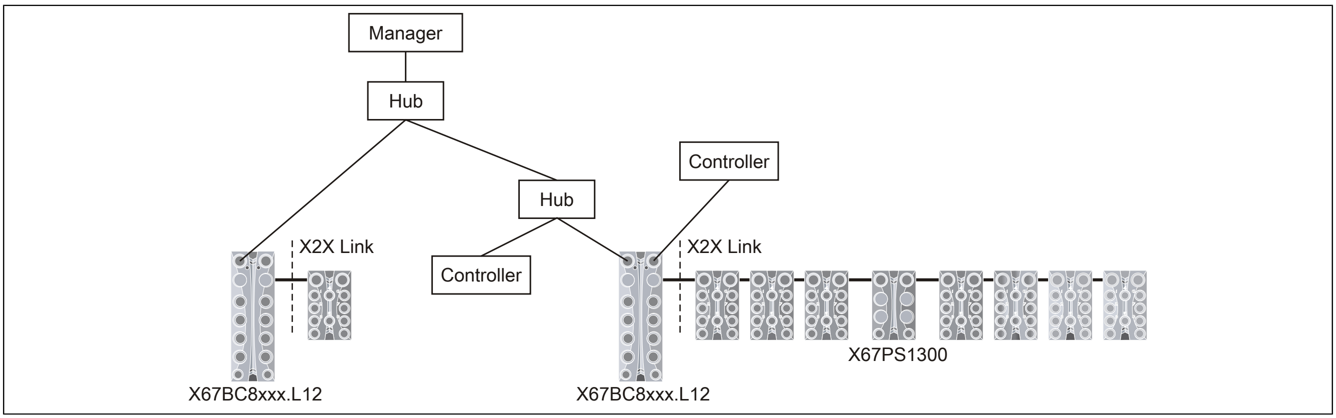
Connection	Pinout		
	Pin	Connector C (male)	Connector D (female)
 	1	24 VDC fieldbus / X2X Link	24 VDC I/O
	2	24 VDC I/O	24 VDC I/O
	3	GND	GND
	4	GND	GND
	C → Connector (male) in module, supply for I/O power supply D → Connector (female) in module, routing of I/O power supply		

Information:

If the summation current of the outputs is >4 A, current must also be supplied via connector D, pin 2.

2.4 System configuration

A digital mixed module is already integrated in the bus controller. Maximum 250 I/O modules can be connected to the bus controller.



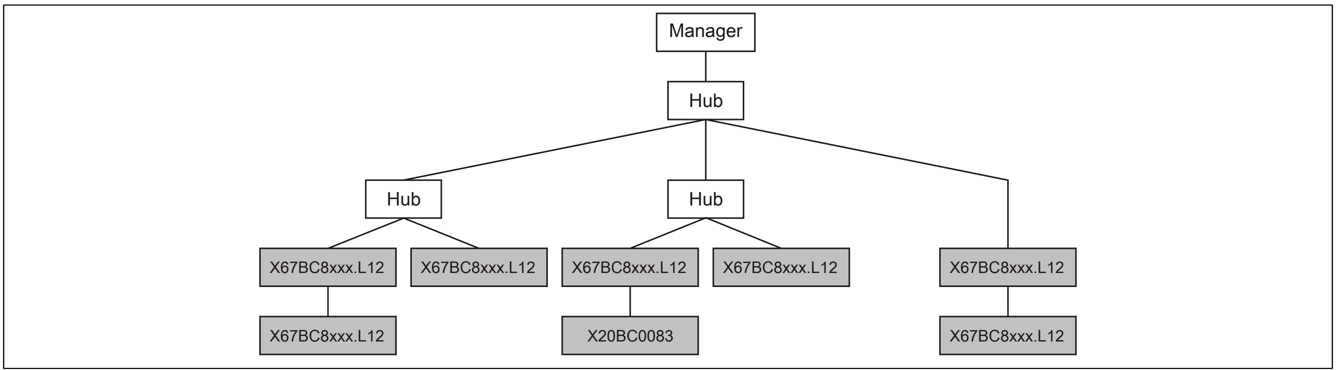
Information:

15 W are made available from the bus controller for additional X67 modules or other modules based on X2X Link.

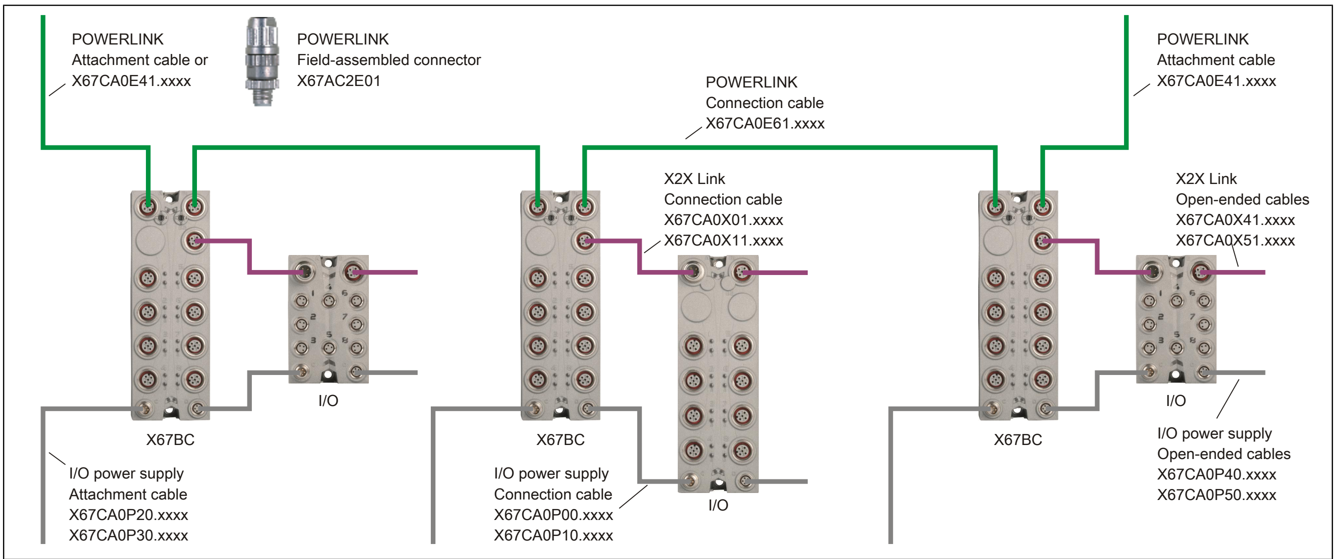
System supply module X67PS1300 is needed for additional power. This system supply module provides 15 W for additional modules. Each should be installed in the middle of the modules to be supplied with power.

2.4.1 Integrating into a POWERLINK network

The bus controller is used in a tree or line structure as follows:

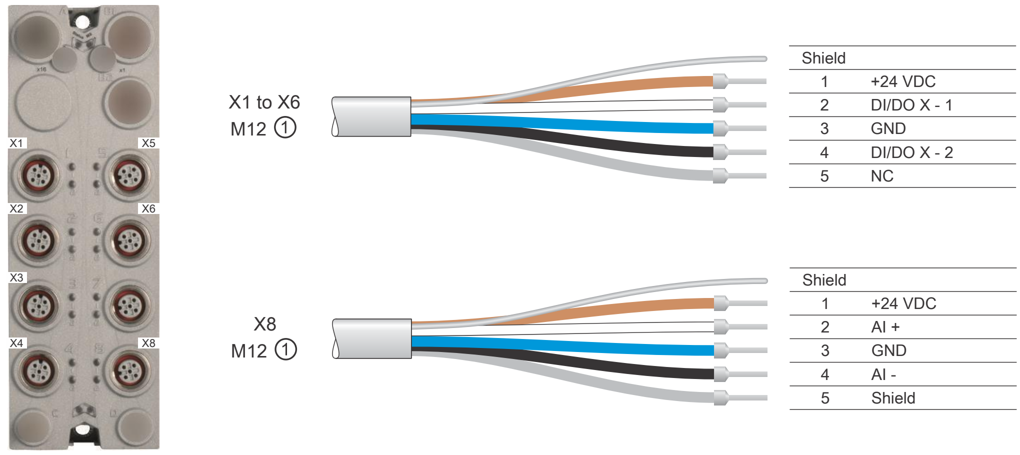


2.5 Required cables and connectors



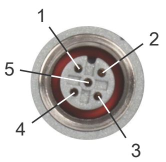
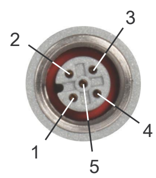
3 Integrated I/O channels

3.1 Pinout

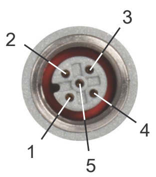


① X67CA0A41.xxxx: M12 sensor cable, straight
X67CA0A51.xxxx: M12 sensor cable, angled

3.1.1 Connections X1 to X6

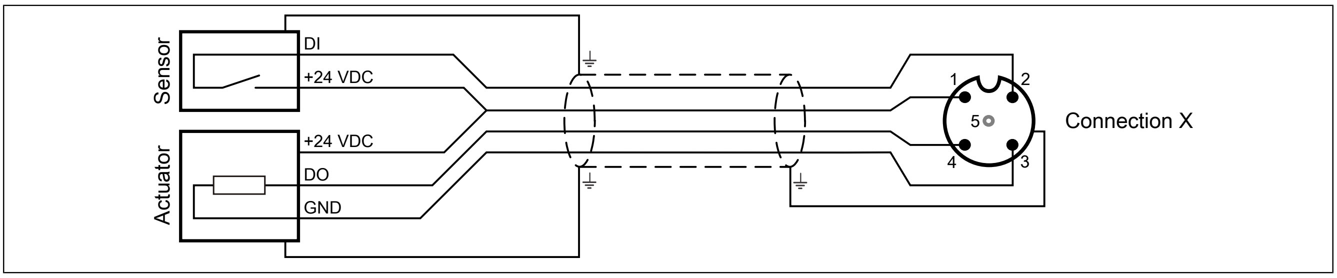
M12, 5-pin	Pinout	
Connection 1 to 4	**Pin**	**Name**
	1	24 VDC sensor/actuator power supply[1)]
	2	Input/Output x-1
	3	GND
	4	Input/Output x-2
	5	NC
 Connection 5 to 6	Shield connection made via threaded insert in the module. 1) The sensor/actuator power supply is not permitted to be external. X1 to X6 → A-coded (female), input/output	

3.1.2 Connector X8

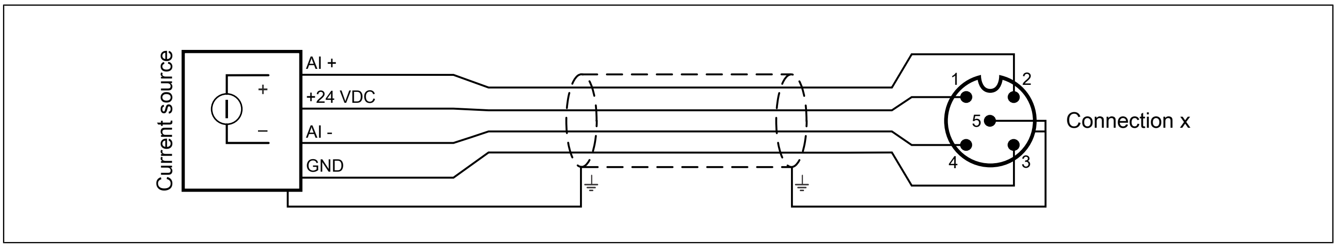
M12, 5-pin	Pinout	
Connection 8	**Pin**	**Name**
	1	Sensor power supply 24 VDC
	2	Input +
	3	GND
	4	Input -
	5	Shield[1)]
	1) Shielding also provided by threaded insert in the module. X8 → A-coded (female), input	

3.2 Connection examples

Digital inputs/outputs



Analog input



4 Function description

4.1 POWERLINK

POWERLINK is an Ethernet-based, real-time capable fieldbus. POWERLINK extends the IEEE 802.3 Ethernet standard by a deterministic access method and also defines a CANopen-compatible fieldbus interface. POWERLINK distinguishes between process and service data in the same way as CANopen. Process data (PDO) is exchanged cyclically in the cyclic phase, while service data (SDO) is transferred acyclically. Service data objects are transmitted in the acyclic phases of POWERLINK using a connection-oriented protocol. The cyclic transfer of data in PDOs is enabled by "mapping".

For additional information, see POWERLINK bus controller user's manual and www.br-automation.com/en/technologies/powerlink.

4.2 Digital inputs and outputs

Digital inputs

Filtering the inputs is not possible. The input state is collected with a fixed offset to the network cycle and transferred in the same cycle.

Digital outputs

On the module, the output states of the outputs are compared to the target states. The control of the output driver is used for the target state. A change in the output state resets monitoring for that output. The status of each individual channel can be read out.

> **Information:**
>
> **Registers are described in "Digital and analog inputs/outputs" on page 18.**

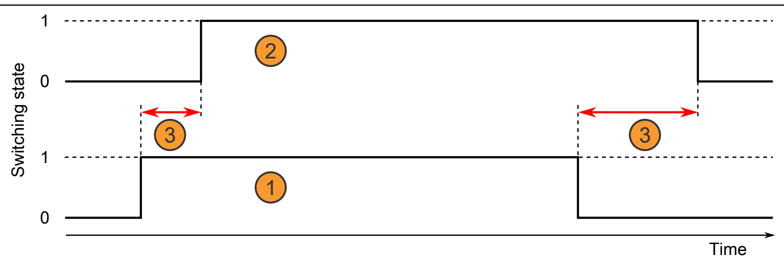
4.3 Propagation delay measurement

Propagation delay measurement is used to measure the switching delay between the output and corresponding feedback input. There are 6 measuring channels for the measurement that are defined by a permanent assignment of the output and input channels.

Measurement channel		
Output 1	→	Input 1
...	→	...
Output 6	→	Input 6

The internal feedback signal of the respective digital output is used as the initial value for the measurement. Due to the system, however, a measurement error of up to 0.3 ms ±2.5% can occur during the measurement.

If no measurement has been performed since module startup or the last clear procedure, the registers return value 0.



1 Switching signal of the digital output
2 Feedback signal on the digital input
3 Measured propagation delay difference

Edge polarity

Propagation delay measurement can be applied to both rising and falling edges. Rising edges are only applied when the output is active; falling edges are only applied when the output is inactive. In addition, the edge polarity of the input signal can be inverted to enable the detection of opposite edge pairs.

Normal		Inverted	
Output	Input	Output	Input
Rising edge	Rising edge	Rising edge	Falling edge
Falling edge	Falling edge	Falling edge	Rising edge

Information:

Registers are described in **"Propagation delay measurement" on page 20****.**

4.4 Analog input

The module is equipped with 1 analog input with a configurable input filter with input ramp limiting. The minimum cycle time must be >400 μs. The filter function is disabled for shorter cycle times.

When the input filter is activated, the channels are sampled at millisecond intervals. The conversion takes place asynchronously to the network cycle.

Information:

The register is described in **"Configuration - Analog input filters" on page 18****.**

4.4.1 Filter level

A filter can be defined to prevent large input steps. This filter is used to bring the input value closer to the actual analog value over a period of several bus cycles.
Filtering takes place after any input ramp limiting has been carried out.

Formula for calculating the input value:

$$\text{Value}_{\text{New}} = \text{Value}_{\text{Old}} - \frac{\text{Value}_{\text{Old}}}{\text{Filter level}} + \frac{\text{Input value}}{\text{Filter level}}$$

Adjustable filter levels:

Value	Filter level
0	Filter switched off
1	Filter level 2
2	Filter level 4
3	Filter level 8
4	Filter level 16
5	Filter level 32
6	Filter level 64
7	Filter level 128

The following examples show the functionality of the filter based on an input step and a disturbance.

Example 1

The input value jumps from 8000 to 16000. The diagram shows the calculated value with the following settings:

Input ramp limiting = 0

Filter level = 2 or 4

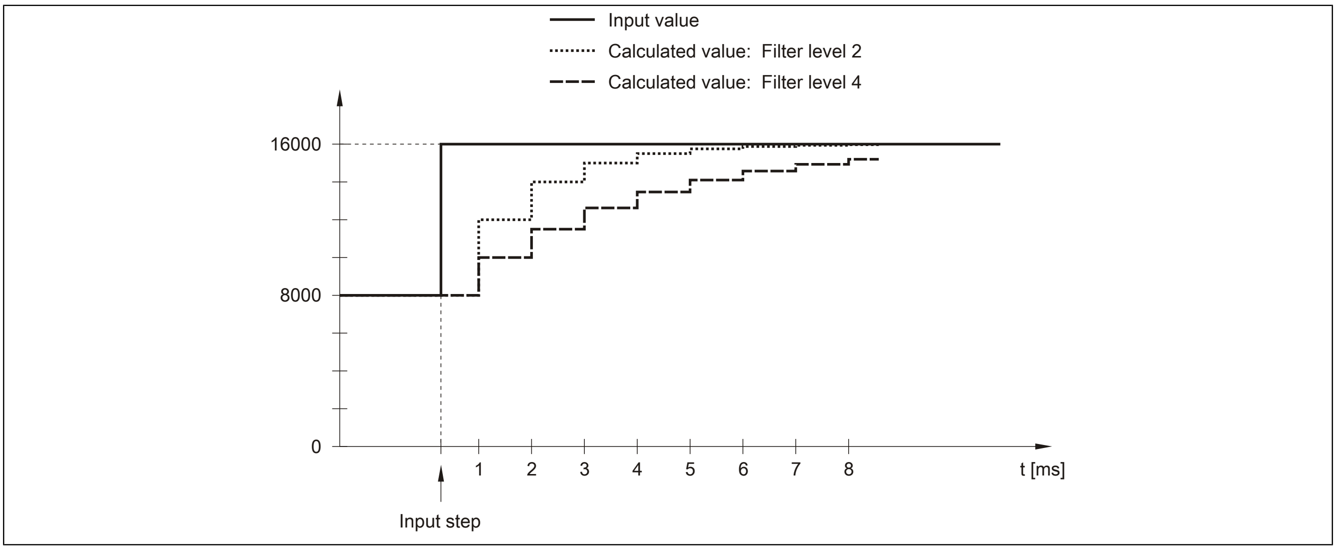


Figure 1: Calculated value during input step

Example 2

A disturbance interferes with the input value. The diagram shows the calculated value with the following settings:

Input ramp limiting = 0

Filter level = 2 or 4

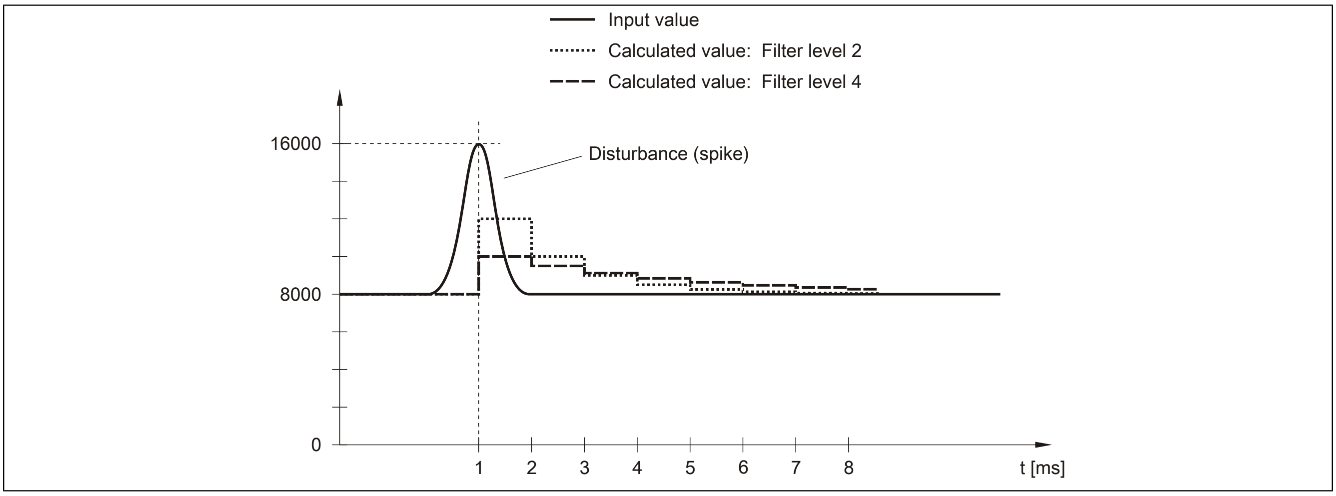


Figure 2: Calculated value during disturbance

4.4.2 Input ramp limiting

Input ramp limiting can only be performed in conjunction with filtering. Input ramp limiting is performed before filtering.

The difference of the input value change is checked for exceeding the specified limit. In the event of overshoot, the tracked input value is equal to the old value ± the limit value.

Configurable limit values:

Value	Limit value
0	The input value is used without limitation.
1	0x3FFF = 16383
2	0x1FFF = 8191
3	0x0FFF = 4095
4	0x07FF = 2047
5	0x03FF = 1023
6	0x01FF = 511
7	0x00FF = 255

Input ramp limiting is well suited for suppressing disturbances (spikes). The following examples show the functionality of input ramp limiting based on an input step and a disturbance.

Example 1

The input value jumps from 8000 to 17000. The diagram shows the tracked input value with the following settings:

Input ramp limiting = 4 = 0x07FF = 2047

Filter level = 2

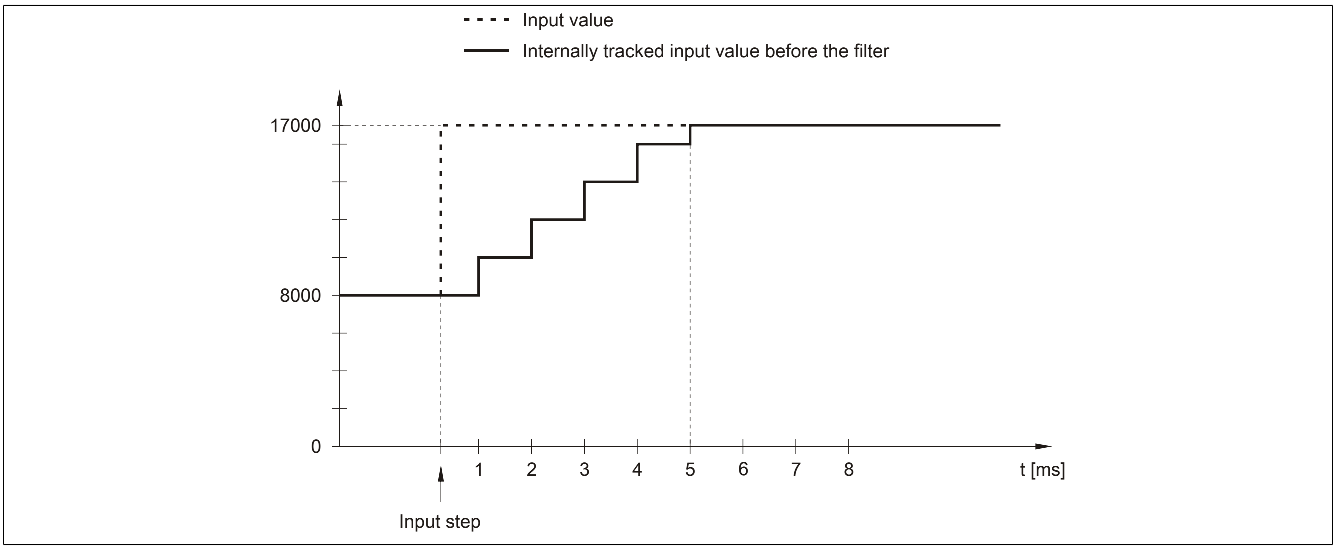


Figure 3: Tracked input value for input step

Example 2

A disturbance interferes with the input value. The diagram shows the tracked input value with the following settings:

Input ramp limiting = 4 = 0x07FF = 2047

Filter level = 2

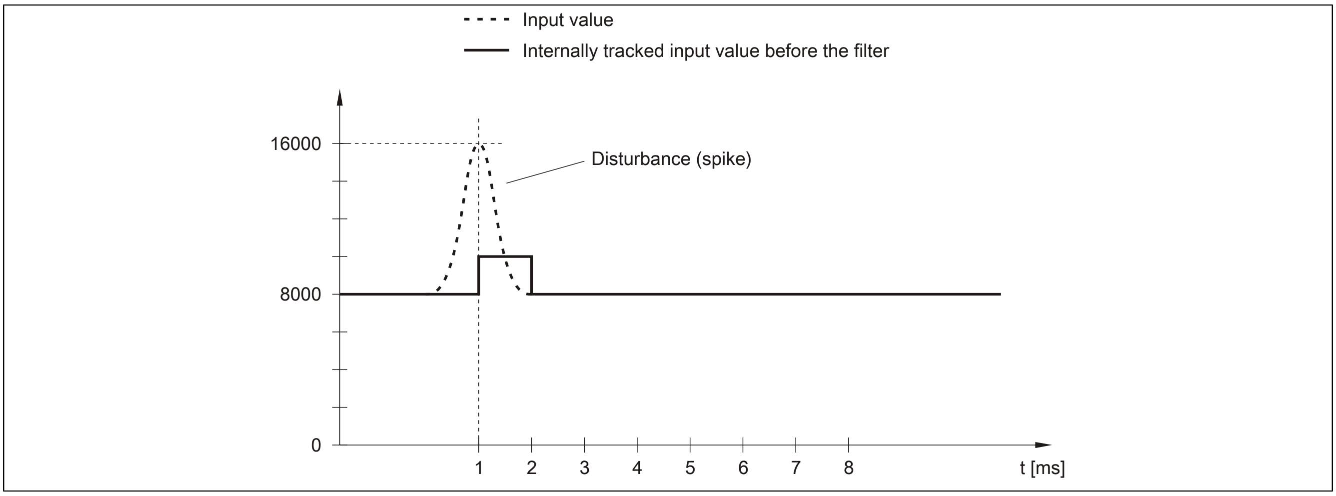


Figure 4: Tracked input value for disturbance

5 Commissioning

5.1 SGx target systems

SG3

This module is not supported on SG3 target systems.

SG4

The module comes with preinstalled firmware. The firmware is also part of the Automation Runtime operating system for the PLC. With different versions, the Automation Runtime firmware is loaded onto the module.

Current firmware is made available automatically by updating Automation Runtime.

6 Register description

6.1 General data points

In addition to the registers described in the register description, the module has additional general data points. These are not module-specific but contain general information such as serial number and hardware variant.

General data points are described in section "Additional information - General data points" in the X67 system user's manual.

6.2 Function model 0 - Standard

Register	Fixed offset	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
Configuration							
32	-	ConfigOutput01 (analog input filter)	USINT				•
34	-	ConfigOutput02 (input inversion)	USINT				•
Digital and analog inputs/outputs							
0	1	Input state of the digital inputs	USINT	•			
		DigitalInput01	Bit 0				
		...	...				
		DigitalInput06	Bit 5				
1	2	State of the digital outputs and the analog input	USINT	•			
		StatusDigitalOutput01	Bit 0				
		...	...				
		StatusDigitalOutput06	Bit 5				
		UnderflowAnalogInput01	Bit 6				
		OverflowAnalogInput01	Bit 7				
2	0	Switching state of digital outputs	USINT			•	
		DigitalOutput01	Bit 0				
		...	...				
		DigitalOutput06	Bit 5				
4	3	AnalogInput01	Int	•			
Propagation delay measurement							
3	1	Clearing values of time pairs	USINT			•	
		ClearTime01	Bit 0				
		...	...				
		ClearTime06	Bit 5				
2 + N*4	1 + N*4	GateTimeRising0N (index N = 1 to 6)	UINT	•			
4 + N*4	3 + N*4	GateTimeFalling0N (index N = 1 to 6)	UINT	•			

Fixed modules require their data points to be in a specific order in the X2X frame. Cyclic access occurs according to a predefined offset, not based on the register address.

Acyclic access continues to be based on the register numbers.

6.3 Configuration

6.3.1 Configuration - Analog input filters

Name:
ConfigOutput01

The filter level and input ramp limiting of the input filter are set in this register.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 2	Defines the filter level	000	Filter switched off
		001	Filter level 2
		010	Filter level 4
		011	Filter level 8
		100	Filter level 16
		101	Filter level 32
		110	Filter level 64
		111	Filter level 128
3	Reserved	0	
4 - 6	Defines input ramp limiting	000	The input value is applied without limiting.
		001	Limit value = 0x3FFF (16383)
		010	Limit value = 0x1FFF (8191)
		011	Limit value = 0x0FFF (4095)
		100	Limit value = 0x07FF (2047)
		101	Limit value = 0x03FF (1023)
		110	Limit value = 0x01FF (511)
		111	Limit value = 0x00FF (255)
7	Reserved	0	

6.3.2 Input inversion

Name:
ConfigOutput02

In this register, the Edge polarity can be set for digital inputs 1 to 6 for time recording. The state of the digital input registers is not affected.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Name	Value	Information
0	Polarity of digital input 1	0	The input state is not inverted based on digital output 1.
		1	The input state is inverted based on digital output 1.
...		...	
5	Polarity of digital input 6	0	The input state is not inverted based on digital output 6.
		1	The input state is inverted based on digital output 6.
6 - 7	Reserved	0	

6.4 Digital and analog inputs/outputs

6.4.1 Input state of the digital inputs

Name:
DigitalInput01 to DigitalInput06

This register contains the input state of digital inputs 1 to 6.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Name	Value	Information
0	DigitalInput01	0 or 1	Input state - Digital input 1
...		...	
5	DigitalInput06	0 or 1	Input state - Digital input 6
6 - 7	Reserved	-	

6.4.2 State of the digital outputs and the analog input

Name:
StatusDigitalOutput01 to StatusDigitalOutput06
UnderflowAnalogInput01
OverflowAnalogInput01

This register contains the state of digital outputs 1 to 6 as well as the analog input.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Name	Value	Information
Digital output status			
0	StatusDigitalOutput01	0	Channel 01: No error
		1	Channel 01: Short circuit or overload
...		...	
5	StatusDigitalOutput06	0	Channel 06: No error
		1	Channel 06: Short circuit or overload
Analog input status			
6	UnderflowAnalogInput01	0	No error
		1	Measured value < 0
7	OverflowAnalogInput01	0	No error
		1	Measured value > 32767

6.4.3 Switching state of digital outputs

Name:
DigitalOutput01 to DigitalOutput06

This register stores the switching state of digital outputs 1 to 6.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Name	Value	Information
0	DigitalOutput01	0	Digital output 01 reset
		1	Digital output 01 set
...		...	
5	DigitalOutput06	0	Digital output 06 reset
		1	Digital output 06 set
6 - 7	Reserved	-	

6.4.4 Input value of the analog input

Name:
AnalogInput01

This register contains the analog input value.

Data type	Values	Input signal:
INT	0 to 32767	Current signal 0 to 20 mA

6.5 Propagation delay measurement

6.5.1 Clearing values of time pairs

Name:
ClearTime01 to ClearTime06

When these register bits change from 0 to 1, the values of registers "GateTimeRising" on page 20 and "GateTimeFalling" on page 20 assigned to the channel are set to zero.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Name	Value	Information
0	ClearTime01	0	Do not reset
		1	Reset register pair 01
...		...	
5	ClearTime06	0	Do not reset
		1	Reset register pair 06
6 - 7	Reserved	-	

6.5.2 Switch-on time difference

Name:
GateTimeRising01 to GateTimeRising06

This register indicates the measured time between switching on output DigitalOutput0x and reading back the signal edge of input DigitalInput0x.

After 6.5535 seconds (or any multiple) a counter overflow occurs and the value starts again at 0. Measurements longer than 6.5535 seconds must therefore be performed from the application.

Data type	Values	Information
UINT	0 to 65535	Propagation delay in 0.1 ms

6.5.3 Switch-off time difference

Name:
GateTimeFalling01 to GateTimeFalling06

This register indicates the measured time between switching off output DigitalOutput0x and reading back the signal edge of input DigitalInput0x.

After 6.5535 seconds (or any multiple) a counter overflow occurs and the value starts again at 0. Measurements longer than 6.5535 seconds must therefore be performed from the application.

Data type	Values	Information
UINT	0 to 65535	Propagation delay in 0.1 ms

6.6 Minimum I/O update time

The minimum I/O update time specifies how far the bus cycle can be reduced so that an I/O update is performed in each cycle.

Minimum I/O update time
250 μs

6.7 Minimum cycle time

The minimum cycle time specifies how far the bus cycle can be reduced without communication errors occurring. It is important to note that very fast cycles reduce the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time
250 μs