FAIRCHILD
SEMICONDUCTOR®

July 2013

FDMS3660AS

PowerTrench® Power Stage

Asymmetric Dual N-Channel MOSFET

Features

Q1: N-Channel

- Max $r_{DS(on)}$ = 8 mΩ at V_{GS} = 10 V, I_D = 13 A
- Max $r_{DS(on)}$ = 11 mΩ at V_{GS} = 4.5 V, I_D = 11 A

Q2: N-Channel

- Max $r_{DS(on)}$ = 1.8 mΩ at V_{GS} = 10 V, I_D = 30 A
- Max $r_{DS(on)}$ = 2.2 mΩ at V_{GS} = 4.5 V, I_D = 27 A
- Low inductance packaging shortens rise/fall times, resulting in lower switching losses
- MOSFET integration enables optimum layout for lower circuit inductance and reduced switch node ringing
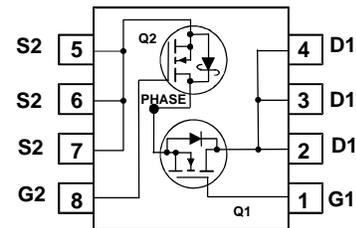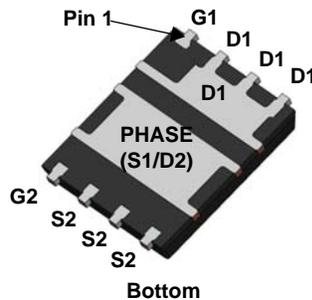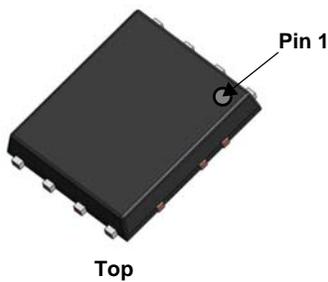- RoHS Compliant

General Description

This device includes two specialized N-Channel MOSFETs in a dual PQFN package. The switch node has been internally connected to enable easy placement and routing of synchronous buck converters. The control MOSFET (Q1) and synchronous SyncFET™ (Q2) have been designed to provide optimal power efficiency.

Applications

- Computing
- Communications
- General Purpose Point of Load
- Notebook VCORE

Top

Bottom

Pin 1   G1   D1   D1   D1   D1   PHASE (S1/D2)   G2   S2   S2   S2

S2	5	Q2	4 D1
S2	6	PHASE	3 D1
S2	7		2 D1
G2	8	Q1	1 G1

MOSFET Maximum Ratings T_A = 25 °C unless otherwise noted

Symbol	Parameter		Q1	Q2	Units
V_{DS}	Drain to Source Voltage		30	30	V
V_{GS}	Gate to Source Voltage (Note 3)		±20	±12	V
I_D	Drain Current -Continuous	T_C = 25 °C	56	130	A
	-Continuous	T_A = 25 °C	13[1a]	30[1b]	
	-Pulsed	(Note 4)	70	140	
E_{AS}	Single Pulse Avalanche Energy		73[5]	150[6]	mJ
P_D	Power Dissipation for Single Operation	T_A = 25 °C	2.2[1a]	2.5[1b]	W
	Power Dissipation for Single Operation	T_A = 25 °C	1.0[1c]	1.0[1d]	
T_J, T_{STG}	Operating and Storage Junction Temperature Range		-55 to +150		°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction to Ambient		57[1a]	50[1b]	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient		125[1c]	120[1d]	
$R_{\theta JC}$	Thermal Resistance, Junction to Case		3.5	2.2	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
27CF 32CD	FDMS3660AS	Power 56	13 "	12 mm	3000 units

Electrical Characteristics T_J = 25 °C unless otherwise noted

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units

Off Characteristics

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 µA, V_{GS} = 0 V I_D = 1 mA, V_{GS} = 0 V	Q1 Q2	30 30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 µA, referenced to 25 °C I_D = 10 mA, referenced to 25 °C	Q1 Q2		16 29		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 24 V, V_{GS} = 0 V	Q1 Q2			1 500	µA µA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = 20 V, V_{DS} = 0 V V_{GS} = 12 V, V_{DS} = 0 V	Q1 Q2			100 100	nA nA

On Characteristics

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 µA V_{GS} = V_{DS}, I_D = 1 mA	Q1 Q2	1.1 1.2	2.0 1.5	2.7 2.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250 µA, referenced to 25 °C I_D = 10 mA, referenced to 25 °C	Q1 Q2		-6 -3		mV/°C
$r_{DS(on)}$	Drain to Source On Resistance	V_{GS} = 10 V, I_D = 13 A V_{GS} = 4.5 V, I_D = 11 A V_{GS} = 10 V, I_D = 13 A, T_J = 125 °C	Q1		5.9 8.5 7.9	8 11 11	mΩ
		V_{GS} = 10 V, I_D = 30 A V_{GS} = 4.5 V, I_D = 27 A V_{GS} = 10 V, I_D = 30 A, T_J = 125 °C	Q2		1.2 1.5 1.8	1.8 2.2 2.7	
g_{FS}	Forward Transconductance	V_{DS} = 5 V, I_D = 13 A V_{DS} = 5 V, I_D = 30 A	Q1 Q2		173 240		S

Dynamic Characteristics

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
C_{iss}	Input Capacitance	Q1: V_{DS} = 15 V, V_{GS} = 0 V, f = 1 MHZ	Q1 Q2		1485 4150	2230 6225	pF
C_{oss}	Output Capacitance	Q2: V_{DS} = 15 V, V_{GS} = 0 V, f = 1 MHZ	Q1 Q2		397 1195	595 1795	pF
C_{rss}	Reverse Transfer Capacitance		Q1 Q2		37 117	70 245	pF
R_g	Gate Resistance		Q1 Q2	0.1 0.1	1.6 1.0	3.2 2.0	Ω

Switching Characteristics

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
$t_{d(on)}$	Turn-On Delay Time		Q1 Q2		9 12	17 22	ns
t_r	Rise Time	Q1: V_{DD} = 15 V, I_D = 13 A, R_{GEN} = 6 Ω	Q1 Q2		3 5	10 10	ns
$t_{d(off)}$	Turn-Off Delay Time	Q2: V_{DD} = 15 V, I_D = 30 A, R_{GEN} = 6 Ω	Q1 Q2		21 38	33 60	ns
t_f	Fall Time		Q1 Q2		3 5	10 10	ns
Q_g	Total Gate Charge	V_{GS} = 0 V to 10 V	Q1 Q2		21 64	30 90	nC
Q_g	Total Gate Charge	V_{GS} = 0 V to 4.5 V	Q1 Q2		10 30	13 43	nC
Q_{gs}	Gate to Source Gate Charge	Q1: V_{DD} = 15 V, I_D = 13 A Q2: V_{DD} = 15 V, I_D = 30 A	Q1 Q2		4.5 9		nC
Q_{gd}	Gate to Drain "Miller" Charge		Q1 Q2		2.0 9		nC

Electrical Characteristics T_J = 25 °C unless otherwise noted

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
Drain-Source Diode Characteristics							
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 13 A (Note 2) V_{GS} = 0 V, I_S = 2 A (Note 2) V_{GS} = 0 V, I_S = 30 A (Note 2) V_{GS} = 0 V, I_S = 2 A (Note 2)	Q1 Q1 Q2 Q2		0.84 0.74 0.77 0.48	1.2 1.2 1.2 1.2	V
t_{rr}	Reverse Recovery Time	Q1: I_F = 13 A, di/dt = 100 A/µs	Q1 Q2		25 33	40 53	ns
Q_{rr}	Reverse Recovery Charge	Q2: I_F = 30 A, di/dt = 300 A/µs	Q1 Q2		9 41	18 66	nC

Notes:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.
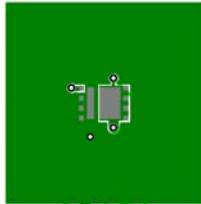
a. 57 °C/W when mounted on a 1 in^2 pad of 2 oz copper
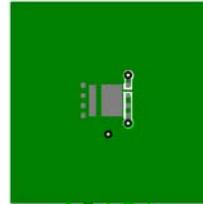
b. 50 °C/W when mounted on a 1 in^2 pad of 2 oz copper
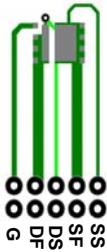
c. 125 °C/W when mounted on a minimum pad of 2 oz copper

d. 120 °C/W when mounted on a minimum pad of 2 oz copper

2. Pulse Test: Pulse Width < 300 µs, Duty cycle < 2.0%.
3. As an N-ch device, the negative Vgs rating is for low duty cycle pulse ocurrence only. No continuous rating is implied with the negative Vgs rating.
4. Pulsed Id limited by junction temperature, td<=100 µS, please refer to SOA curve for more details.
5. E_{AS} of 73 mJ is based on starting T_J = 25 °C; N-ch: L = 3 mH, I_{AS} = 7 A, V_{DD} = 30 V, V_{GS} = 10 V. 100% test at L= 0.1 mH, I_{AS} = 23 A.
6. E_{AS} of 150 mJ is based on starting T_J = 25 °C; N-ch: L = 3 mH, I_{AS} = 10 A, V_{DD} = 30 V, V_{GS} = 10 V. 100% test at L= 0.1 mH, I_{AS} = 31 A.

Typical Characteristics (Q1 N-Channel) T_J = 25 °C unless otherwise noted
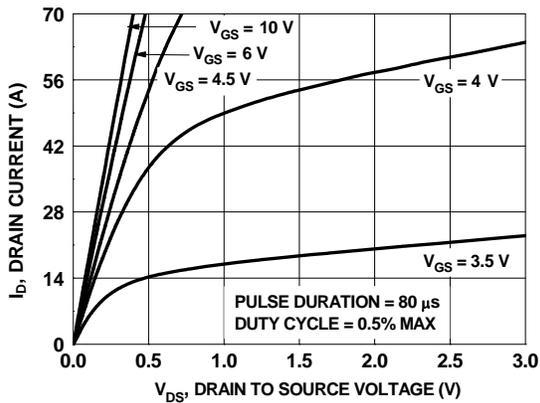

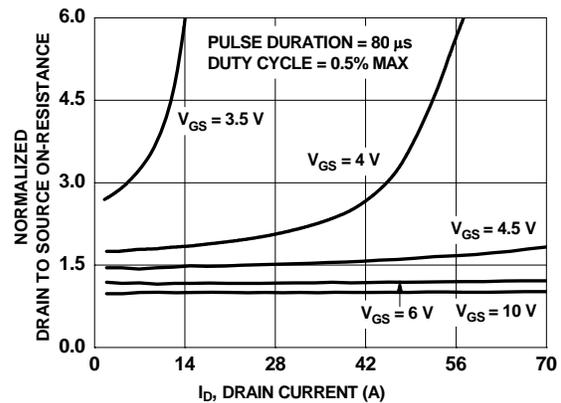**Figure 1. On Region Characteristics**

Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage
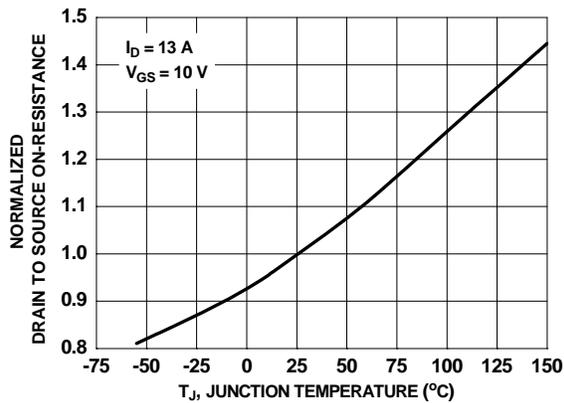

Figure 3. Normalized On Resistance vs Junction Temperature
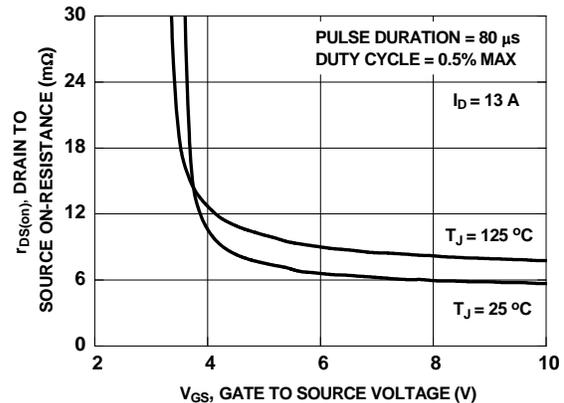

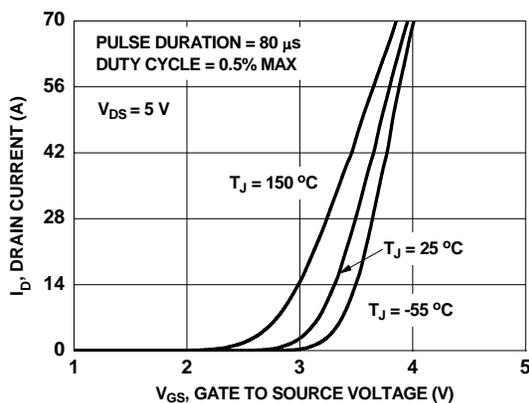**Figure 4. On-Resistance vs Gate to Source Voltage**

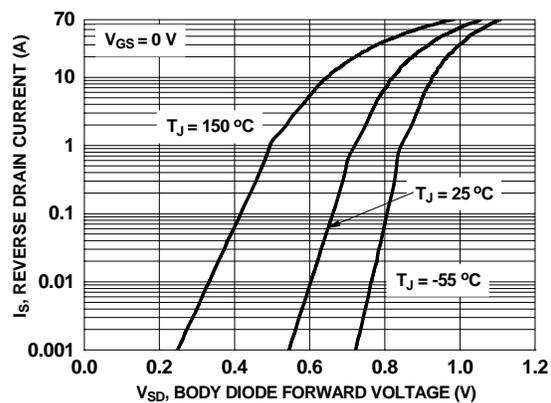**Figure 5. Transfer Characteristics**

Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics (Q1 N-Channel) T_J = 25 °C unless otherwise noted
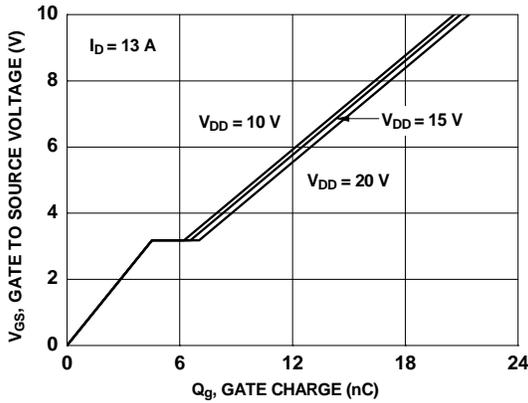
Figure 7. Gate Charge Characteristics
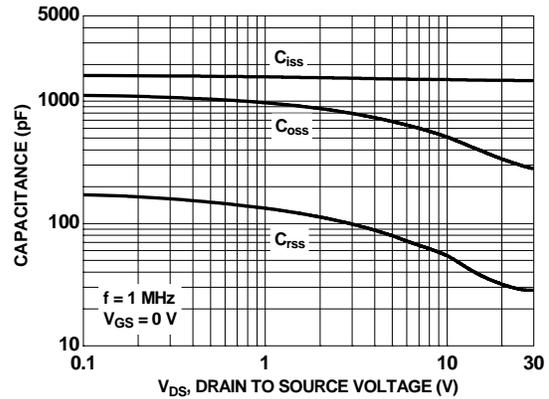
Figure 8. Capacitance vs Drain to Source Voltage
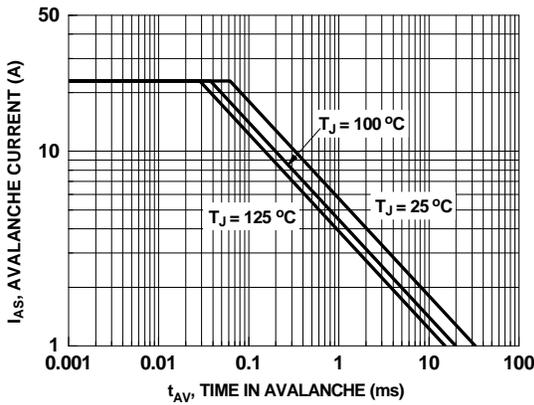

Figure 9. Unclamped Inductive Switching Capability
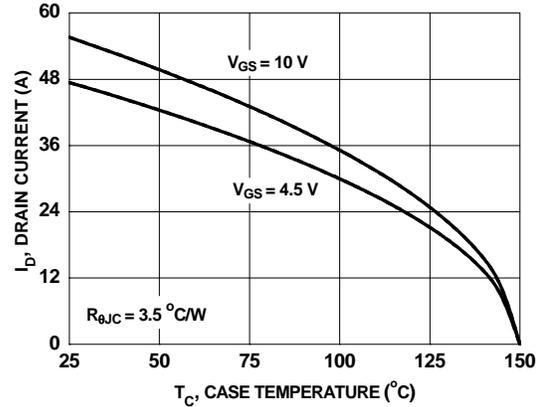

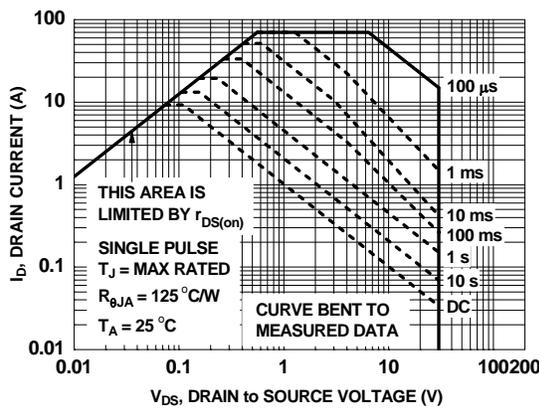Figure 10. Maximum Continuous Drain Current vs Case Temperature
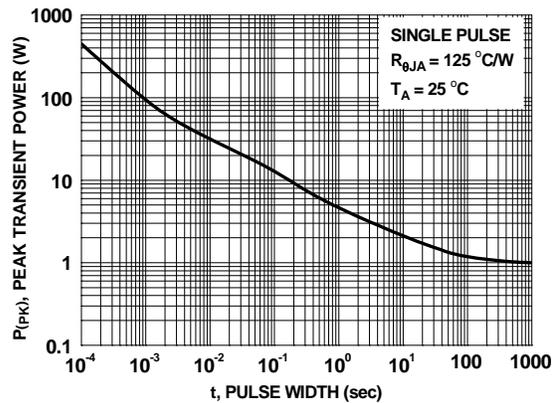

Figure 11. Forward Bias Safe Operating Area

Figure 12. Single Pulse Maximum Power Dissipation

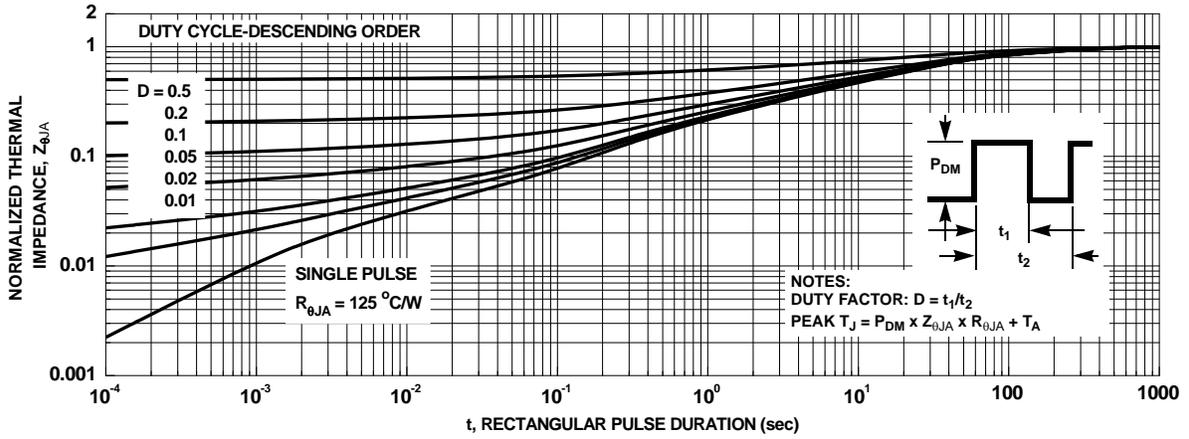## Typical Characteristics (Q1 N-Channel) T_J = 25 °C unless otherwise noted

DUTY CYCLE-DESCENDING ORDER

D = 0.5
0.2
0.1
0.05
0.02
0.01

NORMALIZED THERMAL IMPEDANCE, $Z_{\theta JA}$

SINGLE PULSE

$R_{\theta JA}$ = 125 ^{o}C/W

P_{DM}

t_1

t_2

NOTES:
DUTY FACTOR: D = t_1/t_2
PEAK T_J = P_{DM} x $Z_{\theta JA}$ x $R_{\theta JA}$ + T_A

t, RECTANGULAR PULSE DURATION (sec)

Figure 13. Junction-to-Ambient Transient Thermal Response Curve

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Typical Characteristics (Q2 N-Channel) T_J = 25 °C unlenss otherwise noted
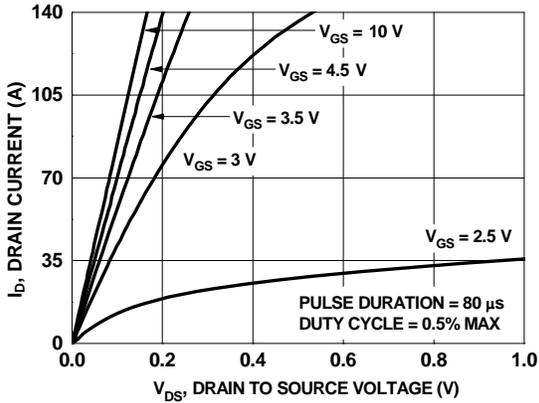
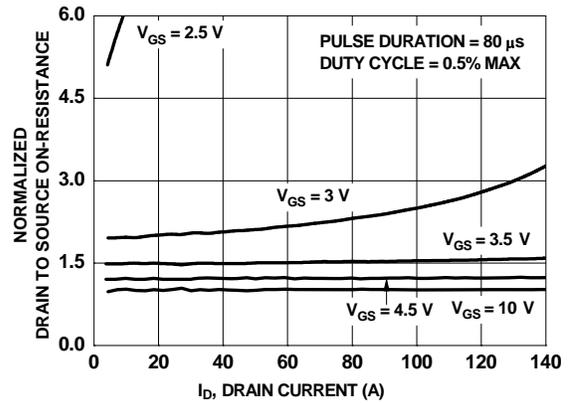

Figure 14. On-Region Characteristics

Figure 15. Normalized on-Resistance vs Drain Current and Gate Voltage
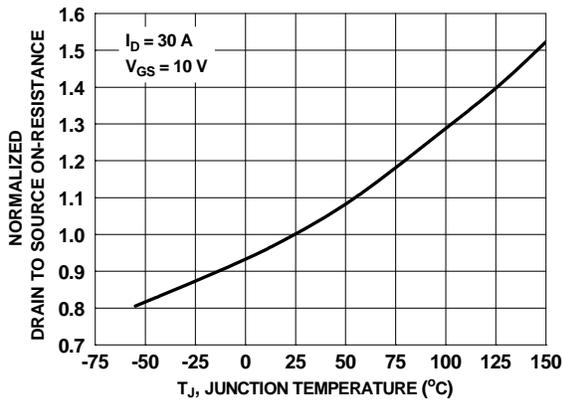

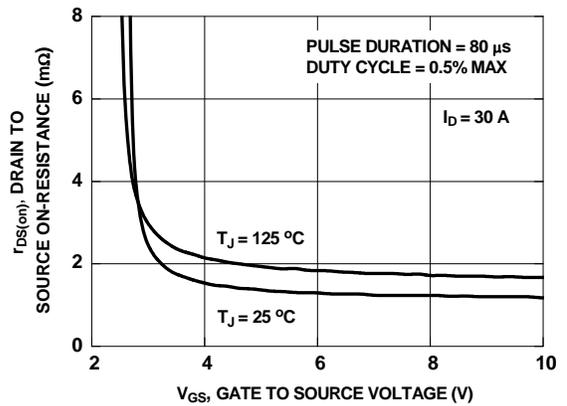**Figure 16. Normalized On-Resistance vs Junction Temperature**

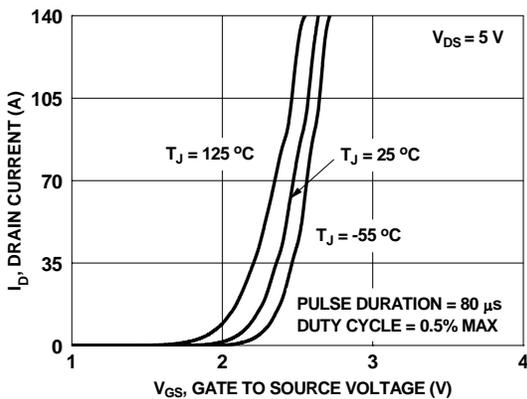**Figure 17. On-Resistance vs Gate to Source Voltage**
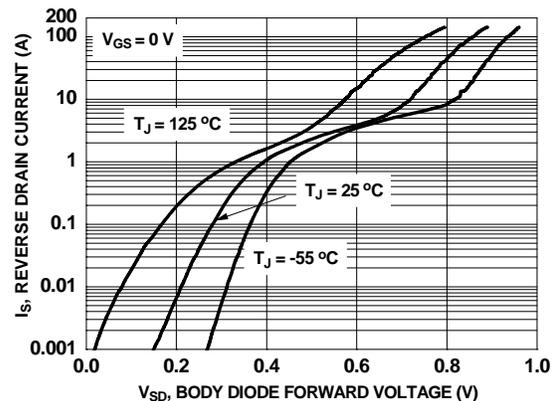

Figure 18. Transfer Characteristics

Figure 19. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics (Q2 N-Channel) T_J = 25 °C unless otherwise noted
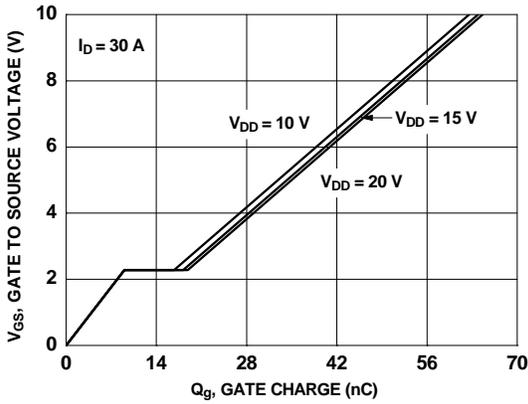
Figure 20. Gate Charge Characteristics
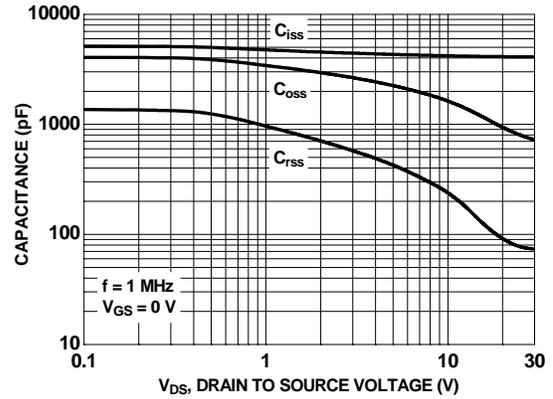
Figure 21. Capacitance vs Drain to Source Voltage

Figure 22. Unclamped Inductive Switching Capability

Figure 23. Maximun Continuous Drain Current vs Case Temperature

Figure 24. Forward Bias Safe Operating Area
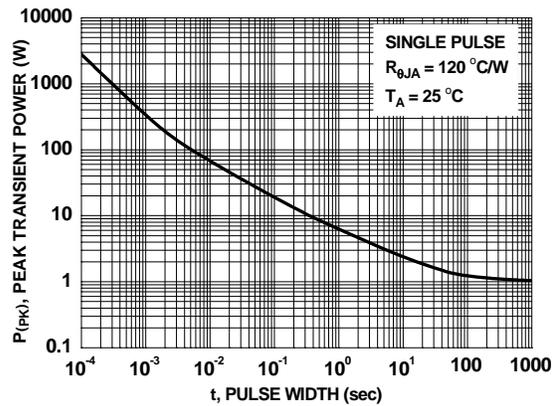
Figure 25. Single Pulse Maximum Power Dissipation

Typical Characteristics (Q2 N-Channel) T_J = 25 ^{o}C unless otherwise noted
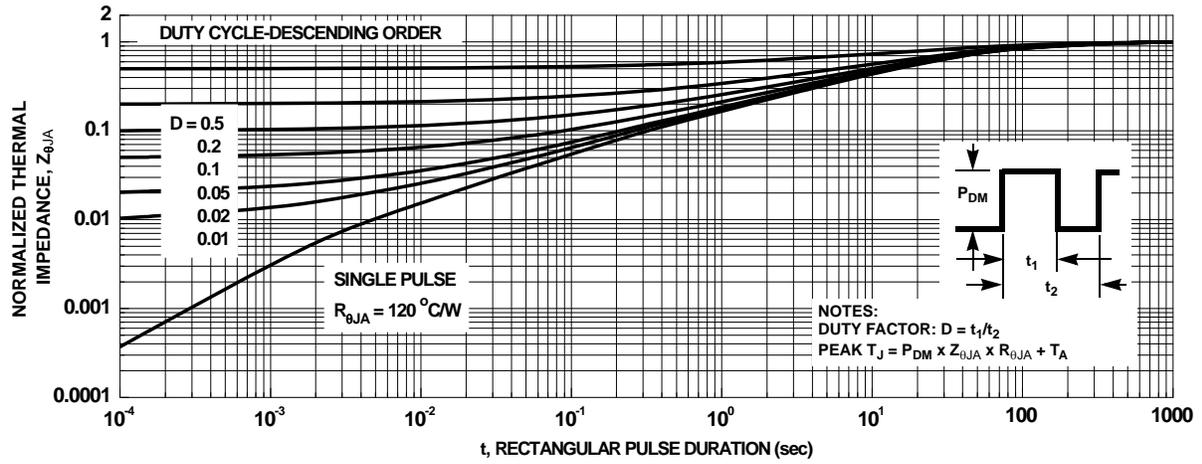
Figure 26. Junction-to-Ambient Transient Thermal Response Curve

Typical Characteristics (continued)

SyncFET™ Schottky body diode Characteristics
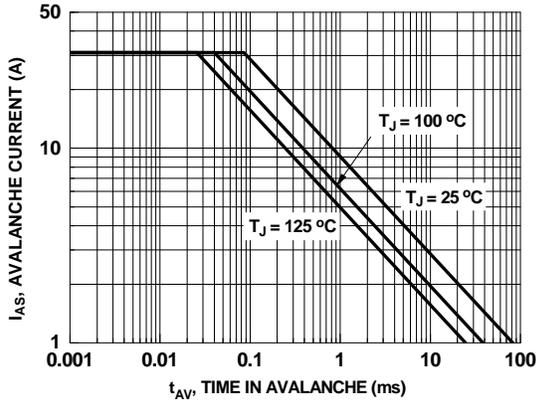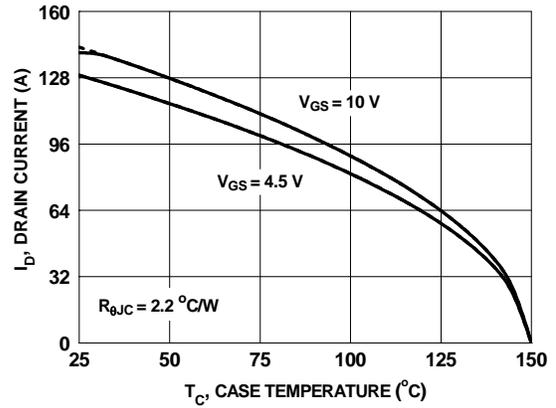
Fairchild's SyncFET™ process embeds a Schottky diode in parallel with PowerTrench MOSFET. This diode exhibits similar characteristics to a discrete external Schottky diode in parallel with a MOSFET. Figure 27 shows the reverse recovery characteristic of the FDMS3660AS.

Schottky barrier diodes exhibit significant leakage at high temperature and high reverse voltage. This will increase the power in the device.
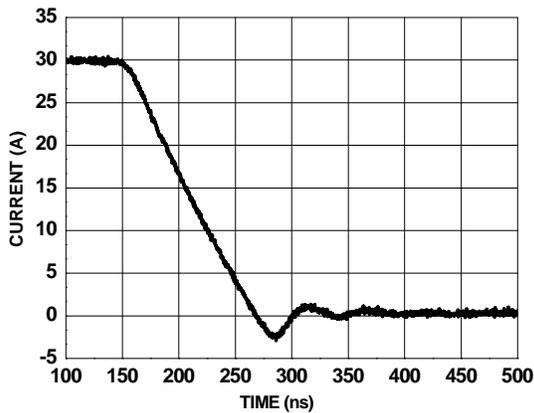
Figure 27. FDMS3660AS SyncFET™ Body Diode Reverse Recovery Characteristic
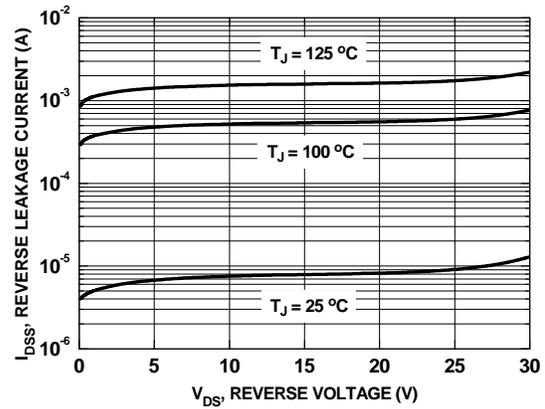
Figure 28. SyncFET™ Body Diode Reverse Leakage Versus Drain-Source Voltage

Dimensional Outline and Pad Layout

TOP VIEW

5.10 / 4.90

6.25 / 5.90

PKG ₵

PIN # 1 INDICATOR

0.10 C (2X)

0.10 C (2X)

A

B

8   5

1   4

SIDE VIEW

SEE DETAIL A

RECOMMENDED LAND PATTERN FOR SAWN / PUNCHED TYPE

2.00

4.00

0.00 ₵

1.27 TYP

0.65 TYP

0.63

2.52

1.60

KEEP OUT AREA

2.15

0.00 ₵

4.16

1.21

2.13

2.31

0.63

3.15

1.18

0.59

3.18

5.10

8 7 6 5

1 2 3 4

BOTTOM VIEW
OPTION - A (SAWN TYPE)

0.10 Ⓜ C A B
0.05 Ⓜ C

0.65 / 0.38

3.16 / 2.80

0.70 / 0.36

0.35 / 0.30 (6X)

1.34 / 1.12

1 2 3 4

0.66 ? 05

2.25 / 2.05

4.08 / 3.70

0.65 / 0.38

8 7 6 5

1.02 / 0.82

0.44 / 0.24

0.61 / 0.31 (8X)

1.27

3.81

DETAIL 'A'
(SCALE: 2X)

// 0.10 C

8X

0.08 C

1.10 / 0.90

0.35 / 0.15

0.05 / 0.00

C

SEATING PLANE

Dimensional Outline and Pad Layout

TOP VIEW

SIDE VIEW

DETAIL 'B'
(SCALE: 2X)

DETAIL 'C'
(SCALE: 2X)

SEATING PLANE

BOTTOM VIEW
OPTION - B (PUNCHED TYPE)

NOTES: UNLESS OTHERWISE SPECIFIED
A) PACKAGE STANDARD REFERENCE:
   JEDEC REGISTRATION, MO-240, VARIATION AA.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS DO NOT INCLUDE BURRS OR
   MOLD FLASH. MOLD FLASH OR BURRS DOES
   NOT EXCEED 0.10MM.
D) DIMENSIONING AND TOLERANCING PER
   ASME Y14.5M-1994.
E) IT IS RECOMMENDED TO HAVE NO TRACES
   OR VIAS WITHIN THE KEEP OUT AREA.
F) DRAWING FILE NAME:

FDMS3660AS PowerTrench® Power Stage

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CorePOWER™	Green FPS™ e-Series™	QS™	TinyCalc™
CROSSVOLT™	Gmax™	Quiet Series™	TinyLogic®
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Current Transfer Logic™	IntelliMAX™		TinyPower™
DEUXPEED®	ISOPLANAR™	™	TinyPWM™
Dual Cool™	Marking Small Speakers Sound Louder	Saving our world, 1mW/W/kW at a time™	TinyWire™
EcoSPARK®	and Better™	SignalWise™	TranSiC®
EfficentMax™	MegaBuck™	SmartMax™	TriFault Detect™
ESBC™	MICROCOUPLER™	SMART START™	TRUECURRENT®*
	MicroFET™	Solutions for Your Success™	µSerDes™
®	MicroPak™	SPM®	
Fairchild®	MicroPak2™	STEALTH™	
Fairchild Semiconductor®	MillerDrive™	SuperFET®	UHC®
FACT Quiet Series™	MotionMax™	SuperSOT™-3	Ultra FRFET™
FACT®	mWSaver™	SuperSOT™-6	UniFET™
FAST®	OptoHiT™	SuperSOT™-8	VCX™
FastvCore™	OPTOLOGIC®	SupreMOS®	VisualMax™
FETBench™	OPTOPLANAR®	SyncFET™	VoltagePlus™
			XS™

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As used here in:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.

2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

ANTI-COUNTERFEITING POLICY
Fairchild Semiconductor Corporation's Anti-Counterfeiting Policy. Fairchild's Anti-Counterfeiting Policy is also stated on our external website, www.Fairchildsemi.com, under Sales Support.

Counterfeiting of semiconductor parts is a growing problem in the industry. All manufactures of semiconductor products are experiencing counterfeiting of their parts. Customers who inadvertently purchase counterfeit parts experience many problems such as loss of brand reputation, substandard performance, failed application, and increased cost of production and manufacturing delays. Fairchild is taking strong measures to protect ourselves and our customers from the proliferation of counterfeit parts. Fairchild strongly encourages customers to purchase Fairchild parts either directly from Fairchild or from Authorized Fairchild Distributors who are listed by country on our web page cited above. Products customers buy either from Fairchild directly or from Authorized Fairchild Distributors are genuine parts, have full traceability, meet Fairchild's quality standards for handing and storage and provide access to Fairchild's full range of up-to-date technical and product information. Fairchild and our Authorized Distributors will stand behind all warranties and will appropriately address and warranty issues that may arise. Fairchild will not provide any warranty coverage or other assistance for parts bought from Unauthorized Sources. Fairchild is committed to combat this global problem and encourage our customers to do their part in stopping this practice by buying direct or from authorized distributors.

PRODUCT STATUS DEFINITIONS
Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

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