

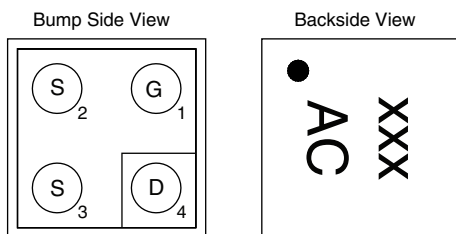


P-Channel 8 V (D-S) MOSFET

PRODUCT SUMMARY

V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A) ^a	Q_g (Typ.)
- 8	0.068 at $V_{GS} = - 4.5$ V	- 3.1	6.7 nC
	0.088 at $V_{GS} = - 2.5$ V	- 2.7	
	0.155 at $V_{GS} = - 1.5$ V	- 2.1	
	0.290 at $V_{GS} = - 1.2$ V	- 0.5	

MICRO FOOT



Device Marking: xxx = Date/Lot Traceability Code
AC

Ordering Information: Si8805EDB-T2-E1 (Lead (Pb)-free and Halogen-free)

FEATURES

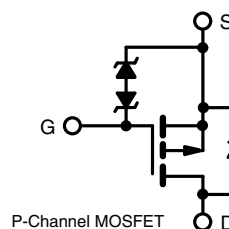
- TrenchFET[®] Power MOSFET
- Ultra Small 0.8 mm x 0.8 mm Outline
- Ultra Thin 0.357 mm Height
- Typical ESD Protection 1500 V HBM
- Material categorization:
For definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- Portable Devices such as Cell Phones, Smart Phones, Tablet PCs and Media Players
 - Load Switch for Low Voltage Gate Drive
 - Load Switch for 1.2 V Power Line



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C, unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	- 8	V
Gate-Source Voltage	V_{GS}	± 5	
Continuous Drain Current ($T_J = 150$ °C)	I_D	$T_A = 25$ °C	A
		$T_A = 70$ °C	
		$T_A = 25$ °C	
		$T_A = 70$ °C	
Pulsed Drain Current	I_{DM}	- 15	A
Continuous Source-Drain Diode Current	I_S	$T_A = 25$ °C	
		$T_A = 25$ °C	
Maximum Power Dissipation	P_D	$T_A = 25$ °C	W
		$T_A = 70$ °C	
		$T_A = 25$ °C	
		$T_A = 70$ °C	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 150	°C
Soldering Recommendations (Peak Temperature) ^c		260	

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{a, d}	R_{thJA}	105	135	°C/W
Maximum Junction-to-Ambient ^{b, e}		200	260	

Notes:

- Surface mounted on 1" x 1" FR4 board with full copper, $t = 5$ s.
- Surface mounted on 1" x 1" FR4 board with minimum copper, $t = 5$ s.
- Refer to IPC/JEDEC (J-STD-020), no manual or hand soldering.
- Maximum under steady state conditions is 185 °C/W.
- Maximum under steady state conditions is 330 °C/W.

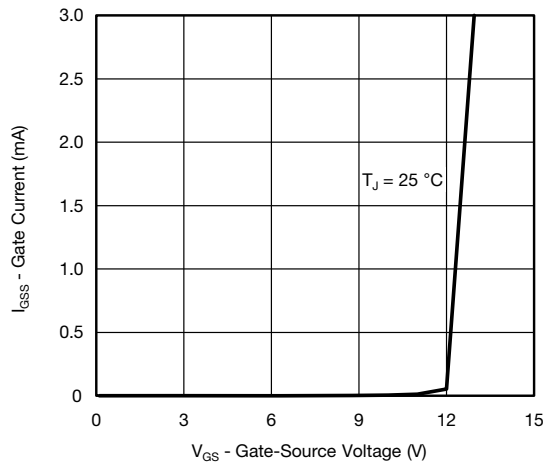
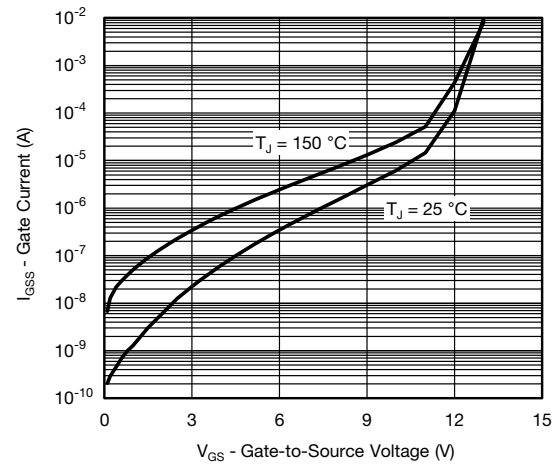
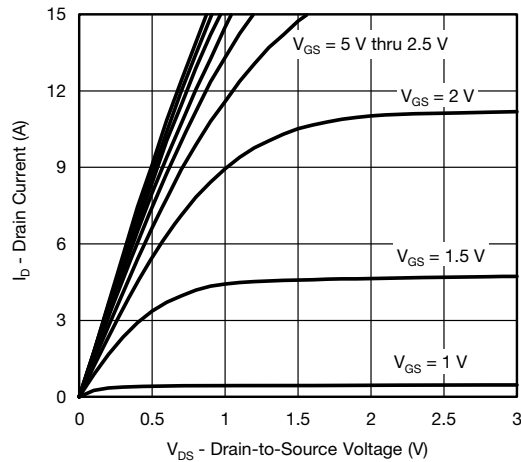
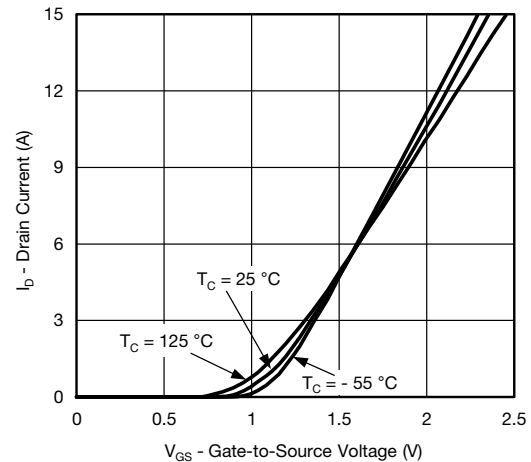
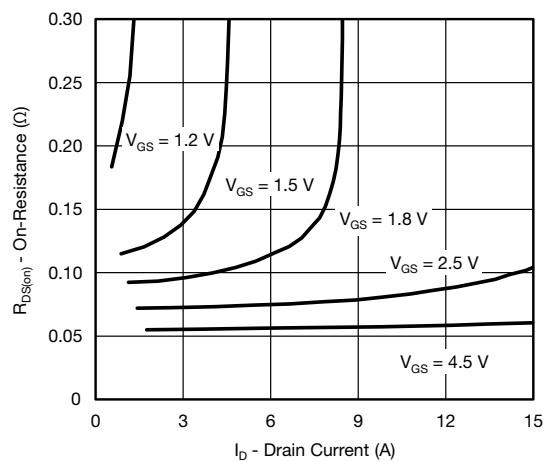
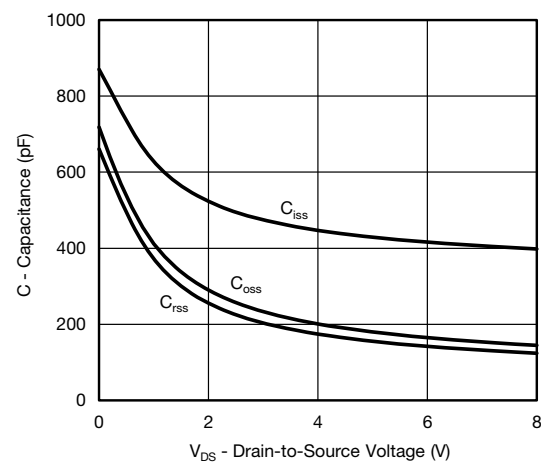
SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = - 250 μA	- 8			V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	I _D = - 250 μA		- 4		mV/°C
V _{GS(th)} Temperature Coefficient	ΔV _{GS(th)} /T _J			2.1		
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = - 250 μA	- 0.35		- 0.7	V
Gate-Source Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 5 V			± 1.5	μA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = - 8 V, V _{GS} = 0 V			- 1	
		V _{DS} = - 8 V, V _{GS} = 0 V, T _J = 55 °C			- 10	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≤ - 4 V, V _{GS} = - 4.5 V	- 5			A
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = - 4.5 V, I _D = - 1.5 A		0.056	0.068	Ω
		V _{GS} = - 2.5 V, I _D = - 1.5 A		0.070	0.088	
		V _{GS} = - 1.5 V, I _D = - 0.5 A		0.115	0.155	
		V _{GS} = - 1.2 V, I _D = - 0.3 A		0.190	0.290	
Forward Transconductance ^a	g _{fs}	V _{DS} = - 4 V, I _D = - 1.5 A		8		S
Dynamic ^b						
Total Gate Charge	Q _g	V _{DS} = - 4 V, V _{GS} = - 4.5 V, I _D = - 1.5 A		6.7	10	nC
Gate-Source Charge	Q _{gs}			0.7		
Gate-Drain Charge	Q _{gd}			1.8		
Gate Resistance	R _g	f = 1 MHz		10		Ω
Turn-On Delay Time	t _{d(on)}	V _{DD} = - 4 V, R _L = 2.7 Ω I _D ≅ - 1.5 A, V _{GEN} = - 4.5 V, R _g = 1 Ω		13	25	ns
Rise Time	t _r			13	25	
Turn-Off Delay Time	t _{d(off)}			25	50	
Fall Time	t _f			17	35	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C			- 0.7	A
Pulse Diode Forward Current	I _{SM}				- 15	
Body Diode Voltage	V _{SD}	I _S = - 1.5 A, V _{GS} = 0 V		- 0.8	- 1.2	V
Body Diode Reverse Recovery Time	t _{rr}	I _F = - 1.5 A, dI/dt = 100 A/μs, T _J = 25 °C		35	70	ns
Body Diode Reverse Recovery Charge	Q _{rr}			15	30	nC
Reverse Recovery Fall Time	t _a			15		ns
Reverse Recovery Rise Time	t _b			20		

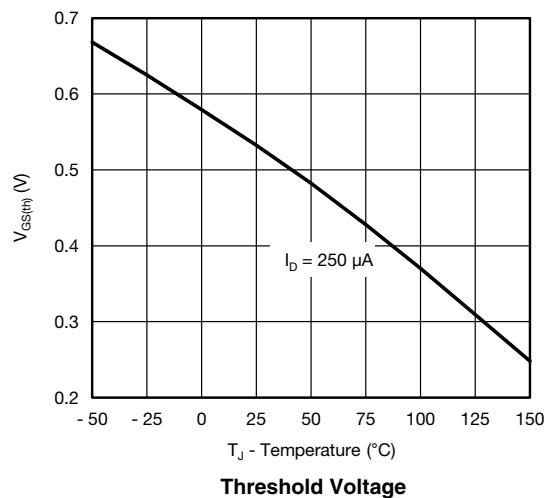
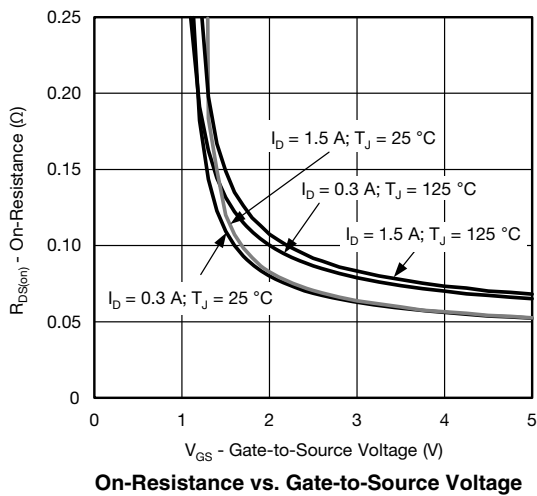
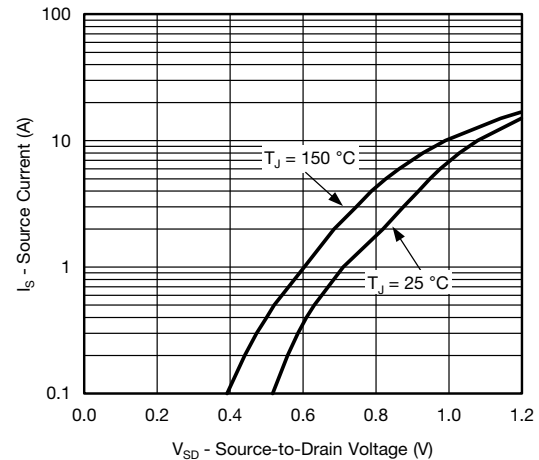
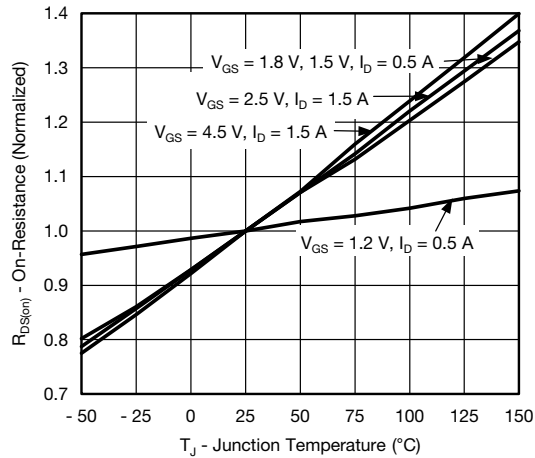
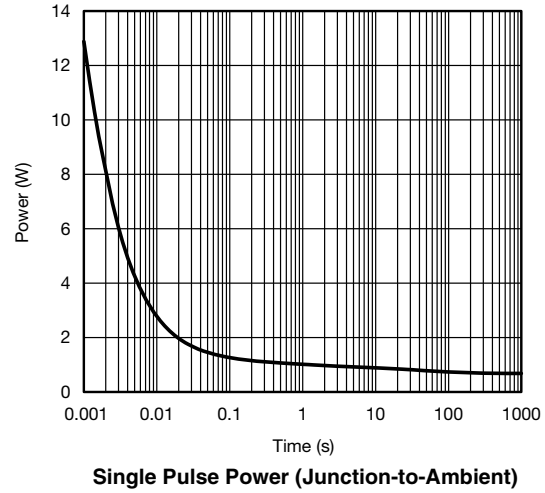
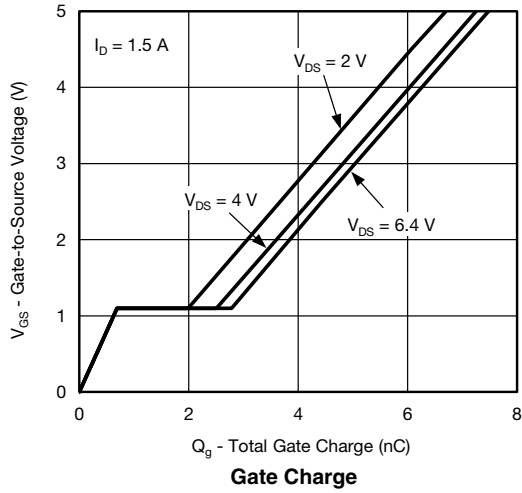
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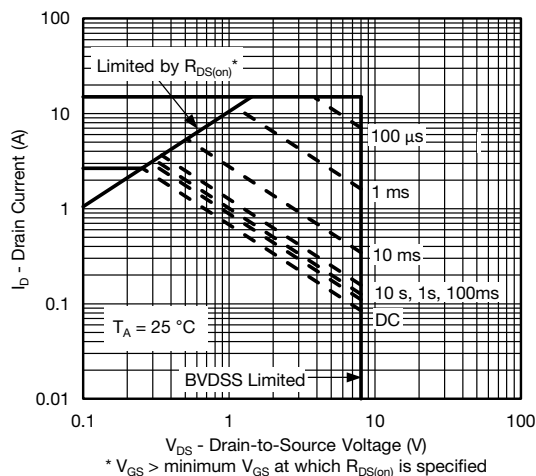
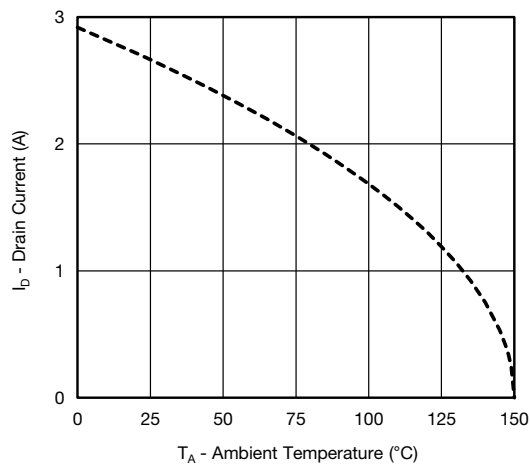
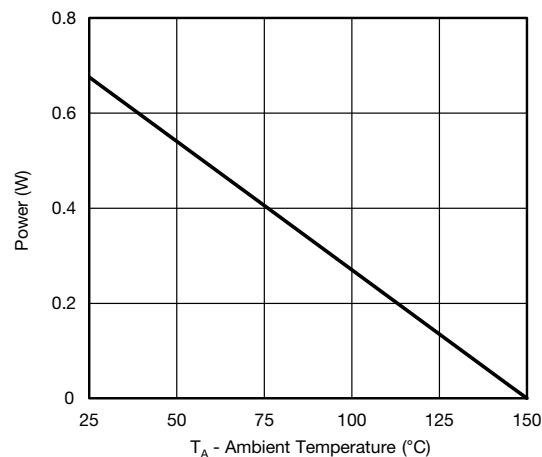
a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$

b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.


TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Gate Current vs. Gate-Source Voltage

Gate Current vs. Gate-Source Voltage

Output Characteristics

Transfer Characteristics

On-Resistance vs. Drain Current

Capacitance

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)**Safe Operating Area, Junction-to-Ambient****Current Derating*****Power Derating**

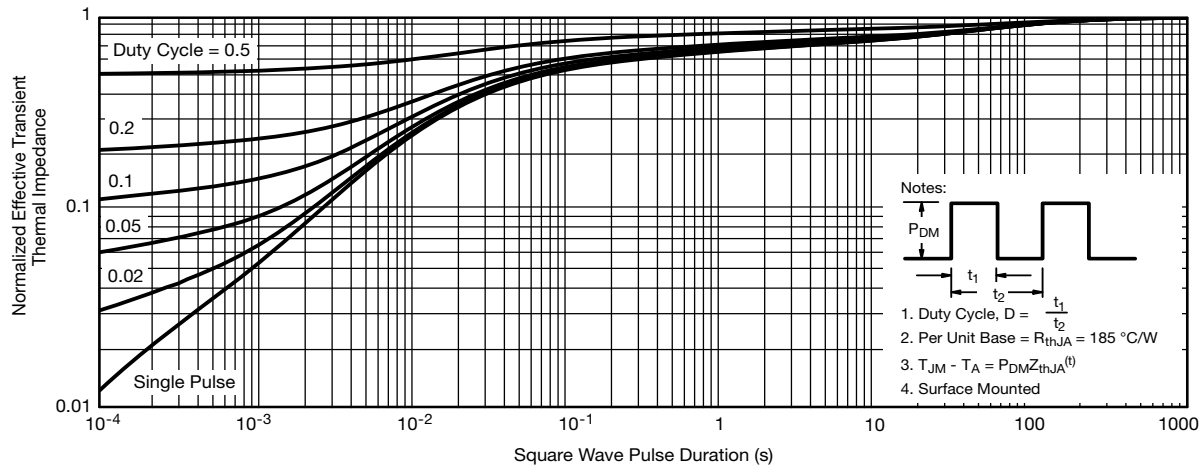
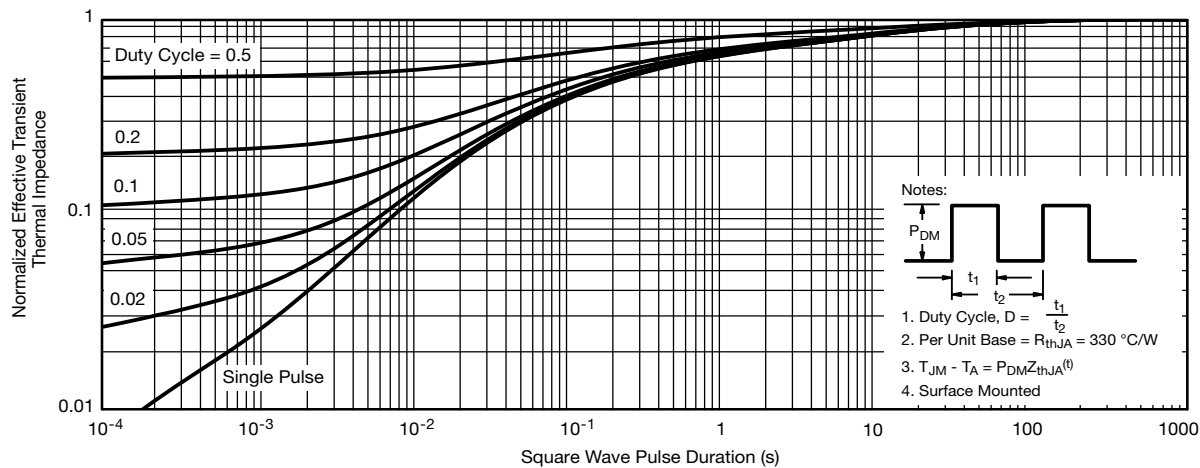
Note:

When mounted on 1" x 1" FR4 with full copper.

* The power dissipation P_D is based on $T_{J(max)} = 150\text{ °C}$, using junction-to-ambient thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

Si8805EDB

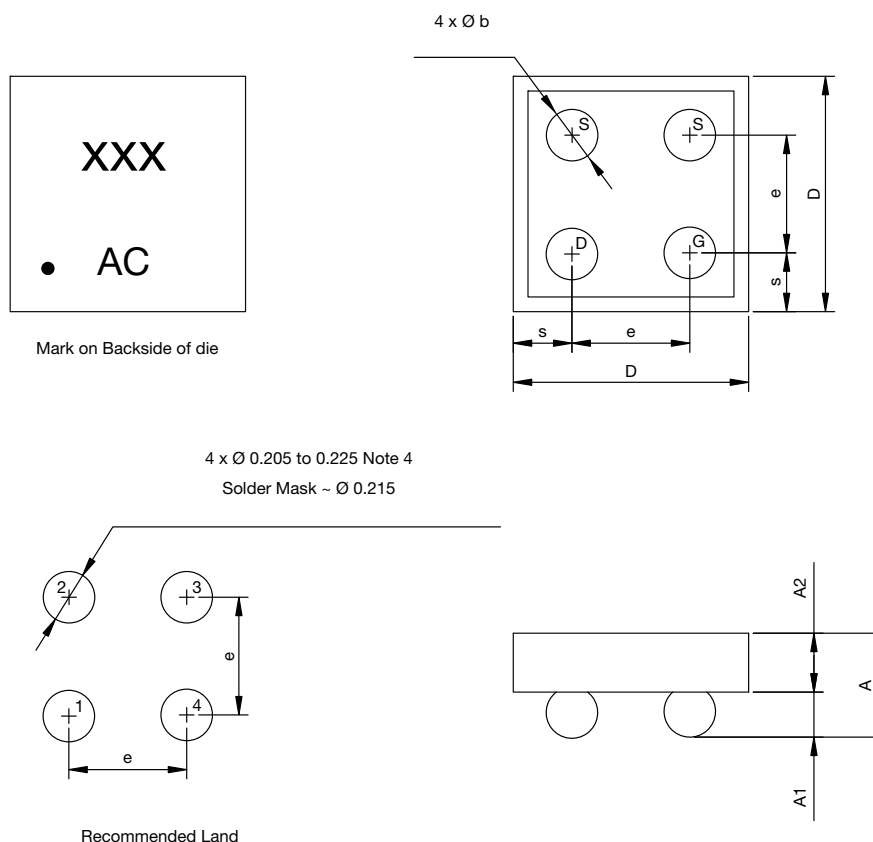
Vishay Siliconix

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)**Normalized Thermal Transient Impedance, Junction-to-Ambient (on 1" x 1" FR4 board with maximum copper)****Normalized Thermal Transient Impedance, Junction-to-Ambient (on 1" x 1" FR4 board with minimum copper)**



PACKAGE OUTLINE

MICRO FOOT 0.8 mm x 0.8 mm: 4-BUMP (2 x 2, 0.4 mm PITCH)



Notes (unless otherwise specified):

1. All dimensions are in millimeters.
2. Four (4) solder bumps are lead (Pb)-free 95.5Sn/3.5Ag/0.7Cu with diameter Ø 0.165 mm to Ø 0.185 mm.
3. Backside surface is coated with a Ti/Ni/Ag layer.
4. Non-solder mask defined copper landing pad.
5. • is location of pin 1.

Dim.	Millimeters ^a			Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	0.314	0.357	0.400	0.0124	0.0141	0.0157
A ₁	0.127	0.157	0.187	0.0050	0.0062	0.0074
A ₂	0.187	0.200	0.213	0.0074	0.0079	0.0084
b	0.165	0.175	0.185	0.0064	0.0068	0.0072
e	0.400			0.0157		
s	0.180	0.200	0.220	0.0070	0.0078	0.0086
D	0.760	0.800	0.840	0.0299	0.0314	0.0330

Notes:

- a. Use millimeters as the primary measurement.

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