## TOSHIBA

#### TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

## TC74LCX574F,TC74LCX574FW,TC74LCX574FT,TC74LCX574FK

Low-Voltage Octal D-Type Flip-Flop with 5-V Tolerant Inputs and Outputs

The TC74LCX574F/FW/FT/FK is a high-performance CMOS octal D-type flip-flop. Designed for use in 3.3-V systems, it achieves high-speed operation while maintaining the CMOS low power dissipation.

The device is designed for low-voltage (3.3 V) V<sub>CC</sub> applications, but it could be used to interface to 5 V supply environment for both inputs and outputs.

This 8-bit D-type flip-flop is controlled by a clock input (CK) and an output enable input ( $\overline{OE}$ ). When the  $\overline{OE}$  input is high, the eight outputs are in a high-impedance state.

All inputs are equipped with protection circuits against static discharge.

### **Features**

- Low-voltage operation:  $V_{CC} = 2.0$  to 3.6 V ٠
- High-speed operation:  $t_{pd} = 8.5 \text{ ns} (max) (V_{CC} = 3.0 \text{ to } 3.6 \text{ V})$ •
- Output current: |IOH|/IOL = 24 mA (min) (VCC = 3.0 V)
- Latch-up performance: ±500 mA •
- Available in JEDEC SOP, JEITA SOP and TSSOP
- Power-down protection provided on all inputs and outputs •

Weight

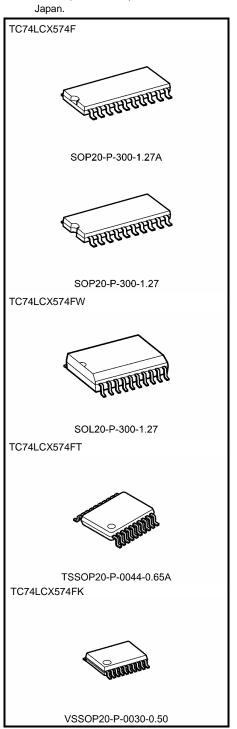
SOP20-P-300-1.27A

TSSOP20-P-0044-0.65A : 0.08 g (typ.) VSSOP20-P-0030-0.50 : 0.03 g (typ.)

SOP20-P-300-1.27

SOL20-P-300-1.27

Pin and function compatible with the 74 series (74AC/VHC/HC/F/ALS/LS etc.) 574 type



Note: xxxFW (JEDEC SOP) is not available in

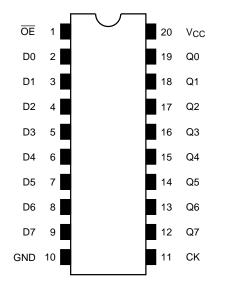
: 0.22 g (typ.)

: 0.22 g (typ.)

: 0.46 g (typ.)

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## Pin Assignment (top view)



### **Truth Table**

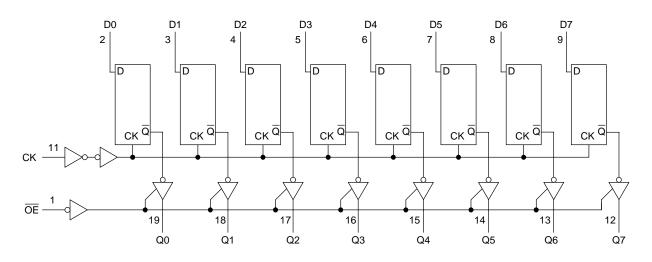
	Inputs	Outputs	
ŌE	СК	D	Outputs
н	Х	Х	Z
L		Х	Qn
L		L	L
L		Н	н

X: Don't care

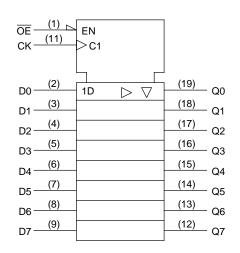
Z: High impedance

Qn: No change

## System Diagram



## IEC Logic Symbol



## Absolute Maximum Ratings (Note 1)

Characteristics	Symbol	Rating	Unit	
Power supply voltage	V <sub>CC</sub>	-0.5 to 7.0	V	
DC input voltage	V <sub>IN</sub>	-0.5 to 7.0	V	
		-0.5 to 7.0 (Note 2)		
DC output voltage	V <sub>OUT</sub>	–0.5 to V <sub>CC</sub> + 0.5 (Note 3)	V	
Input diode current	I <sub>IK</sub>	-50	mA	
Output diode current	I <sub>OK</sub>	±50 (Note 4)	mA	
DC output current	IOUT	±50	mA	
Power dissipation	PD	180	mW	
DC V <sub>CC</sub> /ground current	I <sub>CC</sub> /I <sub>GND</sub>	±100	mA	
Storage temperature	T <sub>stg</sub>	-65 to 150	°C	

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Note 2: Output in OFF state

- Note 3: High or low state. IOUT absolute maximum rating must be observed.
- Note 4:  $V_{OUT} < GND, V_{OUT} > V_{CC}$

### **Recommended Operating Conditions (Note 1)**

Characteristics	Symbol	Rating	Unit	
Power supply voltage	Vcc	2.0 to 3.6	V	
rower supply voltage	vcc	1.5 to 3.6 (Note 2)	v	
Input voltage	V <sub>IN</sub>	0 to 5.5	V	
Output voltage	V <sub>OUT</sub>	0 to 5.5 (Note 3)	V	
Output voltage		0 to V <sub>CC</sub> (Note 4)	v	
Output current	1//	±24 (Note 5)	mA	
	IOH/IOL	±12 (Note 6)	IIIA	
Operating temperature	T <sub>opr</sub>	-40 to 85	°C	
Input rise and fall time	dt/dv	0 to 10 (Note 7)	ns/V	

Note 1: The recommended operating conditions are required to ensure the normal operation of the device. Unused inputs must be tied to either VCC or GND.

Note 2: Data retention only

Note 3: Output in OFF state

Note 4: High or low state

Note 5:  $V_{CC} = 3.0 \text{ to } 3.6 \text{ V}$ 

Note 6:  $V_{CC} = 2.7$  to 3.0 V

Note 7:  $V_{IN} = 0.8$  to 2.0 V,  $V_{CC} = 3.0$  V

## **Electrical Characteristics**

## DC Characteristics (Ta = -40 to 85°C)

Characte	eristics	Symbol	Test Condition			Min	Мах	Unit
Character		Cynize.			V <sub>CC</sub> (V)		max	Onit
Input voltage	H-level	V <sub>IH</sub>	-	_	2.7 to 3.6	2.0		V
input voltage	L-level	VIL	-	_	2.7 to 3.6		0.8	v
				I <sub>OH</sub> = -100 μA	2.7 to 3.6	V <sub>CC</sub> - 0.2		
	H-level	V <sub>OH</sub>	$V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OH} = -12 \text{ mA}$	2.7	2.2	_	
				I <sub>OH</sub> = -18 mA	3.0	2.4	_	
Output voltage				$I_{OH} = -24 \text{ mA}$	3.0	2.2	_	
			V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	$I_{OL} = 100 \ \mu A$	2.7 to 3.6	_	0.2	
		level V <sub>OL</sub>		$I_{OL} = 12 \text{ mA}$	2.7	_	0.4	
	L-level			$I_{OL} = 16 \text{ mA}$	3.0	_	0.4	
			$I_{OL} = 24 \text{ mA}$	3.0	_	0.55		
Input leakage currer	nt	I <sub>IN</sub>	$V_{IN} = 0$ to 5.5 V	V <sub>IN</sub> = 0 to 5.5 V		_	±5.0	μA
3-state output off-sta	ate current	I <sub>OZ</sub>	$V_{IN} = V_{IH}$ or $V_{IL}$ $V_{OUT} = 0$ to 5.5 V		2.7 to 3.6	_	±5.0	μA
Power off leakage c	urrent	I <sub>OFF</sub>	$V_{IN}/V_{OUT} = 5.5 V$		0	_	10.0	μΑ
Quiescent supply current	1	$V_{IN} = V_{CC}$ or GND		2.7 to 3.6		10.0		
Quiescent supply cu		Icc	$V_{IN}/V_{OUT} = 3.6 \text{ to } 5.5 \text{ V}$		2.7 to 3.6	_	±10.0	μA
Increase in I <sub>CC</sub> per i	nput	Δl <sub>CC</sub>	$V_{IH} = V_{CC} - 0.6 V$		2.7 to 3.6	_	500	

### AC Characteristics (Ta = -40 to 85°C)

Characteristics	Symbol	Test Condition	V <sub>CC</sub> (V)	Min	Max	Unit
			2.7	_		N 41 I-
Maximum clock frequency	f <sub>max</sub>	Figure 1, Figure 2	$\textbf{3.3}\pm\textbf{0.3}$	150	_	MHz
Propagation delay time	t <sub>pLH</sub>	Figure 4. Figure 2	2.7	_	9.5	
(CK-Q)	t <sub>pHL</sub>	Figure 1, Figure 2	$\textbf{3.3}\pm\textbf{0.3}$	1.5	8.5	ns
Output apphla time	t <sub>pZL</sub>	Figure 1 Figure 2	2.7	_	9.5	
Output enable time	t <sub>pZH</sub>	Figure 1, Figure 3	$\textbf{3.3}\pm\textbf{0.3}$	1.5	8.5	ns
Output disable time	t <sub>pLZ</sub>		2.7	_	7.0	ns
	tput disable time Figure 1, Figure 3		$\textbf{3.3}\pm\textbf{0.3}$	1.5	6.5	
Minimum pulse width	t <sub>w</sub> (H)	Figure 1, Figure 2	2.7	3.3	_	ns
(CK)	t <sub>w</sub> (L)		$\textbf{3.3}\pm\textbf{0.3}$	3.3	—	115
Minimum act un timo		Figure 1, Figure 2	2.7	2.5	_	20
Minimum set-up time	ts		$\textbf{3.3}\pm\textbf{0.3}$	2.5	—	ns
Minimum hold time	+.		2.7	1.5	_	ns
	t <sub>h</sub>	Figure 1, Figure 2	$\textbf{3.3}\pm\textbf{0.3}$	1.5	—	115
Output to output skew tosLH tosHL	t <sub>osLH</sub>	(Nete)	2.7	_	_	ns
	(Note)	$\textbf{3.3}\pm\textbf{0.3}$		1.0	115	

Note: Parameter guaranteed by design.

 $(t_{osLH} = |t_{pLHm} - t_{pLHn}|, t_{osHL} = |t_{pHLm} - t_{pHLn}|)$ 

#### Dynamic Switching Characteristics (Ta = 25°C, input: $t_r = t_f = 2.5$ ns, $C_L = 50$ pF, $R_L = 500 \Omega$ )

Characteristics	Symbol	Test Condition	V <sub>CC</sub> (V)	Тур.	Unit
Quiet output maximum dynamic $V_{OL}$	V <sub>OLP</sub>	$V_{IH} = 3.3 \text{ V}, V_{IL} = 0 \text{ V}$	3.3	0.8	V
Quiet output minimum dynamic $V_{OL}$	V <sub>OLV</sub>	$V_{IH} = 3.3 \text{ V}, V_{IL} = 0 \text{ V}$	3.3	0.8	V

#### **Capacitive Characteristics (Ta = 25°C)**

Characteristics	Symbol	Test Condition	V <sub>CC</sub> (V)	Тур.	Unit
Input capacitance	CIN		3.3	7	pF
Output capacitance	COUT		3.3	8	pF
Power dissipation capacitance	C <sub>PD</sub>	$f_{IN} = 10 \text{ MHz}$ (Note)	3.3	25	pF

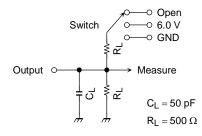
Note: C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption.

Average operating current can be obtained by the equation:

 $I_{CC (opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \text{ (per bit)}$ 

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## **AC Test Circuit**



Parameter	Switch
t <sub>pLH</sub> , t <sub>pHL</sub>	Open
t <sub>pLZ</sub> , t <sub>pZL</sub>	6.0 V
t <sub>pHZ</sub> , t <sub>pZH</sub>	GND
t <sub>w</sub> , t <sub>s</sub> , t <sub>h</sub> , f <sub>max</sub>	Open



## **AC Waveform**

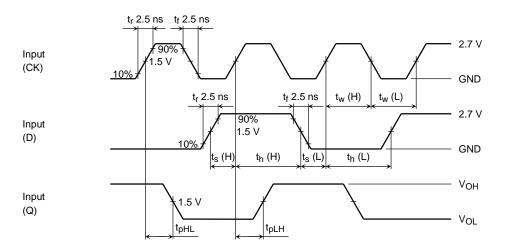
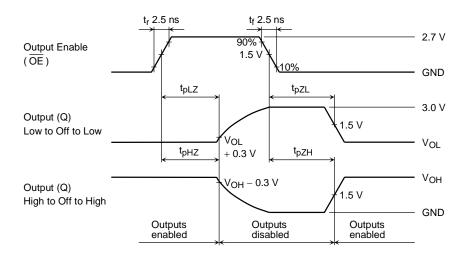
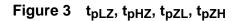


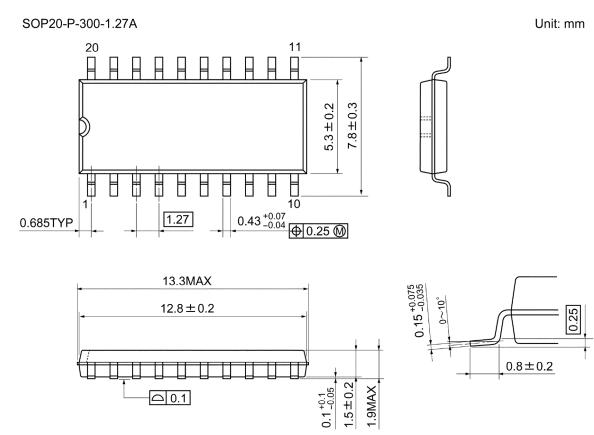
Figure 2 t<sub>pLH</sub>, t<sub>pHL</sub>, t<sub>w</sub>, t<sub>s</sub>, t<sub>h</sub>





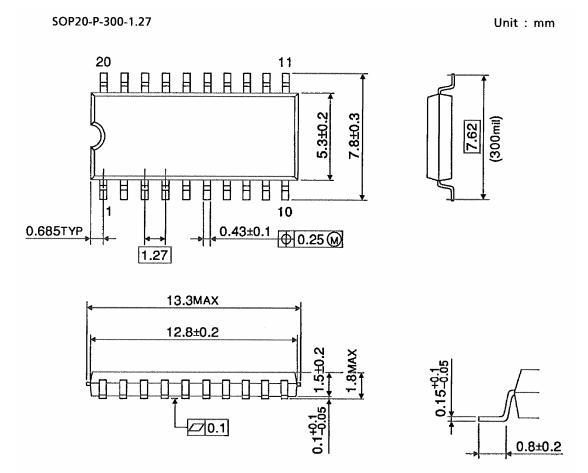
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## **Package Dimensions**



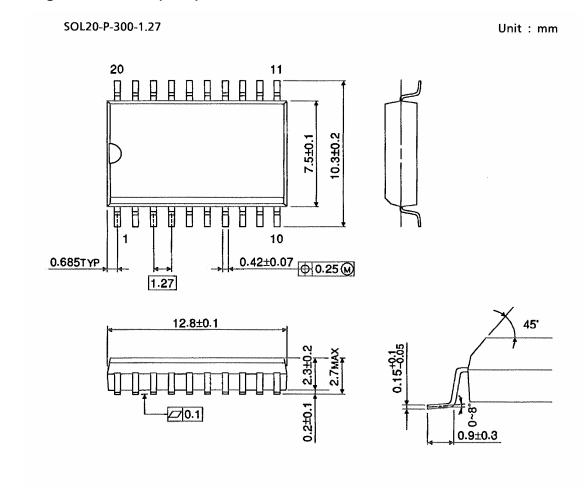
Weight: 0.22 g (typ.)

## **Package Dimensions**



Weight: 0.22 g (typ.)

## Package Dimensions (Note)



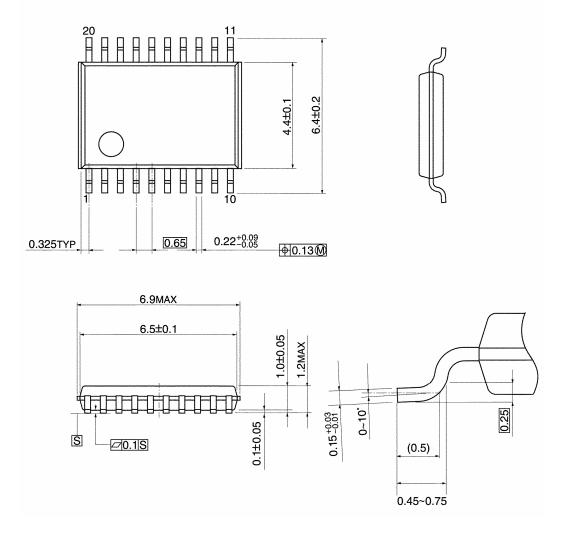
Note: This package is not available in japan.

Weight: 0.46 g (typ.)

## Package Dimensions

TSSOP20-P-0044-0.65A

Unit: mm

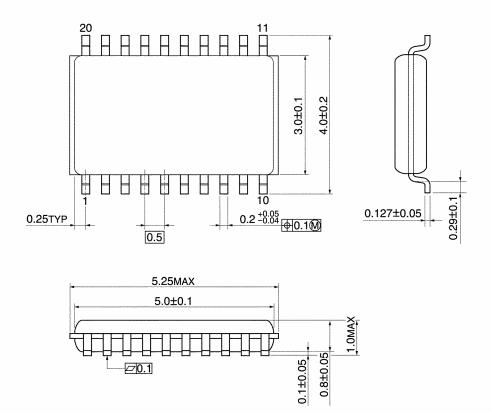


Weight: 0.08 g (typ.)

## Package Dimensions

VSSOP20-P-0030-0.50

Unit: mm



Weight: 0.03 g (typ.)

Note: Lead (Pb)-Free Packages

SOP20-P-300-1.27A TSSOP20-P-0044-0.65A VSSOP20-P-0030-0.50

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Handbook" etc. 021023\_A

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