OLED DISPLAY MODULE

Product Specification

Preliminary

CUSTOMER	**Standard**	
PRODUCT NUMBER	**DD-160128FC-2A**	
CUSTOMER APPROVAL		**Date**

INTERNAL APPROVALS		
Product Mgr	Doc. Control	Electr. Eng
Bruno Recaldini	**Anthony Perkins**	**Bazile Peter**
Date: 22 Nov 06	Date: 22 Nov 06	Date: 22 Nov 06

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REVISION RECORD

Rev.	Date	Page	Chapt.	Comment	ECR no.
A	22 Nov 06			First Issue	

1 MAIN FEATURES

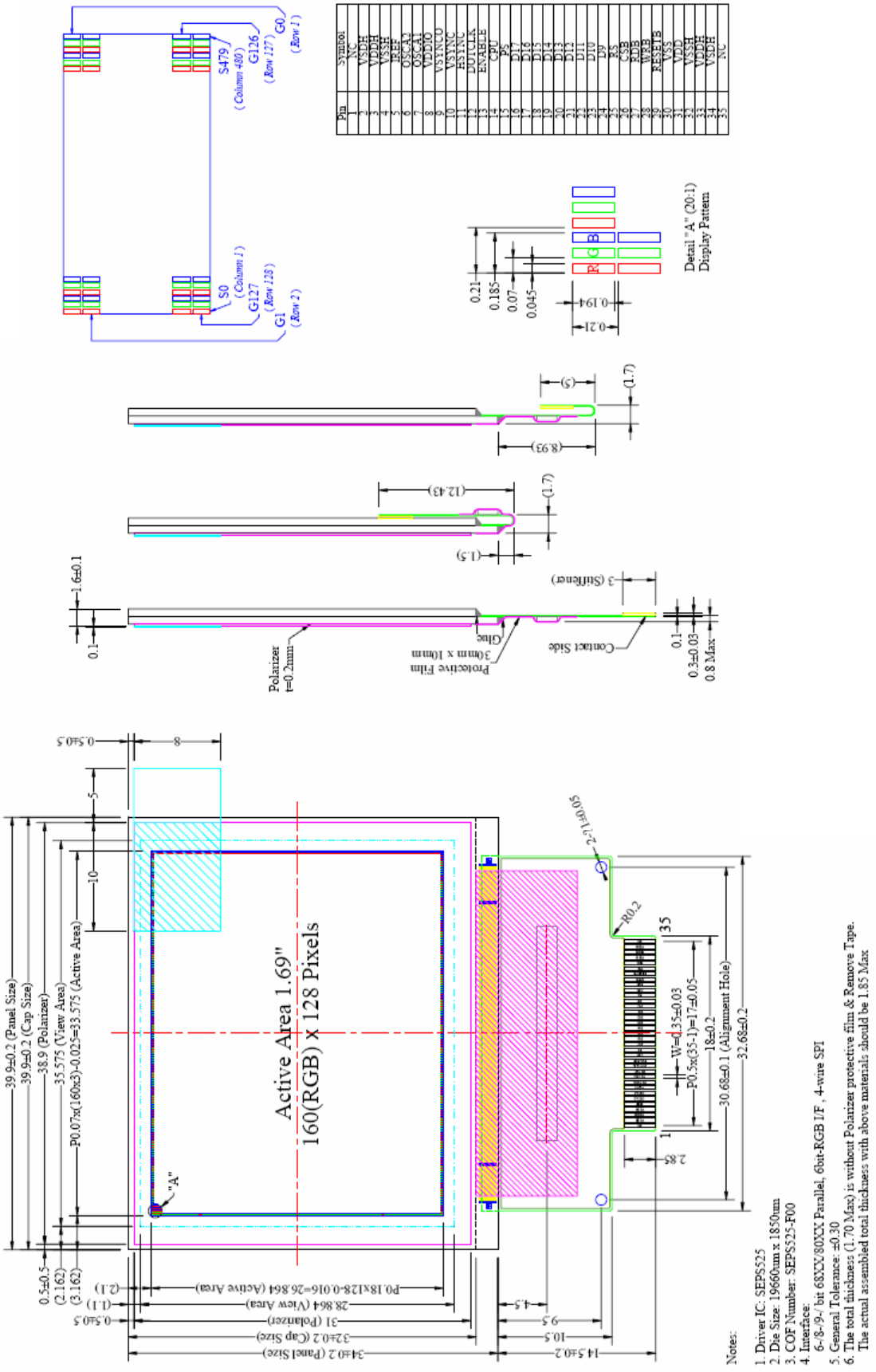
ITEM	CONTENTS
Display Format	160 (RGB) x 128 Dots
Overall Dimensions	Glass 39.9 x 34.0 x 1.7 mm
Colour	262,144 Colour
Active Area	33.575 x 26.864 mm
Viewing Area	35.575 x 28.864 mm
Display Mode	Passive Matrix (1.69”)
Driving Method	1/128 duty
Driver IC	SEPS525
Operating temperature	-30 ~ +70
Storage temperature	-40 ~ +80

2 MECHANICAL SPECIFICATION

2.1 MECHANICAL CHARACTERISTICS

ITEM	CHARACTERISTIC	UNIT
Display Format	160 (RGB) x 128	Dots
Overall Dimensions	Glass 39.9 x 34.0 x 1.7	mm
Viewing Area	35.575 x 28.864	mm
Active Area	33.575 x 26.864	mm
Dot Size	0.045 x RGB x 0.194	mm
Dot Pitch	0.07 x RGB x 0.21	mm
Weight	4.5	g
IC Controller/Driver	SEPS525F0A (COF)	

2.2 MECHANICAL DRAWING



Pin	Symbol
1	VSS
2	VDDH
3	VSSH
4	TEE
5	OSCA1
6	OSCA2
7	VDDIO
8	VSYNCO
9	VSYNC
10	HSYNC
11	DOTCLK
12	ENABLE
13	CPU
14	PS
15	D17
16	D16
17	D15
18	D14
19	D13
20	D12
21	D11
22	D10
23	D9
24	RS
25	CSB
26	RDB
27	WRB
28	RESETB
29	VSS
30	VDD
31	VSSH
32	VDDH
33	VSSH
34	VDDH
35	NC

3 ELECTRICAL SPECIFICATION

3.1 ABSOLUTE MAXIMUM RATINGS

VSS = 0 V, Ta = 25 °C

Item	Symbol	Min	Max	Unit	Note
Supply Voltage	V_{DD}	-0.3	4	V	Note 1, 2
Supply Voltage for I/O Pins	V_{DDIO}	-0.3	4	V	
Driver Supply Voltage	V_{DDH}	-0.3	19.5	V	
Operating Temperature	Top	-30	70	°C	
Storage Temperature	Tst	-40	80	°C	
Static Electricity	Be sure that you are grounded when handling displays.				

Note 1: All the above voltages are on the basis of "GND=0V".

Note 2: When this module is used beyond the above absolute maximum ratings, permanent damage to the module may occur. Also for normal operations it's desirable to use this module under the conditions according to Section 3.2 "Electrical Characteristics". If this module is used beyond these conditions the module may malfunction and the reliability could deteriorate.

3.2 ELECTRICAL CHARACTERISTICS

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Supply Voltage	V_{DD}		2.6	2.8	3.3	V
Supply Voltage x I/O pins	V_{DDIO}		1.6	2.8	3.3	V
Driver Supply Voltage	V_{DDH}		13.5	14	14.5	V
High Level Input	V_{IH}		0.8xV_{DD}	-	V_{DD}	V
Low Level Input	V_{IL}		0	-	0.4	V
High Level Output	V_{OH}		V_{DD}-0.4	-	-	V
Low Level Output	V_{OL}		-	-	0.4	V
Operating current for VDD	I_{VDD}	Note 4	-	2.5	3.5	mA
		Note 5	-	2.5	3.5	
Operating current for VDDH	I_{VDDH}	Note 4	-	25	31	mA
		Note 5	-	8	10	
Sleep mode current for VDD	$I_{VDD\ SLEEP}$		-	1	5	µA
Sleep mode current for VDDH	$I_{VDDH\ SLEEP}$		-	1	5	µA

Note 4 VDD & VDDIO = 2.8V, VDDH = 14V, Lbr at 100cd/m² , full white with polarizer, software initial setting follow section 3.2.1 Reference Parameter table 5.4.1 for normal operation mode.
Note 5 VDD & VDDIO = 2.8V, VDDH = 14V, Lbr at 30cd/m², full white with polarizer, software initial setting follow section 3.2.1 Reference parameter Table 5.4.1 for power saving mode.

3.3 INTERFACE PIN ASSIGNMENT

Mating Connector type: 35-pin, 0.5 mm pitch FFC/FPC. Type: AVX 04-6238-035-000-800

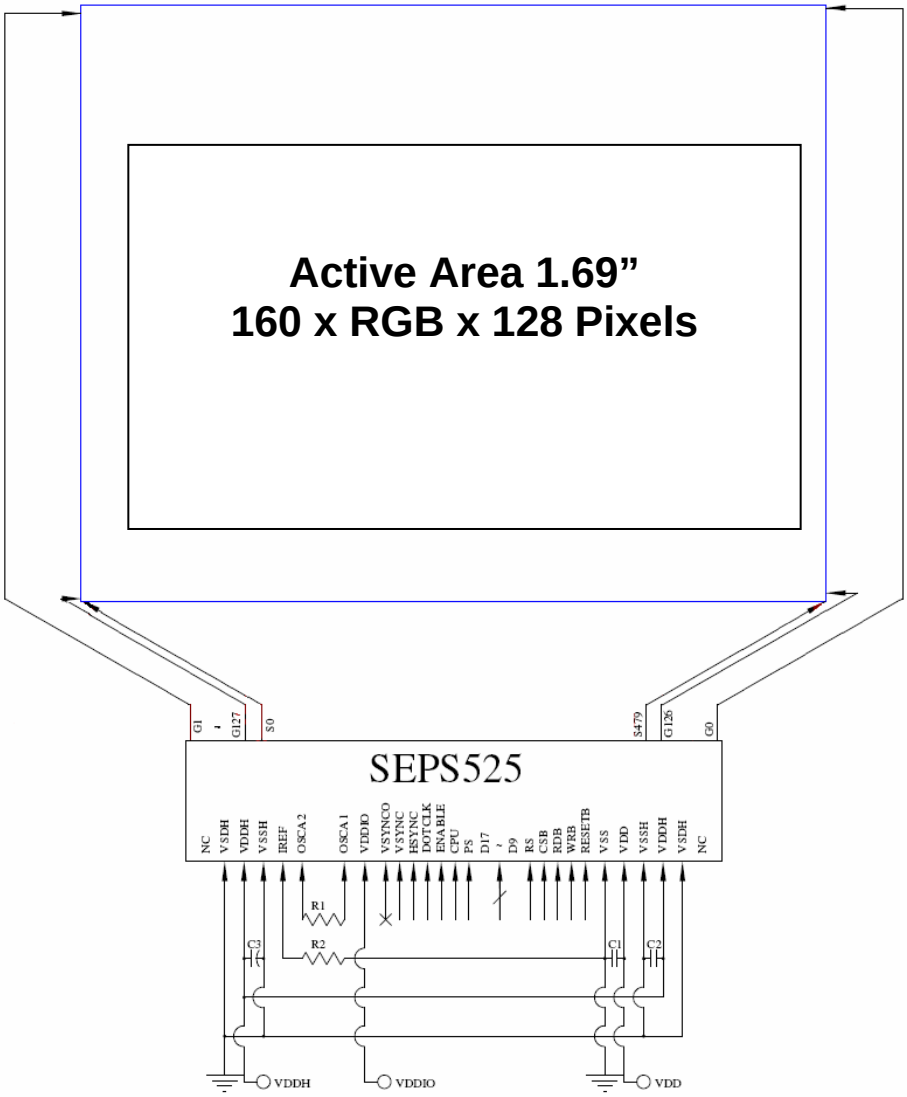
<table>
<tr><th>No.</th><th>Symbol</th><th>Function</th></tr>
<tr><td>1</td><td>N.C.</td><td>No Connection</td></tr>
<tr><td>2</td><td>VSDH</td><td>Data Driver Ground</td></tr>
<tr><td>3</td><td>VDDH</td><td>Data, Scan Driver Power supply</td></tr>
<tr><td>4</td><td>VSSH</td><td>Scan Driver Ground</td></tr>
<tr><td>5</td><td>IREF</td><td>Current reference for brightness Adjustment
Connect 68KΩ Resistor to VSS</td></tr>
<tr><td>6</td><td>OSCA2</td><td rowspan="2">Fine Adjustment for Oscillation
Connect a 10KΩ Resistor between OSCA1 and OSCA2.
OSCA1 is selected for External clock mode.</td></tr>
<tr><td>7</td><td>OSCA1</td></tr>
<tr><td>8</td><td>VDDIO</td><td>MPU I/F PAD Power Supply</td></tr>
<tr><td>9</td><td>VSYNCO</td><td rowspan="5">RGB Mode functional Pins

VSYNCO : Vertical Sync Output
VSYNC: Vertical Sync Input
HSYNC : Horizontal Sync Input
DOTCLK : Dot Clock Input
ENNABLE : Video Enable Input</td></tr>
<tr><td>10</td><td>VSYNC</td></tr>
<tr><td>11</td><td>HSYNC</td></tr>
<tr><td>12</td><td>DOTCLK</td></tr>
<tr><td>13</td><td>ENABLE</td></tr>
<tr><td>14</td><td>CPU</td><td>Select CPU type
Low: 80-Series High: 68-Series</td></tr>
<tr><td>15</td><td>PS</td><td>Select Parallel/Serial Interface
Low: Serial High: Parallel</td></tr>
<tr><td>16</td><td>D17</td><td rowspan="9">Host Data Input/Output Bus.
These pins are 9-bit bi-directional data bus to be connected with MCU data bus.

<table><tr><th>PS</th><th>Description</th></tr><tr><td>1</td><td>8-bit Bus: D17 to D10
9-bit Bus: D17 to D9</td></tr><tr><td>0</td><td>D[17] SCL: Synchronous Clock Input
D[16] SDI: Serial Data Input
D[15] SDO: Serial Data Output</td></tr></table></td></tr>
<tr><td>17</td><td>D16</td></tr>
<tr><td>18</td><td>D15</td></tr>
<tr><td>19</td><td>D14</td></tr>
<tr><td>20</td><td>D13</td></tr>
<tr><td>21</td><td>D12</td></tr>
<tr><td>22</td><td>D11</td></tr>
<tr><td>23</td><td>D10</td></tr>
<tr><td>24</td><td>D9</td></tr>
<tr><td>25</td><td>RS</td><td>Selects Data/Command
Low: Command High: Parameter/data</td></tr>
<tr><td>26</td><td>CSB</td><td>Chip Select
Low: SEPS525 is selected and can be accessed
High: SEPS525 is not selected and cannot be accessed</td></tr>
</table>

27	RDB	Read or Read/Write enable 80-system bus interface: read strobe signal (active low) 68-system bus interface: bus enable strobe (active high) When serial mode, fix it to VDD or VSS level
28	WRB	Write or Read/Write select 80-system bus interface: write strobe signal (active low) 68-system bus interface: read/write select Low: write, High: read When serial mode, fix it to VDD or VSS level
29	RESETB	Chip Reset Reset SEPS525 (active low)
30	VSS	Logic ground
31	VDD	Logic power supply
32	VSSH	Scan driver ground
33	VDDH	Data scan driver power supply
34	VSDH	Data driver ground
35	NC	No connection

3.4 BLOCK DIAGRAM



MCU Interface Selection: PS and CPU
Pins connected to MCU interface: D17~D9, RS, CSB, RDB, WRB, RESETB, ENABLE, DOTCLK, HSYNC and VSYNC

When RGB mode is used, D[17:12], ENABLE, DOTCLK, HSYNC and VSYNC Should follow the 6-bit RGB interface instruction. Otherwise these four inputs ENABLE, DOTCLK, HSYNC and VSYNC should be tied to VSS Level and VSYNCO should be floating

C1: 1 µF
C2, C3: 4.7µF
R1: 10 kΩ
R2: 68 kΩ

3.5 TIMING CHARACTERISTICS

3.5.1 AC CHARACTERISTICS

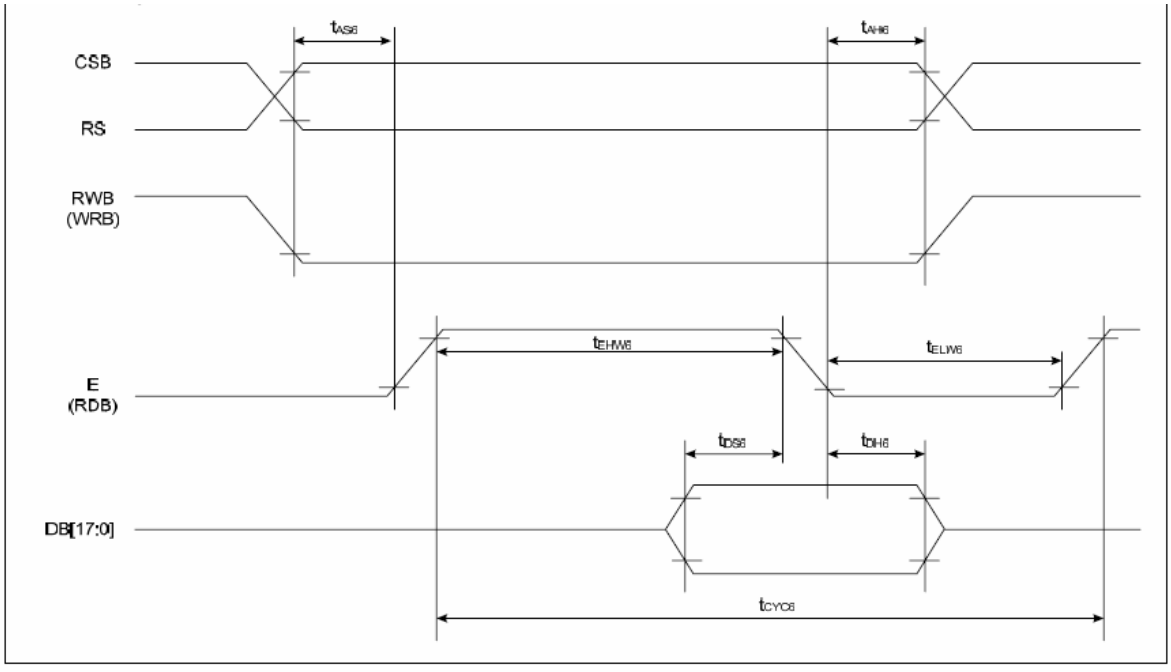
3.5.1.1 6800-Series MPU Parallel Interface Timing Characteristics

VDD = 2.8V, Ta = 25˚C

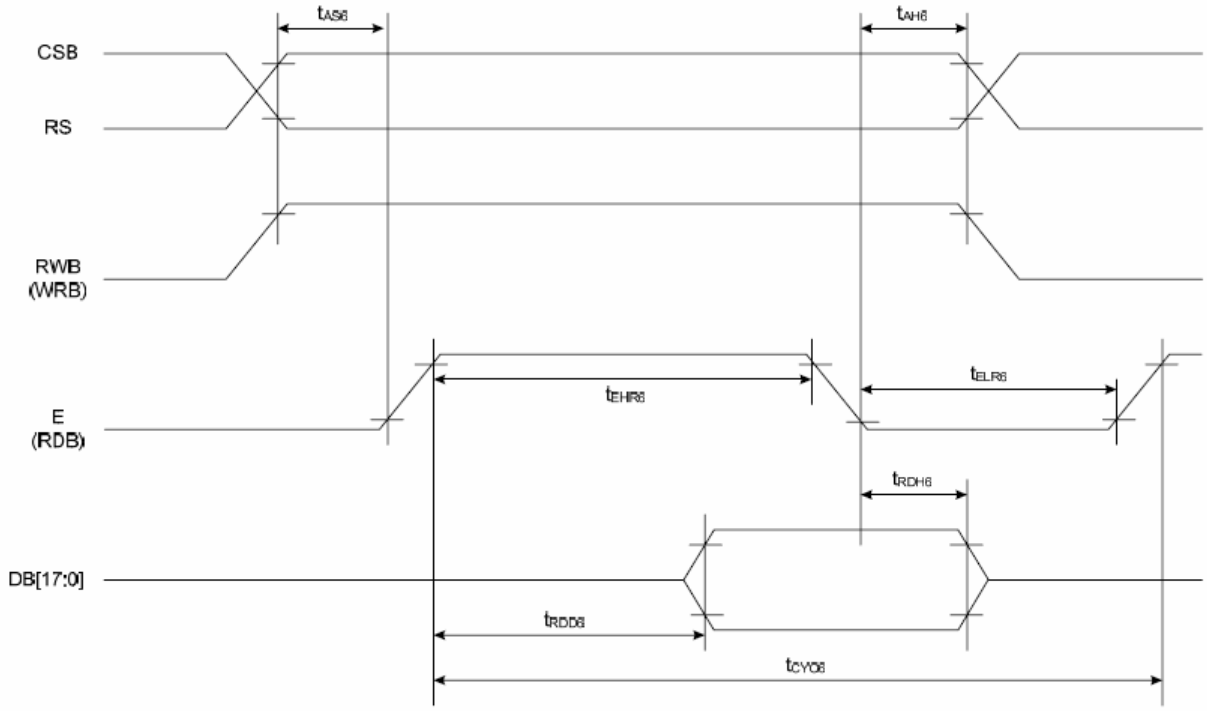
Characteristics	Symbol	Min	Max	Unit	Port
Write Timing					
Address hold timing	tAH6	5	-	nS	CSB
Address setup timing	tAS6	5			RS
System cycle timing Write	tCYC6	100	-	nS	E
"L" pulse width Write	tELW6	45			
"H" pulse width	tEHW6	45			
Data setup timing	tDS6	40	-	nS	DB[17:0]
Data hold timing	tDH6	10			
Read Timing					
Address hold timing	tAH6	10	-	nS	CSB
Address setup timing	tAS6	10			RS
System cycle timing Write	tCYC6	200	-	nS	E
"L" pulse width Write	tELW6	90			
"H" pulse width	tEHW6	90			
Data setup timing (CL= 15pF)	tDS6	0	70	nS	DB[17:0]
Data hold timing (CL= 15pF)	tDH6				

- ***All the timing should be based on 10% and 90% of V_{DD}.***

Write Timing



Read Timing

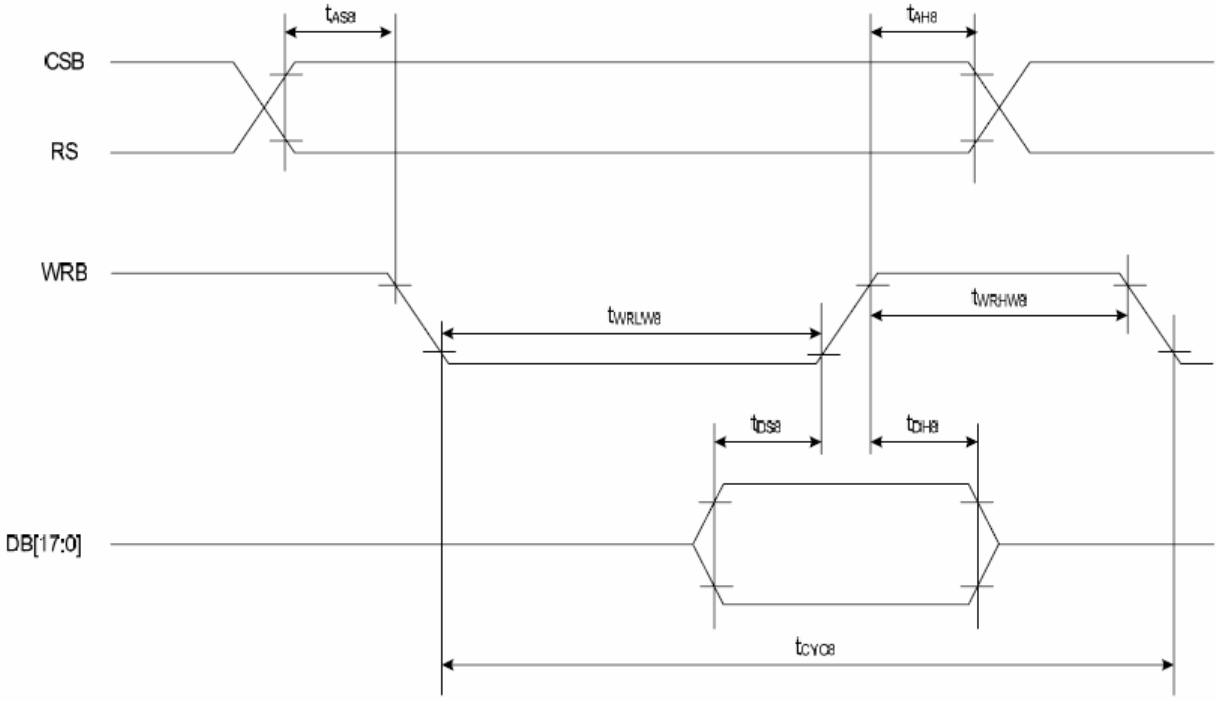


3.5.1.2 8080-Series MPU Parallel Interface Timing Characteristics

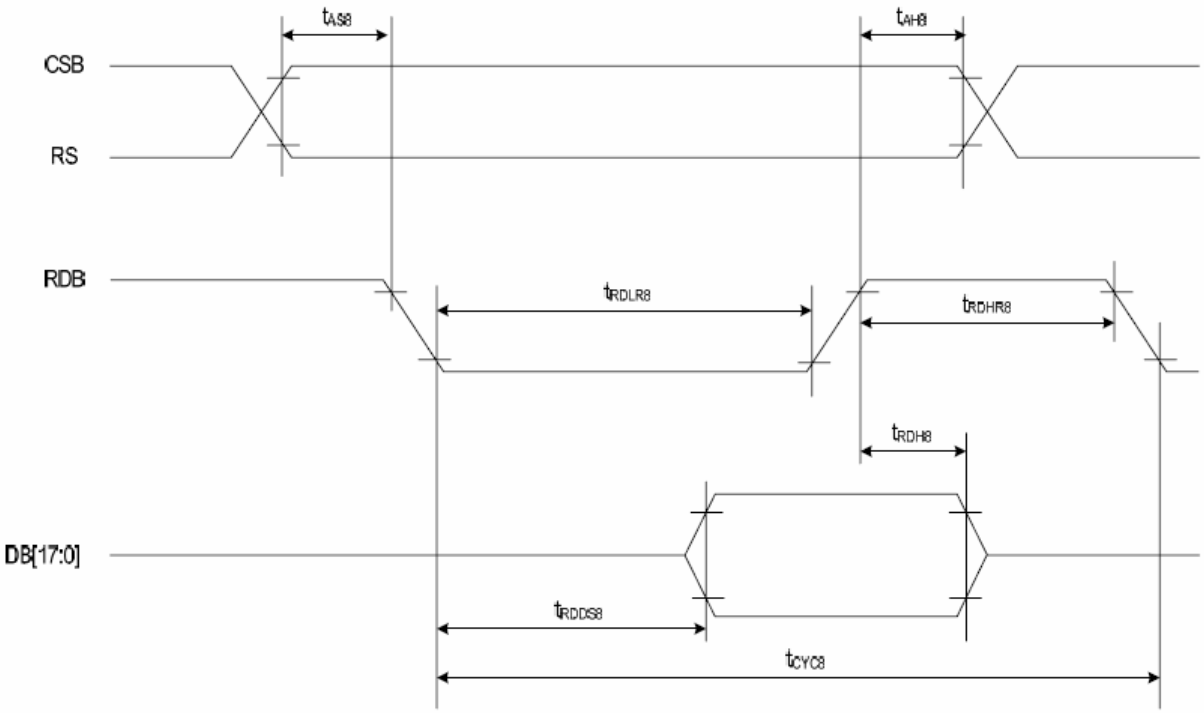
Characteristics	Symbol	Min	Max	Unit	Port
Write Timing					
Address hold timing	tAH8	5	-	nS	CSB
Address setup timing	tAS8	5			RS
System cycle timing Write	tCYC8	100	-	nS	WRB
"L" pulse width Write	tELW8	45			
"H" pulse width	tEHW8	45			
Data setup timing	tDS8	30	-	nS	DB[17:0]
Data hold timing	tDH8	10			
Read Timing					
Address hold timing	tAH8	10	-	nS	CSB
Address setup timing	tAS8	10			RS
System cycle timing Write	tCYC8	200	-	nS	RDB
"L" pulse width Write	tELW8	90			
"H" pulse width	tEHW8	90			
Data setup timing (CL= 15pF)	tDS8	0	60	nS	DB[17:0]
Data hold timing (CL= 15pF)	tDH8				

**** All the timing should be based on 10% and 90% of V_{DD}***

Write Timing



Read timing



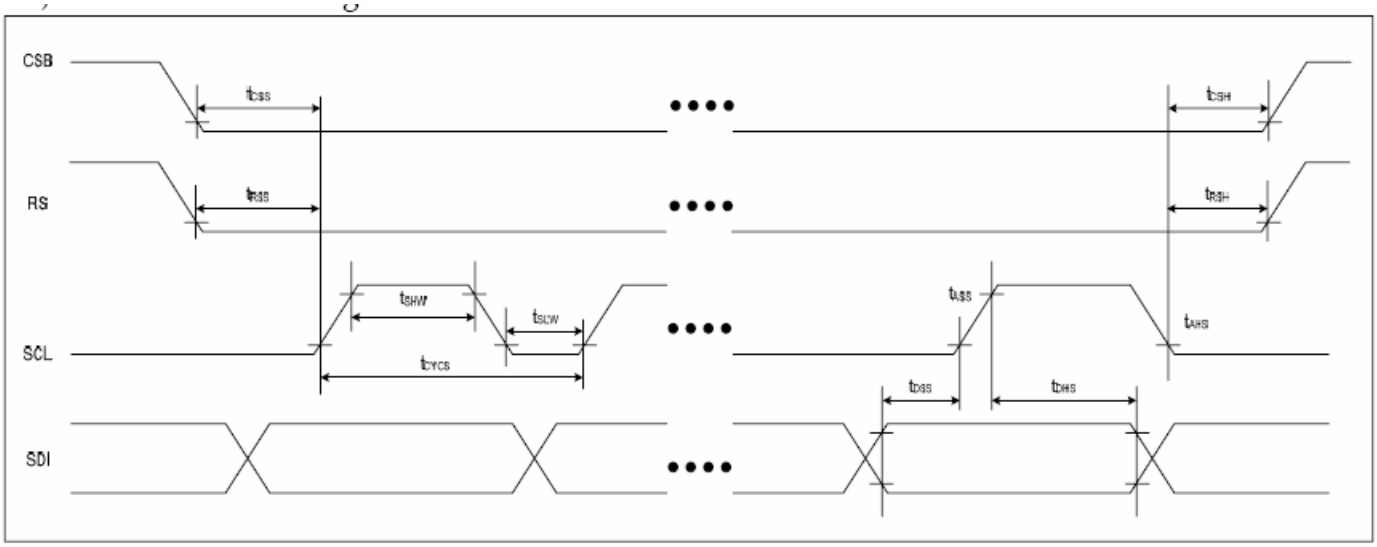
3.5.1.3 Serial Interface Timing Characteristics

VDD = 2.8V , Ta = 25˚C

ITEM	SYMBOL	MIN	MAX	UNIT	PORT
Serial clock cycle SCL	tCYCS	60	-	nS	SCL
"H" pulse width SCL	tSHW	25			
"L" pulse width	tSLW	25			
Data setup timing Data	tDSS	25	-	nS	SDI
Hold timing	tDHS	25			
CSB-SCL timing	tCSS	25	-	nS	CSB
CSB-hold timing	tCSH	25			

**** All the timing should be based on 10% and 90% of V_{DD}***

Serial Interface Timing



4 OPTICAL SPECIFICATION

4.1 OPTICAL CHARACTERISTICS

Characteristics	Symbol	Condition	Min	Typ	Max	Unit
Brightness(White)	L_{br}		70	100	-	cd/m^2
C.I.E.(White)	(X)		0.22	0.26	0.30	-
	(Y)		0.24	0.28	0.32	
C.I.E.(Red)	(X)		0.61	0.65	0.69	-
	(Y)		0.30	0.34	0.38	
C.I.E.(Green)	(X)		0.26	0.30	0.34	-
	(Y)		0.58	0.62	0.66	
C.I.E.(Blue)	(X)		0.10	0.14	0.18	-
	(Y)		0.15	0.19	0.23	
Dark Room Contrast	CR		-	>1000:1	-	-
Viewing Angle			>160	-	-	degree

Optical measurement with polarizer is taken at VDD, VDDIO = 2.8V, VDDH = 14V and the software initial setting with section 5.4.1 Reference parameter table for normal operation mode.

5 FUNCTIONAL SPECIFICATION

5.1 COMMANDS

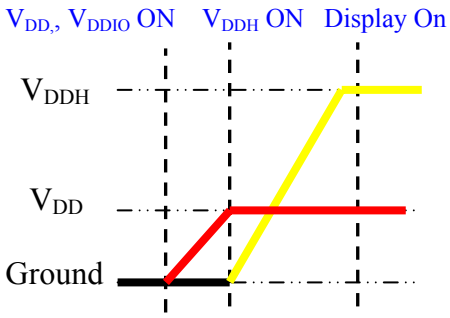
Please refer to the Technical Manual for the SEPS525

5.2 POWER UP/DOWN SEQUENCE

To protect panel and extend the panel lifetime, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources during turn on/off. It gives the panel enough time to complete the action of charge and discharge before/after the operation.

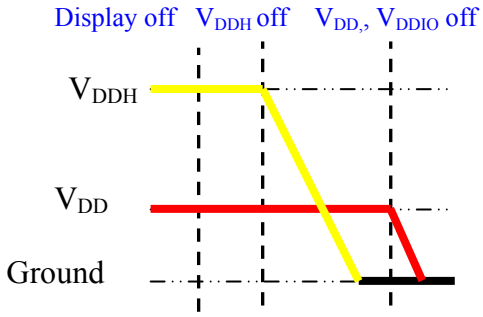
5.2.1 POWER UP SEQUENCE

1. Power up V_{DD} & $V_{DD\ IO}$
2. Send Display off command
3. Clear Screen
4. Power up V_{DDH}
5. Delay 100ms (When V_{DD} & V_{DDIO} is stable)
6. Send Display on command



5.2.2 POWER DOWN SEQUENCE

1. Send Display off command
2. Power down V_{DDH}
3. Delay 100ms
   (When V_{DDH} reach 0 and panel is completely discharges)
4. Power down V_{DD} & V_{DDIO}

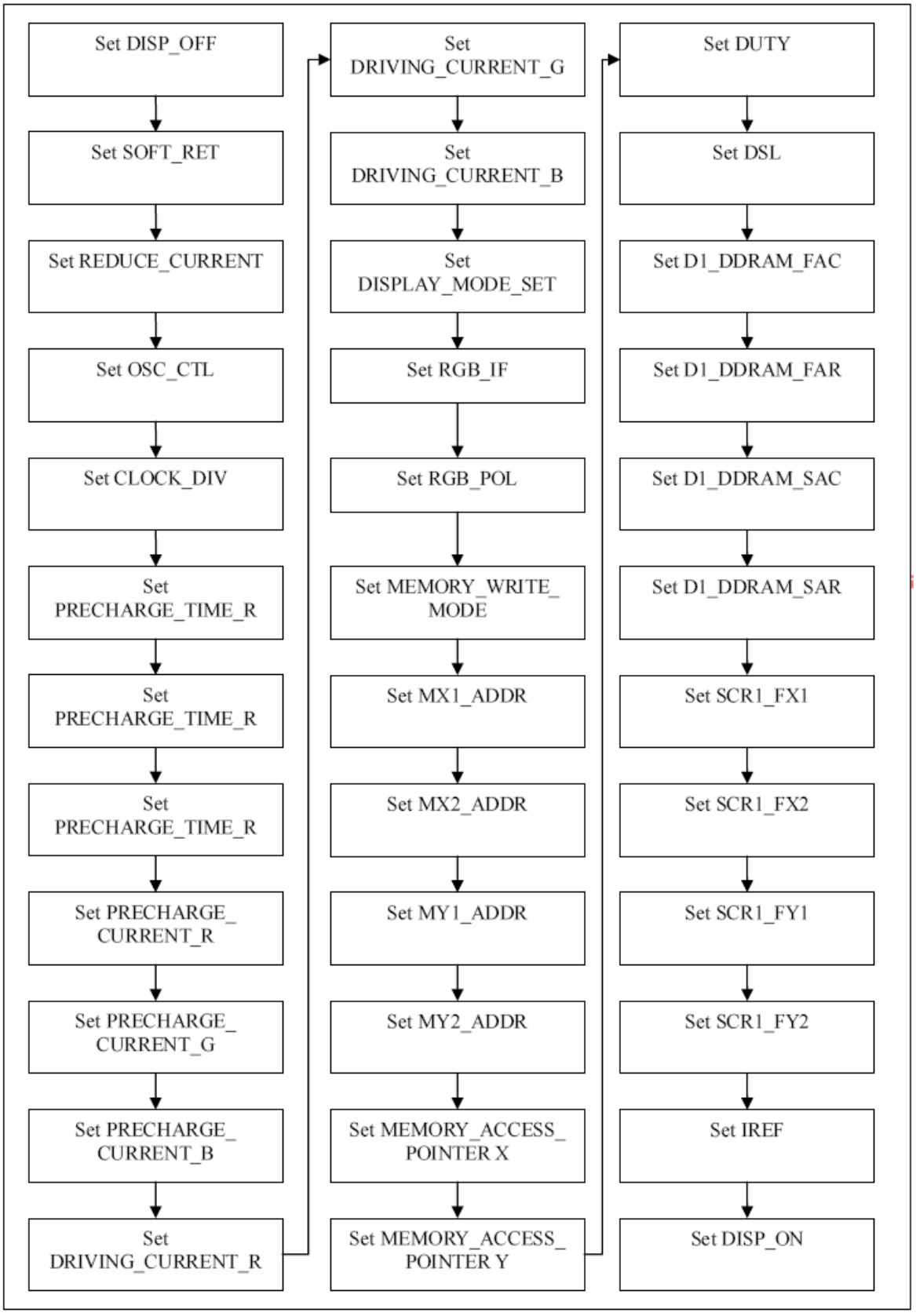


5.3 RESET CIRCUIT

When RESETB input is low, the chip is initialized with the following status:

1. Frame frequency: 90Hz
2. OSC: internal OSC
3. Internal OSC: ON
4. DDRAM write horizontal address: MX1 = 00h, MX2 = 9Fh
5. DDRAM write vertical address: MY1 = 00h, MY2 = 7Fh
6. Display data RAM write: HC = 1, VC = 1, HV = 0
7. RGB data swap: OFF
8. Row scan shift direction: G0, G1, … , G126, G127
9. Column data shift direction: S0, S1, … , S478, S479
10. Display ON/OFF: OFF
11. Panel display size: FX1 = 00h, FX2 = 9Fh, FY1 = 00h, FY2 = 7Fh
12. Display data RAM read column/row address: FAC = 00h, FAR = 00h
13. Pre-charge time(R/G/B): 0 clock
14. Pre-charge current(R/G/B): 0 uA
15. Driving current(R/G/B): 0 uA

5.4 ACTUAL APPLICATION EXAMPLE



5.4.1 Reference Parameters Table

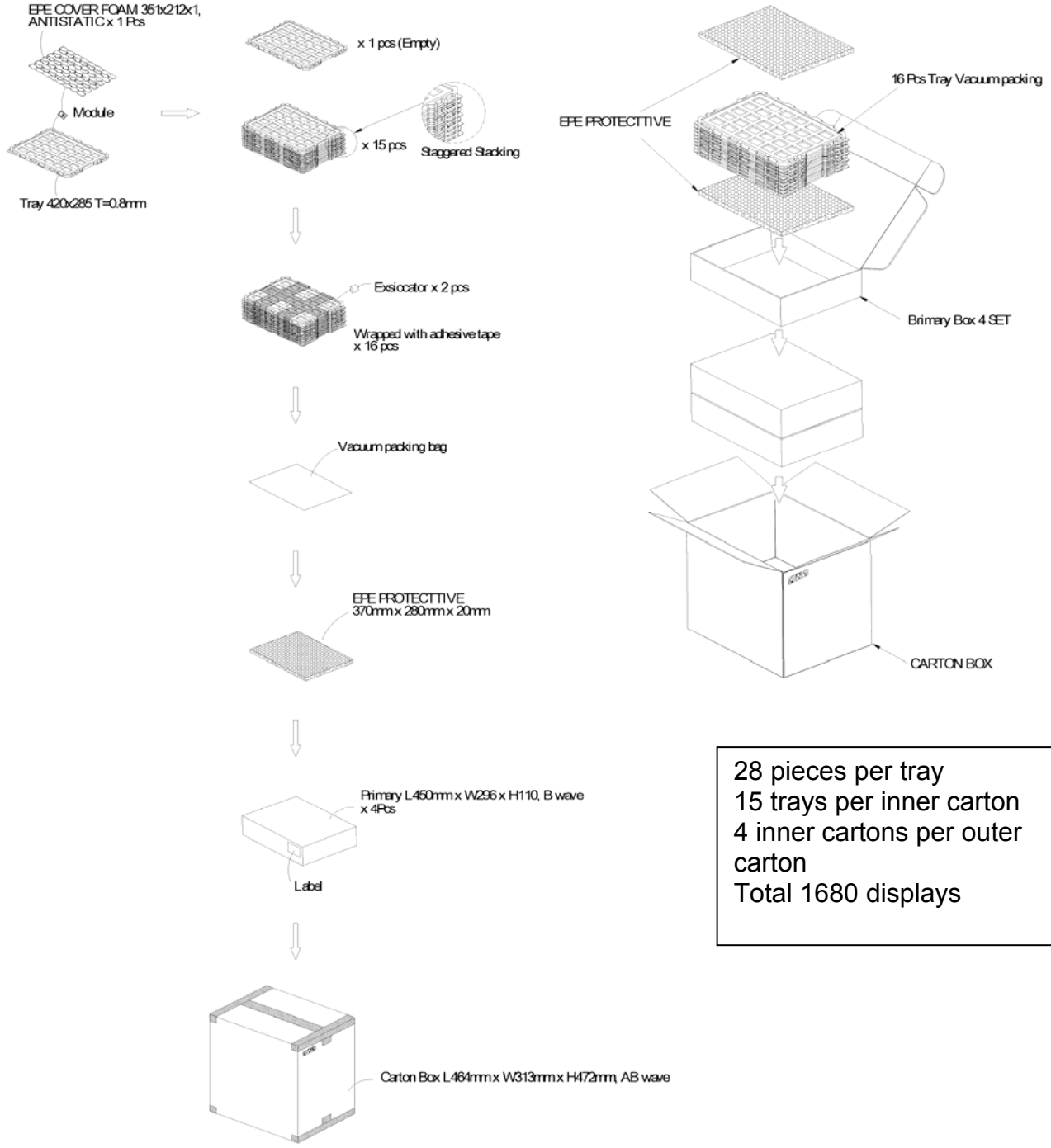
(VDD = 2.8V, Ta = 25˚C)

Command Parameter	Normal operation mode	Power saving mode
Set Display On_Off	0x06, 0x00	
Set SOFT_RST	0x05, 0x00	
Set REDUCE _CURRENT	0x04, 0x01 wait 1ms 0x04,0x00	
Set OSC_CTL	0x02, 0x01	
Set CLOCK_DIV	0x03, 0x09	
Set PRECHARGE_TIME_R	0x08, 0x03	0x08, 0x00
Set PRECHARGE_TIME_G	0x09, 0x05	0x09, 0x00
Set PRECHARGE_TIME_B	0x0A, 0x05	0x0A, 0x00
Set PRECHARGE_CURRENT_R	0x0B, 0x56	0x0B, 0x00
Set PRECHARGE_CURRENT_G	0x0C, 0x4D	0x0C, 0x00
Set PRECHARGE_CURRENT_B	0x0D, 0x46	0x0D, 0x00
Set DRIVING_CURRENT_R	0x10, 0x0A	0x10, 0x0D
Set DRIVING_CURRENT_G	0x11, 0x0A	0x11, 0x0C
Set DRIVING_CURRENT_B	0x12, 0x0A	0x12, 0x0B
Set DISPLAY_MODE_SET	0x13, 0x00	
Set RGB_IF	0x14, 0x01	
Set RGB_POL	0x15, 0x00	
Set MEMORY_WRITE_MODE	0x16, 0x76	
Set MX1_ADDR	0x17, 0x00	
Set MX2_ADDR	0x18, 0x9F	
Set MY1_ADDR	0x19, 0x00	
Set MY2_ADDR	0x1A, 0x7F	
Set MEMORY_ACCESS_POINTER X	0x20, 0x00	
Set MEMORY_ACCESS_POINTER Y	0x21, 0x00	
Set DUTY	0x28, 0x7F	
Set DSL	0x29, 0x00	
Set D1_DDRAM_FAC	0x2E, 0x00	
Set D1_DDRAM_FAR	0x2F, 0x00	
Set D1_DDRAM_SAC	0x31, 0x00	
Set D1_DDRAM_SAR	0x32, 0x00	

Set SCR1_FX1	0x33, 0x00
Set SCR1_FX2	0x34, 0x9F
Set SCR1_FY1	0x35, 0x00
Set SCR1_FY2	0x36, 0x7F
Set IREF	0x80, 0x00
Set DISP_ON_OFF	0x06, 0x01

6 PACKAGING AND LABELLING SPECIFICATION

DENSITRON
DD-160128FC-2A
TW YY MM



28 pieces per tray
15 trays per inner carton
4 inner cartons per outer carton
Total 1680 displays

7 QUALITY ASSURANCE SPECIFICATION

7.1 CONFORMITY

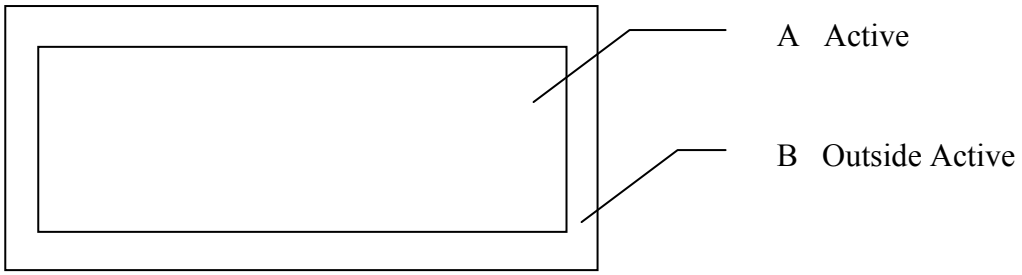
The performance, function and reliability of the shipped products conform to the Product Specification.

7.2 DELIVERY ASSURANCE

7.2.1 DELIVERY INSPECTION STANDARDS

IPC-AA610, class 2 electronic assemblies standard

7.2.2 Zone definition



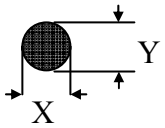
7.2.3 Visual inspection

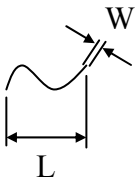
Test and measurement to be conducted under following conditions□

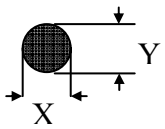
Temperature:	23±5℃
Humidity:	55±15%RH
Fluorescent lamp:	30 W
Distance between the Panel & Eyes of the Inspector:	≧30cm
Distance between the Panel & the lamp:	≧50cm

7.2.4 Standard of appearance inspection

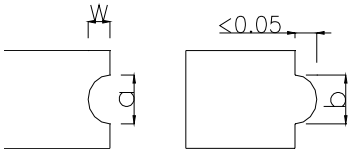
Units: mm

<table>
<tr><th>Class</th><th>Item</th><th>Criteria</th></tr>
<tr><td>Minor</td><td rowspan="2">Packing & Label</td><td>Outside & inside package | Presence of product no., lot no., quantity</td></tr>
<tr><td>Critical</td><td>Product must not be mixed with others and quantity must not be different from that indicated on the label</td></tr>
<tr><td>Major</td><td>Dimension</td><td>Product dimensions must be according to specification and drawing</td></tr>
<tr><td>Major</td><td>Electrical</td><td>Product electrical characteristics must be according to specification</td></tr>
<tr><td>Critical</td><td>OLED Display</td><td>Missing lines, short circuits or wrong patterns on OLED display are not allowed</td></tr>
<tr><td>Minor</td><td>Black spot, white spot, dust</td><td>Round type: as per following drawing
∅ = (X+Y)/2
 

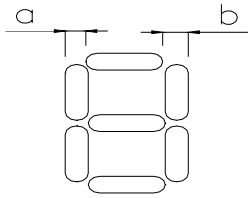
<table><tr><th colspan="3">Acceptable quantity</th></tr><tr><th>Size</th><th>Zone A</th><th>Zone B</th></tr><tr><td>∅<0.1</td><td>Any number</td><td rowspan="4">Any number</td></tr><tr><td>0.1<∅<0.2</td><td>3</td></tr><tr><td>0.2<∅<0.25</td><td>1</td></tr><tr><td>0.25<∅</td><td>0</td></tr></table>
Line type: as per following drawing
 

<table><tr><th colspan="4">Acceptable quantity</th></tr><tr><th>Length</th><th>Width</th><th>Zone A</th><th>Zone B</th></tr><tr><td>- -</td><td>W≤0.05</td><td>Any number</td><td rowspan="3">Any number</td></tr><tr><td>L≤2.0</td><td>W≤0.1</td><td>3</td></tr><tr><td>L>2.0</td><td></td><td>0</td></tr></table>
Total acceptable quantity: 3</td></tr>
<tr><td>Minor</td><td>Polariser scratch</td><td>Scratch on protective film is permitted
Scratch on polariser: same as No. 1</td></tr>
<tr><td>Minor</td><td>Polariser bubble</td><td>∅ = (X+Y)/2
 

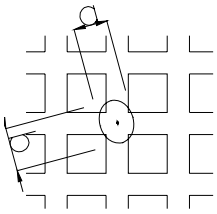
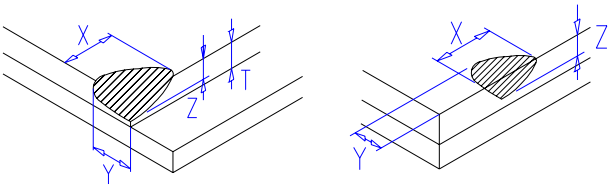
<table><tr><th colspan="3">Acceptable quantity</th></tr><tr><th>Size</th><th>Zone A</th><th>Zone B</th></tr><tr><td>∅<0.5</td><td>Any number</td><td rowspan="2">Any number</td></tr><tr><td>∅>0.5</td><td>0</td></tr></table></td></tr>
</table>

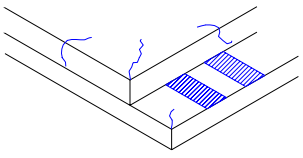
<table>
<tr><th>Class</th><th>Item</th><th>Criteria</th></tr>
<tr><td>Minor</td><td>Segment deformation</td><td>
1b. Pin hole on dot matrix display


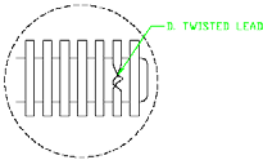
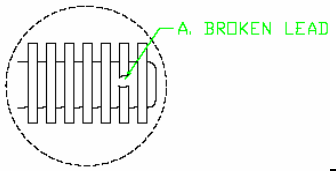
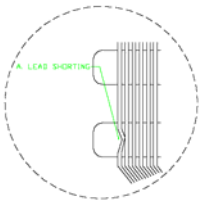
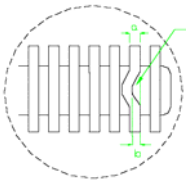
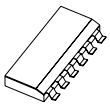
<table>
<tr><td colspan="2">Acceptable quantity</td></tr>
<tr><td>Size</td><td></td></tr>
<tr><td>a,b<0.1</td><td>Any number</td></tr>
<tr><td>(a+b)/2≤0.1</td><td>Any number</td></tr>
<tr><td>0.5<∅<1.0</td><td>3</td></tr>
</table>
Total acceptable quantity: 7

2. Segments / dots with different width


<table>
<tr><td colspan="2">Acceptable</td></tr>
<tr><td>a≥b</td><td>a/b≤4/3</td></tr>
<tr><td>a<b</td><td>a/b>4/3</td></tr>
</table>

3. Alignment layer defect
∅ = (a+b)/2

<table>
<tr><td colspan="2">Acceptable quantity</td></tr>
<tr><td>Size</td><td></td></tr>
<tr><td>∅≤0.4</td><td>Any number</td></tr>
<tr><td>0.4<∅≤1.0</td><td>5</td></tr>
<tr><td>1.0<∅≤1.5</td><td>3</td></tr>
<tr><td>1.5<∅≤2.0</td><td>2</td></tr>
</table>
Total acceptable quantity: 7
</td></tr>
<tr><td>Minor</td><td>Panel Chipping</td><td>
X ≤ 1/6 Panel length
Y ≤ 1
Z ≤ T


</td></tr>
<tr><td>Minor</td><td>Panel Cracking</td><td>
Cracks not allowed

</td></tr>
<tr><td>Minor</td><td>Cupper exposed (pin or film)</td><td>Not allowed if visible by eye inspection</td></tr>
<tr><td>Minor</td><td>Film or Trace Damage</td><td>Not allowed if affect electrical function</td></tr>
</table>

<table>
<tr><th>Class</th><th>Item</th><th>Criteria</th></tr>
<tr><td>Minor</td><td>Contact
Lead Twist</td><td>Not allowed  </td></tr>
<tr><td>Minor</td><td>Contact
Lead
Broken</td><td>Not allowed  </td></tr>
<tr><td rowspan="2">Minor</td><td rowspan="2">Contact
Lead Bent</td><td>Not allowed if
bent lead causes
short circuit  </td></tr>
<tr><td>Not allowed if bent lead
extends horizontally
more than 50%
of its width  </td></tr>
<tr><td>Minor</td><td>Colour
uniformity</td><td colspan="2">Level of sample for approval set as limit sample</td></tr>
<tr><td>Major</td><td rowspan="4">PCB  </td><td colspan="2">No unmelted solder paste should be present on PCB</td></tr>
<tr><td>Critical</td><td colspan="2">Cold solder joints, missing solder connections, or oxidation are not allowed</td></tr>
<tr><td>Minor</td><td colspan="2">No residue or solder balls on PCB are allowed</td></tr>
<tr><td>Critical</td><td colspan="2">Short circuits on components are not allowed</td></tr>
<tr><td>Minor</td><td>Tray
particles</td><td colspan="2"><table><tr><th></th><th>Size</th><th>Quantity</th></tr><tr><td rowspan="2">On tray</td><td>∅<0.2</td><td>Any number</td></tr><tr><td>∅>0.25</td><td>4</td></tr><tr><td rowspan="2">On display</td><td>∅≥0.25</td><td>2</td></tr><tr><td>L = 3</td><td>1</td></tr></table></td></tr>
</table>

7.3 DEALING WITH CUSTOMER COMPLAINTS

7.3.1 Non-conforming analysis

Purchaser should supply Densitron with detailed data of non-conforming sample.
After accepting it, Densitron should complete the analysis in two weeks from receiving the sample.
If the analysis cannot be completed on time, Densitron must inform the purchaser.

7.3.2 Handling of non-conforming displays

If any non-conforming displays are found during customer acceptance inspection which Densitron is clearly responsible for, return them to Densitron.
Both Densitron and customer should analyse the reason and discuss the handling of non-conforming displays when the reason is not clear.
Equally, both sides should discuss and come to agreement for issues pertaining to modification of Densitron quality assurance standard.

8 RELIABILITY SPECIFICATION

8.1 RELIABILITY TESTS

Test Item	Test Condition	Evaluation and assessment
High Temperature Operation	70°C±2, 240 hours	No abnormalities in function and appearance
Low Temperature Operation	-30°C±2, 240 hours	No abnormalities in function and appearance
High Temperature Storage	80°C±2, 240 hours	No abnormalities in function and appearance
Low Temperature Storage	-40°C±2, 240 hours	No abnormalities in function and appearance
High Temperature & High Humidity Storage(Operation)	60°C±2, 90%RH, 120 hours	No abnormalities in function and appearance
Thermal Shock	24 cycle of -40°C 1 Hour, 85°C 1 Hour	No abnormalities in function and appearance

- The brightness should be greater than 50% of the initial brightness.
- The samples used for above tests do not include polarizer.
- No moisture condensation is observed during tests.

8.1.1 FAILURE CHECK STANDARD

After the completion of the described reliability test, the samples were left at room temperature for 2 hrs prior to conducting the failure teat at 23±5 °C; 55±15% RH

8.2 LIFE TIME

Item	Description
1	Function, performance, appearance, etc. shall be free from remarkable deterioration more than 10,000 hours under 70 cd/m² brightness and storage conditions of room temperature (25±10 °C), normal humidity (45±20% RH), and in area not exposed to direct sunlight.
2	End of lifetime is specified as 50% of initial brightness.

9 HANDLING PRECAUTIONS

Safety
If the panel breaks, be careful not to get the organic substance in your mouth or in your eyes.
If the organic substance touches your skin or clothes, wash it off immediately using soap and plenty of water.

Mounting and Design
Place a transparent plate (e.g. acrylic, polycarbonate or glass) on the display surface to protect the display from external pressure. Leave a small gap between the transparent plate and the display surface.
Design the system so that no input signal is given unless the power supply voltage is applied.

Caution during OLED cleaning
Lightly wipe the display surface with a soft cloth soaked with Isopropyl alcohol, Ethyl alcohol or Trichlorotriflorothane.
Do not wipe the display surface with dry or hard materials that will damage the polariser surface.
Do not use aromatic solvents (toluene and xylene), or ketonic solvents (ketone and acetone).

Caution against static charge
As the display uses C-MOS LSI drivers, connect any unused input terminal to V_{DD} or V_{SS}. Do not input any signals before power is turned on.
Also, ground your body, work/assembly table and assembly equipment to protect against static electricity.

Packaging
Displays use OLED elements, and must be treated as such. Avoid strong shock and drop from a height.
To prevent displays from degradation, do not operate or store them exposed directly to sunshine or high temperature/humidity.

Caution during operation
It is indispensable to drive the display within the specified voltage limit since excessive voltage shortens its life.

Other Precautions
When a display module is operated for a long of time with fixed pattern may remain as an after image or slight contrast deviation may occur.
Nonetheless, if the operation is interrupted and left unused for a while, normal state can be restored.
Also, there will be no problem in the reliability of the module.

Storage
Store the display in a dark place where the temperature is 25°C ± 10°C and the humidity below 50%RH.
Store the display in a clean environment, free from dust, organic solvents and corrosive gases.
Do not crash, shake or jolt the display (including accessories).