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## N-Channel, Depletion-Mode, Vertical DMOS FET

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### Features

- High-Input Impedance
- Low-Input Capacitance
- Fast Switching Speeds
- Low On-Resistance
- Free From Secondary Breakdown
- Low Input and Output Leakages

### Applications

- Normally-On Switches
- Battery-Operated Systems
- Converters
- Linear Amplifiers
- Constant Current Sources
- Telecom

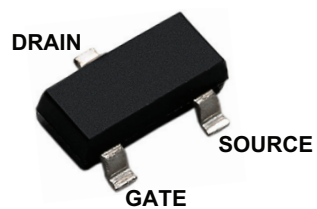
### Description

This low threshold, depletion-mode, normally-on, transistor utilizes an advanced vertical Diffusion Metal Oxide Semiconductor (DMOS) structure and a well proven silicon-gate manufacturing process. This combination produces a device with the power-handling capabilities of bipolar transistors, plus the high-input impedance and positive-temperature coefficient inherent in Metal-Oxide Semiconductor (MOS) devices. Characteristic of all MOS structures, this device is free from thermal runaway and thermally-induced secondary breakdown.

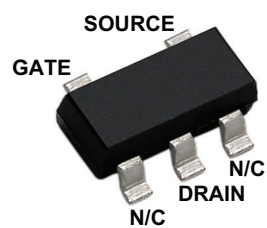
Vertical DMOS Field-Effect Transistors (FETs) are ideally suited to a wide range of switching and amplifying applications where a very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

# DN1509

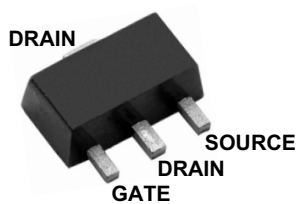
## Package Type



3-Lead SOT-23



5-Lead SOT-23



3-Lead TO-243AA (SOT-89)

See [Table 2-1](#) for pin information

## 1.0 ELECTRICAL CHARACTERISTICS

### ABSOLUTE MAXIMUM RATINGS†

|                                        |                   |
|----------------------------------------|-------------------|
| Drain-to-source voltage.....           | BV <sub>DSX</sub> |
| Drain-to-gate voltage.....             | BV <sub>DGX</sub> |
| Gate-to-source voltage.....            | ±20V              |
| Operating and storage temperature..... | -55°C to +150°C   |

† **Notice:** Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

### 1.1 Electrical Specifications

**TABLE 1-1: DC AND AC CHARACTERISTICS**

| Electrical Specifications: Unless otherwise specified, for all specifications $T_A = T_J = +25^{\circ}\text{C}$ |                                            |      |     |      |                        |                                                                                          |
|-----------------------------------------------------------------------------------------------------------------|--------------------------------------------|------|-----|------|------------------------|------------------------------------------------------------------------------------------|
| Symbol                                                                                                          | Parameter                                  | Min  | Typ | Max  | Units                  | Conditions                                                                               |
| DC Parameters (Note 1, unless otherwise stated)                                                                 |                                            |      |     |      |                        |                                                                                          |
| $BV_{DSX}$                                                                                                      | Drain-to-source breakdown voltage          | 90   | –   | –    | V                      | $V_{GS} = -5\text{V}$ , $I_D = 1.0\mu\text{A}$                                           |
| $V_{GS(OFF)}$                                                                                                   | Gate-to-source off voltage                 | -1.8 | –   | -3.5 | V                      | $I_D = 10\mu\text{A}$                                                                    |
| $\Delta V_{GS(OFF)}$                                                                                            | $V_{GS(OFF)}$ change with temperature      | –    | –   | -4.5 | mV/ $^{\circ}\text{C}$ | $V_{DS} = 15\text{V}$ , $I_D = 10\mu\text{A}$ (Note 2)                                   |
| $I_{GSS}$                                                                                                       | Gate body leakage                          | –    | –   | 100  | nA                     | $V_{GS} = \pm 20\text{V}$ , $V_{DS} = 0\text{V}$                                         |
| $I_{D(OFF)}$                                                                                                    | Drain-to-source leakage current            | –    | –   | 1.0  | $\mu\text{A}$          | $V_{DS} = BV_{DSX}$ , $V_{GS} = -5.0\text{V}$                                            |
|                                                                                                                 |                                            | –    | –   | 1.0  | mA                     | $V_{DS} = 0.8 BV_{DSX}$ , $V_{GS} = -5.0\text{V}$ , $T_A = 125^{\circ}\text{C}$ (Note 2) |
| $I_{DSS}$                                                                                                       | Saturated drain-to-source current          | 300  | 540 | –    | mA                     | $V_{GS} = 0\text{V}$ , $V_{DS} = 25\text{V}$                                             |
| $R_{DS(ON)}$                                                                                                    | Static drain-to-source on-state resistance | –    | 3.2 | 6.0  | $\Omega$               | $V_{GS} = 0\text{V}$ , $I_D = 200\text{mA}$                                              |
| $\Delta R_{DS(ON)}$                                                                                             | Change in $R_{DS(ON)}$ with temperature    | –    | –   | 1.1  | %/ $^{\circ}\text{C}$  | $V_{GS} = 0\text{V}$ , $I_D = 200\text{mA}$ (Note 2)                                     |
| AC Parameters (Note 2)                                                                                          |                                            |      |     |      |                        |                                                                                          |
| $G_{FS}$                                                                                                        | Forward transconductance                   | 200  | –   | –    | mmho                   | $V_{DS} = 10\text{V}$ , $I_D = 200\text{mA}$                                             |
| $C_{ISS}$                                                                                                       | Input capacitance                          |      | 70  | 150  | pF                     | $V_{GS} = -10\text{V}$ , $V_{DS} = 25\text{V}$ ,<br>$f = 1\text{MHz}$                    |
| $C_{OSS}$                                                                                                       | Common source output capacitance           | –    | 20  | 40   |                        |                                                                                          |
| $C_{RSS}$                                                                                                       | Reverse transfer capacitance               | –    | 6.0 | 15   |                        |                                                                                          |
| $t_{d(ON)}$                                                                                                     | Turn-on delay time                         | –    | 12  | 30   | ns                     | $V_{DD} = 25\text{V}$ ,<br>$I_D = 100\text{mA}$ ,<br>$R_{GEN} = 25\Omega$                |
| $t_r$                                                                                                           | Rise time                                  | –    | 16  | 45   |                        |                                                                                          |
| $t_{d(OFF)}$                                                                                                    | Turn-off delay time                        | –    | 15  | 45   |                        |                                                                                          |
| $t_f$                                                                                                           | Fall time                                  | –    | 25  | 60   |                        |                                                                                          |
| Diode Parameters                                                                                                |                                            |      |     |      |                        |                                                                                          |
| $V_{SD}$                                                                                                        | Diode forward voltage drop                 | –    | –   | 1.8  | V                      | $V_{GS} = -5.0\text{V}$ , $I_{SD} = 500\text{mA}$ (Note 1)                               |
| $t_{rr}$                                                                                                        | Reverse recovery time                      | –    | 400 | –    | ns                     | $V_{GS} = -5.0\text{V}$ , $I_{SD} = 500\text{mA}$ (Note 2)                               |

**Note 1:** All DC parameters are 100% tested at 25°C unless otherwise stated. Pulse test: 300 μs pulse, 2% duty cycle.

**2:** Specification is obtained by characterization and is not 100% tested.

# DN1509

**TABLE 1-2: TYPICAL THERMAL RESISTANCE**

| Package           | $\theta_{ja}$       |
|-------------------|---------------------|
| 3-lead SOT-23     | 226°C/W             |
| 5-lead SOT-23     | 157°C/W             |
| TO-243AA (SOT-89) | 78°C/W <sup>1</sup> |

**Note 1:** Mounted on FR4 board, 25 mm × 25 mm × 1.57 mm

**TABLE 1-3: THERMAL CHARACTERISTICS**

| Package           | $I_D$ <sup>1</sup><br>continuous<br>(mA) | $I_D$<br>pulsed<br>(mA) | Power<br>Dissipation<br>@T <sub>A</sub> = 25°C (W) | $I_{DR}$ <sup>1</sup><br>(mA) | $I_{DRM}$<br>(mA) |
|-------------------|------------------------------------------|-------------------------|----------------------------------------------------|-------------------------------|-------------------|
| 5-lead SOT-23     | 200                                      | 500                     | 0.79                                               | 200                           | 500               |
| TO-243AA (SOT-89) | 360                                      | 500                     | 1.6 <sup>2</sup>                                   | 360                           | 500               |

**Note 1:**  $I_D$  continuous is limited by max rated T<sub>J</sub>

**2:** Mounted on FR4 board, 25 mm × 25 mm × 1.57 mm

## 2.0 PIN DESCRIPTION

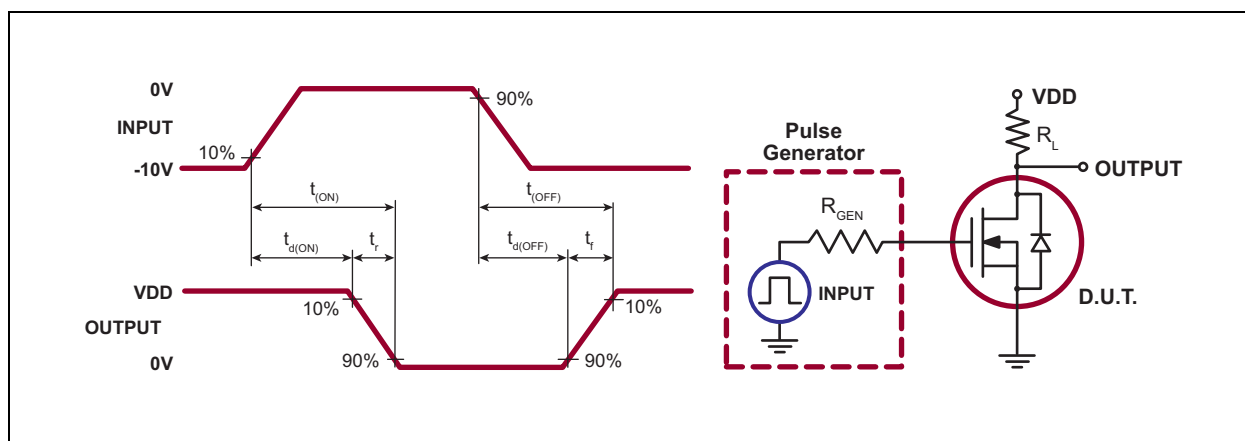
The locations of the pins are listed in [Package Type](#).

**TABLE 2-1: PIN FUNCTION TABLE**

| Pin # SOT-23-3 | Pin # SOT-23-5 | Pin # TO-243AA | Function      |
|----------------|----------------|----------------|---------------|
| 1              | 5              | 1              | GATE          |
| 2              | 4              | 3              | SOURCE        |
| 3              | 2              | 2              | DRAIN         |
| —              | 1,3            | —              | NOT CONNECTED |

## 3.0 APPLICATION INFORMATION

Figure 3-1 shows the switching waveform and test circuit for DN1509.



**FIGURE 3-1:** Switching Waveforms and Test Circuit

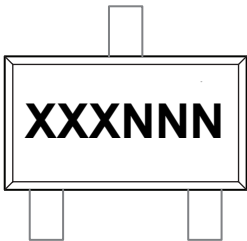
### Product Summary

| $BV_{DSX}/BV_{DGX}$<br>(V) | $R_{DS(ON)}$<br>(max) ( $\Omega$ ) | $I_{DSS}$<br>(min) (mA) |
|----------------------------|------------------------------------|-------------------------|
| 90                         | 6.0                                | 300                     |

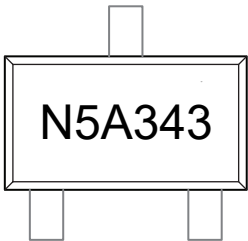
## 4.0 PACKAGING INFORMATION

### 4.1 Package Marking Information

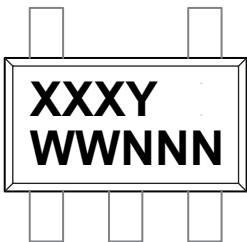
3-Lead SOT-23\*



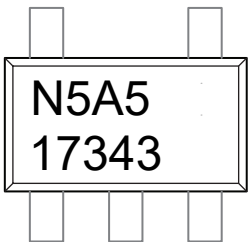
Example



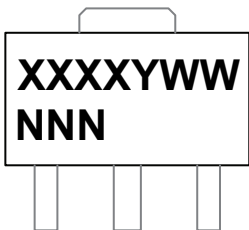
5-Lead SOT-23\*



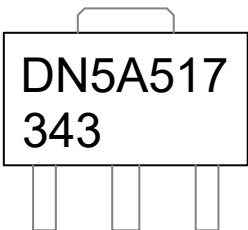
Example



3-Lead TO-243AA\*



Example



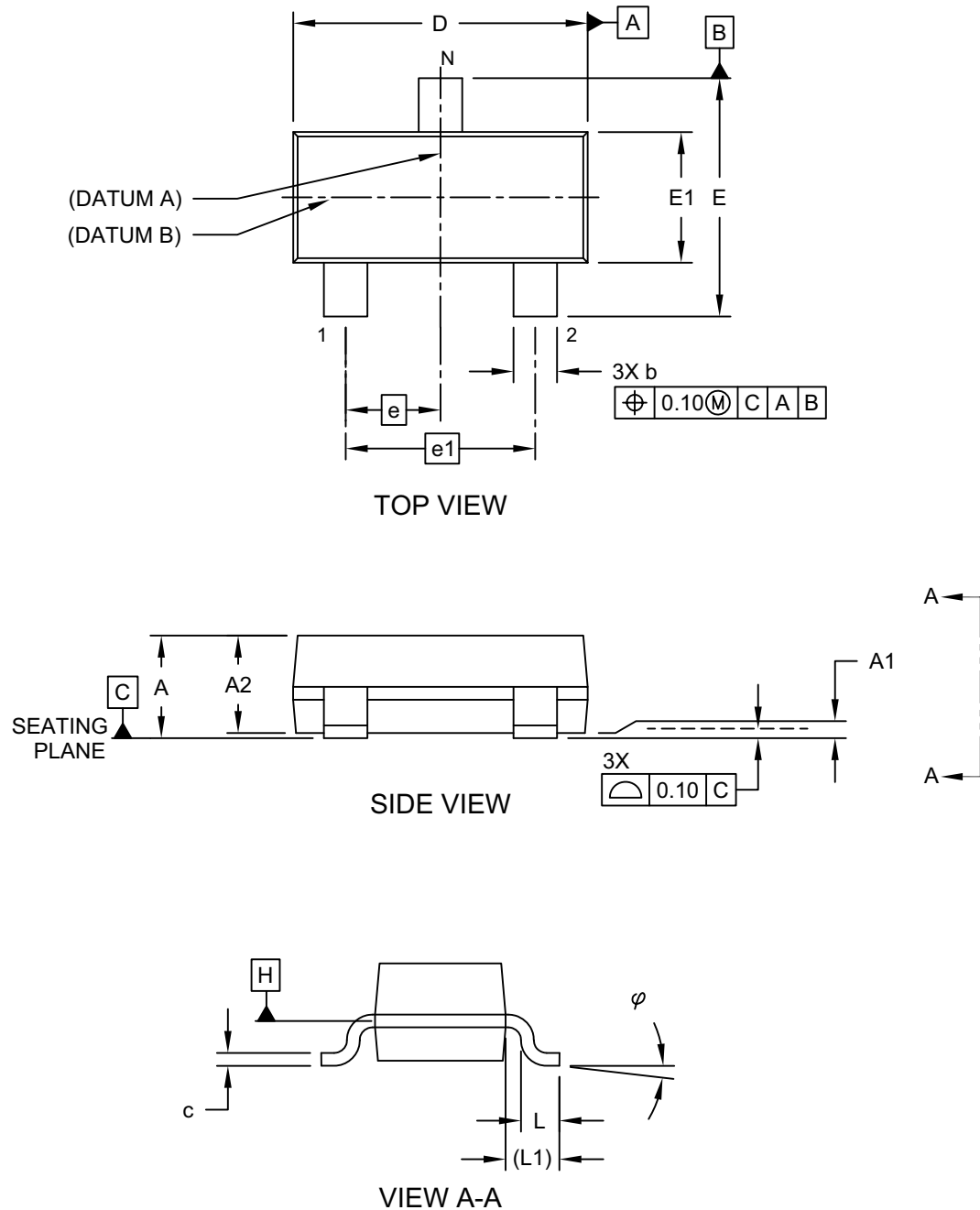
|                |        |                                                                                                                  |
|----------------|--------|------------------------------------------------------------------------------------------------------------------|
| <b>Legend:</b> | XX...X | Product Code or Customer-specific information                                                                    |
|                | Y      | Year code (last digit of calendar year)                                                                          |
|                | YY     | Year code (last 2 digits of calendar year)                                                                       |
|                | WW     | Week code (week of January 1 is week '01')                                                                       |
|                | NNN    | Alphanumeric traceability code                                                                                   |
|                | (e3)   | Pb-free JEDEC designator for Matte Tin (Sn)                                                                      |
|                | *      | This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package. |

**Note:** In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or not include the corporate logo.

## 4.2 Package Outline Drawings

### 3-Lead Plastic Small Outline Transistor (TT) [SOT-23]

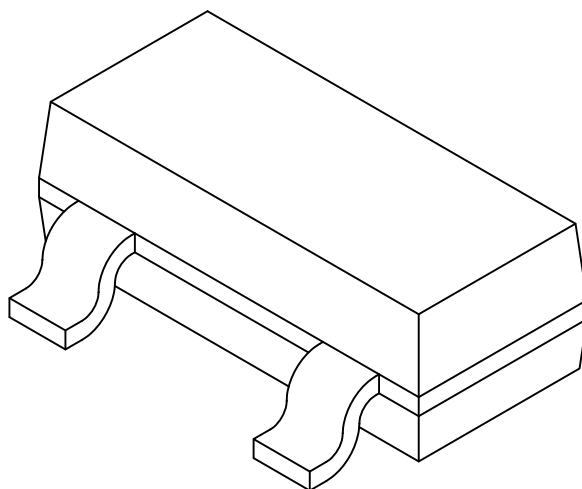
**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Microchip Technology Drawing C04-104 (TT) Rev C Sheet 1 of 2

## 3-Lead Plastic Small Outline Transistor (TT) [SOT-23]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



| Units                    |           | MILLIMETERS |      |      |
|--------------------------|-----------|-------------|------|------|
| Dimension Limits         |           | MIN         | NOM  | MAX  |
| Number of Pins           | N         | 3           |      |      |
| Lead Pitch               | e         | 0.95 BSC    |      |      |
| Outside Lead Pitch       | e1        | 1.90 BSC    |      |      |
| Overall Height           | A         | 0.89        | -    | 1.12 |
| Molded Package Thickness | A2        | 0.79        | 0.95 | 1.02 |
| Standoff                 | A1        | 0.01        | -    | 0.10 |
| Overall Width            | E         | 2.10        | -    | 2.64 |
| Molded Package Width     | E1        | 1.16        | 1.30 | 1.40 |
| Overall Length           | D         | 2.67        | 2.90 | 3.05 |
| Foot Length              | L         | 0.13        | 0.50 | 0.60 |
| Footprint                | (L1)      | 0.42 REF    |      |      |
| Foot Angle               | $\varphi$ | 0°          | -    | 10°  |
| Lead Thickness           | c         | 0.08        | -    | 0.20 |
| Lead Width               | b         | 0.30        | -    | 0.54 |

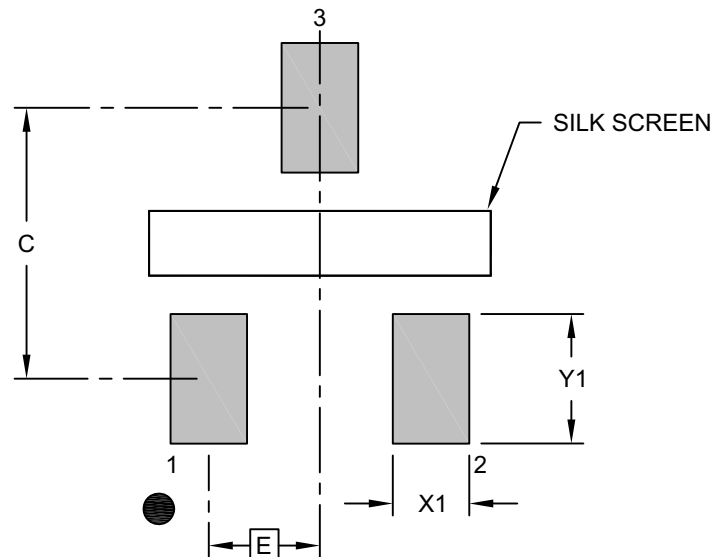
**Notes:**

- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.127mm per side.
- Dimensioning and tolerancing per ASME Y14.5M  
BSC: Basic Dimension. Theoretically exact value shown without tolerances.  
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-104 (TT) Rev C Sheet 2 of 2

## 3-Lead Plastic Small Outline Transistor (TT) [SOT-23]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



### RECOMMENDED LAND PATTERN

|                         | Units | MILLIMETERS |          |      |
|-------------------------|-------|-------------|----------|------|
|                         |       | MIN         | NOM      | MAX  |
| Dimension Limits        |       |             |          |      |
| Contact Pitch           | E     |             | 0.95 BSC |      |
| Contact Pad Spacing     | C     |             | 2.30     |      |
| Contact Pad Width (X3)  | X1    |             |          | 0.65 |
| Contact Pad Length (X3) | Y1    |             |          | 1.10 |

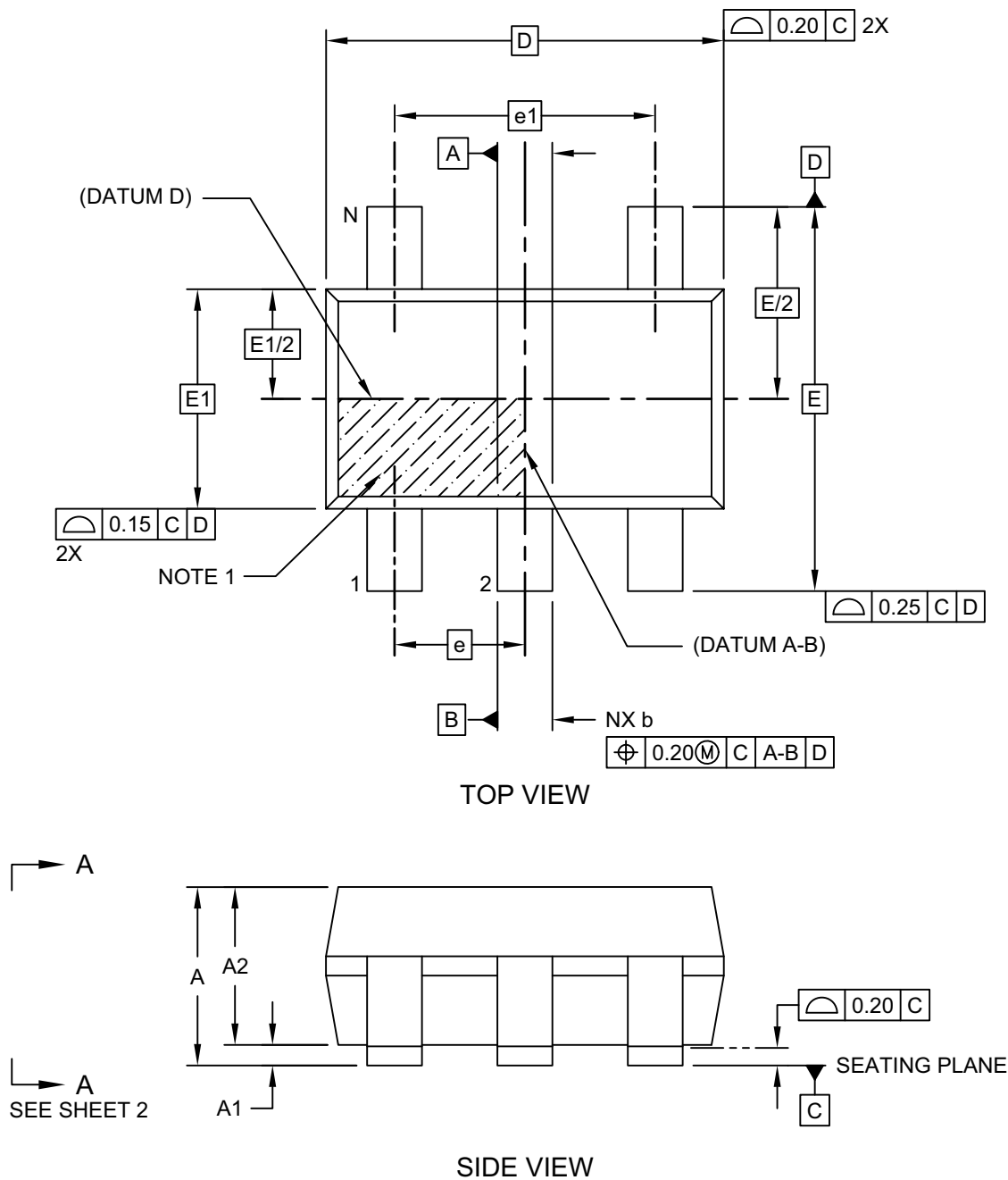
#### Notes:

1. Dimensioning and tolerancing per ASME Y14.5M  
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2104 (TT) Rev B

## 5-Lead Plastic Small Outline Transistor (C7X) [SOT-23]

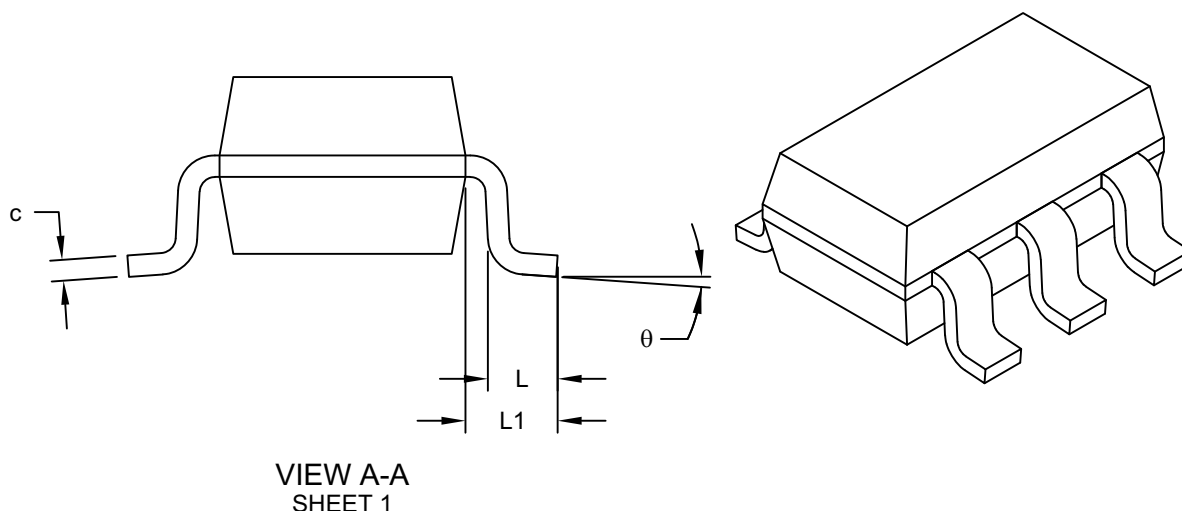
**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Microchip Technology Drawing C04-091-C7X Rev H Sheet 1 of 2

## 5-Lead Plastic Small Outline Transistor (C7X) [SOT-23]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



| Units                    |    | MILLIMETERS |     |      |
|--------------------------|----|-------------|-----|------|
| Dimension Limits         |    | MIN         | NOM | MAX  |
| Number of Pins           | N  | 5           |     |      |
| Pitch                    | e  | 0.95 BSC    |     |      |
| Outside lead pitch       | e1 | 1.90 BSC    |     |      |
| Overall Height           | A  | 0.90        | -   | 1.45 |
| Molded Package Thickness | A2 | 0.89        | -   | 1.30 |
| Standoff                 | A1 | -           | -   | 0.15 |
| Overall Width            | E  | 2.80 BSC    |     |      |
| Molded Package Width     | E1 | 1.60 BSC    |     |      |
| Overall Length           | D  | 2.90 BSC    |     |      |
| Foot Length              | L  | 0.30        | -   | 0.60 |
| Footprint                | L1 | 0.60 REF    |     |      |
| Foot Angle               | θ  | 0°          | -   | 10°  |
| Lead Thickness           | c  | 0.08        | -   | 0.26 |
| Lead Width               | b  | 0.20        | -   | 0.51 |

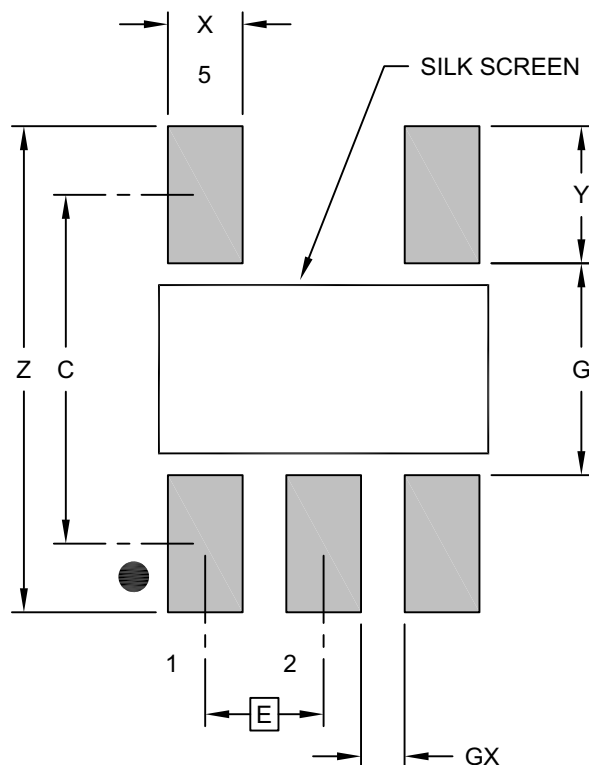
**Notes:**

- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25mm per side.
- Dimensioning and tolerancing per ASME Y14.5M  
BSC: Basic Dimension. Theoretically exact value shown without tolerances.  
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-091-C7X Rev H Sheet 2 of 2

## 5-Lead Plastic Small Outline Transistor (C7X) [SOT-23]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

| Units                   |    | MILLIMETERS |      |      |
|-------------------------|----|-------------|------|------|
| Dimension Limits        |    | MIN         | NOM  | MAX  |
| Contact Pitch           | E  | 0.95 BSC    |      |      |
| Contact Pad Spacing     | C  |             | 2.80 |      |
| Contact Pad Width (X5)  | X  |             |      | 0.60 |
| Contact Pad Length (X5) | Y  |             |      | 1.10 |
| Distance Between Pads   | G  | 1.70        |      |      |
| Distance Between Pads   | GX | 0.35        |      |      |
| Overall Width           | Z  |             |      | 3.90 |

**Notes:**

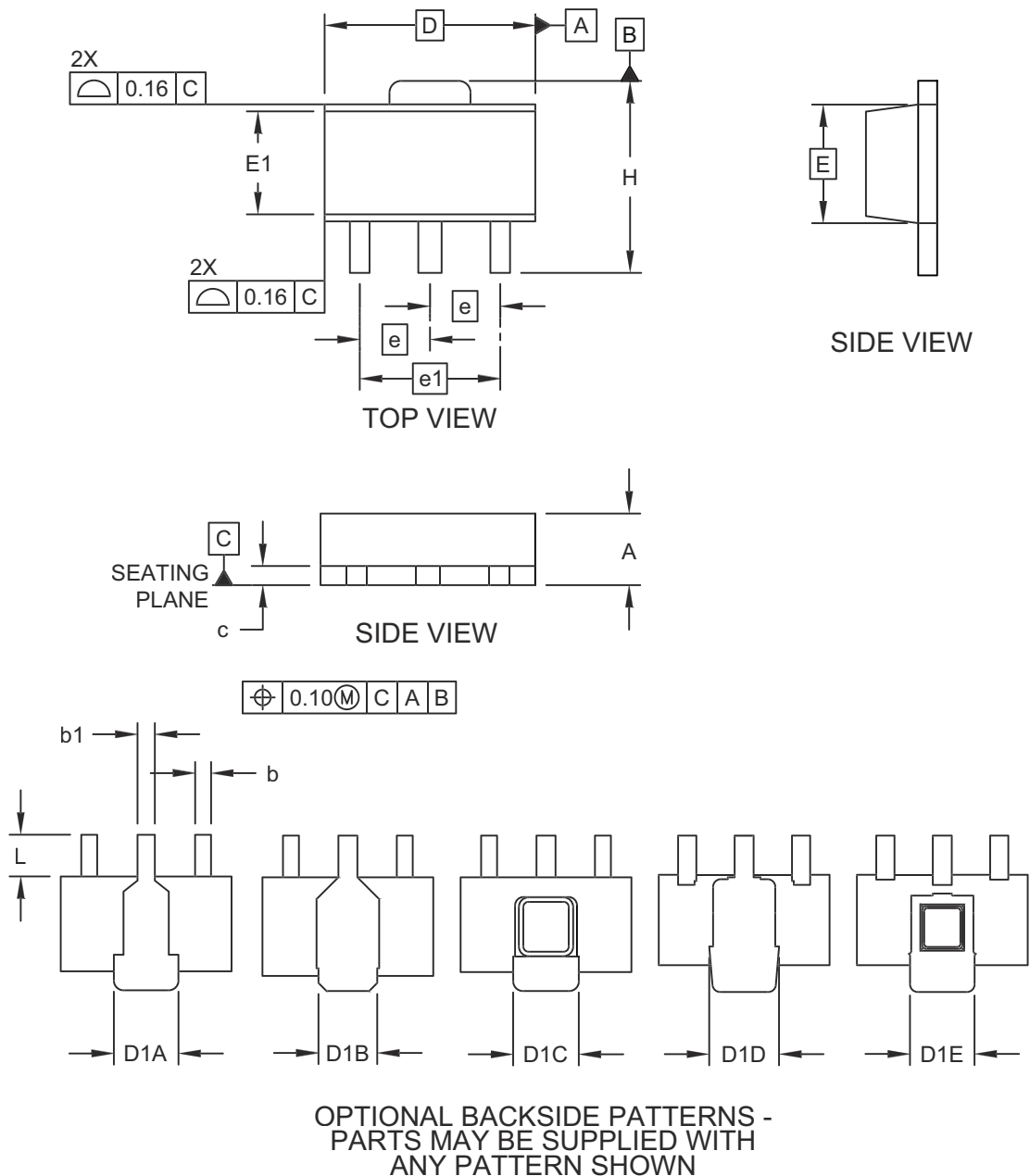
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2091-C7X Rev H

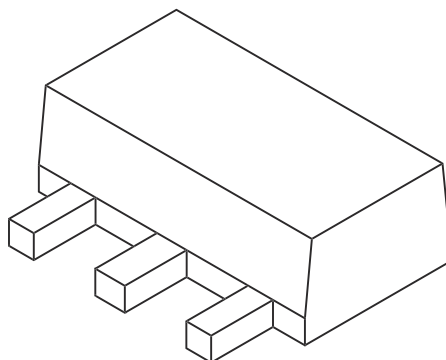
## 3-Lead Plastic Small Outline Transistor (A5X) - [SOT-89]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



## 3-Lead Plastic Small Outline Transistor (A5X) - [SOT-89]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



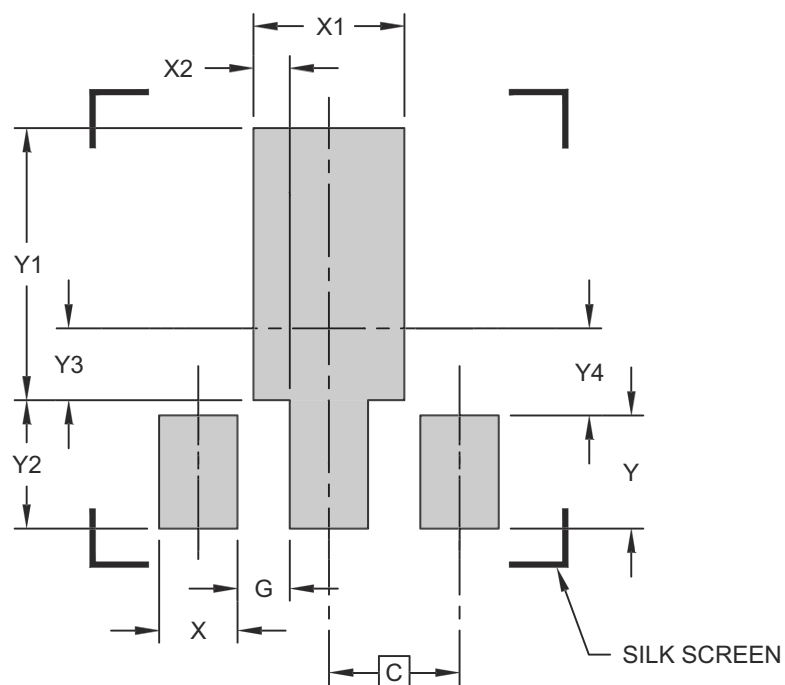
|                                  |     | Units | MILLIMETERS |      |      |
|----------------------------------|-----|-------|-------------|------|------|
| Dimension Limits                 |     |       | MIN         | NOM  | MAX  |
| Number of Leads                  | N   |       | 3           |      |      |
| Pitch                            | e   |       | 1.50 BSC    |      |      |
| Outside Lead Pitch               | e1  |       | 3.00 BSC    |      |      |
| Overall Height                   | A   |       | 1.40        | 1.50 | 1.60 |
| Overall Width                    | H   |       | 3.94        | 4.10 | 4.25 |
| Molded Package Width at Base     | E   |       | 2.50 BSC    |      |      |
| Molded Package Width at Top      | E1  |       | 2.00        | 2.20 | 2.29 |
| Overall Length                   | D   |       | 4.50 BSC    |      |      |
| Tab Length (Option A)            | D1A |       | 1.63        | 1.73 | 1.83 |
| Tab Length (Option B)            | D1B |       | 1.40        | 1.60 | 1.75 |
| Tab Length (Option C)            | D1C |       | 1.62        | 1.73 | 1.83 |
| Tab Length (Option D)            | D1D |       | 1.64 BSC    |      |      |
| Tab Length (Option E)            | D1E |       | 1.62        | 1.73 | 1.83 |
| Foot Length                      | L   |       | 0.73        | 1.10 | 1.20 |
| Lead Thickness                   | c   |       | 0.35        | 0.40 | 0.44 |
| Leads 1 & 3 Width                | b   |       | 0.36        | 0.42 | 0.48 |
| Lead 2 Width                     | b1  |       | 0.41        | 0.47 | 0.56 |
| Leads 1, 2, & 3 Width (Option D) | b   |       | 0.43        | 0.48 | 0.54 |

**Notes:**

1. The Pin 1 visual index feature may vary, but it must be located within the hatched area.
2. The package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M  
BSC: Basic Dimension. Theoretically exact value shown without tolerances.  
REF: Reference Dimension, usually without tolerance, for information purposes only.

## 3-Lead Plastic Small Outline Transistor (A5X) - [SOT-89]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



### RECOMMENDED LAND PATTERN

| Units            | MILLIMETERS |            |     |
|------------------|-------------|------------|-----|
| Dimension Limits | MIN         | NOM        | MAX |
| C                |             | 1.50 (BSC) |     |
| X (3 PLACES)     |             | 0.900      |     |
| X1               |             | 1.733      |     |
| X2 (2 PLACES)    |             | 0.416      |     |
| G (2 PLACES)     |             | 0.600      |     |
| Y (2 PLACES)     |             | 1.300      |     |
| Y1               |             | 3.125      |     |
| Y2               |             | 1.475      |     |
| Y3               |             | 0.825      |     |
| Y4               |             | 1.000      |     |

#### Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-02029-A5X Rev. E

## APPENDIX A: REVISION HISTORY

### Revision C (April 2026)

- Added 3-lead SOT-23 variant.
- Updated file to latest format.

### Revision B (August 2015)

- Minor fix to [Table 1-1](#).

### Revision A (June 2015)

- Converted Supertex inc. document DSFP-DN1509 A103108 to Microchip Datasheet DS20005403.
- Update file to new format.

## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

| <u>PART NO.</u>                                                                                                                                     | <u>[T/XX]<sup>(1)</sup></u>         | <u>-X</u>     | <u>/XXX</u>  |
|-----------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------|---------------|--------------|
| Device                                                                                                                                              | Tape and Reel<br>or<br>Package Type | Environmental | Package Code |
| <b>Device:</b> DN1509 = N-Channel, Depletion-Mode, Vertical DMOS FET                                                                                |                                     |               |              |
| <b>Media Type:</b> T = Tape and Reel, 3000/Reel (C6X)<br>(blank) = Tape and Reel, 3000/Reel for K1 (C7X)<br>= Tape and Reel, 2000/Reel for N8 (A5X) |                                     |               |              |
| <b>Package:</b> V/C6X = SOT-23, 3-lead (Code: C6X)<br>K1 = SOT-23, 5-lead (Code: C7X)<br>N8 = TO-243AA (SOT-89), 3-lead (Code: A5X)                 |                                     |               |              |
| <b>Environmental:</b> G = Lead (Pb)-free/ROHS-compliant package                                                                                     |                                     |               |              |

**Examples:**

- a) DN1509T-V/C6X<sup>2</sup>: Tape and Reel, 3-Lead SOT-23 package
- b) DN1509K1-G: Tape and Reel, 5-Lead SOT-23 package
- c) DN1509N8-G: Tape and Reel, 3-Lead TO-243AA package

**Note 1:** Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.
   
  
**2:** Reel: Lead (Pb)-free/ROHS-compliant package.

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