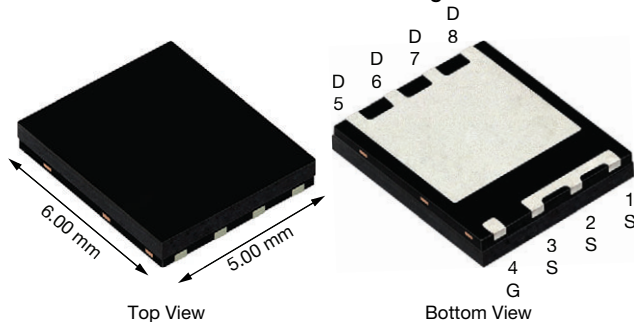


N-Channel 100 V 175°C (D-S) MOSFET

PowerPAK® SO-8SW Single


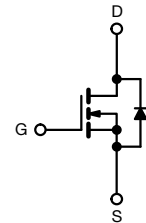
FEATURES

- TrenchFET® Gen V power MOSFET
- Very low $R_{DS(on)} \times Q_g$ figure-of-merit (FOM)
- Leadership $R_{DS(on)}$ minimizes power loss from conduction
- 100 % R_g and UIS tested
- Enhance power dissipation and lower R_{thJC}
- Wettable flank to improved solderability
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912


RoHS
 COMPLIANT
 HALOGEN
FREE

APPLICATIONS

- Synchronous rectification
- DC/DC converters
- OR-ing and hot swap switch
- Power supplies
- Motor drive control
- Battery management



N-Channel MOSFET

PRODUCT SUMMARY	
V_{DS} (V)	100
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 10$ V	0.0027
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 7.5$ V	0.0032
Q_g typ. (nC)	48.1
I_D (A) ^a	203
Configuration	Single

ORDERING INFORMATION	
Package	PowerPAK SO-8SW
Lead (Pb)-free and halogen-free	SiRS5100EPW-T1-RE3

ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C, unless otherwise noted)			
PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	V_{DS}	100	V
Gate-source voltage	V_{GS}	± 20	
Continuous drain current ($T_J = 150$ °C)	I_D	$T_C = 25$ °C	203
		$T_C = 70$ °C	170
		$T_A = 25$ °C	41 ^{b, c}
		$T_A = 70$ °C	34 ^{b, c}
Pulsed drain current ($V_{GS} = 10$ V, $t = 100$ μ s)	I_{DM}	500	A
Continuous source-drain diode current	I_S	$T_C = 25$ °C	
		$T_A = 25$ °C	7.6 ^{b, c}
Single pulse avalanche current	I_{AS}	60	mJ
Single pulse avalanche energy	E_{AS}	180	
Maximum power dissipation	P_D	$T_C = 25$ °C	205
		$T_C = 70$ °C	144
		$T_A = 25$ °C	8.3 ^{b, c}
		$T_A = 70$ °C	5.8 ^{b, c}
Operating junction and storage temperature range	T_J, T_{stg}	-55 to +175	°C
Soldering recommendations (peak temperature) ^c		260	

THERMAL RESISTANCE RATINGS					
PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction-to-ambient ^b	$t \leq 10$ s	R_{thJA}	14	18	°C/W
Maximum junction-to-case (drain)	Steady state	R_{thJC}	0.53	0.73	

Notes

- $T_C = 25$ °C
- Surface mounted on 1" x 1" FR4 board
- $t = 10$ s
- See solder profile (www.vishay.com/doc?73257). The PowerPAK SO-8S is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components



f. Maximum under steady state conditions is 50 °C/W

SPECIFICATIONS ($T_J = 25\text{ °C}$, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-source breakdown voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	100	-	-	V
V_{DS} temperature coefficient	$\Delta V_{DS}/T_J$	$I_D = 10\text{ mA}$	-	59	-	mV/°C
$V_{GS(th)}$ temperature coefficient	$\Delta V_{GS(th)}/T_J$	$I_D = 250\text{ }\mu\text{A}$	-	-8.6	-	
Gate-source threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2	-	4	V
Gate-source leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$	-	-	± 100	nA
Zero gate voltage drain current	I_{DSS}	$V_{DS} = 80\text{ V}, V_{GS} = 0\text{ V}$	-	-	1	μA
		$V_{DS} = 80\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ °C}$	-	-	10	
Drain-source on-state resistance ^a	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 20\text{ A}$	-	0.0022	0.0027	Ω
		$V_{GS} = 7.5\text{ V}, I_D = 20\text{ A}$	-	0.0025	0.0032	
Forward transconductance ^a	g_{fs}	$V_{DS} = 15\text{ V}, I_D = 85\text{ A}$	-	160	-	S
Dynamic ^b						
Input capacitance	C_{iss}	$V_{DS} = 50\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	-	5645	-	μF
Output capacitance	C_{oss}		-	1321	-	
Reverse transfer capacitance	C_{rss}		-	13	-	
Total gate charge	Q_g	$V_{DS} = 50\text{ V}, V_{GS} = 10\text{ V}, I_D = 20\text{ A}$	-	65	97	nC
			-	48	73	
Gate-source charge	Q_{gs}	$V_{DS} = 50\text{ V}, V_{GS} = 7.5\text{ V}, I_D = 20\text{ A}$	-	26	-	
Gate-drain charge	Q_{gd}		-	3.0	-	
Output charge	Q_{oss}		$V_{DS} = 50\text{ V}, V_{GS} = 0\text{ V}$	-	155	
Gate resistance	R_g	$f = 1\text{ MHz}$	0.3	1.5	3	
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 50\text{ V}, R_L = 5\text{ }\Omega, I_D \cong 10\text{ A},$ $V_{GEN} = 10\text{ V}, R_g = 1\text{ }\Omega$	-	18	40	ns
Rise time	t_r		-	8	20	
Turn-off delay time	$t_{d(off)}$		-	35	70	
Fall time	t_f		-	15	30	
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 50\text{ V}, R_L = 5\text{ }\Omega, I_D \cong 10\text{ A},$ $V_{GEN} = 7.5\text{ V}, R_g = 1\text{ }\Omega$	-	23	50	
Rise time	t_r		-	11	25	
Turn-off delay time	$t_{d(off)}$		-	32	65	
Fall time	t_f		-	15	30	
Drain-Source Body Diode Characteristics						
Continuous source-drain diode current	I_S	$T_C = 25\text{ °C}$	-	-	187	A
Pulse diode forward current	I_{SM}		-	-	200	
Body diode voltage	V_{SD}	$I_S = 10\text{ A}, V_{GS} = 0\text{ V}$	-	0.74	1.1	V
Body diode reverse recovery time	t_{rr}	$I_F = 10\text{ A}, di/dt = 100\text{ A}/\mu\text{s},$ $T_J = 25\text{ °C}$	-	117	235	ns
Body diode reverse recovery charge	Q_{rr}		-	172	345	nC
Reverse recovery fall time	t_a		-	37	-	ns
Reverse recovery rise time	t_b		-	80	-	

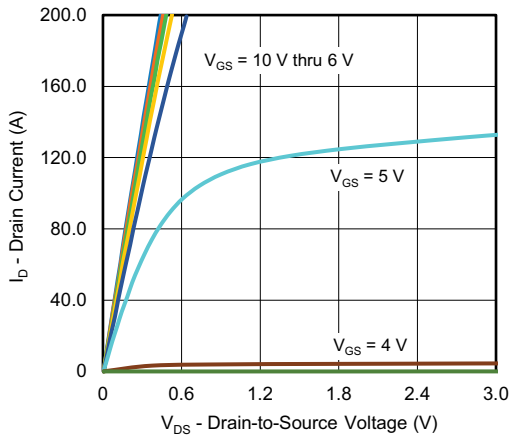
Notes

- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$
- b. Guaranteed by design, not subject to production testing

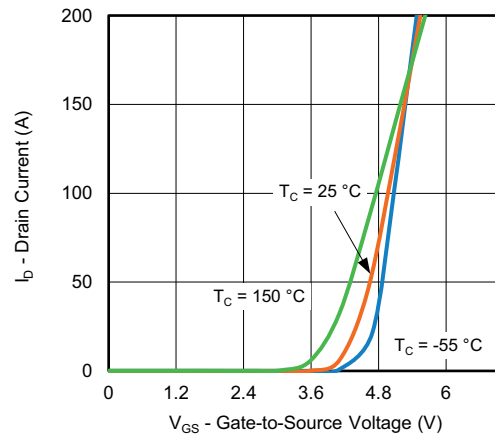
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



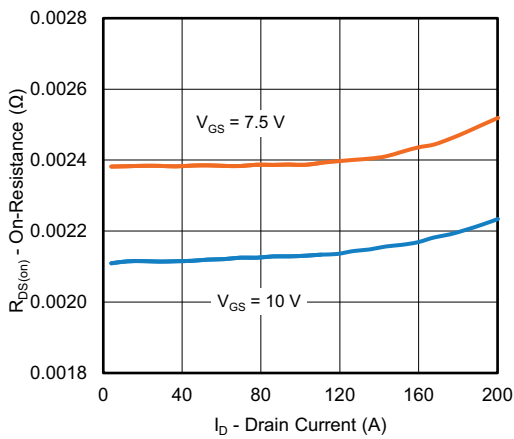
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



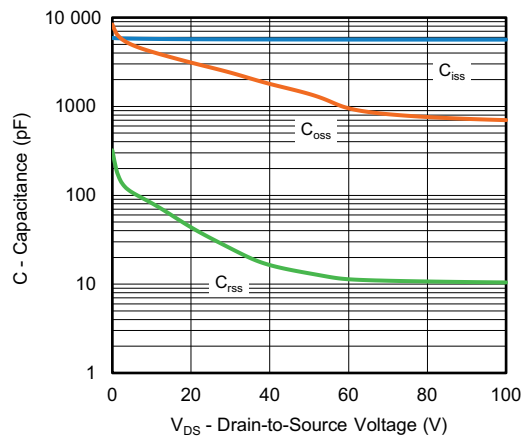
Output Characteristics



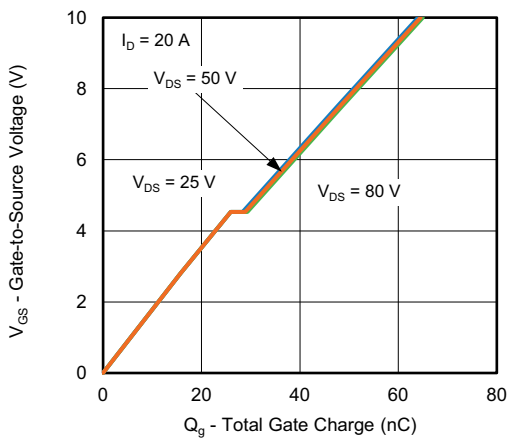
Transfer Characteristics



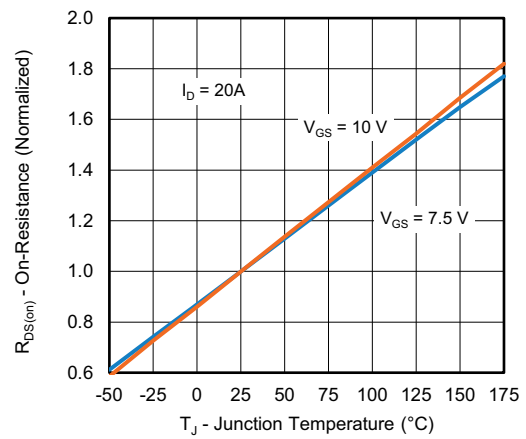
On-Resistance vs. Drain Current and Gate Voltage



Capacitance



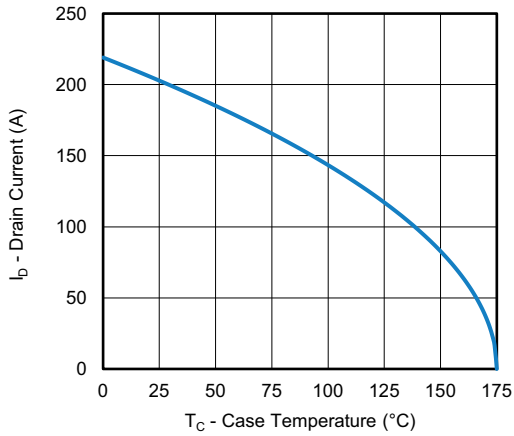
Gate Charge



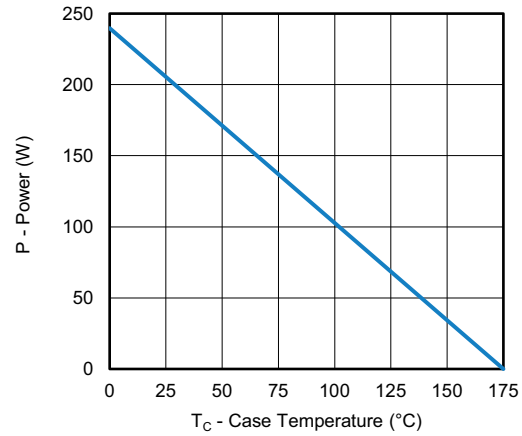
On-Resistance vs. Junction Temperature



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



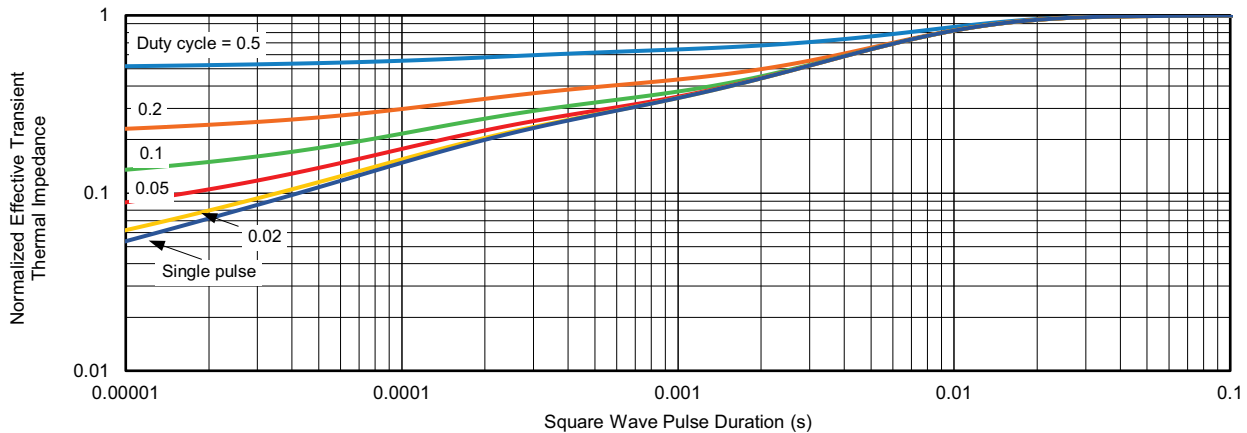
Current Derating ^a



Power, Junction-to-Case

Note

- a. The power dissipation P_D is based on $T_J \text{ max.} = 150 \text{ °C}$, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit

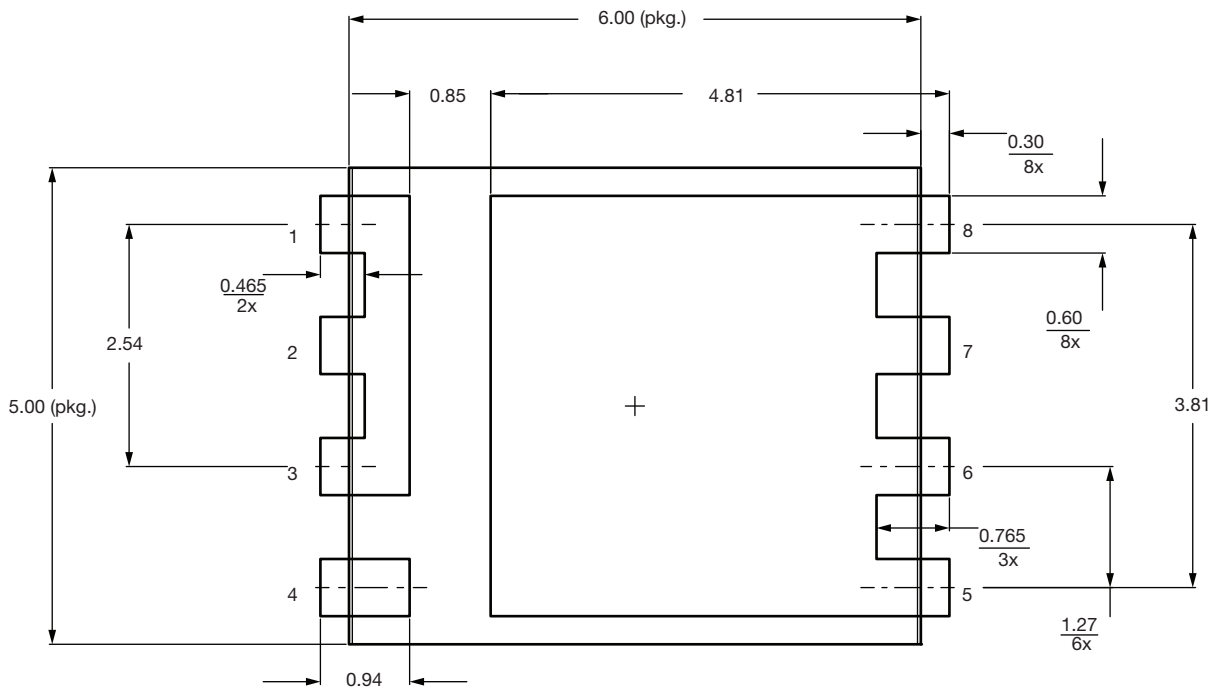
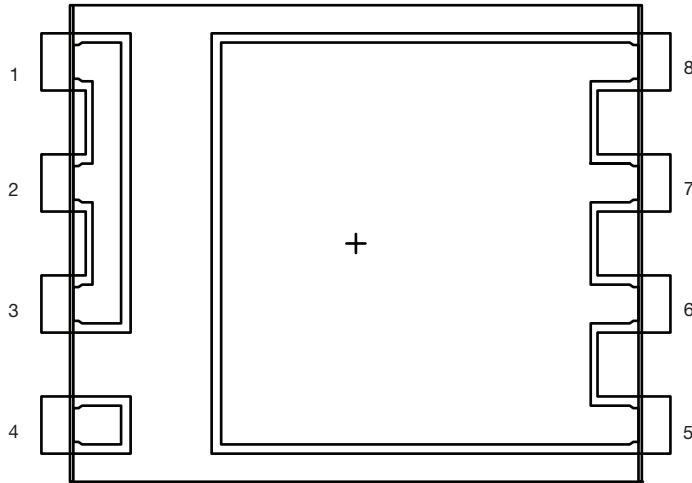


Normalized Thermal Transient Impedance, Junction-to-Case

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Recommended Land Pattern PowerPAK® SO-8SW (PKSO8SWSCCL)



Note

- Dimensions in mm

ECN: C24-0483-Rev. A, 20-May-2024
DWG: 3027



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