

User Registration

Register today to create your account on Silabs.com. Your personalized profile allows you to receive technical document updates, new product announcements, "how-to" and design documents, product change notices (PCN) and other valuable content available only to registered users. http://www.silabs.com/profile

PCN Date: 7/29/2016 Effective Date: 11/2/2016

Title: Si5340-41-42-44-45-46-47-48: Product Revision D

PCN Type:

□ Datasheet

⋈ Product Revision

PCN Details

Description of Change:

Silicon Labs is pleased to announce Revision D of the Si5340/41/42/44/45/46/47/48 devices and revision 1.0 of the corresponding datasheets and errata for these products.

After the effective date of this PCN, customers should begin using Si5340/41/42/44/45/46/47/48 Revision D devices for all new designs and the older Revision B devices will be classified as "Not Recommended for New Designs" (NRND). At this time, Silicon Labs has no plans to EOL the Revision B devices and will continue to support them in full production along with Revision D.

The changes from Revision B to Revision D of the Si5340/41/42/44/45/46/47/48 devices include the following:

- The maximum output frequency for Si5340/41/42/44/45 has been increased to 1.024GHz
- The majority of the errata for Revision B of Si5340/41/42/44/45/46/47/48 have been resolved
- Improvements have been made to the performance and flexibility of the circuits for hitless switching, holdover, loss of lock detection and out of frequency detection

A detailed description of these changes can be found in application note AN1006, available on www.silabs.com.

New datasheets, reference manuals and errata have been created for Revision D. The differences between Si5340/41/42/44/45/46/47/48 Revision B and Revision D datasheets, reference manuals and errata include:

- Replaced electrical specification tables with new characterization test results for Revision D
- Text added to describe new features and programming registers in Revision D
- Correction of typos present in the Revision B documents
- Ordering guides updated to indicate Revision D part numbers
- New errata documents indicate any errata specific to Revision D silicon

ClockBuilder Pro release 2.9 or later supports both Si534x Revision B and Revision D. Customers are encouraged to download the most recent version of CBPro to take advantage of the latest software features and algorithms. A detailed description of changes for each CBPro release is available at http://www.silabs.com/Support%20Documents/Software/ClockBuilder-Pro-README.pdf.

New evaluation boards are available for all Si5340/41/42/44/45/46/47/48 Revision D devices. The Revision D evaluation boards are identified with "-D" in the 7th and 8th characters of the OPN. For example the Si5345 Revision D OPN is SI5345-D-EVB.



Reason for Change:

Improve device performance and fix errata.

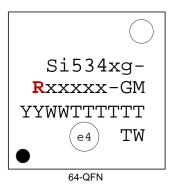
Impact on Form, Fit, Function, Quality, Reliability:

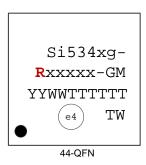
Si5340/41/42/44/45/46/47/48 Revision D devices are pin-compatible and footprint-compatible with Revision B devices; however, Revision D devices are not intended to be drop-in replacements for Revision B devices. As a result of changes to the circuitry in Revision D devices, their performance and behavior will not completely match that of Revision B.

- Customers currently using Revision B in production may continue to do so. Silicon Labs will maintain production of both Revision B and Revision D concurrently.
- Customers that wish to migrate a design from Revision B to Revision D should download the
 latest version of ClockBuilder Pro and create a new custom OPN for Revision D with their
 desired configuration. Once a new Revision D OPN has been created, customers should
 verify functionality of the device in their system prior to starting production with Revision D.
- Silicon Labs does not recommend writing a register file, settings file or regmap that was created for Revision B to a Revision D device. When migrating an existing design from Revision B to Revision D, customers should download the latest version of ClockBuilder Pro and create new register files, settings files or regmap exports to be used with Revision D.

Form: The device top mark has been updated to reflect the change to Revision D. Refer to the diagrams below. For more information, refer to each datasheet's Top Marking section, located at www.silabs.com.

- Device Revision B Top Mark: First character position (R) on line 2 below is a "B".
- Device Revision D Top Mark: First character position (R) on line 2 below is a "D".





Fit: No changes

Function:

- The maximum output frequency for Si5340/41/42/44/45 has been increased to 1.024GHz
- The majority of the errata for Revision B of Si5340/41/42/44/45/46/47/48 have been resolved.
- Improvements have been made to the performance and flexibility of the circuits for hitless switching, holdover, loss of lock detection and out of frequency detection

A detailed description of these functional changes can be found in application note AN1006, available on www.silabs.com.

Quality and Reliability: No changes



Product Identification:

Base OPNs (un-programmed devices):

Existing Part Number	Replacement Part Number	Drop in Compatible Indicator
Si5340A-B-GM	Si5340A-D-GM	See Datasheet
Si5340B-B-GM	Si5340B-D-GM	See Datasheet
Si5340C-B-GM	Si5340C-D-GM	See Datasheet
Si5340D-B-GM	Si5340D-D-GM	See Datasheet
Si5341A-B-GM	Si5341A-D-GM	See Datasheet
Si5341B-B-GM	Si5341B-D-GM	See Datasheet
Si5341C-B-GM	Si5341C-D-GM	See Datasheet
Si5341D-B-GM	Si5341D-D-GM	See Datasheet
Si5342A-B-GM	Si5342A-D-GM	See Datasheet
Si5342B-B-GM	Si5342B-D-GM	See Datasheet
Si5342C-B-GM	Si5342C-D-GM	See Datasheet
Si5342D-B-GM	Si5342D-D-GM	See Datasheet
Si5344A-B-GM	Si5344A-D-GM	See Datasheet
Si5344B-B-GM	Si5344B-D-GM	See Datasheet
Si5344C-B-GM	Si5344C-D-GM	See Datasheet
Si5344D-B-GM	Si5344D-D-GM	See Datasheet
Si5345A-B-GM	Si5345A-D-GM	See Datasheet
Si5345B-B-GM	Si5345B-D-GM	See Datasheet
Si5345C-B-GM	Si5345C-D-GM	See Datasheet
Si5345D-B-GM	Si5345D-D-GM	See Datasheet
Si5346A-B-GM	Si5346A-D-GM	See Datasheet
Si5346B-B-GM	Si5346B-D-GM	See Datasheet
Si5347A-B-GM	Si5347A-D-GM	See Datasheet
Si5347B-B-GM	Si5347B-D-GM	See Datasheet
Si5347C-B-GM	Si5347C-D-GM	See Datasheet
Si5347D-B-GM	Si5347D-D-GM	See Datasheet
Si5348A-B-GM	Si5348A-D-GM	See Datasheet
Si5348B-B-GM	Si5348B-D-GM	See Datasheet
Si5340A-B-GMR	Si5340A-D-GMR	See Datasheet
Si5340B-B-GMR	Si5340B-D-GMR	See Datasheet
Si5340C-B-GMR	Si5340C-D-GMR	See Datasheet
Si5340D-B-GMR	Si5340D-D-GMR	See Datasheet
Si5341A-B-GMR	Si5341A-D-GMR	See Datasheet
Si5341B-B-GMR	Si5341B-D-GMR	See Datasheet
Si5341C-B-GMR	Si5341C-D-GMR	See Datasheet
Si5341D-B-GMR	Si5341D-D-GMR	See Datasheet
Si5342A-B-GMR	Si5342A-D-GMR	See Datasheet
Si5342B-B-GMR	Si5342B-D-GMR	See Datasheet
Si5342C-B-GMR	Si5342C-D-GMR	See Datasheet
Si5342D-B-GMR	Si5342D-D-GMR	See Datasheet



Si5344A-D-GMR	See Datasheet
Si5344B-D-GMR	See Datasheet
Si5344C-D-GMR	See Datasheet
Si5344D-D-GMR	See Datasheet
Si5345A-D-GMR	See Datasheet
Si5345B-D-GMR	See Datasheet
Si5345C-D-GMR	See Datasheet
Si5345D-D-GMR	See Datasheet
Si5346A-D-GMR	See Datasheet
Si5346B-D-GMR	See Datasheet
Si5347A-D-GMR	See Datasheet
Si5347B-D-GMR	See Datasheet
Si5347C-D-GMR	See Datasheet
Si5347D-D-GMR	See Datasheet
Si5348A-D-GMR	See Datasheet
Si5348B-D-GMR	See Datasheet
	Si5344B-D-GMR Si5344C-D-GMR Si5344D-D-GMR Si5345A-D-GMR Si5345B-D-GMR Si5345C-D-GMR Si5345D-D-GMR Si5346A-D-GMR Si5346B-D-GMR Si5347B-D-GMR Si5347B-D-GMR Si5347D-D-GMR Si5347D-D-GMR

Note: The part numbers above include tape and reel variants which are denoted with an "R" at the end of the orderable part number.

Custom OPNs:

Custom OPNs are used for customer-specified, factory pre-programmed devices. The 9th character from the left in a custom OPN identifies the product revision.

- Example: Si5341A-Dxxxxx-GM
 - o "D" refers to the product revision
 - "xxxxx" refers to a unique 5-digit "Sequence ID" code assigned by the ClockBuilder Pro software

Customers currently using Revision B custom OPNs in production may continue to do so. Silicon Labs will maintain production of both Revision B and Revision D concurrently.

Customers that wish to migrate a design from a Revision B custom OPN to a Revision D custom OPN should download the latest version of ClockBuilder Pro and create a new custom OPN for Revision D with their desired configuration. Once a new Revision D OPN has been created, customers should verify functionality of the device in their system prior to starting production with Revision D.

Last Date of Unchanged Product: 11/2/2016

Qualification Samples:

Samples are available now.



Specific conditions of acceptance of this change will be considered on a case by case basis if written notice is submitted within 30 days of this notice. To request further data or inquire about this notification, please contact your local Silicon Labs sales representative. A list of Silicon Labs sales representatives is available at www.silabs.com.

In some cases rejection of a change notice may impact Silicon Labs product pricing, delivery, quality, or reliability.

Customer Early Acceptance Sign Off:

Customers may approve early PCN acceptance by completing the information below:

Early Acceptance:

Date:

Name:

Company:

Company:

Email your early Acceptance approval to: katherine.haggar@silabs.com

Qualification Data:

See below.



Si5340/Si5341 Qualification Report

W7101F1 Product Qualification Plan and Report Rev. E

SIII CON IARS The information contained in this document is PROPRIETARY to Silicon Laboratories, Inc. and shall not be reproduced or used in part or whole without Silicon Laboratories' written consent. The document is uncontrolled if printed or electronically saved.

Part Revs C, D	, TSMC Fabrication, SPI	L Assembly ex	cept as n	oted			
			Lot ID or	Fail/Pass or			
Test Name	Test Condition	Qualification	Start	End	Notes	Summary	Status
Test Group A - Ac	celerated Environment Stress	Tests - 9x9 mm	package				
HAST	JA110		Q35780	0/27	1, 3		
	130°C,85%RH	3 lots, N=>25	Q37205	0/80	1, 3	3 lots	
	Vcc=3.465V, 1,000 hours		Q37535	0/78	1, 3	0/185	Pass
Temp Cycle	JA104		Q35749	0/27	1, 3		
	Cond C: -65°C to 150°C	3 lots, N=>25	Q37203	0/80	1, 3	3 lots	
	500 cycles		Q37534	0/79	1, 3	0/186	Pass
HTSL	JA103		Q35640	0/27	1, 3		
	150°C, 1000hr	3 lots, N=>25	Q37204	0/80	1, 3	3 lots	
			Q37533	0/80	1, 3	0/187	Pass
Test Group A - Ac	celerated Environment Stress	Tests - 7x7 mm	package				
HAST	JA110		Q35780	0/27	1, 3		
	130°C,85%RH	3 lots, N=>25	Q37205	0/80	1, 3	3 lots	
	Vcc=3.465V, 1,000 hours		Q37535	0/78	1, 3	0/185	Pass
Temp Cycle	JA104		Q35850	0/26	1, 3		
	Cond C: -65°C to 150°C	3 lots, N=>25	Q37507	0/27	1, 3	3 lots	
	500 cycles		Q37504	0/27	1, 3	0/80	Pass
HTSL	JA103		Q35640	0/27	1, 3		
	150°C, 1000hr	3 lots, N=>25	Q37204	0/80	1,3	3 lots	
		,	Q37533	0/80	1, 3	0/187	Pass
Test Group B - Acc	celerated Lifetime Simulation	n Tests			·		
HTOL	JA108		Q35606	0/85	4		
	125°C, Dynamic	3 lots, N=>77	Q37081	0/80	2, 4	3 lots	
	Vcc=3.465V, 1000 hours	1	Q38677	0/80	2	0/245	Pass
LTOL	JA108						
	-10°C, Dynamic	1 lot, N=>32	35769	0/34	4	1 lots	
	Vcc=3.465V, 1000 hours				·		Pass
ELFR	JA108		Q37086	0/504	4		
	125°C, Dynamic	3 lots, N=>500	Q37468	0/504	4	3 lots	
	Vcc=3.465V, 48 hours	5 (0(3, 14-2000	Q37468 Q37808	0/504	4	0/1522	Pass
Test Group C - Day	ckage Assembly Integrity Test	-c	20,000	07 304	7	071322	1 433
Wire Bond Shear	JB116		66 4749, 1	0/5	3	T T	
AAU G DOUG SUGGE	30110	Eita NL . 20		1 1	3	21040	
		5 units, N⊨>30	676690.1	0/5		3 lots	D
Mine Deed Dail	W2044		676689.1	0/5	3	0/15	Pass
Wire Bond Pull	M2011		664749.1	0/5	3	,,	
		5 units, N⊨>30	676690.1	0/5	3	3 lots	_
			676689.1	0/5	3	0/15	Pass



Si5340/Si5341 Qualification Report

W7101F1 Product Qualification Plan and Report Rev. E

SIII C. O. N. I. A. R. S. The information contained in this document is PROPRIETARY to Silicon Laboratories, Inc. and shall not be reproduced or used in part or whole without Silicon Laboratories' written consent. The document is uncontrolled if printed or electronically saved.

Test Name	Test Condition	Qualification	Lot ID or Start	Fail/Pass or End	Notes	Summary	Status
Test Group E - E	lectrical Verification						
ESD-HBM	JA114	1 lot, N=>3	Q39073				3 kV
ESD-MWA	JA115	1 lot, N=>3	Q39074				200 V
ESD-CD/M	JC101	1 lot, N=>3	Q39072				1000 V
ESD-CD/M	JC101	1 lot, N=>3	Q35737		3		1000 V
Latch Up	JESD78 ±200m A Overvoltage = 5, 1975V	1 lot, N=>6	Q39075 Q35673	85 C 25 C	4		Pass

Notes

- 1. Parts are Pre-conditioned at MSL2/260°C
- 2. Lot stressed to 2,000 hours
- 3. Leveraged package family qualification data
- 4. Leveraged die family qualification data

This report applies to the following part numbers:						
Si 5341A-C- G/M/R	Si5341B-C-GM/R	Si5341C-C-G/W R	Si 5341D-C-GM/R	Si 53 40 A - C - GM/R		
Si 53 40 B- C- G/W/R	Si5340C-C-G/W R	Si5340 D-C-G/W R				
Si5341A-D-GM/R	Si5341B-D-G/W R	Si5341C-D-G/M/R	Si5341D-D-G/W/R	Si 5340A- D-GM/R		
Si 53 40B- D- GM/R	Si5340C-D-GM/R	Si5340 D- D- G/M/R				



Si5342/Si5344/Si5345 Qualification Report

🖊 🚅 W7101F1 Product Qualification Plan and Report 💎 Rev. E

SIIIICAN IARS The information contained in this document is PROPRIETARY to Silicon Laboratories, Inc. and shall not be reproduced or used in part or whole without Silicon Laboratories' written consent. The document is uncontrolled if printed or electronically saved.

Part Revs C, D,	TSMC Fabrication, SPI	L Assembly ex	cept as n	oted			
Test Name	Test Condition	Qualification	Lot ID or Start	FaiUPass or End	Notes	Summary	Status
Test Group A - Acce	" elerated Environment Stress	Tests - 9x9 mm	package				
HAST	JA110		Q35780	0/27	1, 3		
	130°C,85%RH	3 lots, N=>25	Q37205	0/80	1, 3	3 lots	
	Vcc=3.465V, 1,000 hours		Q37535	0/78	1, 3	0/185	Pass
Temp Cycle	JA104		Q35749	0/27	1, 3		
	Cond C: -65°C to 150°C	3 lots, N=>25	Q37203	0/80	1, 3	3 lots	
	500 cycles		Q37534	0/79	1, 3	0/186	Pass
HTSL	JA103		Q35640	0/27	1, 3		
	150°C, 1000hr	3 lots, N=>25	Q37204	0/80	1, 3	3 lots	
			Q37533	0/80	1, 3	0/187	Pass
Test Group A - Acce	elerated Environment Stress	Tests - 7x7 mm	package				
HAST	JA110		Q35780	0/27	1, 3		
	130°C,85%RH	3 lots, N=>25	Q37205	0/80	1, 3	3 lots	
	Vcc=3.465V, 1,000 hours		Q37535	0/78	1, 3	0/185	Pass
Temp Cycle	JA104		Q35850	0/26	1, 3		
	Cond C: -65°C to 150°C	3 lots, N=>25	Q37507	0/27	1, 3	3 lots	
	500 cycles		Q37504	0/27	1, 3	0/80	Pass
HTSL	JA103		Q35640	0/27	1, 3		
	150°C, 1000hr	3 lots, N=>25	Q37204	0/80	1, 3	3 lots	
	1,000,000,000	1012, 11 120	Q37533	0/80	1, 3	0/187	Pass
Test Group B - Acce	lerated Lifetime Simulation	Tests	Q. 100		., -	21.121	
HTOL	JA108		Q35606	0/85	4		
	125°C, Dynamic	3 lots, N=>77	Q37081	0/80	2, 4	3 lots	
	Vcc=3.465V, 1000 hours		Q38677	0/80	2	0/245	Pass
LTOL	JA108		Q00077	0.00		101240	1 433
	-10°C, Dynamic	1 lot, N=>32	35769	0/34	4	1 lots	
	Vcc=3.465V, 1000 hours	1 (00, 14-702	33707	0,04	7	''''	Pass
ELFR	JA108		Q37086	0/504	4	+ +	, 433
	125°C, Dynamic	3 lots, N=>500	Q37468	0/504	4	3 lots	
	Vcc=3.465V, 48 hours	3 (0(3, 14-7300	Q37400 Q37808	0/514	4	0/1522	Pass
Test Group C - Pack	age Assembly Integrity Test	<u> </u>	Q37000	07304	7	071322	L 022
Wire Bond Shear	JB116	. .	66 4749, 1	0/5	3		
Mule polia alleat	35110	Euroite No.20	676690.1	0/5	3	21-4-	
		5 units, N⊨>30				3 lots	D
Wire Bond Pull	W2044		676689.1	0/5	3	0/15	Pass
wire Bond Pull	M2011	F 11 11 55	664749.1	0/5	3	,,	
		5 units, N=>30	676690.1	0/5	3	3 lots	_
			676689.1	0/5	3	0/15	Pass



Si5342/Si5344/Si5345 Qualification Report

W7101F1 Product Qualification Plan and Report Rev. E

SIIIICAN IARS The information contained in this document is PROPRIETARY to Silicon Laboratories, Inc. and shall not be reproduced or used in part or whole without Silicon Laboratories' written consent. The document is uncontrolled if printed or electronically saved.

Part Revs C,	D, TSMC Fabrication, SP	L Assembly e	cept as n	oted			
Test Name	Test Condition	Qualification	Lot ID or Start	Fail/Pass or End	Notes	Summary	Status
Test Group E - E	lectrical Verification						
ESD-HBM	JA114	1 lot, N=>3	Q39073				3 kV
ESD-MM	JA115	1 lot, N=>3	Q39074				200 V
ESD-CDM	JC101	1 lot, N=>3	Q39072				1000 V
ESD-CDM	JC101	1 lot, N=>3	Q35737		3		1000 V
Latch Up	JESD78 ±200m A Overvoltage = 5.1975V	1 lot, N=>6	Q39075 Q35673	85 C 25 C	4		Pass

Notes:

- 1. Parts are Pre-conditioned at MSL2/260°C
- 2. Lot stressed to 2,000 hours
- 3. Leveraged package family qualification data
- 4. Leveraged die family qualification data

This report applies to the following part numbers:							
Si 53 42 A - C - G/M / R	Si5342B-C-G/M/R	Si5342C-C-G/W/R	Si 5342D-C- GM/R	Si 53 44A-C- G/M/R			
Si 53 44B-C-G/W R	Si5344C-C-GAVR	Si5344D-C-G/W R	Si5345A-C-GM/R	Si 53 45B-C-G/W R			
Si 53 45C - C- GM/R	Si5345 D-C-GM/R						
Si 53 42 A - D - GM/R	Si5342B-D-G/W/R	Si5342C-D-G/M/R	Si 5342D-D-G/W/R	Si 5344A- D-G/M/R			
Si 53 44B- D- GM/R	Si5344C-D-GM/R	Si5344D-D-GM/R	Si 5345A- D- GM/R	Si 5345B- D- G/M/R			
Si 53 45C-D-GM/R	Si5345 D- D- GM/R						



Si5346/Si5347 Qualification Report

🭑 W7101F1 Product Qualification Plan and Report 💎 Rev. E

Part Revs C, D	, TSMC Fabrication, SPI	L Assembly e	cept as n	oted					
			Lot ID or	FaiUPass or		s Summary State			
Test Name	Test Condition	Qualification	Start	End	Notes	Summary	Status		
Test Group A - Ac	celerated Environment Stress	Tests - 9x9 mm	package						
HAST	JA110		Q35780	0/27	1, 3				
	130°C,85%RH	3 lots, N=>25	Q37205	0/80	1, 3	3 lots			
	Vcc=3.465V, 1,000 hours		Q37535	0/78	1, 3	0/185	Pass		
Temp Cycle	JA104		Q35749	0/27	1, 3				
	Cond C: -65°C to 150°C	3 lots, N=>25	Q37203	0/80	1, 3	3 lots			
	500 cycles		Q37534	0/79	1, 3	0/186	Pass		
HTSL	JA103		Q35640	0/27	1, 3				
	150°C, 1000hr	3 lots, N=>25	Q37204	0/80	1, 3	3 lots			
			Q37533	0/80	1, 3	0/187	Pass		
Test Group A - Ac	celerated Environment Stress	Tests - 7x7 mm	package						
HAST	JA110		Q35780	0/27	1, 3				
	130°C,85%RH	3 lots, N=>25	Q37205	0/80	1, 3	3 lots			
	Vcc=3.465V, 1,000 hours		Q37535	0/78	1, 3	0/185	Pass		
Temp Cycle	JA104		Q35850	0/26	1, 3				
	Cond C: -65°C to 150°C	3 lots, N=>25	Q37507	0/27	1, 3	3 lots			
	500 cycles		Q37504	0/27	1, 3	0/80	Pass		
HTSL	JA103		Q35640	0/27	1, 3				
	150°C, 1000hr	3 lots, N=>25	Q37204	0/80	1, 3	3 lots			
		,	Q37533	0/80	1, 3	0/187	Pass		
Test Group B - Ac	celerated Lifetime Simulation	n Tests							
HTOL	JA108		Q35606	0/85	4				
	125°C, Dynamic	3 lots, N=>77	Q37081	0/80	2, 4	3 lots			
	Vcc=3.465V, 1000 hours	0 1000, 11 177	Q38677	0/80	2	0/245	Pass		
LTOL	JA108		Q00077	0.00		0.2.0	. 433		
	-10°C, Dynamic	1 lot, N=>32	35769	0/34	4	1 lots			
	Vcc=3.465V, 1000 hours	1 (00, 14-752	33707	0,34	7	''06	Pass		
ELFR	JA108		007094	0/504	4		L 033		
LLI IX	125°C, Dynamic	3 lots, N=>500	Q37086 Q37468	0/504		3 lots			
	Vcc=3,465V, 48 hours	3 lots, N=>500	Q37468 Q37808	0/514	4 4	0/1522	Pass		
T+ C C	· ·	-	Q37000	07 304	4	071322	P 422		
	ckage Assembly Integrity Test	I.S	Z / 4740 4	0.0	_				
Wire Bond Shear	JB116		664749.1	0/5	3				
		5 units, N⊨>30	676690.1	0/5	3	3 lots	_		
			676689.1	0/5	3	0/15	Pass		
Wire Bond Pull	M2011		664749.1	0/5	3				
		5 units, N=>30	676690.1	0/5	3	3 lots			
			676689.1	0/5	3	0/15	Pass		



Si5346/Si5347 Qualification Report

W7101F1 Product Qualification Plan and Report Rev. E

SIIII. N. N. I. A. B. S. The information contained in this document is PROPRIETARY to Silicon Laboratories, Inc. and shall not be reproduced or used in part or whole without Silicon Laboratories' written consent. The document is uncontrolled if printed or electronically saved.

Test Name	Test Condition	Qualification	Lot ID or Start	Fail/Pass or End	Notes	Summary	Status
Test Group E - E	lectrical Verification						
ESD-HBM	JA114	1 lot, N=>3	Q39073				3 kV
ESD-MM	JA115	1 lot, N=>3	Q39074				200 V
ESD-CDM	JC101	1 lot, N=>3	Q39072				1000 V
ESD-CDM	JC101	1 lot, N=>3	Q35737		3		1000 V
Latch Up	JESD78 ±200m A Overvoltage = 5.1975V	1 lot, N=>6	Q39075 Q35673	85 C 25 C	4		Pass

Notes:

- 1. Parts are Pre-conditioned at MSL2/260°C
- 2. Lot stressed to 2,000 hours
- 3. Leveraged package family qualification data
- 4. Leveraged die family qualification data

This report applies to the following part numbers:							
C-GM/R	Si 53 47C - C - G/M / R	Si 5347B-C-G/W R	Si5347A-C-G/W R	S15346 B-C-G/M/R	Si 53 46 A - C - GM/R		
					Si 53 47D-C-GM/R		
≻GM/R	Si 5347C- D- GM/R	Si 5347B- D- G/M/R	Si5347A-D-G/W R	Si5346 B-D-G/W R	Si 5346 A-D-G/M/R		
					Si 53 47D-D-G/W/R		
<i>y</i> 0,000	3133476-12-0///	31334) B- D- OWN IC	31334) H-D-G/W K	313340 E-D-OWN K			