MAX20430 Four-Output Mini PMIC For Safety Applications

General Description

The MAX20430 is a high-efficiency, four-output DC-DC converter and windowed watchdog. OUT1 is a synchronous step-down converter that converts vehicle battery voltage to 3.3V at up to 2.5A. OUT3 boosts OUT1 to 5V at up to 500mA, while OUT2 and OUT4 low-voltage synchronous step-down converters operate from OUT1 and provide a 0.8V to 3.9875V output voltage range at up to 3A. All outputs achieve ±1.5% output error over load, line, and temperature range.

The device features 2.1MHz fixed-frequency PWM mode for all DC-DC outputs for better noise immunity and load-transient response. The 2.1MHz frequency operation allows for the use of all ceramic capacitors and minimizes external components. The programmable spread-spectrum frequency modulation minimizes radiated electromagnetic emissions. Integrated low R_{DSON} switches improve efficiency at heavy loads and make the layout much simpler with respect to discrete solutions.

The device is offered with factory-preset output voltages. Other features include soft-start, overcurrent, and overtemperature protections.

Applications

- ADAS

Benefits and Features

- Multiple Functions for Small Size
  - Synchronous High-Voltage Buck Converter up to 2.5A
    - Input Voltage Range 3.5V to 40V
    - Output Voltage of 3.3V
  - 5V Synchronous 500mA Boost Converter
  - Dual Synchronous Buck Converters up to 3A
    - 0.8V to 3.9875V in 12.5mV Steps
  - Flexible Power Sequencer for OUT2, OUT3, and OUT4
  - Programmable Challenge/Response or Windowed Watchdog
  - Two Free Programmable UV/OV Voltage Monitors
    - 0.8V to 3.9875V in 12.5mV Steps
  - I^2C Fast Mode Plus Compatible Interface with Packet Error-Checking Option (PEC)
  - 2.1MHz Internal Operation with Spread-Spectrum Option
  - $\overline{RESET}$ Output
  - Current Mode, Forced PWM Operation
- High-Precision for ASIL Applications
  - ±1.5% Output Voltage Accuracy
  - ±1% OV/UV Monitoring
- Diagnostics and Redundant Circuits
  - ASIL C Compliant
  - Redundant Reference
  - BIST Diagnostics
  - Fail Safe on Open Pins
  - Shorted Pin Detection on $\overline{RESET}$
- Mount ID Location Detection
- Robust for the Automotive Environment
- Overtemperature and Short-Circuit Protection
- 5mm x 5mm Side-Wettable TQFN Package
- -40°C to +125°C Grade 1 Automotive Temperature Range

Ordering Information appears at end of datasheet.

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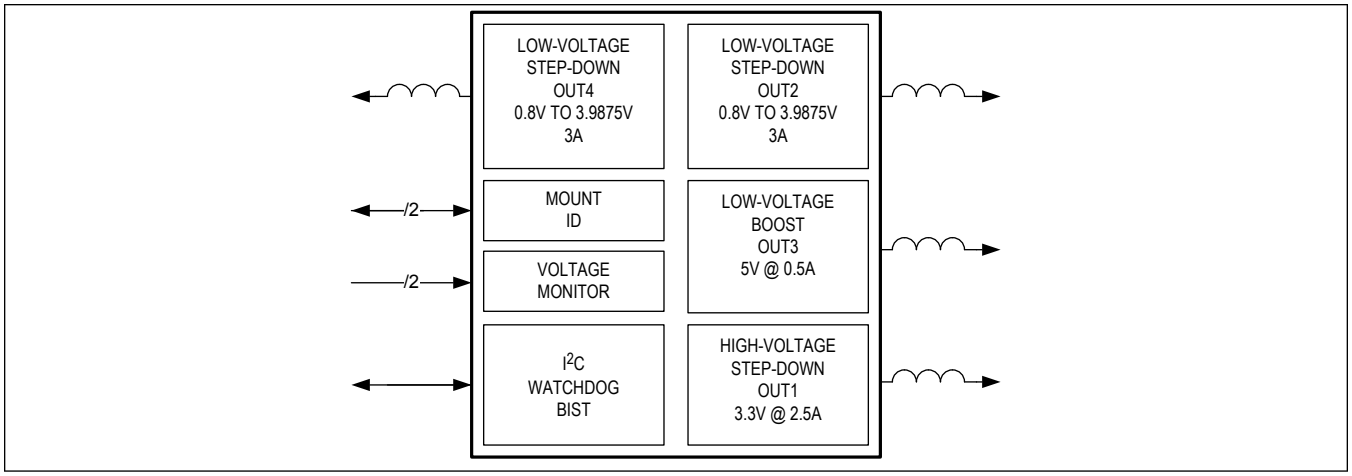
Simplified Block Diagram



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Absolute Maximum Ratings

V_{SUP}, EN to GND ..... -0.3V to +40V
BST to LX1 ..... -0.3V to +6V
PV2, PV4 to PGND_ ..... -0.3V to +6V
BIAS, BIASP to GND ..... -0.3V to +6V
IN5, IN6 to GND ..... -0.3V to BIAS + 0.3V
MD1, MD2 to GND ..... -0.3V to +40V
SCL, SDA, SYNC, $\overline{RESET}$ to GND ..... -0.3V to +6V
OUT1 to GND ..... -0.3V to BIAS+0.3V
OUT2 to GND ..... -0.3V to PV2 + 0.3V
OUT4 to GND ..... -0.3V to PV4 + 0.3V
OUT3 to GND ..... -0.3V to +6V
LX1 to PGND1 (Note 1) ..... -0.3V to V_{SUP} + 0.3V
LX2 to PGND2 (Note 1) ..... -0.3V to PV2 + 0.3V
LX3 to PGND3 (Note 1) ..... -0.3V to OUT3 + 0.3V
LX4 to PGND4 (Note 1) ..... -0.3V to PV4 + 0.3V
GND to PGND_ ..... -0.3V to +0.3V
Output Short-Circuit Duration ..... Continuous
Continuous Power Dissipation (T_A = +70°C)
28-TQFN-EP (Single-Layer Board) (derate 65mW/°C > 70°C) 1702.1mW
28-TQFN-EP (Multilayer Board) (derate 34.5mW/°C > 70°C.) 2758mW
Operating Temperature Range ..... -40°C to 125°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature Range ..... +300°C

Note 1: Self-protected against transient voltages exceeding these limits for ≤ 50ns under normal operation and loads up to the maximum rated output current.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

28-QFN-EP

Package Code	T2855Y+12C
Outline Number	21-100297
Land Pattern Number	90-100102
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	29°C/W
Junction to Case (θ_{JC})	2°C/W

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

Electrical Characteristics

(V_{SUP} = V_{EN} = 13.5V, V_{OUT1} = V_{PV2} = V_{PV4} = 3.3V, V_{BIAS} = 5.0V, T_A = TJ = -40°C to +125°C unless otherwise noted, typical values are at T_A = 25°C under normal conditions unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage Range	V_{SUP}	Fully operational, no BIAS switchover	3.5		36	V
		< 1s			40	
Supply Current	I_{SUP}	EN = low		7	50	µA
		No load, EN = high, V_{OUT1} = 3.3V		24		mA
UVLO	$UVLO_R$	Rising		3.25	3.45	V
	$UVLO_F$	Falling	2.5	2.83		
BIAS, BIASP Voltage		No switchover, V_{SUP} ≥ 5.5V		5		V
BIAS Current Limit			10			mA

Electrical Characteristics (continued)

(V_{SUP} = V_{EN} = 13.5V, V_{OUT1} = V_{PV2} = V_{PV4} = 3.3V, V_{BIAS} = 5.0V, T_A = TJ = -40°C to +125°C unless otherwise noted, typical values are at T_A = 25°C under normal conditions unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
OUT1 (HV BUCK)						
Voltage Accuracy			-1.5		1.5	%
Line Regulation		V_{SUP} = 6V to 36V		0.02		%/V
DMOS High-Side On-Resistance		V_{BIAS} = 5V, I_{LX1} = 0.1A		52	130	mΩ
DMOS Low-Side On-Resistance		V_{BIAS} = 5V, I_{LX1} = 0.1A		47	110	mΩ
High-Side Current-Limit Threshold			3.5	4	4.5	A
Negative Current-Limit Threshold				-1.6		A
Minimum On-Time				65	80	ns
Max Duty Cycle			98	99		%
Switching Phase				0		deg
Soft-Start Time				0.9		ms
OUT2/OUT4 (LV BUCK)						
Supply Voltage Range	V_{PV2},V_{PV4}		3		5.5	V
Voltage Accuracy	V_{OUT2},V_{OUT4}	$I_{LOAD\_}$ = 0A to I_{MAX}, 3.0V ≤ $V_{PV\_}$ ≤ 5.5V	-1.5		1.5	%
HS pMOS On-Resistance		$I_{LX\_}$ = 0.2A		82	150	mΩ
LS nMOS On-Resistance		$I_{LX\_}$ = 0.2A		50	115	mΩ
HS Current-Limit Threshold		Option 1 (1A)	1.4	1.8	2.4	A
		Option 2 (2A)	2.8	3.5	4.6	
		Option 3 (3A)	4.2	5.8	6.9	
LX2, LX4 Leakage Current		$V_{PV\_}$ = 5.5V, LX_ = PGND or PV, T_A = 25°C		1		µA
Negative Current-Limit Threshold				-1		A
Minimum On Time				48	68	ns
Maximum Duty Cycle					100	%
LX2, LX4 Discharge Resistance		Output disabled		47	100	Ω
Switching Phase				180		deg
Soft-Start Time				0.9		ms
OUT3 (BOOST)						
Voltage Accuracy	V_{OUT3}	I_{LOAD} = 0A to I_{MAX}	4.925	5	5.075	V
PMOS On-Resistance		I_{LX3} = 0.19A		125	250	mΩ
NMOS On-Resistance		I_{LX3} = 0.19A		65	130	mΩ

Electrical Characteristics (continued)

(V_{SUP} = V_{EN} = 13.5V, V_{OUT1} = V_{PV2} = V_{PV4} = 3.3V, V_{BIAS} = 5.0V, T_A = TJ = -40°C to +125°C unless otherwise noted, typical values are at T_A = 25°C under normal conditions unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
NMOS Current-Limit Threshold			1.4	2.1	2.7	A
PMOS Negative Current Limit				-500		mA
LX3 Leakage Current		OUT3 = 5.5 V, LX3 = PGND3 or OUT3, T_A = 25°C		1		µA
Maximum Duty Cycle				90		%
OUT3 Discharge Resistance		OUT3 Disabled		340		Ω
Switching Phase				30		deg
Soft-Start Time				1		ms
MD1-2						
Supply Voltage Range			6		36	V
High-Side Wetting Current		MD_ short to ground	10.2	13.6	17	mA
Low-Side Wetting Current		MD_ short to 13.5V	-10.2	-13.6	-17	mA
Input Low Comparator Threshold		9V ≤ V_{SUP} ≤ 16V	V_{SUP} x 0.35	V_{SUP} x 0.25	V_{SUP} x 0.15	V
Input High Comparator Threshold		9V ≤ V_{SUP} ≤ 16V	V_{SUP} x 0.65	V_{SUP} x 0.75	V_{SUP} x 0.85	V
Pullup Resistor			25	50	75	kΩ
Pulldown Resistor			25	50	75	kΩ
Open Voltage		Pin open, CONFIGM = 0x0F	V_{SUP} x 0.45	V_{SUP} x 0.50	V_{SUP} x 0.55	V
ANALOG (IN5, IN6)						
Input Current	$I_{IN\_}$	V_{IN5}/V_{IN6} = 1.8V, Set point programmed to 1.8V		20		µA
V_{IN} Programmable Range		12.5 mV increments	0.8		3.9875	V
OV/UV Accuracy		At OTP configured setpoint	-1		1	%
		Over full range when changing via I2C	-1.5		1.5	
OV Threshold				104		%
UV Threshold				96		%
Analog Delay Filter		10% below/above threshold		2	4	µs
OSCILLATOR						
Frequency	f_{SW}	Internally Generated	1.95	2.1	2.25	MHz
Spread Spectrum		CONFIG1.SSE = 1 (pseudo-random)		±3		%
THERMAL OVERLOAD						
Thermal Shutdown Temperature		T_J rising		175		°C

Electrical Characteristics (continued)

(V_{SUP} = V_{EN} = 13.5V, V_{OUT1} = V_{PV2} = V_{PV4} = 3.3V, V_{BIAS} = 5.0V, T_A = TJ = -40°C to +125°C unless otherwise noted, typical values are at T_A = 25°C under normal conditions unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Hysteresis				15		°C
RESET (OUT1-4)						
OV Threshold		Rising	103	104	105	%
UV Threshold		Falling	95	96	97	%
Active Hold Period	t_H	HT[1:0] = 00		9.8		ms
		HT[1:0] = 01		19.5		
		HT[1:0] = 10		29.3		
		HT[1:0] = 11		39.0		
Delay Filter		10% below/above threshold		2	4	µs
Output-High Leakage Current		T_A = 25°C		1		µA
Output Low Level		Sinking -2mA			0.2	V
EN						
Input High Level	V_{IH}		2.4			V
Input Low Level	V_{IL}				0.6	V
Pull-down				1		MΩ
SYNC INPUT						
Input High Level	V_{IH}		1.5			V
Input Low Level	V_{IL}				0.5	V
Input Hysteresis				0.1		V
SYNC Input Pull-down		EN high		100		kΩ
SYNC Input Frequency Range		50% duty cycle	1.5		3	MHz
FPS						
FPS Start Delay from SD1 Soft-Start Done	t_{FPSDLY}			2		µs
FPS Timeslot	t_{TS1}	TS = '00'		2.4		ms
	t_{TS2}	TS = '01'		4.9		
	t_{TS3}	TS = '10'		9.8		
	t_{TS4}	TS = '11'		19.5		
I^2C INTERFACE						
Input High Voltage	V_{IH}		1.2			V
Input Low Voltage	V_{IL}				0.5	V
Output Low Voltage	V_{OL}	ISINK = 4mA			0.4	V
Clock Frequency	f_{SCL}				1.1	MHz
Setup Time (Repeated) START	$t_{SU:STA}$		260			ns
Hold Time (Repeated) START	$t_{HD:STA}$		260			ns

Electrical Characteristics (continued)

(V_{SUP} = V_{EN} = 13.5V, V_{OUT1} = V_{PV2} = V_{PV4} = 3.3V, V_{BIAS} = 5.0V, T_A = TJ = -40°C to +125°C unless otherwise noted, typical values are at T_A = 25°C under normal conditions unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SCL Low Time	t_{LOW}			500			ns
SCL High Time	t_{HIGH}			260			ns
Data Setup Time	$t_{SU:DAT}$			50			ns
Data Hold Time	$t_{HD:DAT}$			0			ns
Setup Time for STOP Condition	$t_{SU:STO}$			260			ns
Spike Suppression					50		ns
Operating I/O Voltage Range				1.7		3.6	V
SCL/SDA Fall Time	t_f	Fast Mode (Note 3)				220	ns
		Fast Mode Plus (Note 3)				120	

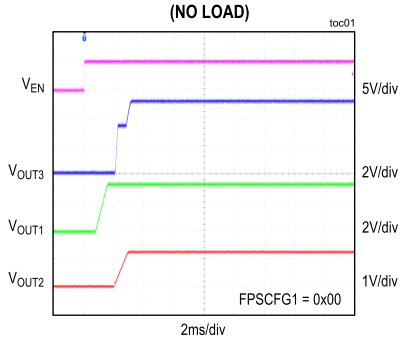
Note 2: Limits are 100% tested at TA = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.

Note 3: Not production tested. Guaranteed by design.

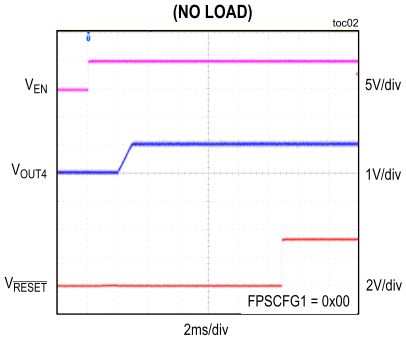
Typical Operating Characteristics

(V_{SUP} = EN = 13.5V. T_A = 25°C, unless otherwise noted.)

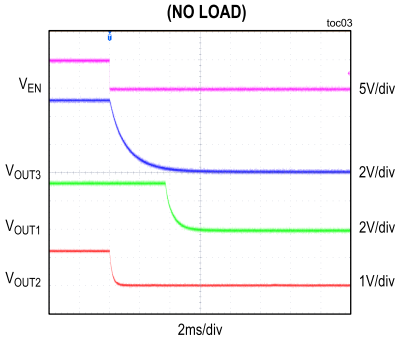
STARTUP WAVEFORM 1
(NO LOAD)



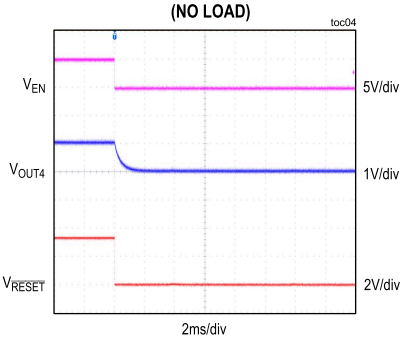
STARTUP WAVEFORM 2
(NO LOAD)



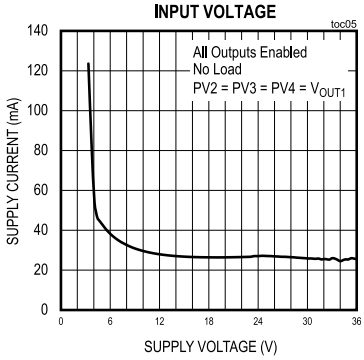
SHUTDOWN WAVEFORM 1
(NO LOAD)



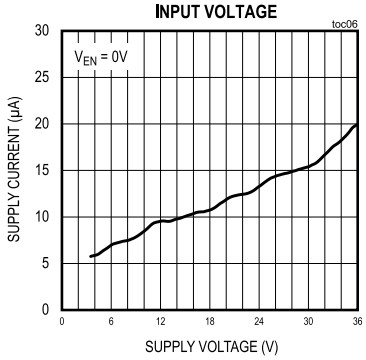
STARTUP WAVEFORM 2
(NO LOAD)



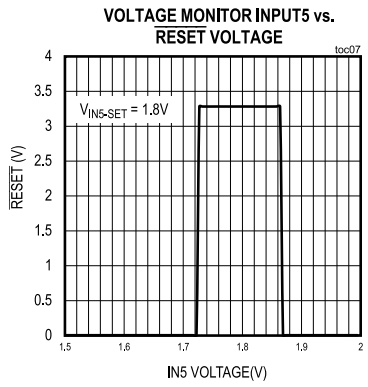
QUIESCENT CURRENT vs.
INPUT VOLTAGE



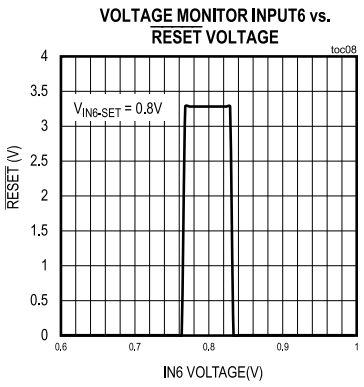
SHUTDOWN CURRENT vs.
INPUT VOLTAGE



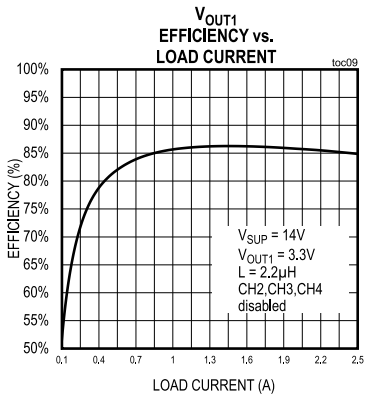
VOLTAGE MONITOR INPUT5 vs.
RESET VOLTAGE



VOLTAGE MONITOR INPUT6 vs.
RESET VOLTAGE



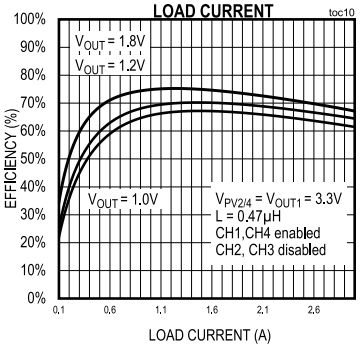
VOUT1
EFFICIENCY vs.
LOAD CURRENT



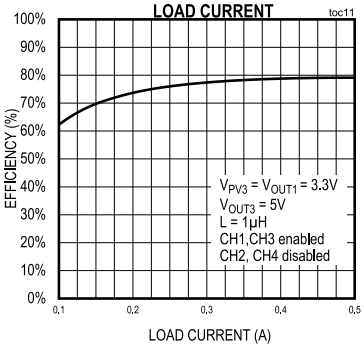
Typical Operating Characteristics (continued)

(V_{SUP} = EN = 13.5V. T_A = 25°C, unless otherwise noted.)

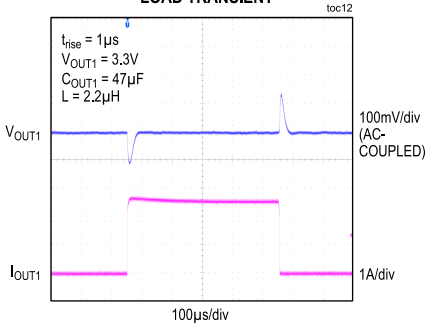
$V_{OUT2/4}$ SYSTEM EFFICIENCY vs. LOAD CURRENT



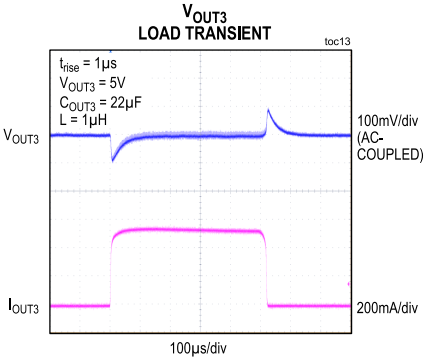
V_{OUT3} SYSTEM EFFICIENCY vs. LOAD CURRENT



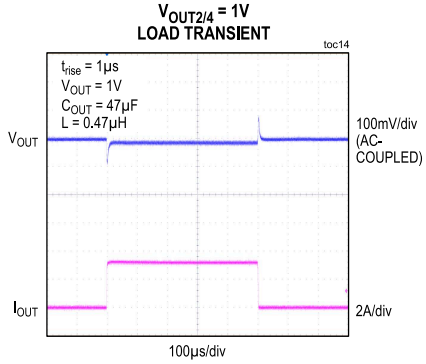
V_{OUT1} LOAD TRANSIENT



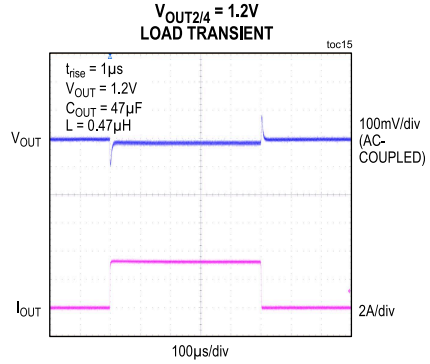
V_{OUT3} LOAD TRANSIENT



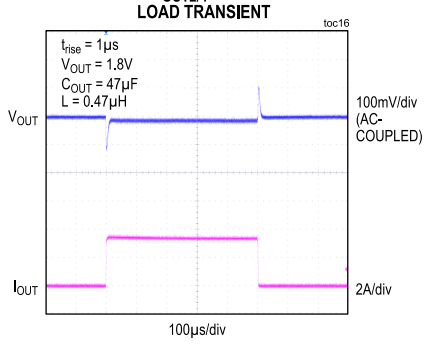
$V_{OUT2/4}$ = 1V LOAD TRANSIENT



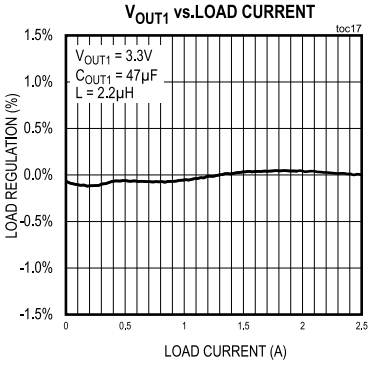
$V_{OUT2/4}$ = 1.2V LOAD TRANSIENT



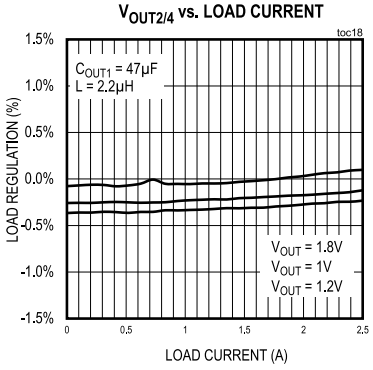
$V_{OUT2/4}$ = 1.8V LOAD TRANSIENT



LOAD REGULATION V_{OUT1} vs.LOAD CURRENT



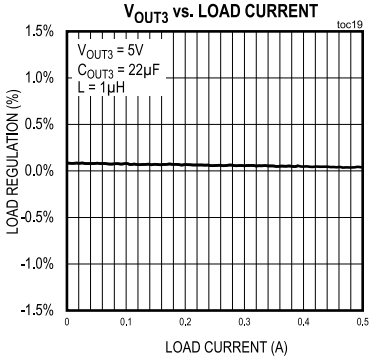
LOAD REGULATION $V_{OUT2/4}$ vs. LOAD CURRENT



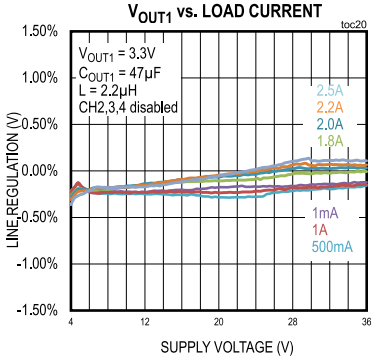
Typical Operating Characteristics (continued)

(V_{SUP} = EN = 13.5V. T_A = 25°C, unless otherwise noted.)

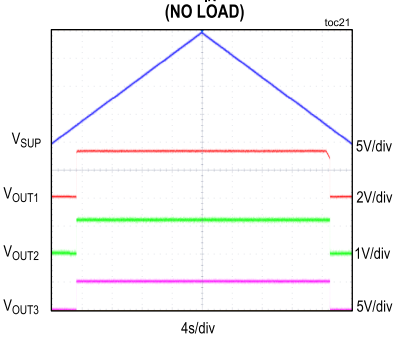
LOAD REGULATION
V_{OUT3} vs. LOAD CURRENT



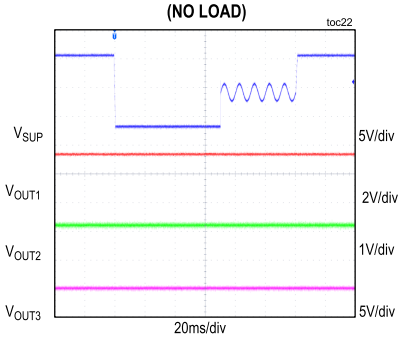
LINE REGULATION
V_{OUT1} vs. LOAD CURRENT



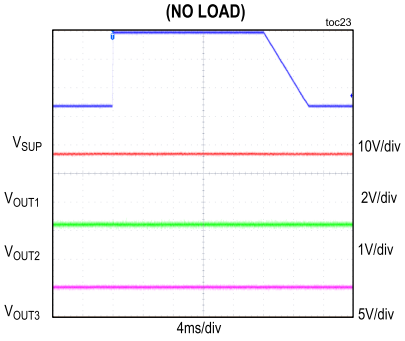
SLOW V_{IN} RAMP
(NO LOAD)



COLD CRANK
(NO LOAD)

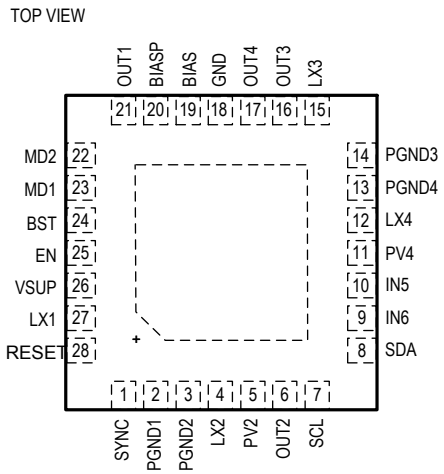


LOAD-DUMP TEST
(NO LOAD)



Pin Configuration

MAX20430



Pin Description

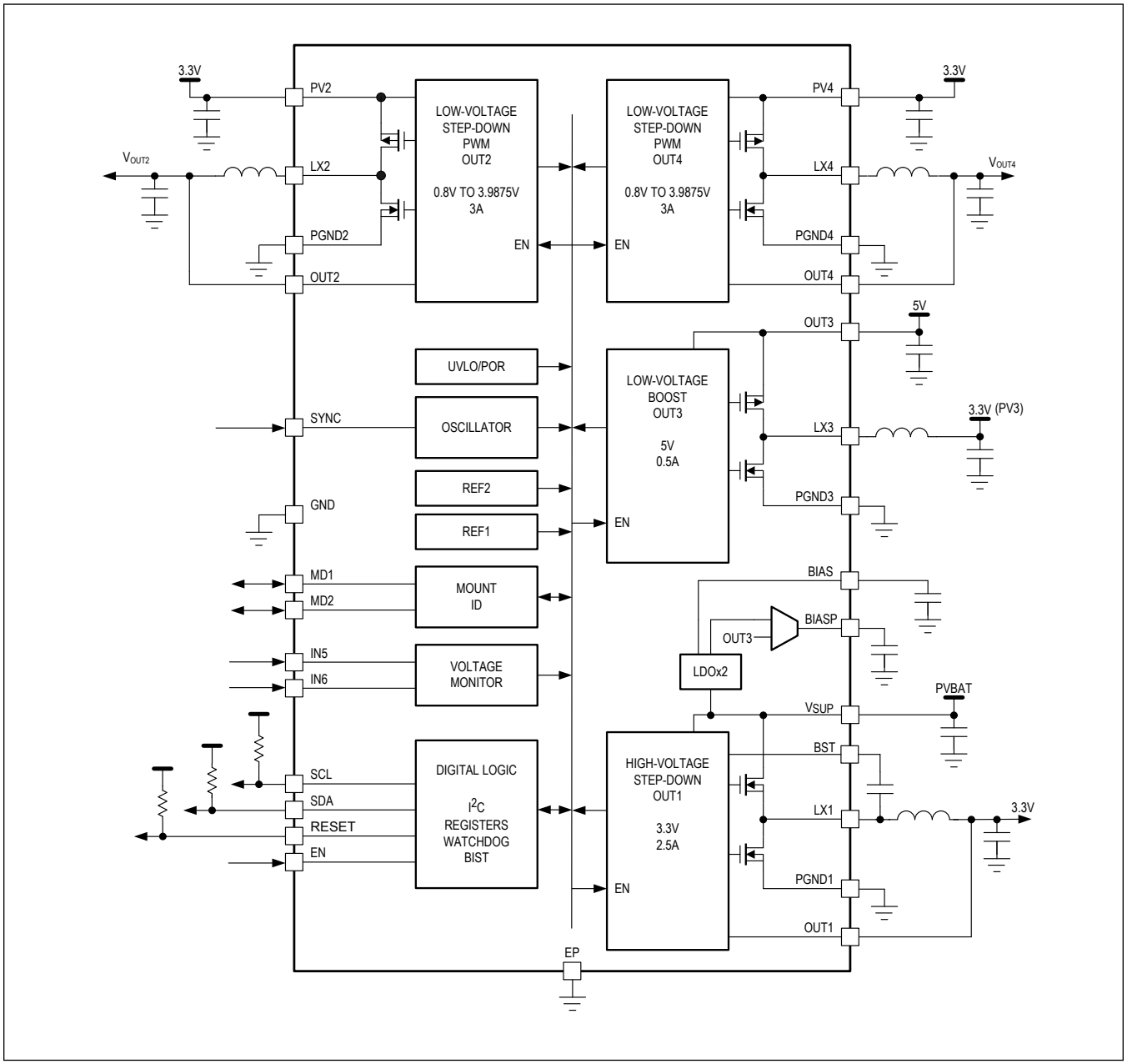
PIN	NAME	FUNCTION
1	SYNC	SYNC Input. Connect SYNC to BIAS for a 2.1MHz switching frequency. Connect SYNC to an external clock if a different switching frequency is required.
2	PGND1	Power Ground for OUT1. Connect all PGND pins together.
3	PGND2	Power Ground for OUT2. Connect all PGND pins together.
4	LX2	Inductor Connection for Channel 2. Connect LX2 to the switched side of the inductor.
5	PV2	OUT2 Power Supply Input. This must be connected to OUT1 and bypassed with a 4.7µF ceramic capacitor.
6	OUT2	OUT2 Voltage Sense Input
7	SCL	I^2C Clock Input
8	SDA	I^2C Data I/O
9	IN6	Voltage Monitor Input 6. Connect an external supply that is to be monitored to this input. The OV6/UV6 violation can be mapped to the $\overline{\text{RESET}}$ pin.
10	IN5	Voltage Monitor Input 5. Connect an external supply that is to be monitored to this input. The OV5/UV5 violation can be mapped to the $\overline{\text{RESET}}$ pin.
11	PV4	OUT4 Power Supply Input. This must be connected to OUT1 and bypassed with a 4.7µF ceramic capacitor.
12	LX4	Inductor Connection for Channel 4. Connect LX4 to the switched side of the inductor.
13	PGND4	Power Ground for OUT4. Connect all PGND pins together.
14	PGND3	Power Ground for OUT3. Connect all PGND pins together.
15	LX3	Inductor Connection for Channel 3. Connect LX3 to the switched side of the inductor.
16	OUT3	OUT3 Voltage Output

Pin Description (continued)

PIN	NAME	FUNCTION
17	OUT4	OUT4 Voltage-Sense Input
18	GND	Ground
19	BIAS	High voltage LDO output, regulates at 5V. Connect a 2.2uF ceramic capacitor from BIAS to GND.
20	BIASP	Noisy high voltage LDO output, regulates at 5V. Connect a 2.2µF ceramic capacitor from BIASP to GND. After boost converter finishes softstart, this pin connects to OUT3.
21	OUT1	OUT1 Voltage Sense Input
22	MD2	Mount ID Input 2
23	MD1	Mount ID Input 1
24	BST	Bootstrap Capacitor Connection. Connect a 0.1µF ceramic capacitor from BST to LX1.
25	EN	Active-High Enable Input. Drive EN HIGH for normal operation. The IC will power sequence all outputs as factory programmed.
26	V_{SUP}	IC Supply Input. Connect a 4.7µF or larger ceramic capacitor from V_{SUP} to PGND1.
27	LX1	Inductor Connection for Channel 1. Connect LX1 to the switched side of the inductor.
28	$\overline{RESET}$	Open-Drain Reset Output. This output remains low for the programmed hold time after all mapped outputs have reached their regulation level (see the Electrical Characteristics table). To obtain a logic signal, pull up $\overline{RESET}$ with an external resistor.
--	EP	Connect the exposed pad to the ground plane. This is the main path for thermal transfer.

Functional Diagrams

Functional Diagram 1



Detailed Description

The MAX20430 is a high-efficiency, four-output DC-DC converter and a windowed watchdog. OUT1 is a synchronous step-down converter that converts vehicle battery voltage to 3.3V at up to 2.5A. OUT3 boosts OUT1 to 5V at up to 500mA, while OUT2 and OUT4 low-voltage synchronous step-down converters operate from OUT1 and provide a 0.8V to 3.9875V output voltage range at up to 3A.

The programmable spread-spectrum frequency modulation minimizes radiated electromagnetic emissions. Integrated low R_{DSON} switches improve efficiency at heavy loads and make the layout much simpler with respect to discrete solutions.

Challenge/Response Watchdog and Reset Control

The challenge/response watchdog uses a linear feedback shift register (LFSR) to calculate the response to the current key. The MCU can read the current key at any time from the WDKEY register. The response must be written after t_{WD1} time expires and before t_{WD2} time expires. The timing of the open and close windows is programmable through the I^2C. Any valid watchdog refresh will terminate the open window and initialize the closed window.

Any assertion of $\overline{RESET}$ restarts the watchdog. Upon exiting the reset condition (when $\overline{RESET}$ de-asserts after the expiration of the hold timer), the update window is immediately opened and extended to allow the MCU time to boot before being required to update the watchdog. If the device is configured as a standard windowed watchdog (WDCDIV.SWW = 1) then writing any value to the WDKEY will result in a valid watchdog refresh signal, and the value written will be ignored.

There are three types of watchdog violations: WD_LFSR, WD_EXP, and WD_UV. If configured as a challenge/response watchdog, writing the incorrect response to the WDKEY register will result in the written value being ignored and an LFSR violation. Writing the correct response in challenge/response mode during an open window will result in a refresh and the WDKEY register being updated. Writing the correct response in challenge/response mode during a closed window will result in the write being ignored and a UV violation. Not refreshing the watchdog during the open window will result in an EXP violation.

If a watchdog violation is detected, the watchdog will assert $\overline{RESET}$, and re-start upon exiting the reset condition. The internal violation counter is reset only during power-on.

The watchdog is enabled when WD_EN bit is 1 and the $\overline{RESET}$ pin is de-asserted. The WD_LOCK bit must be set to 0 to configure or disable the watchdog to prevent unintended re-configuring of the watchdog.

When the watchdog is configured as a simple windowed watchdog, it can be refreshed by writing any value to the WDKEY register, though the written value will be ignored.

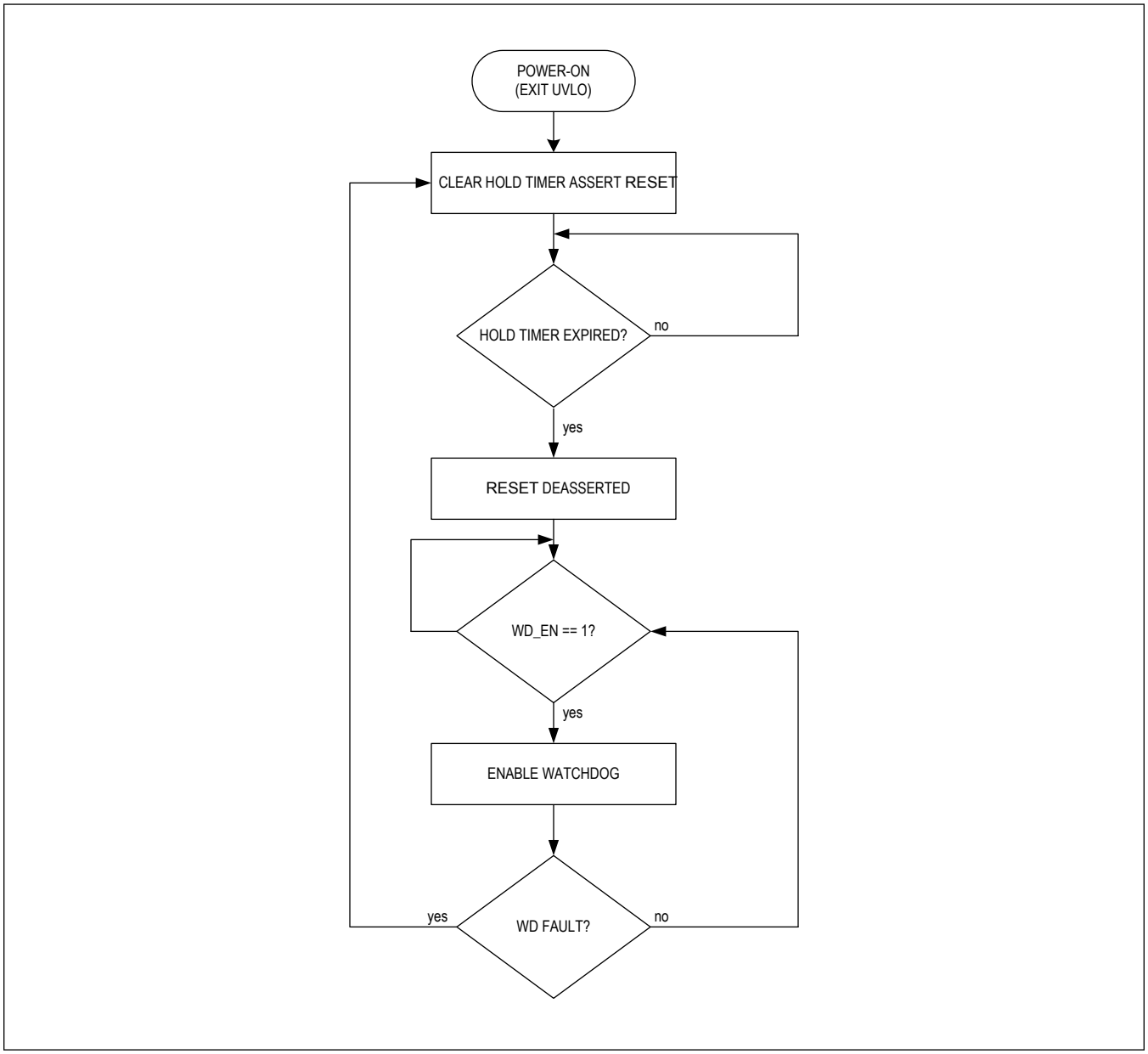


Figure 1. Watchdog Control

Flexible Power Sequencer (FPS)

When EN goes high, the device is powered on and the OUT1 channel is enabled. Once the OUT1 channel has reached a nominal voltage, the flexible power sequencer (FPS) power-up sequence begins. The time between power-up time slots is factory-selectable between values of 2.5ms (typ), 4.9ms (typ), 9.8ms (typ),and 19.5ms (typ). When the EN pin goes low, the device turns off.

A POR_RST event can re-initialize the FPS to the programmed time slots set in the PUx[1:0] registers. For this operation, the RSTMAP[6:1] bits must be cleared.

Flexible Power Sequencer Timing

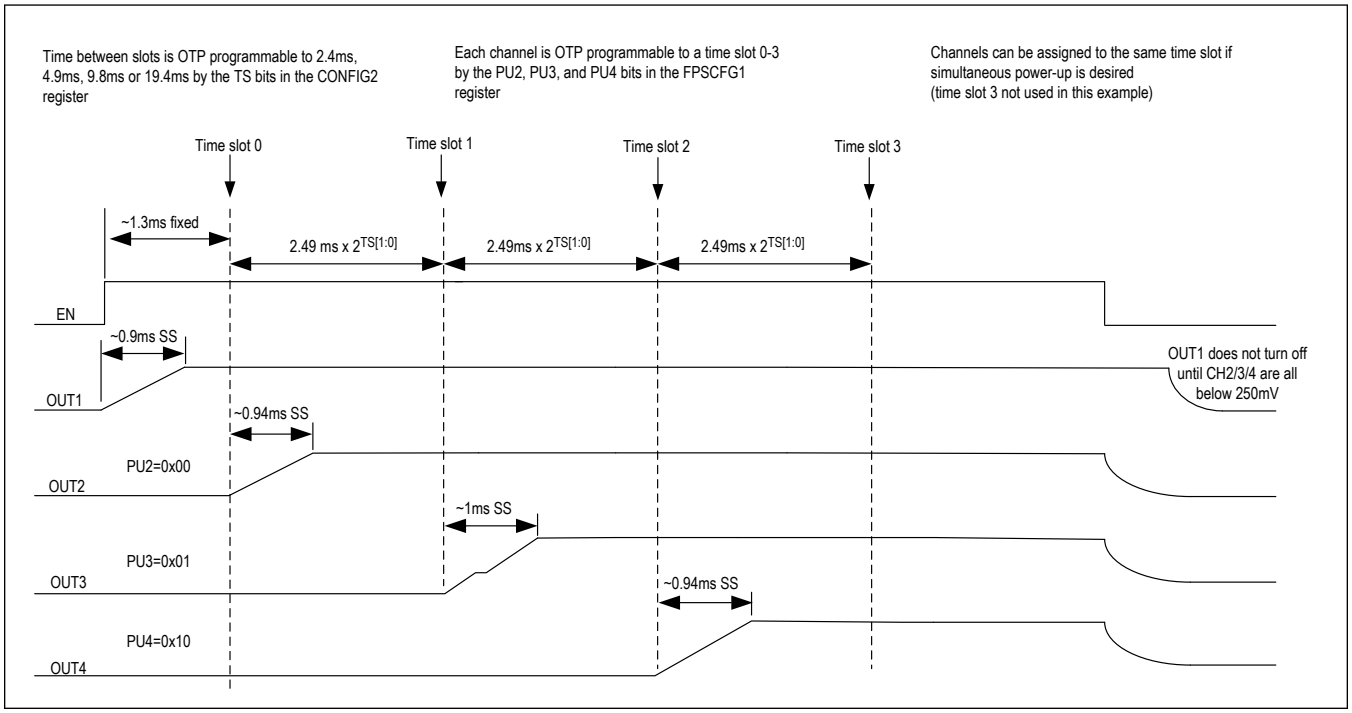


Figure 2. Flexible Power Sequencer (FPS) Timing

$\overline{\text{RESET}}$ Output

The device features an open-drain reset output that asserts low when the corresponding mapped output voltages are outside the UV/OV window, UVLO is asserted, or a watchdog violation occurs. $\overline{\text{RESET}}$ remains asserted for a fixed hold-timeout period after the mapped inputs rise to the regulated voltage. The fixed hold-timeout period is selectable with the HT[1:0] register bits as 9.8ms (typ), 19.5ms(typ), 29.3ms(typ), or 39ms(typ). To obtain a logic signal, place a pullup resistor between the $\overline{\text{RESET}}$ pin and the system I/O voltage. The source mapping to this pin is fully programmable.

Enable Input Pin (EN)

The EN pin is an active-high enable input. When the EN pin goes high, the four DC-DC converters power up in the programmed order. OUT1 must power up first since all other DC-DC converters are cascaded from OUT1. If the EN pin is brought low before the device has finished initializing, the device will stay on for up to 1ms (typ) while a shutdown is executed. The device can be kept enabled by setting the EN_HOLD bit to 1 in the CONFIG1 register. See Figure 3; EN_HOLD is cleared to 0 when the $\overline{\text{RESET}}$ pin is asserted to prevent the power supply from getting stuck on.

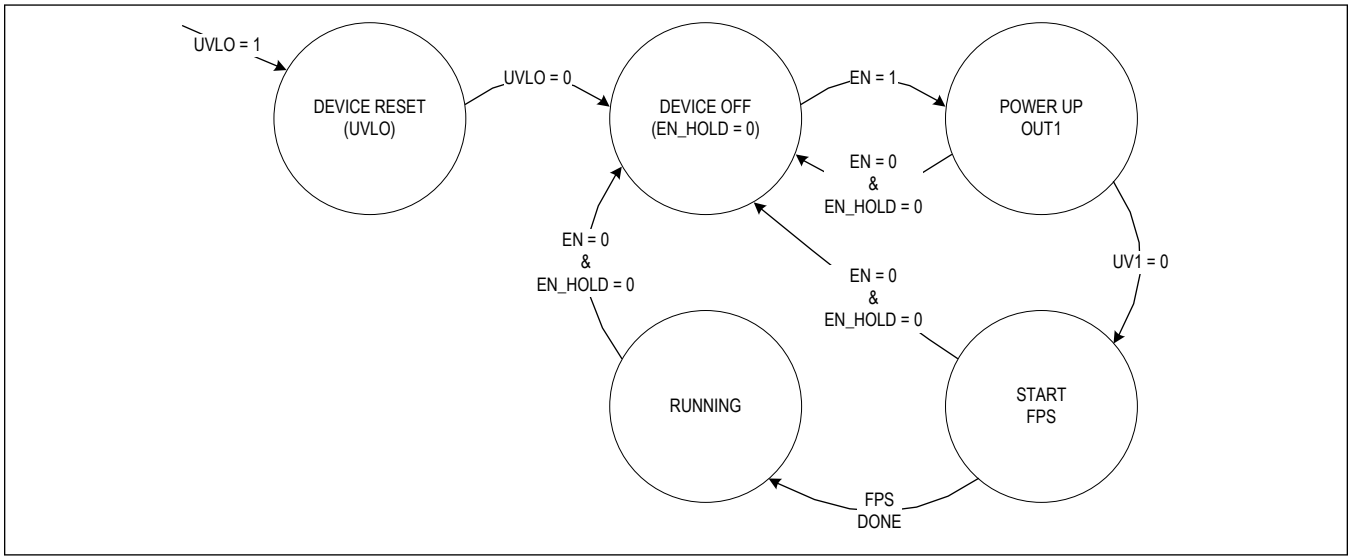


Figure 3. Power-On Control State Diagram

Mount ID Input Pins (MD1 , MD2)

The MD1 and MD2 inputs are used to identify the location of the module using the connector keying method. The MAX20430 provides a wetting current of 10mA (min). The pins handle loss of ground, which is indicated by -16V(min) on the connector pin.

The procedure for reading the state and setting the wetting current of the MD1 and MD2 pins is as follows:

1. After power-up, set CONFIGM to 0x0F, which will enable an internal resistor-divider on MD1/MD2 pins.
2. Read register STATM to determine the state.
3. Set the wetting current according to the state of each input, and disable the internal resistor-divider. For example, if MD1 is connected to ground, then enable the high-side wetting current.

To verify that the MD1 and MD2 input is functional, complete diagnostics as follows:

1. Set CONFIGM to 0x0F, which will enable an internal resistor-divider on the MD1/MD2 pins. If the MD1/MD2 pins are open circuit, the internal resistor-divider will hold the MD1/MD2 pins at mid-rail,(50% x V_{SUP}). Then read register STATM to verify that both MD1/MD2 pins are either high or low, and not mid-rail. A mid-rail MD1/MD2 pin indicates an open-circuit fault.
2. Set CONFIGM to 0x1F. Read the STATM register to verify that the MD2 comparator reports high and the MD1 comparator reports low.
3. Set CONFIGM to 0x2F. Read the STATM register to verify that the MD2 comparator reports low and the MD1 comparator reports high.
4. Set CONFIGM to 0x00 to disable the internal resistor-divider and complete the diagnostics.

Mount ID Diagram

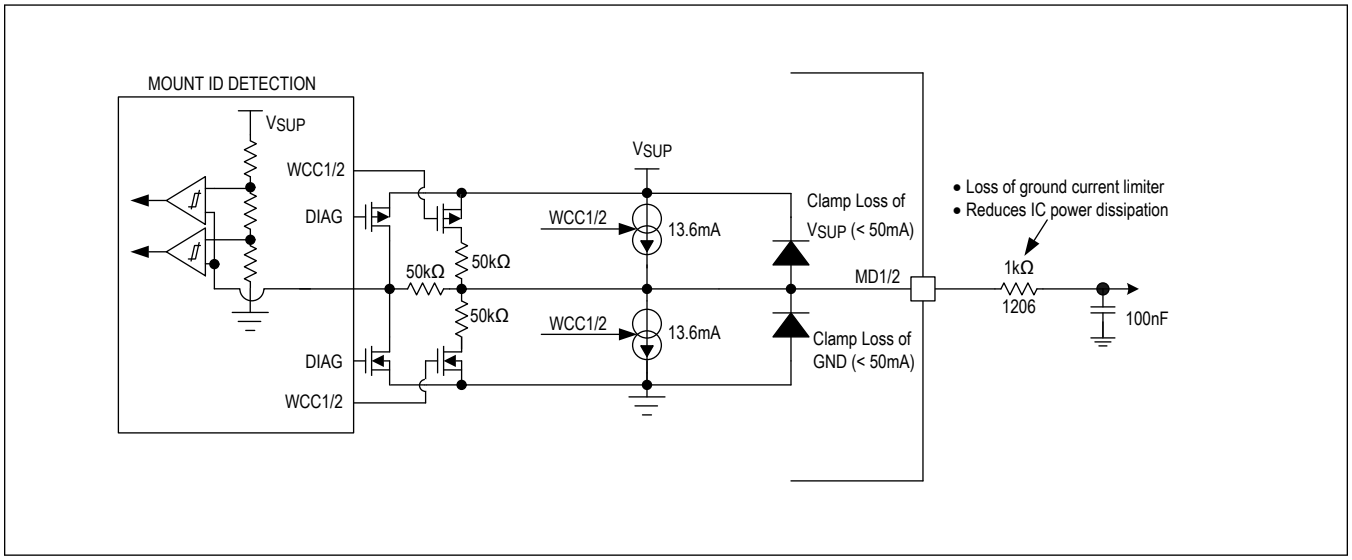


Figure 4. Mount ID Detection (One Channel Shown)

OFF Comparators

The MAX20430 includes an OFF comparator for each output voltage. The comparators assert if the output voltage drops below 0.25V (typ), and are tested for proper operation at power-on. If one of the comparators fails the BIST test, the INTERR bit is set and the comparator state can be read from the status register. The OFF comparators ensure that all outputs assigned to an FPS are discharged before the FPS power-up sequence is initiated.

OV Shutdown Comparators

The MAX20430 includes OV shutdown comparators for each output voltage. If one of the comparators is asserted, then the MAX20430 will turn off all outputs and trigger a UVLO event, reloading OTP and re-running BIST on the comparators. Once power is re-applied, the device powers up normally. If an output is overloaded and the overload is released, it is possible for the output to overshoot and trigger the OV shutdown. OV shutdown comparators are gated with the CONFIGE register, and have no effect on a disabled channel.

UV/OV Comparators

The MAX20430 includes a UV and OV comparator for each output voltage and the voltage on IN5/6. The comparators are tested for proper operation at power-on. If one of the comparators fails the BIST test, the INTERR bit is set in the STATD register. The comparators have a built-in programmable filter time that is controlled by CONFIG2.DF[3:0], which prevents small transients exceeding the UV or OV comparator from triggering a $\overline{\text{RESET}}$ event. This programmable digital filter allows an application-specific setting of filter time up to 28.6µs.

OV and UV comparators are not gated by the CONFIGE register and always report the status of the channel.

Internal Oscillator

The device has a spread-spectrum oscillator that varies the internal operating frequency up by ±3% relative to the internally generated operating frequency of 2.1MHz (typ). The spread frequency generated is psuedorandom with a repeat rate well below the audio band (< 20Hz). Spread spectrum is enabled when CONFIG1.SSE is set to 1.

Overtemperature Protection

Thermal overload protection limits the total power dissipation in the MAX20430. When the junction temperature exceeds 175°C, the device will immediately turn off all output channels and reset the FPS. Once the junction temperature cools by 15°C, the FPS will re-enable and start up according to the programmed sequence.

I²C Interface

The MAX20430 features an I²C, 2-wire serial interface consisting of a serial-data line (SDA) and a serial-clock line (SCL). SDA and SCL facilitate communication between the MAX20430 and the master at clock rates up to 1MHz. The master, typically a microcontroller, generates SCL and initiates data transfer on the bus. Figure 5 shows the 2-wire interface timing diagram.

A master device communicates to the MAX20430 by transmitting the proper address followed by the data word. Each transmit sequence is framed by a START (S) or REPEATED START (Sr) condition and a STOP (P) condition. Each word transmitted over the bus is 8 bits long and is always followed by an acknowledge clock pulse.

The MAX20430 SDA line operates as both an input and an open-drain output. The pullup resistor value on the SDA bus should be large enough to keep the open-drain pulldown current less than 4mA (max) to guarantee the MAX20430 can pull SDA below 0.4V. The MAX20430 SCL line operates as an input only. The SCL and SDA inputs suppress noise spikes to assure proper device operation, even on a noisy bus.

Timing Diagram

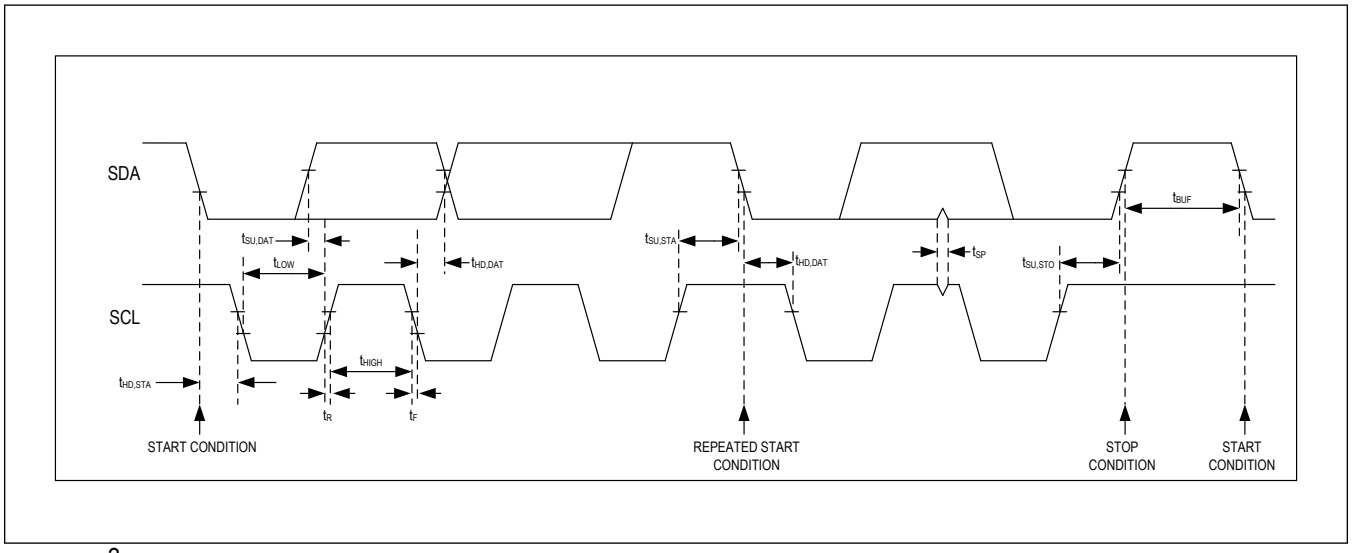


Figure 5. I²C Timing Diagram

Bit Transfer

One data bit is transferred during each SCL cycle. The data on SDA must remain stable during the high period of the SCL pulse. Changes in SDA while SCL is high are control signals (see the START and STOP Conditions section). SDA and SCL idle high when the I²C bus is not busy.

STOP and START Conditions

A master device initiates communication by issuing a START condition. A START condition is a high-to-low transition on SDA with SCL high. A STOP condition is a low-to-high transition on SDA while SCL is high (Figure 6). A START (S) condition from the master signals the beginning of a transmission to the MAX20430. The master terminates transmission and frees the bus by issuing a STOP (P) condition. The bus remains active if a REPEATED START (Sr) condition is

generated instead of a STOP condition.

START, STOP, and REPEATED START Conditions

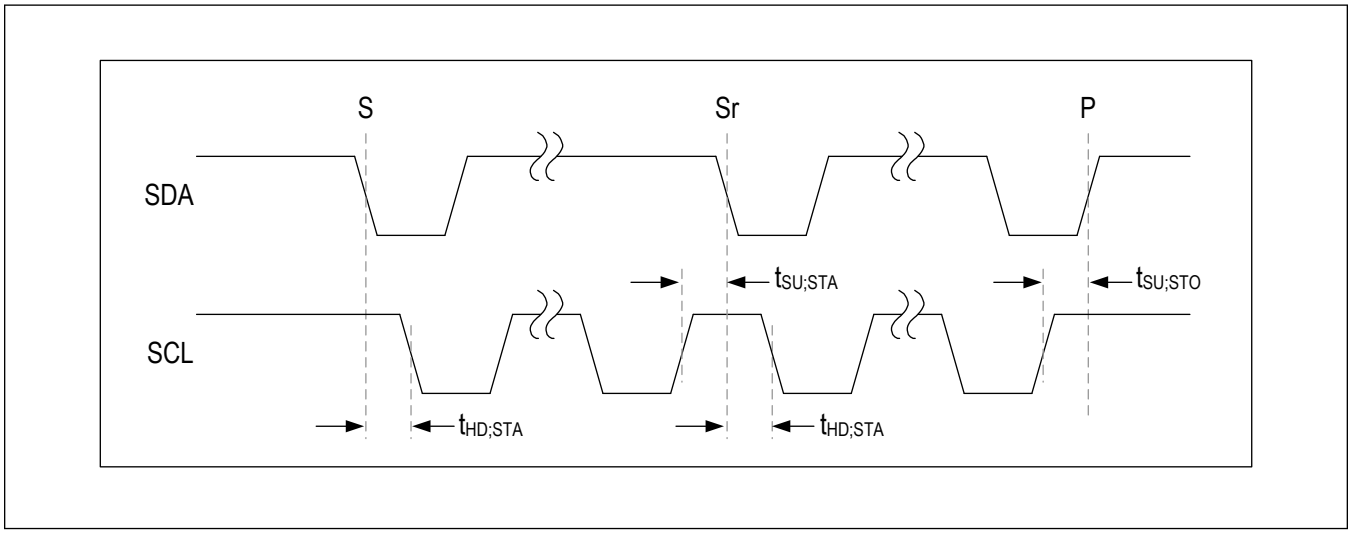


Figure 6. START, STOP, and REPEATED START Conditions

Early STOP Condition

The MAX20430 recognizes a STOP condition at any point during data transmission unless the STOP condition occurs in the same high pulse as a START condition.

Clock Stretching

In general, the clock signal generation for the I²C bus is the responsibility of the master device. The I²C specification allows slow slave devices to alter the clock signal by holding down the clock line, a process typically called clock stretching. The MAX20430 does not use any form of clock stretching to hold down the clock line.

I²C General Call Address

The MAX20430 does not implement the I²C specification's general call address. If the MAX20430 detects the general call address (0b0000_0000) it will not issue an acknowledge.

Packet Error Checking (PEC)

In order to increase fault coverage on the I²C interface, an optional packet error checking (PEC) byte is supported. This follows the SMBus implementation, which has a CRC-8 polynomial of $x^8 + x^2 + x + 1$. The PEC calculation does not include ACK, NACK, START, STOP, nor Repeated START bits. This means that the PEC is computed over the entire message from the first START condition. Only 1 byte can be written per I²C packet. Any data after the PEC byte will not be written.

If PEC is enabled (PECE = 1), the device will NACK an incorrect PEC byte and the written register data will be ignored.

Slave Address

The address is defined as the seven most significant bits (MSbs) followed by the R/W bit. Set the R/W bit to 1 to configure the device to read mode. Set the R/W bit to 0 to configure the device to write mode. The address is the first byte of information sent to the device after the START condition. The slave address is factory preset (see Ordering Information for the 7-bit address for each version). The factory-programmable I²C addresses are 0x38 through 0x3B.

Acknowledge

The acknowledge bit (ACK) is a clocked ninth bit that the device uses to handshake receipt of each data byte Figure 7. The device pulls down SDA during the master-generated ninth clock pulse. The SDA line must remain stable and low during the high period of the acknowledge clock pulse. Monitoring ACK allows for detection of unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master can reattempt communication.

If packet error checking (PEC) is enabled (PECE = 1), the device will NACK an incorrect PEC byte and the written register data will be ignored.

Acknowledge Condition

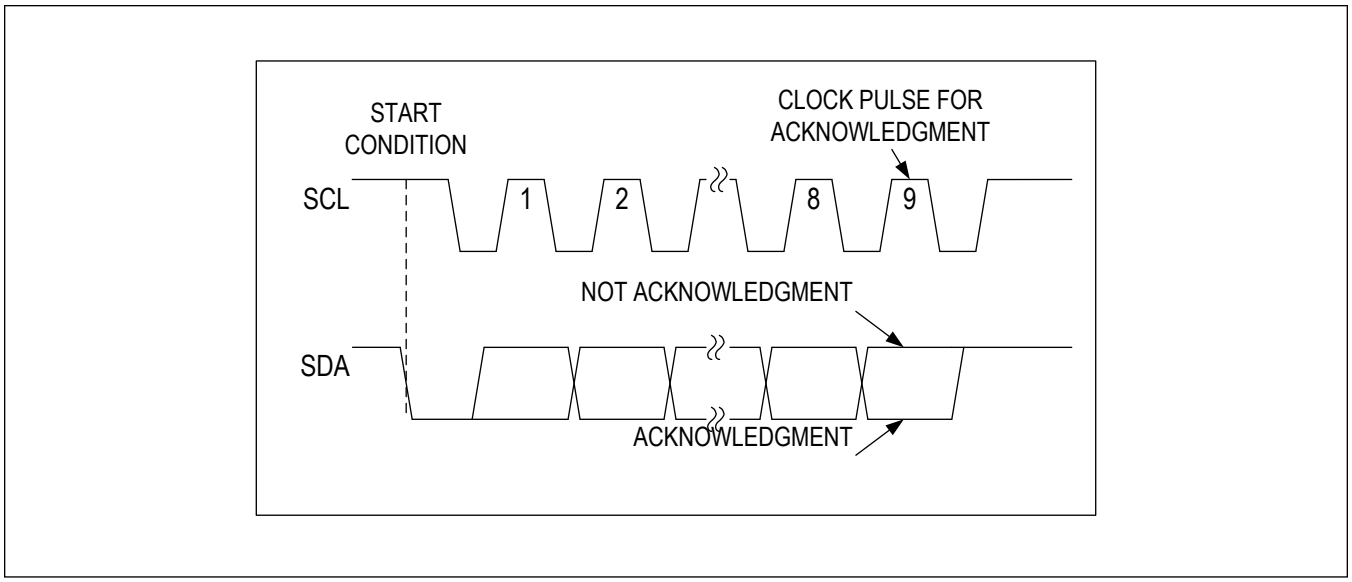


Figure 7. Acknowledge Condition

Write Data Format

A write to the device includes transmission of the following:

- START condition
- Slave address with the write bit set to 0
- 1 byte of data to register address
- 1 byte of data to the command register
- STOP condition

Figure 8 illustrates the proper format for one frame.

Read Data Format

A read from the device includes the following:

- Transmission of a START condition
- Slave address with the write bit set to 0
- 1 byte of data to register address
- Restart condition
- Slave address with read bit set to 1
- 1 byte of data to the command register
- STOP condition

Figure 8 illustrates the proper format for one frame.

Data Format of I²C Interface

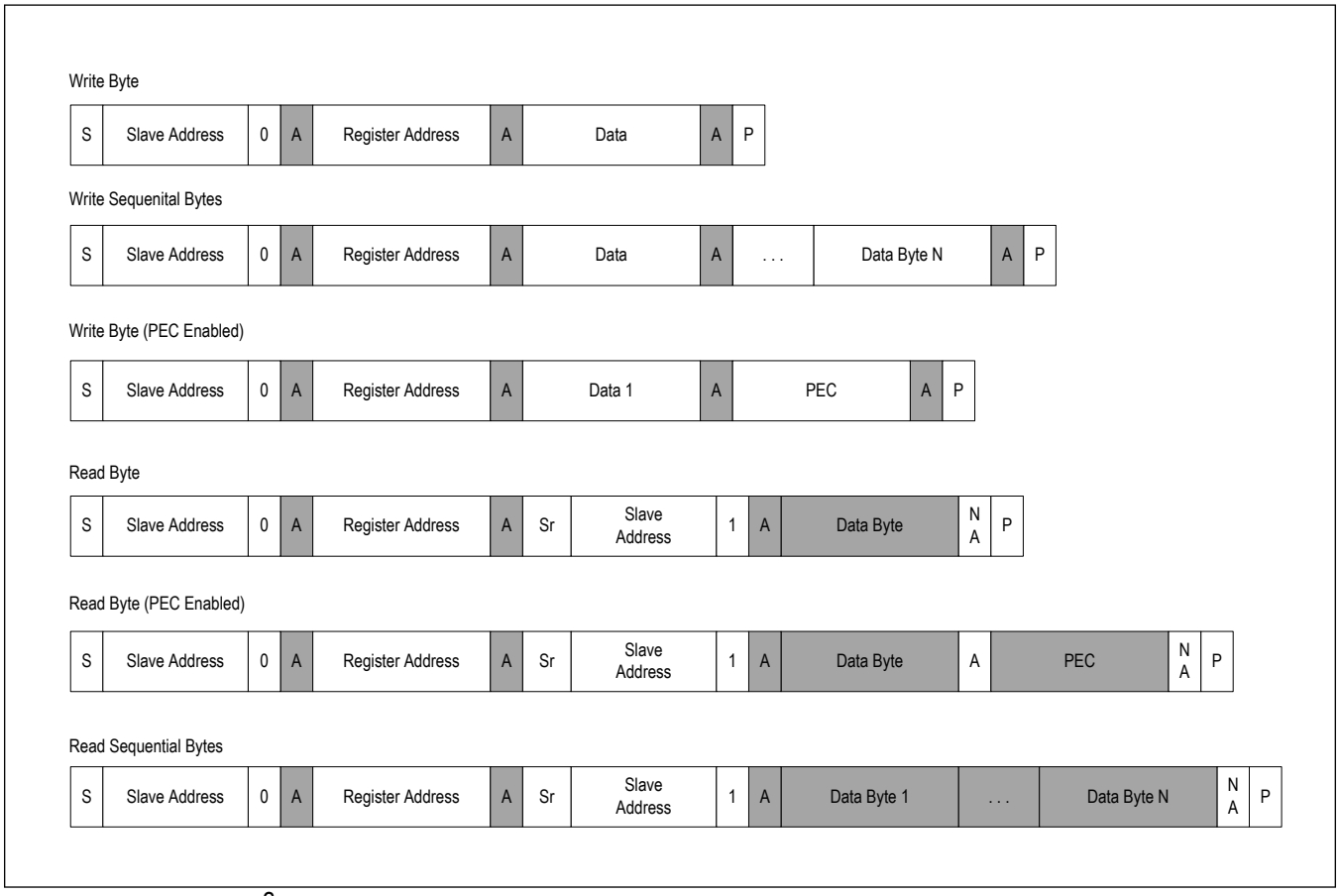


Figure 8. Data Format of I²C Interface

Register Map

USER

ADDRESS	NAME	MSB							LSB
USER_CMDS									
0x00	CID[7:0]	R[1:0]		ID[5:0]					
0x01	CONFIG1[7:0]	–	–	–	–	EN_HOLD	SSE	PROT	PECE
0x02	CONFIG2[7:0]	HT[1:0]		TS[1:0]		DF[3:0]			
0x03	CONFIGE[7:0]	–	–	–	–	EN[4:2]			–
0x04	CONFIGM[7:0]	–	–	DIAG[1:0]		WCC2[1:0]		WCC1[1:0]	
0x05	FPSCFG1[7:0]	PU4[1:0]		PU3[1:0]		PU2[1:0]		–	–
0x06	PORRST[7:0]	–	–	–	–	–	–	–	POR_RST
0x07	PINMAP1[7:0]	–	–	RSTMAP[6:1]					
0x08	STATUV[7:0]	–	–	UV[6:1]					
0x09	STATOV[7:0]	–	–	OV[6:1]					
0x0A	STATOFF[7:0]	–	–	OFF[6:1]					
0x0B	STATD[7:0]	–	–	–	RSTERR	POR	–	THSD	INTERR
0x0C	STATM[7:0]	–	–	–	–	MD2H	MD2L	MD1H	MD1L
0x0D	STATWD[7:0]	–	–	–	RESETB_STAT	WD_OPEN	WD_LFSR	WD_UV	WD_EXP
0x0E	VOUT2[7:0]	OUT2[7:0]							
0x0F	VOUT4[7:0]	OUT4[7:0]							
0x10	VIN5[7:0]	IN5[7:0]							
0x11	VIN6[7:0]	IN6[7:0]							
0x12	WDCDIV[7:0]	–	WD_SWW	WD_DIV[5:0]					
0x13	WDCFG1[7:0]	WD_OPN[3:0]				WD_CLO[3:0]			
0x14	WDCFG2[7:0]	–	–	–	–	WD_EN	WD_1UD[2:0]		
0x15	WDKEY[7:0]	WD_KEY[7:0]							
0x16	WDPROT[7:0]	–	–	–	–	–	–	–	WD_PROT

Register Details

CID (0x0)

BIT	7	6	5	4	3	2	1	0
Field	R[1:0]		ID[5:0]					
Reset	0b00							
Access Type	Read Only		Write, Read, Ext					

BITFIELD	BITS	DESCRIPTION	DECODE
R	7:6	Silicon Revision Information	00 = Pass 1 Silicon 01 = Pass 2 Silicon 10 = Pass 3 Silicon 11 = Pass 4 Silicon
ID	5:0	Chip Configuration Identification. This is a unique number identifying the factory configuration of the device. This helps identify/verify the configuration without having to look at all configuration registers.	See ordering information.

CONFIG1 (0x1)

Configuration Register 1 (Read/Write)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	EN_HOLD	SSE	PROT	PECE
Reset	–	–	–	–	OTP	OTP	OTP	OTP
Access Type	–	–	–	–	Write, Read, Ext	Write, Read	Write, Read, Ext	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
EN_HOLD	3	Enable Hold. Overrides the EN pin to keep the device enabled. This bit is cleared when RESETB is asserted.	0 = EN pin controls power down 1 = Device enabled. Ignores EN pin state
SSE	2	Spread Spectrum Enable.	0 = Disabled 1 = Enabled
PROT	1	Lock Protection. If this bit is set to 1 by factory default, then it can't be cleared. If 0 by default, then this bit can be changed through the I^2C.	0 = All registers can be written. 1 = Writes are ignored to protected registers.
PECE	0	Packet Error Checking Enable. Set this bit to a 1 to enable PEC or 0 to disable PEC.	0 = Disabled. 1 = Enabled.

CONFIG2 (0x2)

Configuration Register 2 (Read/Write, Protected: writeable when LOCK = 0)

BIT	7	6	5	4	3	2	1	0
Field	HT[1:0]		TS[1:0]		DF[3:0]			
Reset	OTP		OTP		OTP			
Access Type	Write, Read		Write, Read		Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
HT	7:6	RESET Hold Time Selection. This is the amount of time that the RESET pin is active (low) after the event that caused the RESET pin to activate is removed.	00 = 9.8ms 01 = 19.5ms 10 = 29.3ms 11 = 39ms
TS	5:4	Time Slot Time. These bits define the time between timeslots.	00 = 2.4ms 01 = 4.9ms 10 = 9.8ms 11 = 19.5ms
DF	3:0	OV/UV Digital Filter. Adds additional filtering to all OV/UV comparators.	Added Filter Time = DF[3:0] x 1.9µs (±1µs nom)

CONFIGE (0x3)

Channel Enable Configuration Register (Read/Write, Protected: writeable when LOCK = 0)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	EN[4:2]			–
Reset	–	–	–	–	OTP			–
Access Type	–	–	–	–	Write, Read			–

BITFIELD	BITS	DESCRIPTION	DECODE
EN	3:1	Main Output Enable for OUT2(EN2), OUT3(EN3), and OUT4(EN4). When an output is enabled, the FPS will control when the output is on or off.	0 = Output Disabled 1 = Output Enabled

CONFIGM (0x4)

Mount ID Configuration Register (Read/Write)

BIT	7	6	5	4	3	2	1	0
Field	–	–	DIAG[1:0]		WCC2[1:0]		WCC1[1:0]	
Reset	–	–	OTP		OTP		OTP	
Access Type	–	–	Write, Read		Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
DIAG	5:4	Mount ID Diagnostics. After setting the diagnostic mode, read the STATM register to check the comparator state.	00 = Normal mode 01 = Short MD1 comparator inputs to ground and MD2 comparator inputs to V_{SUP} 10 = Short MD1 comparator inputs to V_{SUP} and MD2 comparator inputs to GND 11 = Reserved
WCC2	3:2	Mount ID 2 Control. Sets the mode of the MD2 pin. The STATM should be read when WC2 is set to 11 to ensure a correct reading.	00 = Wetting current and resistor divider disabled 01 = Low-side wetting current enabled and resistor divider disabled 10 = High-side wetting current enabled and resistor divider disabled 11 = Resistor-divider enabled and wetting current disabled
WCC1	1:0	Mount ID 1 Control. Sets the mode of the MD1 pin. The STATM should be read when WC1 is set to 11 to ensure a correct reading.	00 = Wetting current and resistor divider disabled 01 = Low-side wetting current enabled and resistor divider disabled 10 = High-side wetting current enabled and resistor divider disabled 11 = Resistor-divider enabled and wetting current disabled

FPSCFG1 (0x5)

Flexible Power Sequencer Configuration Register 1 (Read/Write, Protected: writeable when LOCK = 0)

BIT	7	6	5	4	3	2	1	0
Field	PU4[1:0]		PU3[1:0]		PU2[1:0]		–	–
Reset	OTP		OTP		OTP		–	–
Access Type	Write, Read		Write, Read		Write, Read		–	–

BITFIELD	BITS	DESCRIPTION	DECODE
PU4	7:6	OUT4 Power-Up Time Slot. OUT4 powers up in time slot set by PU4[1:0].	t_{PU4} = PU4[1:0] x 2.44 x ($2^{TS[1:0]}$) ms
PU3	5:4	OUT3 Power-Up Time Slot. OUT3 powers up in time slot set by PU3[1:0].	t_{PU3} = PU3[1:0] x 2.44 x ($2^{TS[1:0]}$) ms
PU2	3:2	OUT2 Power-Up Time Slot. OUT2 powers up in time slot set by PU2[1:0].	t_{PU2} = PU2[1:0] x 2.44 x ($2^{TS[1:0]}$) ms

PORRST (0x6)

Power On Reset Emulation Register (Read/Write, Protected: writeable when LOCK = 0)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	POR_RST
Reset	–	–	–	–	–	–	–	0x0
Access Type	–	–	–	–	–	–	–	Write, Read, Ext

BITFIELD	BITS	DESCRIPTION	DECODE
POR_RST	0	The POR_RST bit emulates a power-on-reset condition, re-initlaizing the FPS sequence and watchdog while retaining programmed register values and performing comparator BIST. OTP CRC calculation is not performed when executing this command. This bit is self-clearing, and cannot be written when LOCK = 1.	0 = No Effect 1 = Initialze POR Emulation

PINMAP1 (0x7)

RESETB Pin Mapping Register (Read/Write, Protected: writeable when LOCK = 0)

BIT	7	6	5	4	3	2	1	0
Field	–	–	RSTMAP[6:1]					
Reset	–	–	OTP					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
RSTMAP	5:0	RESETB Pin Mapping for OUT1(RSTMAP1), OUT2(RSTMAP2), OUT3(RSTMAP3), OUT4(RSTMAP4), IN5(RSTMAP5), and IN6 (RSTMAP6). Defines which voltage monitors are mapped to the RESETB pin.	0 = OV[x] and UV[x] not mapped to RESETB pin 1 = OV[x] and UV[x] are mapped to RESETB pin

STATUV (0x8)

UV Comparator Status Register (Read Clear)

BIT	7	6	5	4	3	2	1	0
Field	–	–	UV[6:1]					
Reset	–	–	0x0					
Access Type	–	–	Read Clears All					

BITFIELD	BITS	DESCRIPTION	DECODE
UV	5:0	UV Comparator Status for OUT1 (UV1), OUT2 (UV2), OUT3 (UV3), OUT4 (UV4), IN5 (UV5), IN6 UV6)	0 = UV[x] is above UV threshold 1 = UV[x] below UV threshold (or passed BIST when exiting POR)

STATOV (0x9)

OV Comparator Status Register (Read Clear)

BIT	7	6	5	4	3	2	1	0
Field	–	–	OV[6:1]					
Reset	–	–	0x0					
Access Type	–	–	Read Clears All					

BITFIELD	BITS	DESCRIPTION	DECODE
OV	5:0	OV Comparator Status for OUT1 (OV1), OUT2 (OV2), OUT3 (OV3), OUT4 (OV4), IN5 (OV5), IN6 OV6)	0 = OV[x] is below OV threshold 1 = OV[x] above OV threshold (or passed BIST when exiting POR)

STATOFF (0xA)

OFF Comparator Status Register (Read Clear)

BIT	7	6	5	4	3	2	1	0
Field	–	–	OFF[6:1]					
Reset	–	–	0x0					
Access Type	–	–	Read Clears All					

BITFIELD	BITS	DESCRIPTION	DECODE
OFF	5:0	OFF Comparator Status for OUT1 (OFF1), OUT2 (OFF2), OUT3 (OFF3), OUT4 (OFF4), IN5 (OFF5), IN6 (OFF6)	0 = OFF[x] is above OFF threshold 1 = OFF[x] is below OFF threshold (or passed BIST when exiting POR)

STATD (0xB)

Diagnostic Status Register (Read Only, Read Clear)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	RSTERR	POR	–	THSD	INTERR
Reset	–	–	–	0x0		–		
Access Type	–	–	–	Read Clears All	Read Clears All	–	Read Clears All	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
RSTERR	4	RESETB Fault. The RESETB pin state is latched into this register when deasserting RESETB.	0 = No fault detected 1 = Short to supply detected during BIST
POR	3	Power On Reset. Indicates if the device just exited power on reset.	0 = No POR occurred since last read 1 = A POR has occurred since the last read This indicates that all BIST information is available in the status registers
THSD	1	Thermal Shutdown Indication	0 = No thermal shutdown 1 = Thermal shutdown has occurred since last read

BITFIELD	BITS	DESCRIPTION	DECODE
INTERR	0	Internal Error	0 = No internal error detected 1 = Internal error detected (OTP CRC failure, OV/UV comparator test failure)

STATM (0xC)

Mount ID Status Register (Read Only)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	MD2H	MD2L	MD1H	MD1L
Reset	–	–	–	–	0x0	0x0	0x0	0x0
Access Type	–	–	–	–	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
MD2H	3	Mount ID 2 High Comparator Input Real-Time Status. **Note:** The WCC2 bits must be set to 11 for this status bit to be valid.	0 = Input is below the threshold 1 = Input is above the threshold
MD2L	2	Mount ID 2 Low Comparator Input Real-Time Status. **Note:** The WCC2 bits must be set to 11 for this status bit to be valid.	0 = Input is below the threshold 1 = Input is above the threshold
MD1H	1	Mount ID 1 High Comparator Input Real-Time Status. **Note:** The WCC1 bits must be set to 11 for this status bit to be valid.	0 = Input is below the threshold 1 = Input is above the threshold
MD1L	0	Mount ID 1 Low Comparator Input Real-Time Status. **Note:** The WCC1 bits must be set to 11 for this status bit to be valid.	0 = Input is below the threshold 1 = Input is above the threshold

STATWD (0xD)

Watchdog Status Register (Read Only, Read Clear). When the watchdog is enabled, these status bits are mapped to the RESET pin and are not maskable.

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	RESETB_STAT	WD_OPEN	WD_LFSR	WD_UV	WD_EXP
Reset	–	–	–	0x0	0x0	0x0	0x0	0x0
Access Type	–	–	–	Read Only	Read Only	Read Clears All	Read Clears All	Read Clears All

BITFIELD	BITS	DESCRIPTION	DECODE
RESETB_STAT	4	RESETB Pin State. Allows verification of the state of the RESETB pin. This is the real-time RESETB pin state.	0 = RESETB is low 1 = RESETB is high
WD_OPEN	3	Watchdog Open Window. This bit indicates that it is permissable to update the watchdog. This bit shows real-time status.	0 = Watchdog update not open 1 = Watchdog ok to update
WD_LFSR	2	LFSR Write Mismatch. The MCU/SoC did not write the correct value to the WDKEY register.	0 = LFSR key match 1 = LFSR key mismatch since last read

BITFIELD	BITS	DESCRIPTION	DECODE
WD_UV	1	Watchdog Update Violation. The MCU/SoC wrote to the WDKEY register before t_{wd1} expired.	0 = No violation detected 1 = Watchdog updated too early
WD_EXP	0	Watchdog Open Window Expired. The MCU/SoC did not write to the WDKEY register before t_{wd2} expired.	0 = Watchdog timer not expired 1 = Watchdog timer expired

VOUT2 (0xE)

OUT2 Output Voltage Register (Read/Write, Protected: writeable when LOCK = 0)

BIT	7	6	5	4	3	2	1	0
Field	OUT2[7:0]							
Reset	OTP							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
OUT2	7:0	OUT2 Voltage Setting	V_{OUT2} = OUT2[7:0] x 12.5mV + 0.800V (0.8V to 3.9875V)

VOUT4 (0xF)

OUT4 Output Voltage Register (Read/Write, Protected: writeable when LOCK = 0)

BIT	7	6	5	4	3	2	1	0
Field	OUT4[7:0]							
Reset	OTP							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
OUT4	7:0	OUT4 Voltage Setting	V_{OUT4} = OUT4[7:0] x 12.5mV + 0.800V (0.8V to 3.9875V)

VIN5 (0x10)

IN5 Input Voltage Monitor Register (Read/Write, Protected: writeable when LOCK = 0)

BIT	7	6	5	4	3	2	1	0
Field	IN5[7:0]							
Reset	OTP							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
IN5	7:0	Input 5 Voltage Monitor Setting	V_{IN5} = IN5[7:0] x 12.5mV + 0.800V (0.8V to 3.9875V)

VIN6 (0x11)

IN6 Input Voltage Monitor Register (Read/Write, Protected: writeable when LOCK = 0)

BIT	7	6	5	4	3	2	1	0
Field	IN6[7:0]							
Reset	OTP							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
IN6	7:0	Input 6 Voltage Monitor Setting	V_{IN6} = IN6[7:0] x 12.5mV + 0.800V (0.8V to 3.9875V)

WDCDIV (0x12)

Watchdog Clock Divider Register (Read/Write, Protected: writeable when WDLOCK = 0)

** If the watchdog is enabled this register should only be updated once before the first watchdog update after exiting RESET to prevent a possible watchdog violation.

BIT	7	6	5	4	3	2	1	0
Field	–	WD_SWW	WD_DIV[5:0]					
Reset	–	OTP	OTP					
Access Type	–	Write, Read	Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
WD_SWW	6	Simple Windowed Watchdog Enable	0 = Challenge/response watchdog enabled 1 = Standard windowed watchdog enabled
WD_DIV	5:0	Watchdog Clock Divider	t_{WDCLK} = (WD_DIV[5:0]+1) x 121.905µs

WDCFG1 (0x13)

Watchdog Configuration Register 1 (Read/Write, Protected: writeable when WDLOCK = 0)

** If the watchdog is enabled this register should only be updated immediately following a refresh to prevent a possible watchdog violation.

BIT	7	6	5	4	3	2	1	0
Field	WD_OPN[3:0]				WD_CLO[3:0]			
Reset	OTP				OTP			
Access Type	Write, Read				Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
WD_OPN	7:4	Watchdog Open Window. Sets the number of watchdog clock cycles before the open window starts.	t_{WD1} = t_{WDCLK} x (WD_OPN[3:0]+1) x 8
WD_CLO	3:0	Watchdog Close Window. Sets the number of watchdog clock cycles before the close window starts.	t_{WD2} = t_{WD1} + t_{WDCLK} x (WD_CLO[3:0]+1) x 8

WDCFG2 (0x14)

Watchdog Configuration Register 2 (Read/Write, Protected: writeable when WDLOCK = 0)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	WD_EN	WD_1UD[2:0]		
Reset	–	–	–	–	OTP	OTP		
Access Type	–	–	–	–	Write, Read	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
WD_EN	3	Watchdog Enable	0 = Disabled 1 = Enabled
WD_1UD	2:0	First Update Extension. Sets the number of extra t_{WD2} cycles after POR to the normal t_{WD2}.	$t_{1STWD2} = t_{WD2}$ x (WD_1UD[2:0] + 1)

WDKEY (0x15)

Watchdog Key Register (Read/Write)

BIT	7	6	5	4	3	2	1	0
Field	WD_KEY[7:0]							
Reset	0xAA							
Access Type	Write, Read, Ext							

BITFIELD	BITS	DESCRIPTION
WD_KEY	7:0	Watchdog Key. The current key can be read from this register. To update the watchdog, the next value in the sequence must be written to this register. If configured as a simple windowed watchdog, writing any value to the WDKEY register will refresh the watchdog and the value written will be ignored. If configured as a challenge/response watchdog, writing the incorrect response to the WDKEY register will result in the value written being ignored and a WD_LFSR violation. Writing the correct response in challenge/response mode during an open window will result in a refresh and the WDKEY register being updated. Writing the correct response in challenge/response mode during a closed window will result in the write being ignored and a WD_UV violation. LFSR polynomial: $x^8 + x^6 + x^5 + x^4 + 1$

WDPROT (0x16)

Watchdog Lock Protect Register (Read/Write)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	WD_PROT
Reset	–	–	–	–	–	–	–	0x0
Access Type	–	–	–	–	–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
WD_PROT	0	Watchdog Lock Protection	0 = Watchdog configuration registers are writeable 1 = Watchdog configuration registers are read-only

Applications Information

Input Capacitors

The input-bypass filter capacitors reduce peak currents drawn from the power source, as well as noise and voltage ripple on the input caused by the circuit's switching. A 4.7µF X7R ceramic capacitor is recommended for V_{SUP}, PV2, PV4, and for the input of the boost converter. See Typical Application Circuit for reference.

Inductor Selection

The MAX20430 design is optimized to be used with inductor values shown in Table 1. The saturation current rating should be higher than the peak current limit (max) for the respective converter. See the Typical Application Circuit for reference.

Table 1. Inductor Selection

INDUCTOR	VALUE	UNIT
L1	2.2	µH
L2	0.47 - 0.68	µH
L3	1.0	µH
L4	0.47 - 0.68	µH

Output Capacitors

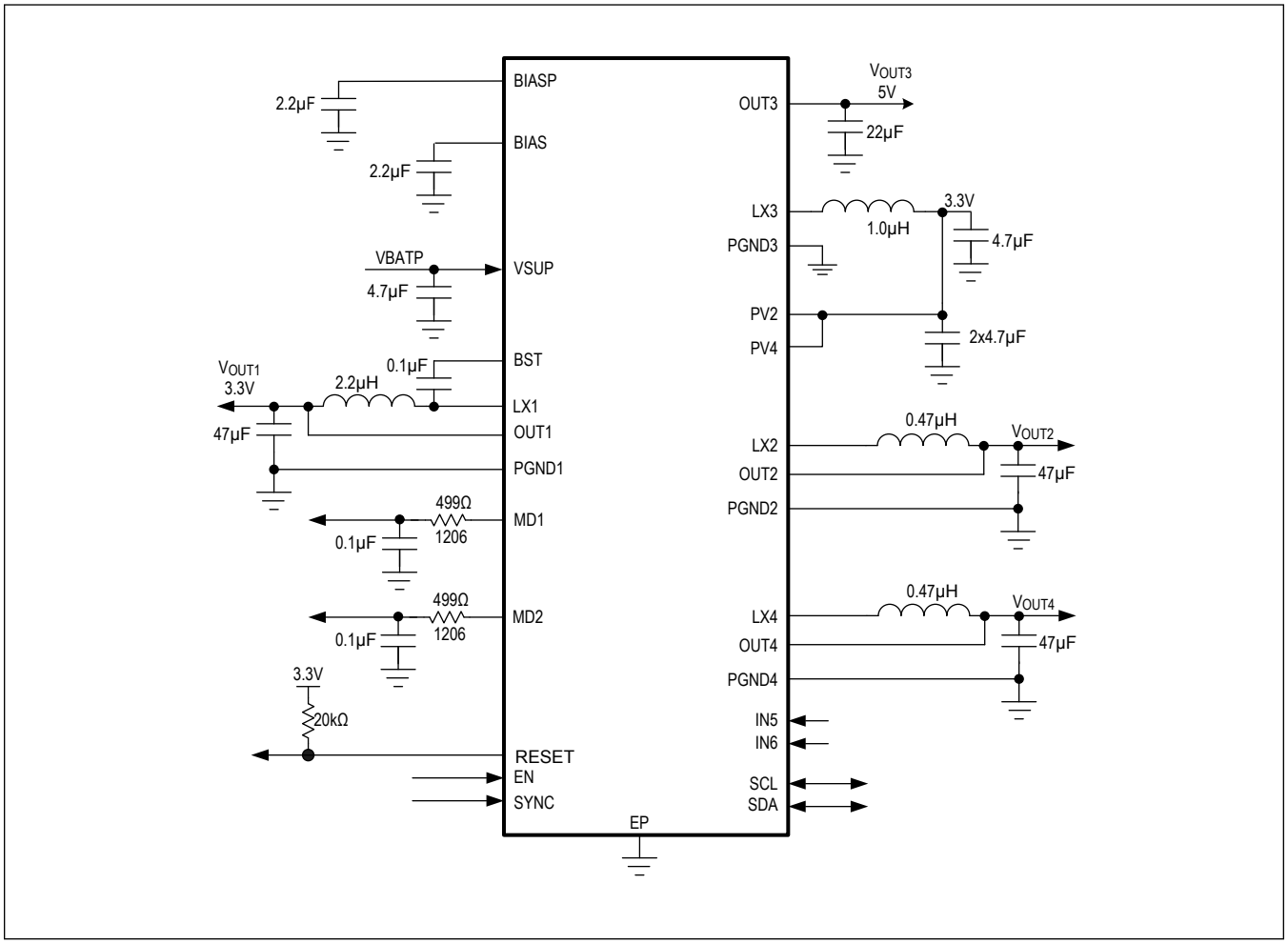
The MAX20430 DC-DC converters are designed to be stable with low-ESR ceramic capacitors. Other capacitor types are not recommended, as the ESR zero can affect stability of the device. The nominal recommended value for each part number is shown in Table 2. The de-rated capacitance should not fall below the minimum value. The phase margin and transients must be measured in the final circuit to verify that proper stability is achieved.

Table 2. Output Capacitor Selection

OUTPUT	MINIMUM VALUE	NOMINAL VALUE	UNIT
C_{OUT1}	15	47	µF
C_{OUT2}	10.5 x $I_{OUT(MAX)}/V_{OUT}$	27.5 x $I_{OUT(MAX)}/V_{OUT}$	µF
C_{OUT3}	12	22	µF
C_{OUT4}	10.5 x $I_{OUT(MAX)}/V_{OUT}$	27.5 x $I_{OUT(MAX)}/V_{OUT}$	µF

Typical Application Circuits

Typical Application Circuit



Ordering Information

PART	CID	V_{OUT2}	V_{OUT4}	I_{OUT2}	I_{OUT4}	CONFIG1	CONFIG2	FPSCFG1	I^2C
MAX20430ATIBB/VY+*	0x10	1.1V (0x18)	1.8V (0x50)	3A	3A	0x04	0x21	0x00	0x38
MAX20430ATIA/VY+	0x01	1.2V (0x20)	1.0V (0x10)	3A	3A	0x05	0x21	0x00	0x38
MAX20430ATICA/VY+*	0x03	1.2V (0x20)	1.35V (0x2C)	3A	3A	0x04	0x61	0x00	0x38

/VY Denotes side-wettable automotive qualified parts

+ Denotes a lead(Pb)-free/RoHS-compliant package

T Denotes tape-and-reel

** Future product - contact factory for availability*

Contact factory for other sequence options

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	10/19	Initial release	—