

P-Channel 40 V (D-S), 175 °C MOSFET

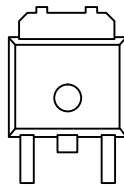
PRODUCT SUMMARY

V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A) ^d
- 40	0.0094 at $V_{GS} = - 10$ V	- 50
	0.0145 at $V_{GS} = - 4.5$ V	- 50

FEATURES

- TrenchFET[®] Power MOSFETs
- 175 °C Junction Temperature
- Compliant to RoHS Directive 2002/95/EC

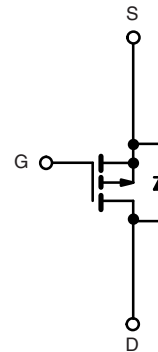

RoHS
COMPLIANT

TO-252


G D S

Top View

Drain Connected to Tab

Ordering Information: SUD50P04-09L-E3 (Lead (Pb)-free)


P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS $T_A = 25$ °C, unless otherwise noted

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	- 40	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current ($T_J = 175$ °C)	I_D	$T_C = 25$ °C	- 50 ^d
		$T_C = 125$ °C	- 50 ^d
Pulsed Drain Current	I_{DM}	- 100	A
Avalanche Current	I_{AS}	- 50	
Single Avalanche Energy ^a	E_{AS}	125	mJ
Power Dissipation	P_D	$T_C = 25$ °C	136 ^c
		$T_A = 25$ °C	3 ^{b, c}
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 175	°C

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Junction-to-Ambient ^b	R_{thJA}	$t \leq 10$ s	15	18
		Steady State	40	50
Junction-to-Case	R_{thJC}	0.82	1.1	°C/W

Notes:

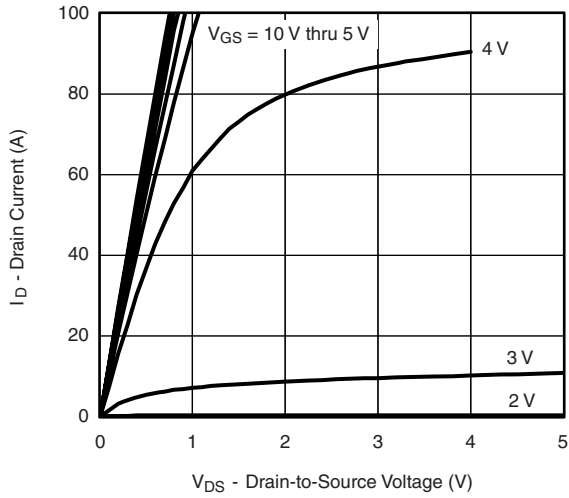
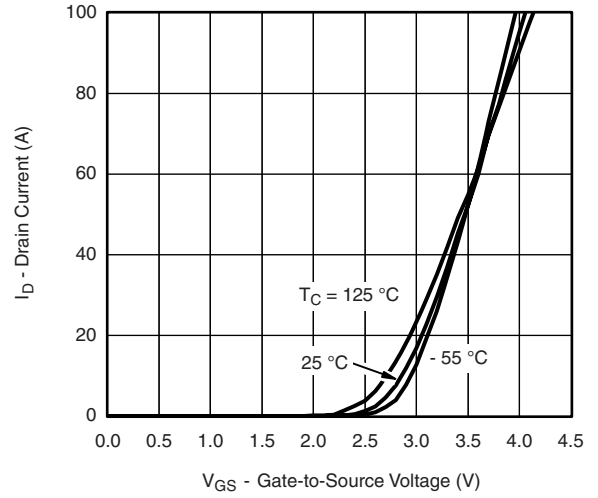
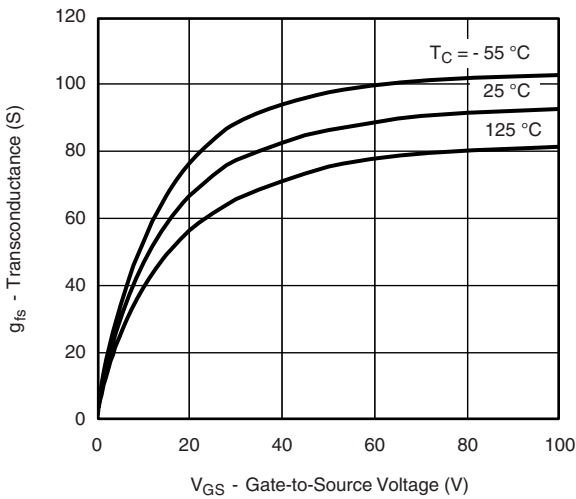
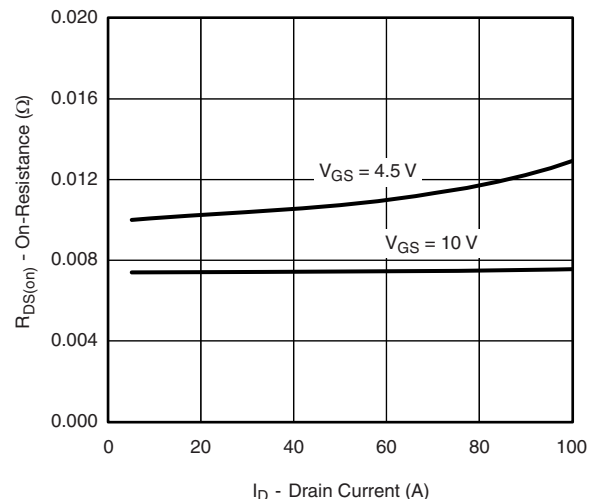
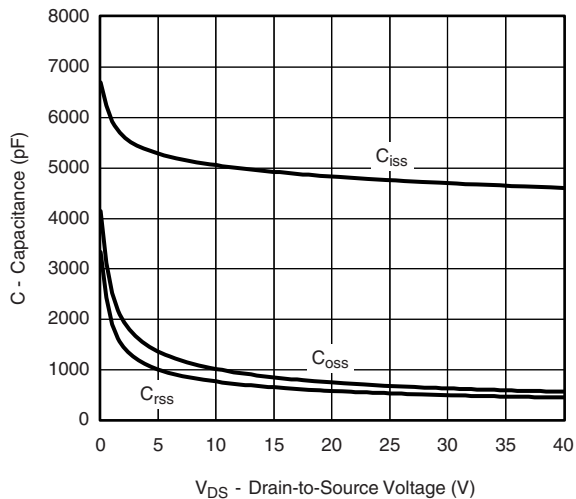
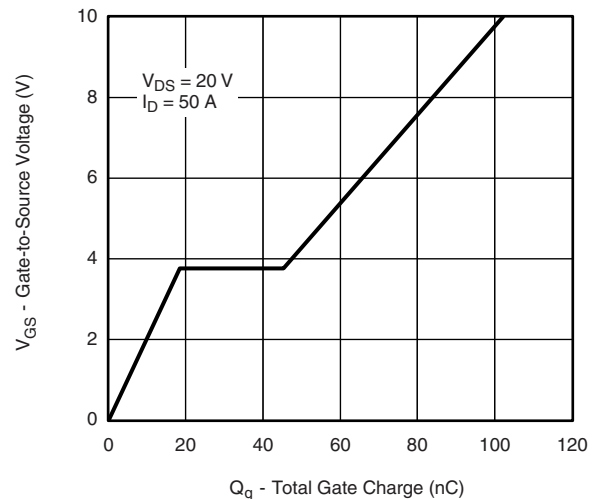
- Duty cycle ≤ 1 %.
- When mounted on 1" square PCB (FR-4 material).
- See SOA curve for voltage derating.
- Package limited.

SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$	-40			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	-1		-3	
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -32\text{ V}, V_{GS} = 0\text{ V}$			-1	μA
		$V_{DS} = -32\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$			-50	
		$V_{DS} = -32\text{ V}, V_{GS} = 0\text{ V}, T_J = 175\text{ }^\circ\text{C}$			-150	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} = -5\text{ V}, V_{GS} = -10\text{ V}$	-50			A
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = -10\text{ V}, I_D = -24\text{ A}$		0.0075	0.0094	Ω
		$V_{GS} = -10\text{ V}, I_D = -50\text{ A}, T_J = 125\text{ }^\circ\text{C}$			0.014	
		$V_{GS} = -10\text{ V}, I_D = -50\text{ A}, T_J = 175\text{ }^\circ\text{C}$			0.017	
		$V_{GS} = -4.5\text{ V}, I_D = -18\text{ A}$		0.0115	0.0145	
Forward Transconductance ^a	g_{fs}	$V_{DS} = -5\text{ V}, I_D = -24\text{ A}$		73		S
Dynamic^b						
Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}, V_{DS} = -25\text{ V}, f = 1\text{ MHz}$		4800		μF
Output Capacitance	C_{oss}			700		
Reverse Transfer Capacitance	C_{rss}			550		
Total Gate Charge ^c	Q_g	$V_{DS} = -20\text{ V}, V_{GS} = -10\text{ V}, I_D = -50\text{ A}$		102	150	nC
Gate-Source Charge ^c	Q_{gs}			18.5		
Gate-Drain Charge ^c	Q_{gd}			27		
Turn-On Delay Time ^c	$t_{d(on)}$	$V_{DD} = -20\text{ V}, R_L = 0.4\text{ }\Omega$ $I_D \cong -50\text{ A}, V_{GEN} = -10\text{ V}, R_g = 6\text{ }\Omega$		10	15	ns
Rise Time ^c	t_r			60	90	
Turn-Off Delay Time ^c	$t_{d(off)}$			145	220	
Fall Time ^c	t_f			140	220	
Source Drain-Diode Ratings and Characteristics $T_C = 25\text{ }^\circ\text{C}$ ^b						
Continuous Current	I_S				-50	A
Pulsed Current	I_{SM}				-100	
Forward Voltage ^a	V_{SD}	$I_F = -50\text{ A}, V_{GS} = 0\text{ V}$		-1.0	-1.5	V
Reverse Recovery Time	t_{rr}	$I_F = -50\text{ A}, dI/dt = 100\text{ A}/\mu\text{s}$		55	85	ns

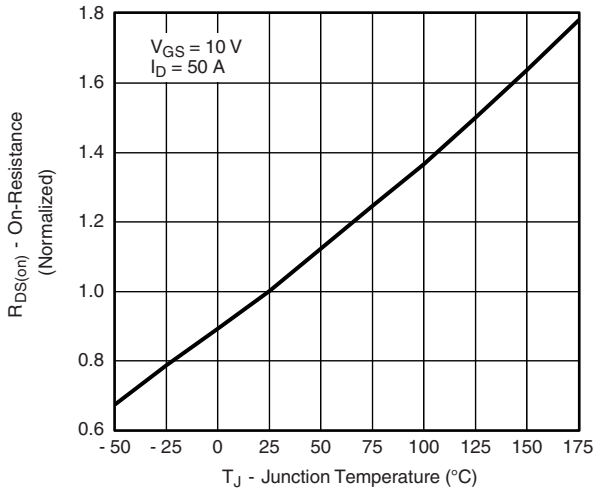
Notes:

- Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
- Guaranteed by design, not subject to production testing.
- Independent of operating temperature.

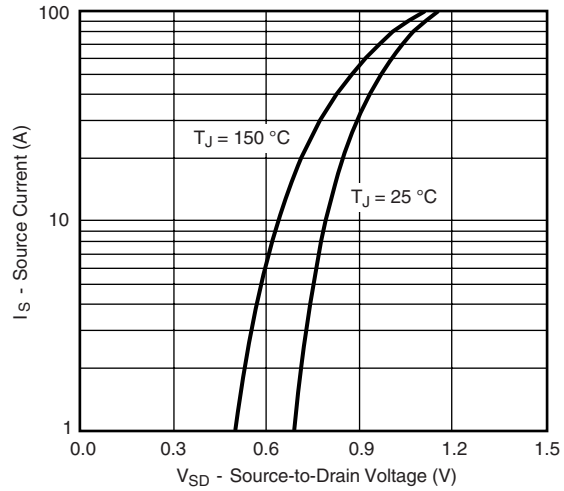
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

Output Characteristics

Transfer Characteristics

Transconductance

On-Resistance vs. Drain Current

Capacitance

Gate Charge

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

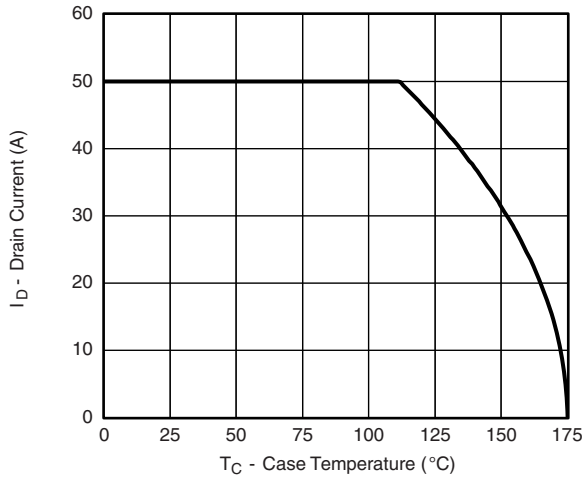


On-Resistance vs. Junction Temperature

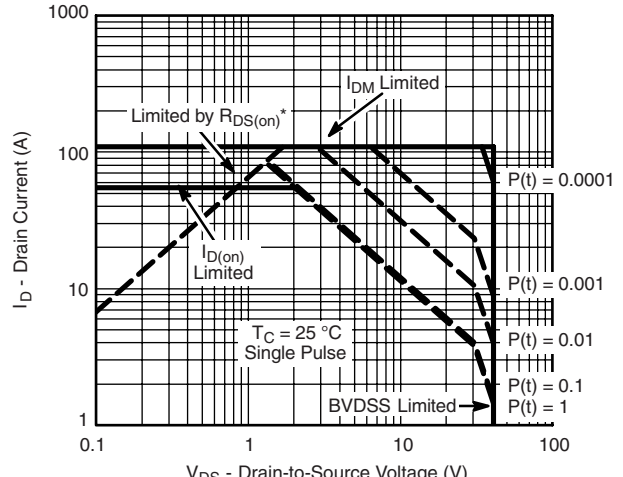


Source-Drain Diode Forward Voltage

THERMAL RATINGS

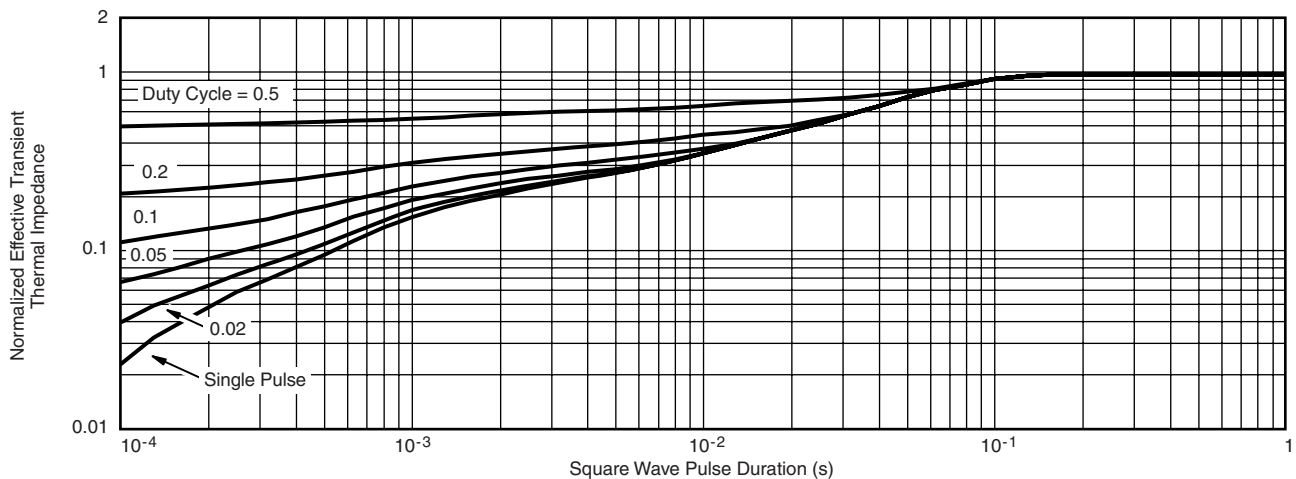


Maximum Avalanche and Drain Current vs. Case Temperature



* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area

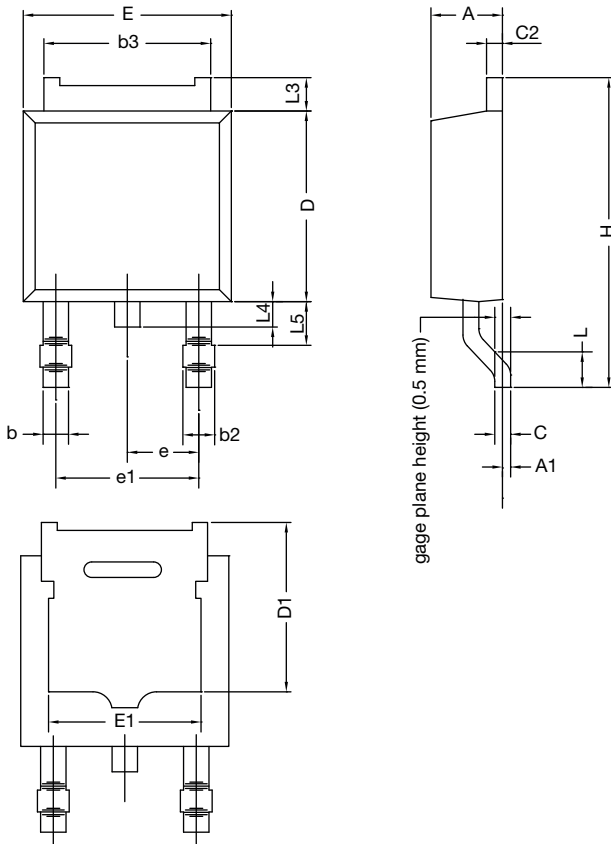


Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?72243.



TO-252AA Case Outline

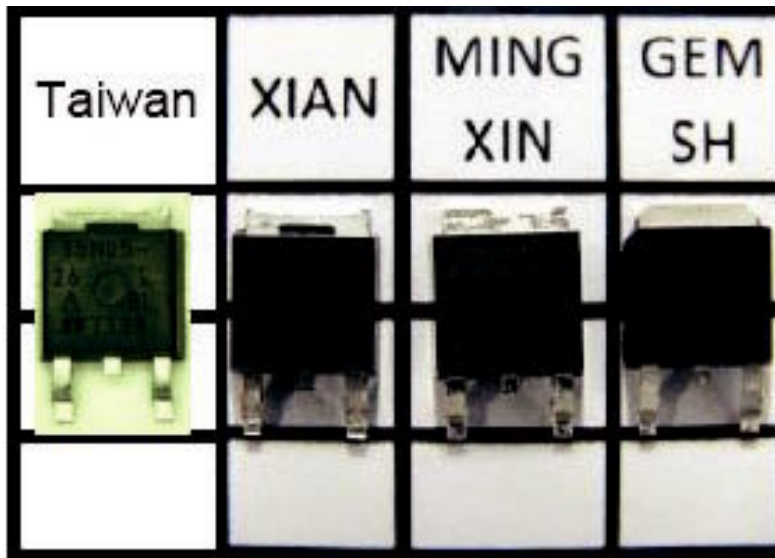


DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	2.18	2.38	0.086	0.094
A1	-	0.127	-	0.005
b	0.64	0.88	0.025	0.035
b2	0.76	1.14	0.030	0.045
b3	4.95	5.46	0.195	0.215
C	0.46	0.61	0.018	0.024
C2	0.46	0.89	0.018	0.035
D	5.97	6.22	0.235	0.245
D1	4.10	-	0.161	-
E	6.35	6.73	0.250	0.265
E1	4.32	-	0.170	-
H	9.40	10.41	0.370	0.410
e	2.28 BSC		0.090 BSC	
e1	4.56 BSC		0.180 BSC	
L	1.40	1.78	0.055	0.070
L3	0.89	1.27	0.035	0.050
L4	-	1.02	-	0.040
L5	1.01	1.52	0.040	0.060

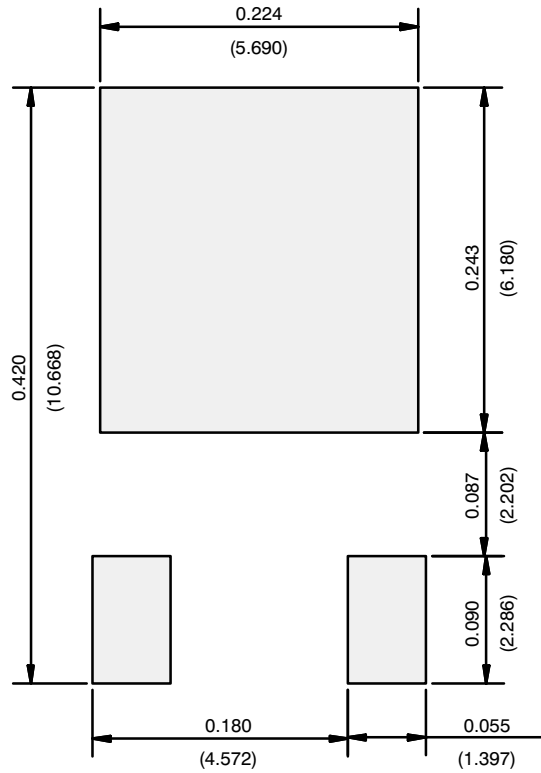
ECN: T13-0359-Rev. O, 03-Jun-13
DWG: 5347

Notes

- Dimension L3 is for reference only.
- Xi'an, Mingxin, and GEM SH actual photo.



RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)



Recommended Minimum Pads
Dimensions in Inches/(mm)

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