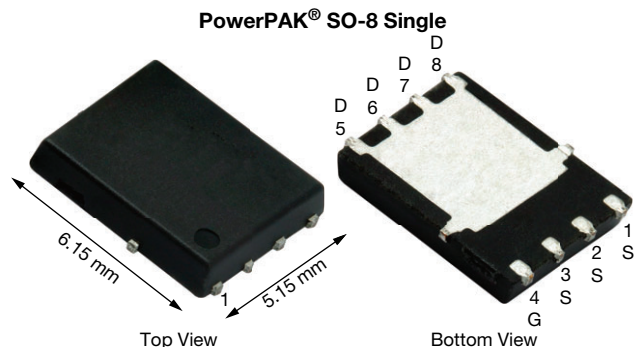


P-Channel 40 V (D-S) MOSFET



PRODUCT SUMMARY	
V_{DS} (V)	-40
$R_{DS(on)}$ max. (Ω) at $V_{GS} = -10$ V	0.0045
$R_{DS(on)}$ max. (Ω) at $V_{GS} = -4.5$ V	0.0057
Q_g typ. (nC)	82.7
I_D (A)	-101.4 ^a
Configuration	Single

FEATURES

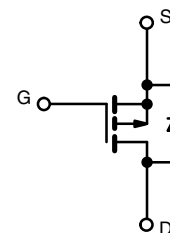
- TrenchFET® Gen IV p-channel power MOSFET
- Ultra low $R_{DS} \times Q_g$ FOM product
- 100 % R_g and UIS tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- Adapter and charger switch
- Load switch
- Motor drive control
- DC/DC converter
- Power supplies
- Battery management



P-Channel MOSFET

ORDERING INFORMATION

Package	PowerPAK SO-8
Lead (Pb)-free, halogen-free, BLR and IOL	SiR4407DP-T1-UE3

ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	V_{DS}	-40	V
Gate-source voltage	V_{GS}	± 20	
Continuous drain current ($T_J = 150$ °C)	$T_C = 25$ °C	-101.4	A
	$T_C = 70$ °C	-80	
	$T_A = 25$ °C	-24.5 ^{b, c}	
	$T_A = 70$ °C	-19.6 ^{b, c}	
Pulsed drain current ($t = 100$ μ s)	I_{DM}	-350	
Continuous source-drain diode current	$T_C = 25$ °C	-75.7	
	$T_A = 25$ °C	-4.5 ^{b, c}	
Single pulse avalanche current	I_{AS}	-40	
Single pulse avalanche energy	E_{AS}	80	mJ
Maximum power dissipation	$T_C = 25$ °C	83.3	W
	$T_C = 70$ °C	53.3	
	$T_A = 25$ °C	5.0 ^{b, c}	
	$T_A = 70$ °C	3.2 ^{b, c}	
Operating junction and storage temperature range	T_J, T_{stg}	-55 to +150	°C
Soldering recommendations (peak temperature) ^c		260	

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction-to-ambient ^b	R_{thJA}	20	25	°C/W
Maximum junction-to-case (drain)	R_{thJC}	1.2	1.5	

Notes

- $T_C = 25$ °C
- Surface mounted on 1" x 1" FR4 board
- $t = 10$ s
- See solder profile (www.vishay.com/doc?73257). The PowerPAK 1212-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components
- Maximum under steady state conditions is 65 °C/W



SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-source breakdown voltage	V _{DS}	V _{GS} = 0 V, I _D = -250 μA	-40	-	-	V
V _{DS} temperature coefficient	ΔV _{DS} /T _J	I _D = -10 mA	-	-32	-	mV/°C
V _{GS(th)} temperature coefficient	ΔV _{GS(th)} /T _J	I _D = -250 μA	-	4.5	-	
Gate-source threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = -250 μA	-1	-	-2.3	V
Gate-source leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V	-	-	100	nA
Zero gate voltage drain current	I _{DSS}	V _{DS} = -40 V, V _{GS} = 0 V	-	-	-1	μA
		V _{DS} = -40 V, V _{GS} = 0 V, T _J = 70 °C	-	-	-15	
Drain-source on-state resistance ^a	R _{DS(on)}	V _{GS} = -10 V, I _D = -20 A	-	0.0032	0.0045	Ω
		V _{GS} = -4.5 V, I _D = -20 A	-	0.0041	0.0057	
Forward transconductance ^a	g _{fs}	V _{DS} = -15 V, I _D = -20 A	-	95	-	S
Dynamic ^b						
Input capacitance	C _{iss}	V _{DS} = -20 V, V _{GS} = 0 V, f = 1 MHz	-	8860	-	pF
Output capacitance	C _{oss}		-	660	-	
Reverse transfer capacitance	C _{rss}		-	726	-	
Total gate charge	Q _g	V _{DS} = -20 V, V _{GS} = -10 V, I _D = -20 A	-	177	266	nC
Gate-source charge	Q _{gs}	V _{DS} = -20 V, V _{GS} = -4.5 V, I _D = -20 A	-	82.7	124	
Gate-drain charge	Q _{gd}		-	25.7	-	
Gate resistance	R _g	f = 1 MHz	0.9	2.2	3.7	Ω
Turn-on delay time	t _{d(on)}	V _{DD} = -20 V, R _L = 1 Ω, I _D ≡ -20 A, V _{GEN} = -10 V, R _g = 1 Ω	-	15	30	ns
Rise time	t _r		-	41	82	
Turn-off delay time	t _{d(off)}		-	96	192	
Fall time	t _f		-	39	78	
Turn-on delay time	t _{d(on)}	V _{DD} = -20 V, R _L = 1 Ω, I _D ≡ -20 A, V _{GEN} = -4.5 V, R _g = 1 Ω	-	43	86	
Rise time	t _r		-	124	248	
Turn-off delay time	t _{d(off)}		-	98	196	
Fall time	t _f		-	80	160	
Drain-Source Body Diode Characteristics						
Continuous source-drain diode current	I _S	T _C = 25 °C	-	-	-75.7	A
Pulse diode forward current	I _{SM}		-	-	-350	
Body diode voltage	V _{SD}	I _S = -5 A, V _{GS} = 0 V	-	-0.73	-1.1	V
Body diode reverse recovery time	t _{rr}	I _F = -20 A, di/dt = 100 A/μs, T _J = 25 °C	-	23	46	ns
Body diode reverse recovery charge	Q _{rr}		-	26	52	nC
Reverse recovery fall time	t _a		-	15	-	ns
Reverse recovery rise time	t _b		-	11	-	

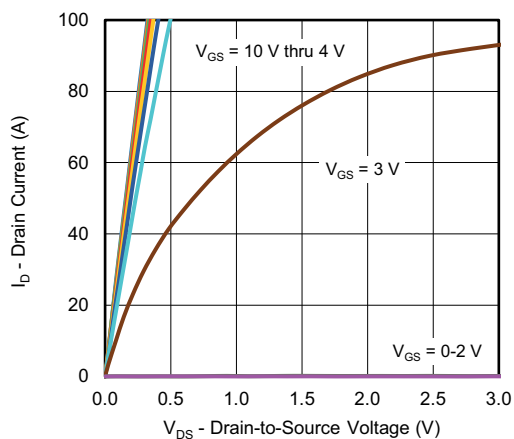
Notes

- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$
b. Guaranteed by design, not subject to production testing

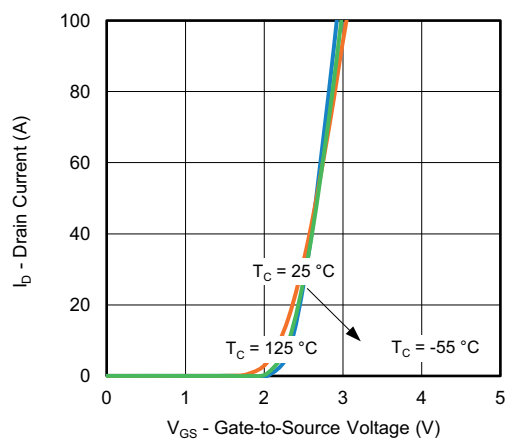
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



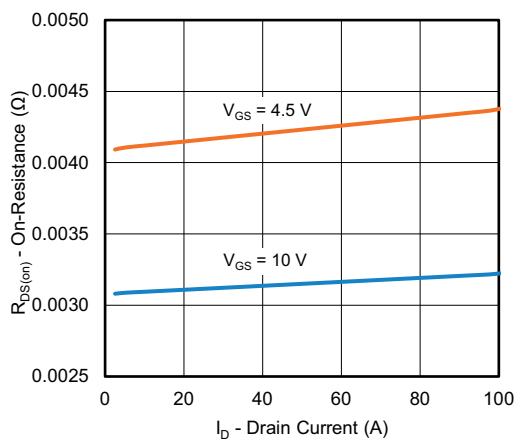
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



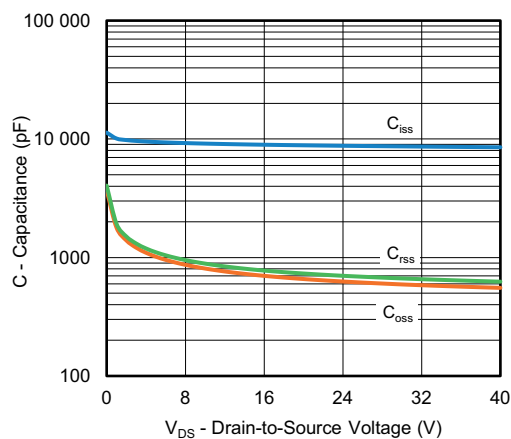
Output Characteristics



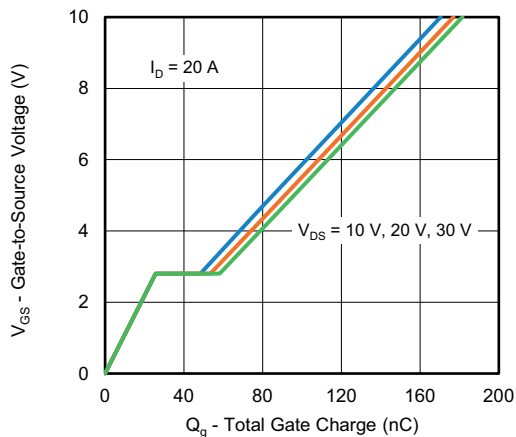
Transfer Characteristics



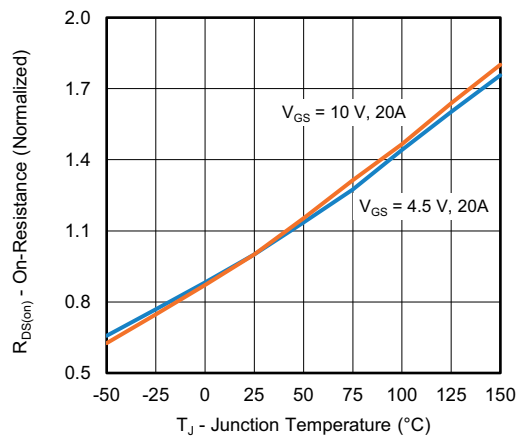
On-Resistance vs. Drain Current and Gate Voltage



Capacitance



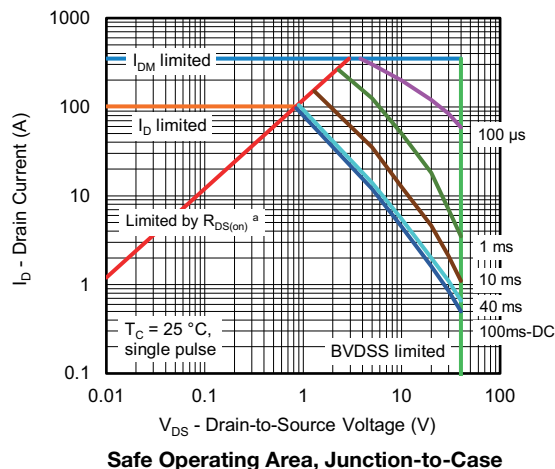
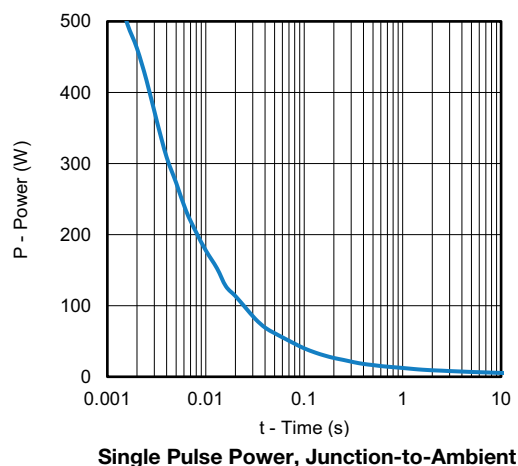
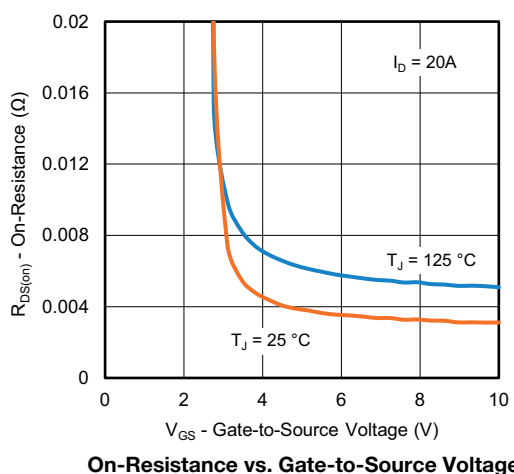
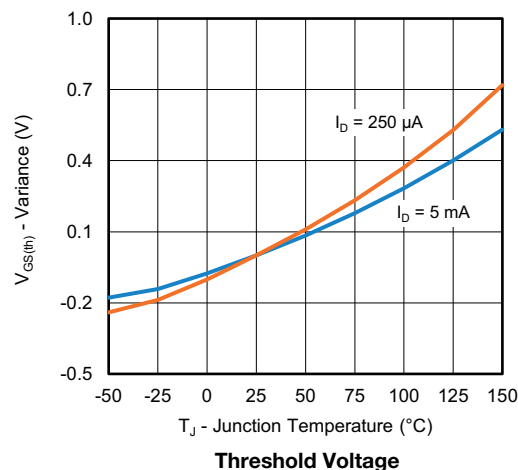
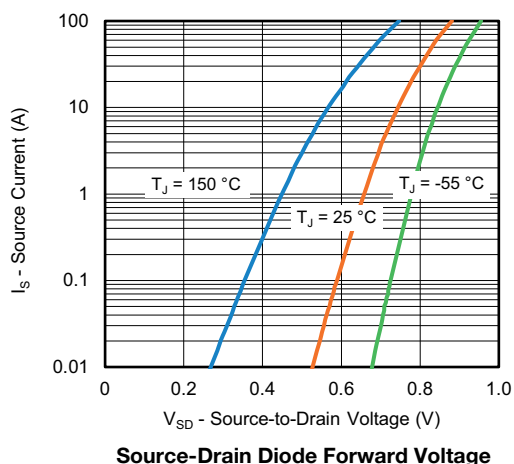
Gate Charge



On-Resistance vs. Junction Temperature



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

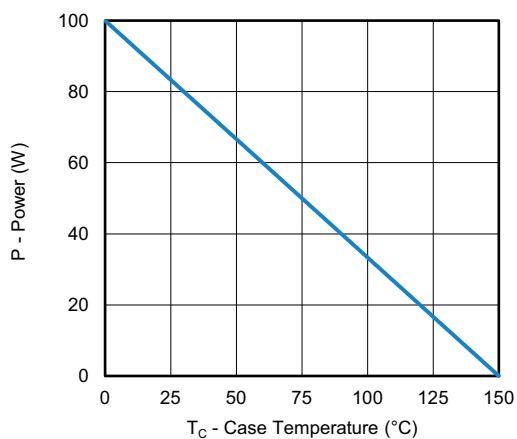
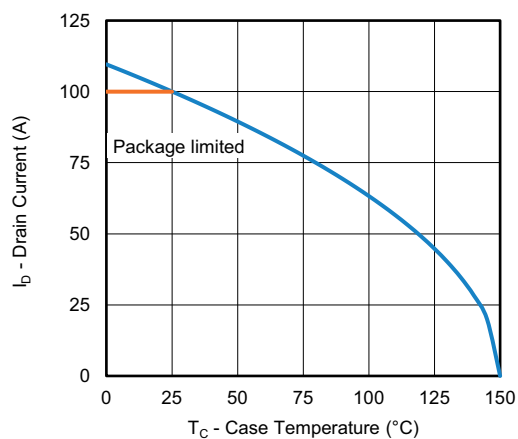


Note

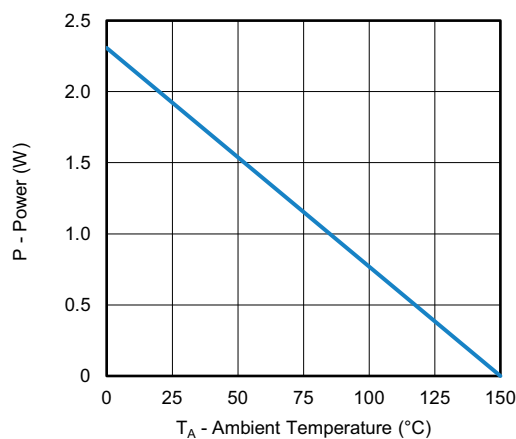
a. $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Power, Junction-to-Case



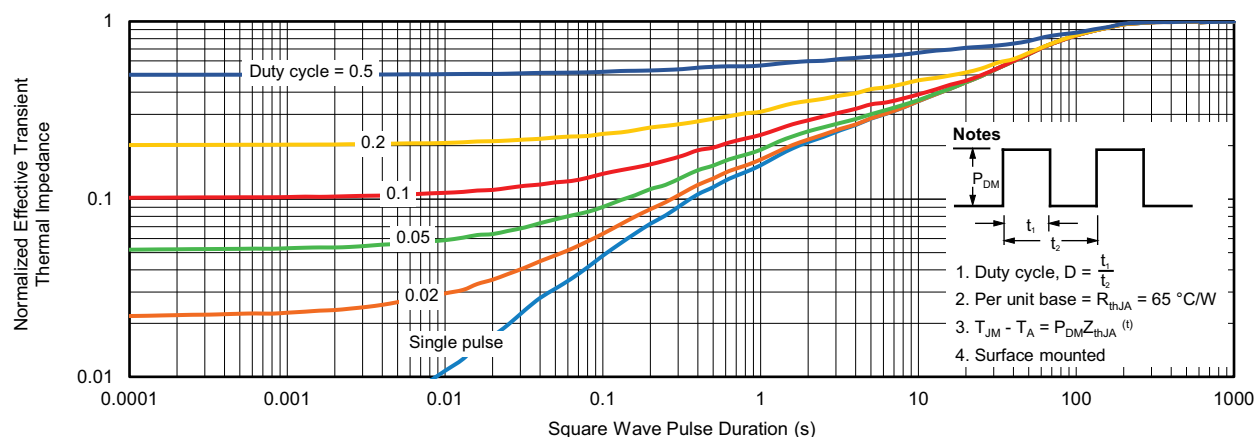
Power, Junction-to-Ambient

Note

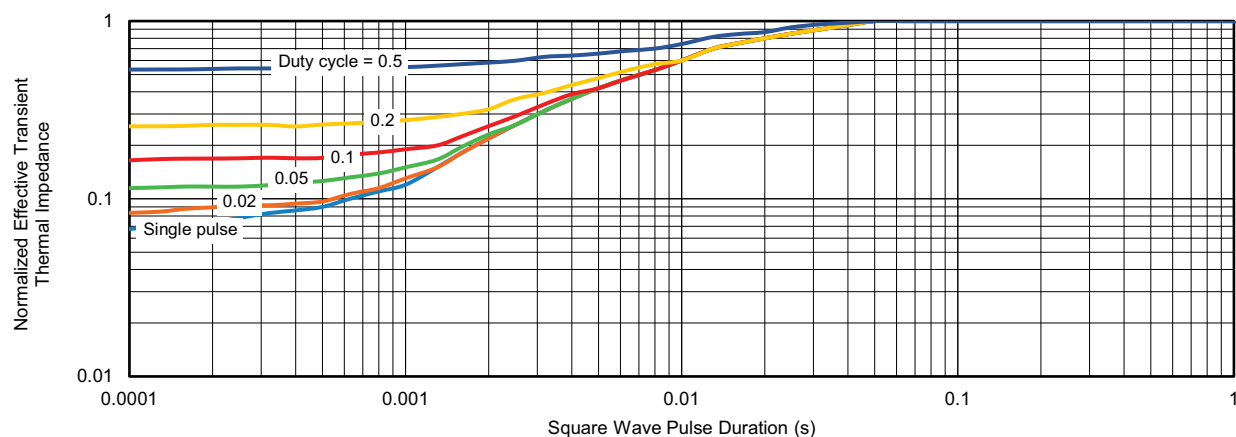
- a. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

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