i6A Reference Design
Application Note

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1. Design Consideration
   • TDK-Lambda’s power module provides all the power train components in one compact package allowing the end user quickly to design a custom power system. The purpose of this reference design is to assist the engineer to design the printed circuit board and select the additional components from commonly available material.
   • TDK-Lambda Technical Support will be glad to assist you further.

2. Reference Design
   • Picture 1 shows a basic circuitry for basic mode operation.
   • Trim:
     • $R_{\text{TRIM}}_{\text{MAX}}$ with 0.75kΩ sets the maximum output voltage to 18V.
     • With $R_{\text{TRIM}}$ the output voltage can be adjusted over the specified output voltage range of 3.3V to 18V.
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3. BOM

- Below list shows the additional used components for the reference design

<table>
<thead>
<tr>
<th>Ref designator</th>
<th>Value, Rating</th>
<th>Manufacturer</th>
<th>Part number</th>
</tr>
</thead>
<tbody>
<tr>
<td>C1, C2</td>
<td>Cap 22µF, 50V</td>
<td>TDK</td>
<td>CKG57NX5R1H226M500JH</td>
</tr>
<tr>
<td>C3</td>
<td>Cap 100µF, 50V</td>
<td>Panasonic</td>
<td>EEE-HD1H101P</td>
</tr>
<tr>
<td>C4</td>
<td>Cap 47µF, 25V</td>
<td>TDK</td>
<td>C3216X5R1E476M160AC</td>
</tr>
<tr>
<td>R_{trim}</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>R_{trim_{max}}</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

4. Design Recommendations

- \( R_{\text{TRIM}} \):
  Choose the value of \( R_{\text{trim}} \) from the i6A datasheet page 14 according your output voltage requirement.
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5. Full Feature option - Phase shift Synchronization

- The i6A modules can be synchronized to one another or to an external clock within +/- 20% of nominal value shown on electrical characteristics page by using pin 32 (SYNC) and pin 33 (MS). Interleaving of switching can also be achieved to achieve input noise cancellation.

Picture 2 shows the basic connection between two modules.

- Module 1 (U$1) is set in Clock Master mode (Pin33). Pin 32 becomes an output.
- Module 2 (US2) is set in Clock Slave mode (Pin33) with 180 degree phase shift. Pin 32 becomes an input.
6. Full Feature option – Sequencing

- The i6A modules can be.

Picture 3 shows the basic connection between two modules.

- Module 1 (U$1) is set in Clock Master mode (Pin33). Pin 32 becomes an output.
- Module 2 (US2) is set in Clock Slave mode (Pin33) with 180 degree phase shift. Pin 32 becomes an input.