

N-channel 650 V, 0.6 Ω typ., 7 A MDmesh II Plus™ low Q_g Power MOSFET in a TO-220FP package

Datasheet - preliminary data

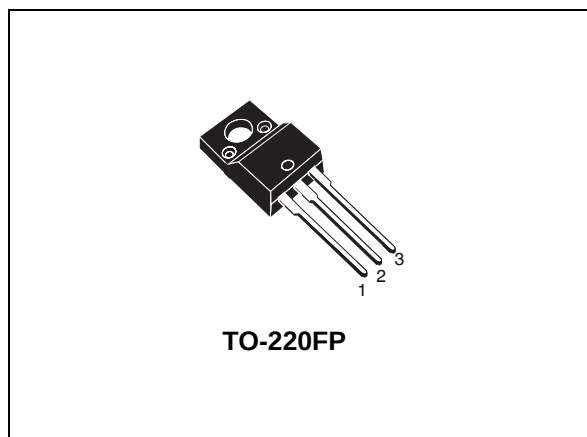
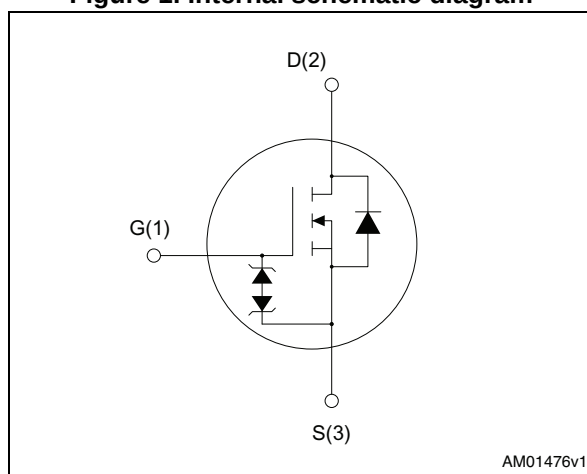


Figure 1. Internal schematic diagram



Features

Order code	V_{DS}	$R_{DS(on)}$ max	I_D
STF11N65M2(045Y)	650 V	0.67 Ω	7 A

- Extremely low gate charge
- Lower $R_{DS(on)}$ x area vs previous generation
- Low gate input resistance
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET developed using a new generation of MDmesh™ technology: MDmesh II Plus™ low Q_g . This revolutionary Power MOSFET associates a vertical structure to the company's strip layout to yield one of the world's lowest on-resistance and gate charge. It is therefore suitable for the most demanding high efficiency converters.

Table 1. Device summary

Order code	Marking	Package	Packaging
STF11N65M2(045Y)	11N65M2	TO-220FP	Tube

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	± 25	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ °C}$	7	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100\text{ °C}$	4.4	A
$I_{DM}^{(2)}$	Drain current (pulsed)	28	A
$P_{TOT}^{(1)}$	Total dissipation at $T_C = 25\text{ °C}$	25	W
$dv/dt^{(3)}$	Peak diode recovery voltage slope (starting $T_j = 25\text{ °C}$, $I_D = I_{AS}$, $V_{DD} = 50\text{ V}$)	15	V/ns
$dv/dt^{(4)}$	MOSFET dv/dt ruggedness	50	V/ns
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink ($t = 1\text{ s}$; $T_C = 25\text{ °C}$)	2500	V
T_{stg}	Storage temperature	- 55 to 150	°C
T_j	Max. operating junction temperature	150	

1. The value is rated according to Rthj-case and limited by package.
2. Pulse width limited by T_{jmax}
3. $I_{SD} \leq 7\text{ A}$, $di/dt \leq 400\text{ A}/\mu\text{s}$; $V_{DS\text{ peak}} < V_{(BR)DSS}$, $V_{DD} = 80\% V_{(BR)DSS}$.
4. $V_{DS} \leq 520\text{ V}$

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-case}}$	Thermal resistance junction-case max	5	°C/W
$R_{thj\text{-amb}}$	Thermal resistance junction-amb max	62.5	°C/W

Table 4. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T_{jmax})	1.5	A
E_{AS}	Single pulse avalanche energy (starting $T_j = 25\text{ °C}$, $I_D = I_{AR}$; $V_{DD} = 50$)	110	mJ

2 Electrical characteristics

($T_C = 25\text{ °C}$ unless otherwise specified)

Table 5. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage ($V_{GS} = 0$)	$I_D = 1\text{ mA}$	650			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = 650\text{ V}$			1	μA
		$V_{DS} = 650\text{ V}, T_C = 125\text{ °C}$			100	μA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 25\text{ V}$			± 10	μA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2	3	4	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}, I_D = 3.5\text{ A}$		0.6	0.67	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 100\text{ V}, f = 1\text{ MHz}, V_{GS} = 0$	-	410	-	pF
C_{oss}	Output capacitance		-	20	-	pF
C_{rss}	Reverse transfer capacitance		-	0.95	-	pF
$C_{oss\text{ eq.}}^{(1)}$	Equivalent output capacitance	$V_{DS} = 0\text{ to }520\text{ V}, V_{GS} = 0$	-	83	-	pF
R_G	Intrinsic gate resistance	$f = 1\text{ MHz open drain}$	-	6.4	-	Ω
Q_g	Total gate charge	$V_{DD} = 520\text{ V}, I_D = 7\text{ A}, V_{GS} = 10\text{ V}$ (see Figure 15)	-	12.5	-	nC
Q_{gs}	Gate-source charge		-	3.2	-	nC
Q_{gd}	Gate-drain charge		-	5.8	-	nC

1. $C_{oss\text{ eq.}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 325 \text{ V}$, $I_D = 3.5 \text{ A}$, $R_G = 4.7 \text{ } \Omega$, $V_{GS} = 10 \text{ V}$ (see Figure 14 and 19)	-	9.5	-	ns
t_r	Rise time		-	7.5	-	ns
$t_{d(off)}$	Turn-off delay time		-	26	-	ns
t_f	Fall time		-	15	-	ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		7	A
$I_{SDM}^{(1)(2)}$	Source-drain current (pulsed)		-		28	A
$V_{SD}^{(3)}$	Forward on voltage	$I_{SD} = 7 \text{ A}$, $V_{GS} = 0$	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 7 \text{ A}^{(2)}$, $di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 60 \text{ V}$ (see Figure 16)	-	318		ns
Q_{rr}	Reverse recovery charge		-	2.5		nC
I_{RRM}	Reverse recovery current		-	15.5		A
t_{rr}	Reverse recovery time	$I_{SD} = 7 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 60 \text{ V}$, $T_J = 150 \text{ } ^\circ\text{C}$ (see Figure 16)	-	437		ns
Q_{rr}	Reverse recovery charge		-	3.2		nC
I_{RRM}	Reverse recovery current		-	15		A

1. Pulse width limited by safe operating area
2. Test condition is referred to through-hole package
3. Pulsed: pulse duration = $300 \text{ } \mu\text{s}$, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

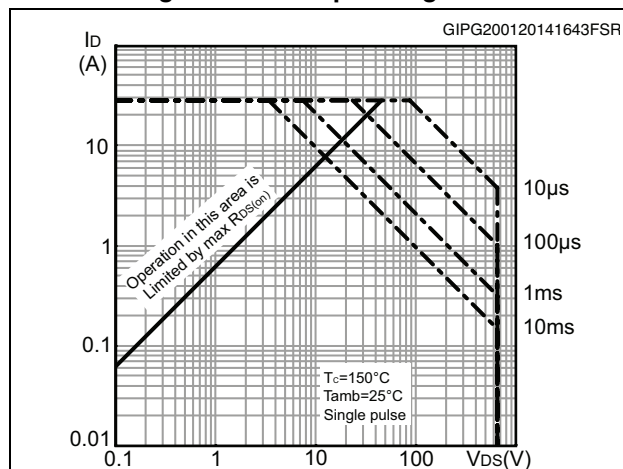


Figure 3. Thermal impedance

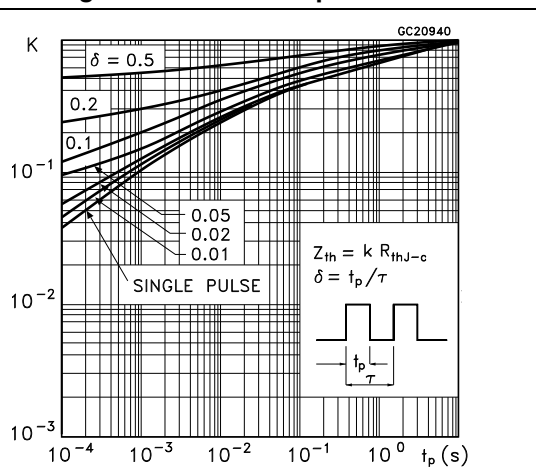


Figure 4. Output characteristics

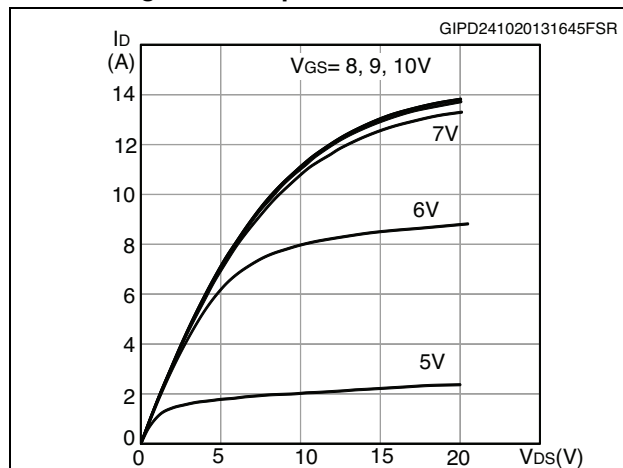


Figure 5. Transfer characteristics

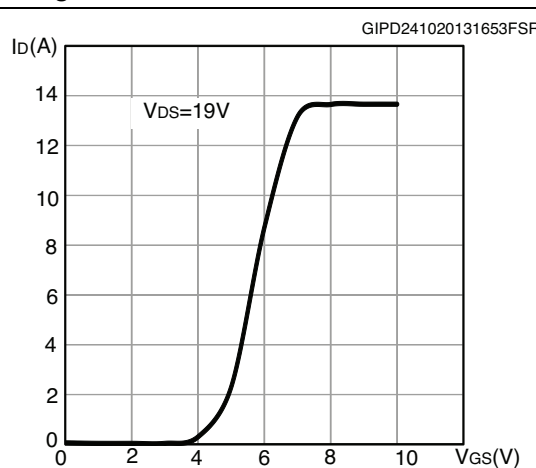
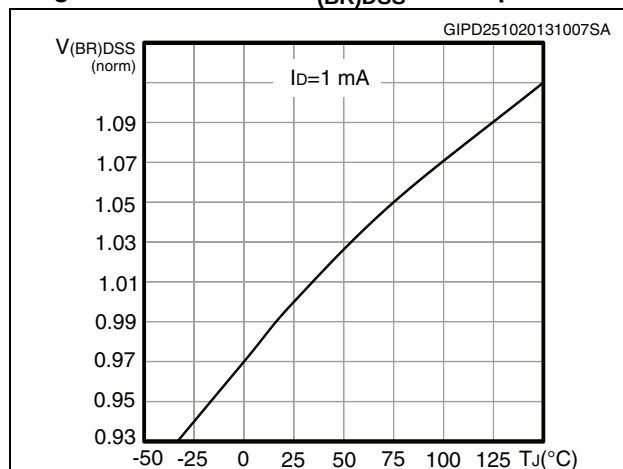
Figure 6. Normalized $V_{(BR)DSS}$ vs temperature

Figure 7. Static drain-source on-resistance

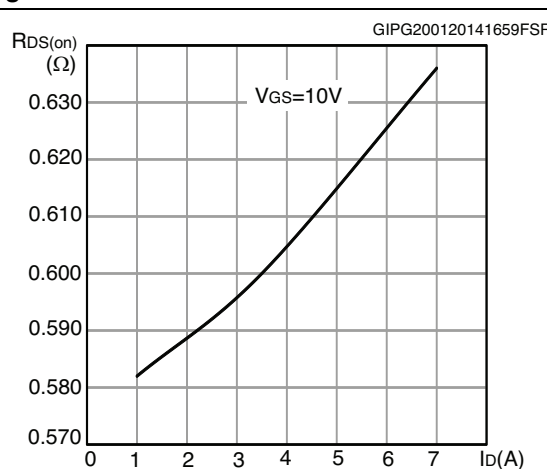


Figure 8. Gate charge vs gate-source voltage

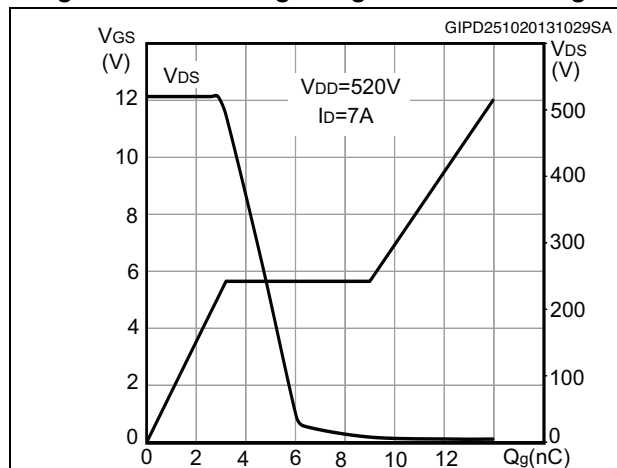


Figure 9. Capacitance variations

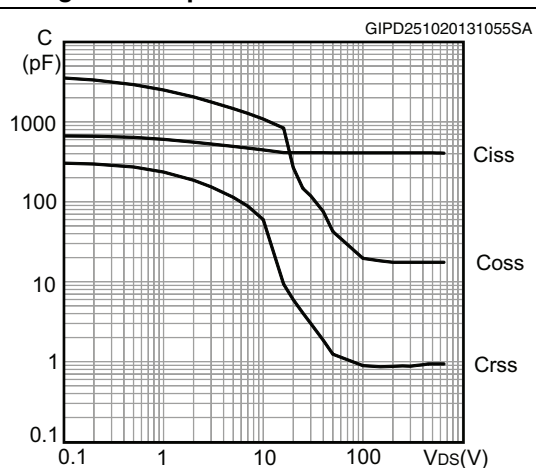


Figure 10. Normalized gate threshold voltage vs temperature

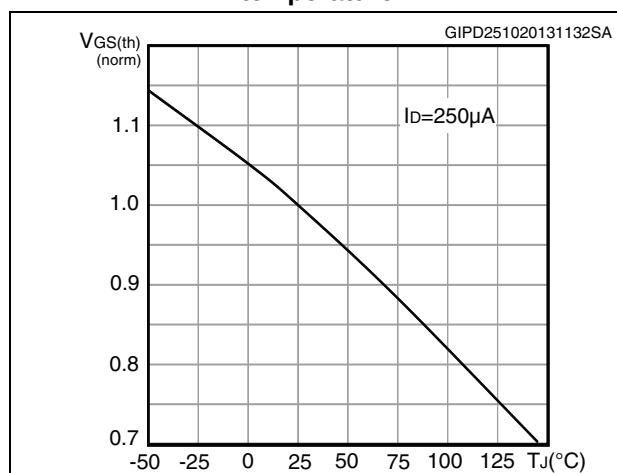


Figure 11. Normalized on-resistance vs temperature

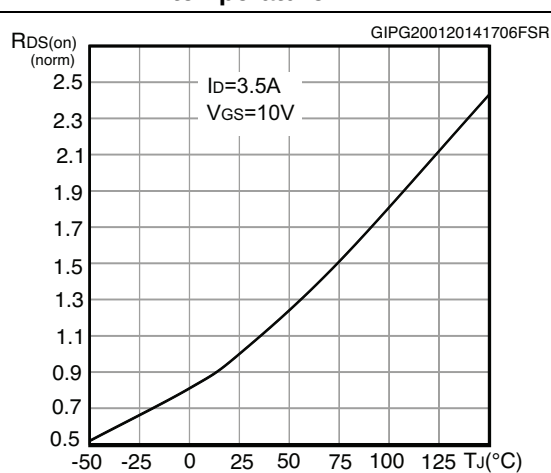


Figure 12. Source-drain diode forward characteristics

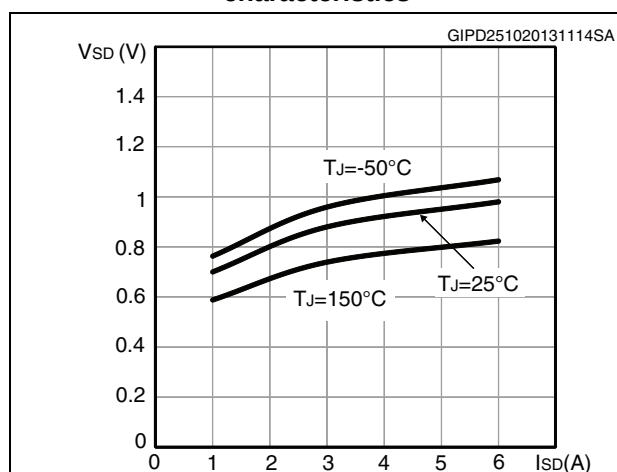
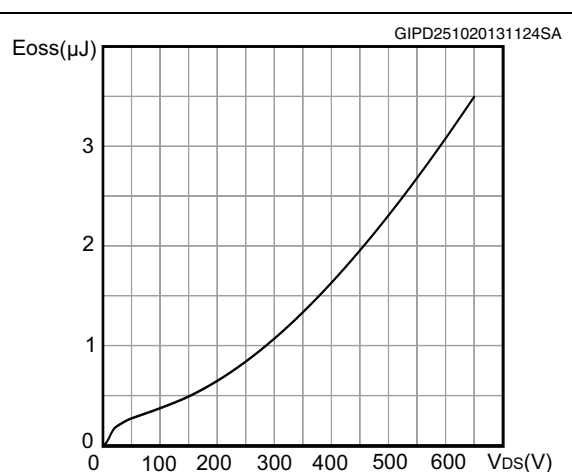


Figure 13. Output capacitance stored energy



3 Test circuits

Figure 14. Switching times test circuit for resistive load

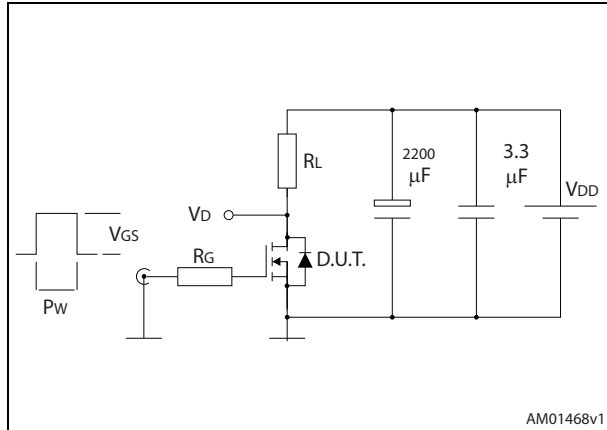


Figure 15. Gate charge test circuit

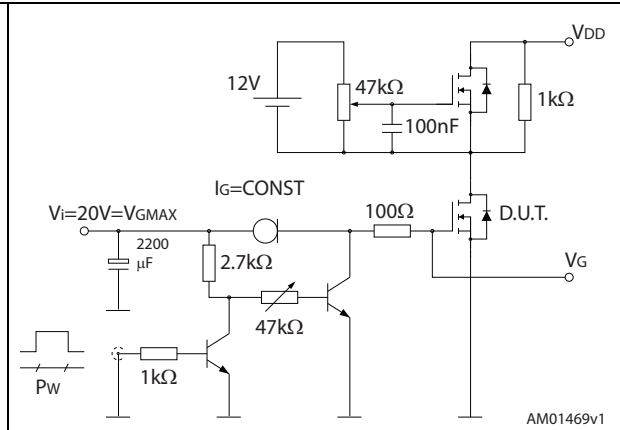


Figure 16. Test circuit for inductive load switching and diode recovery times



Figure 17. Unclamped inductive load test circuit

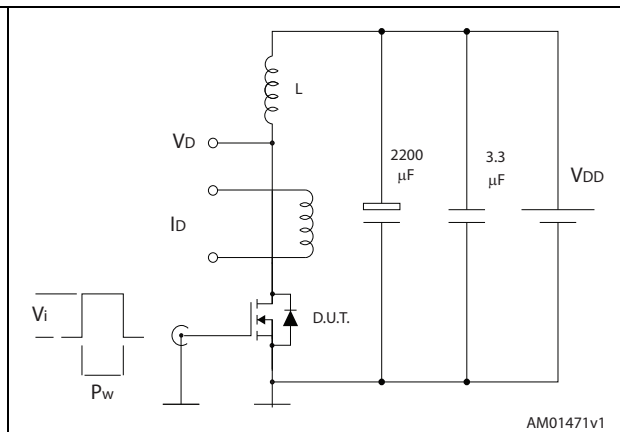


Figure 18. Unclamped inductive waveform

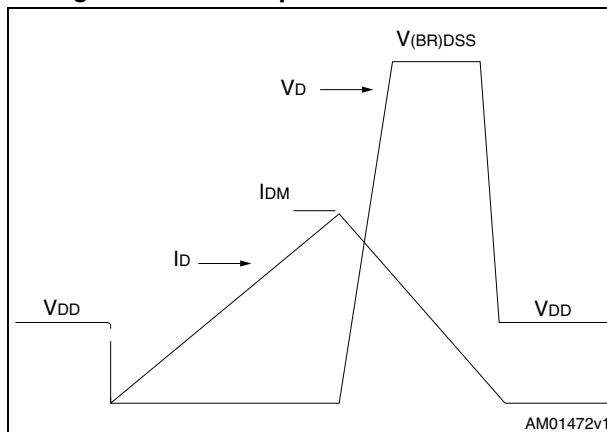
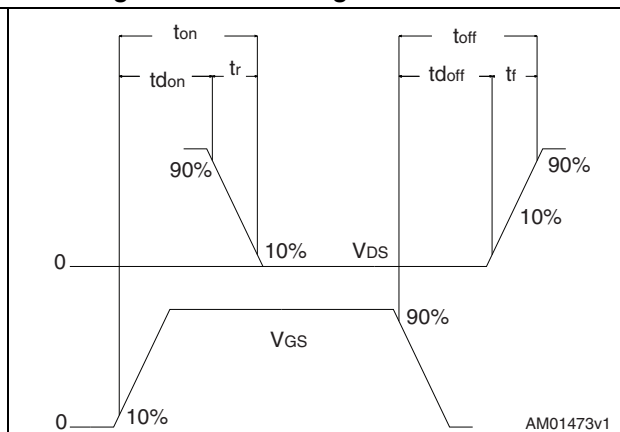


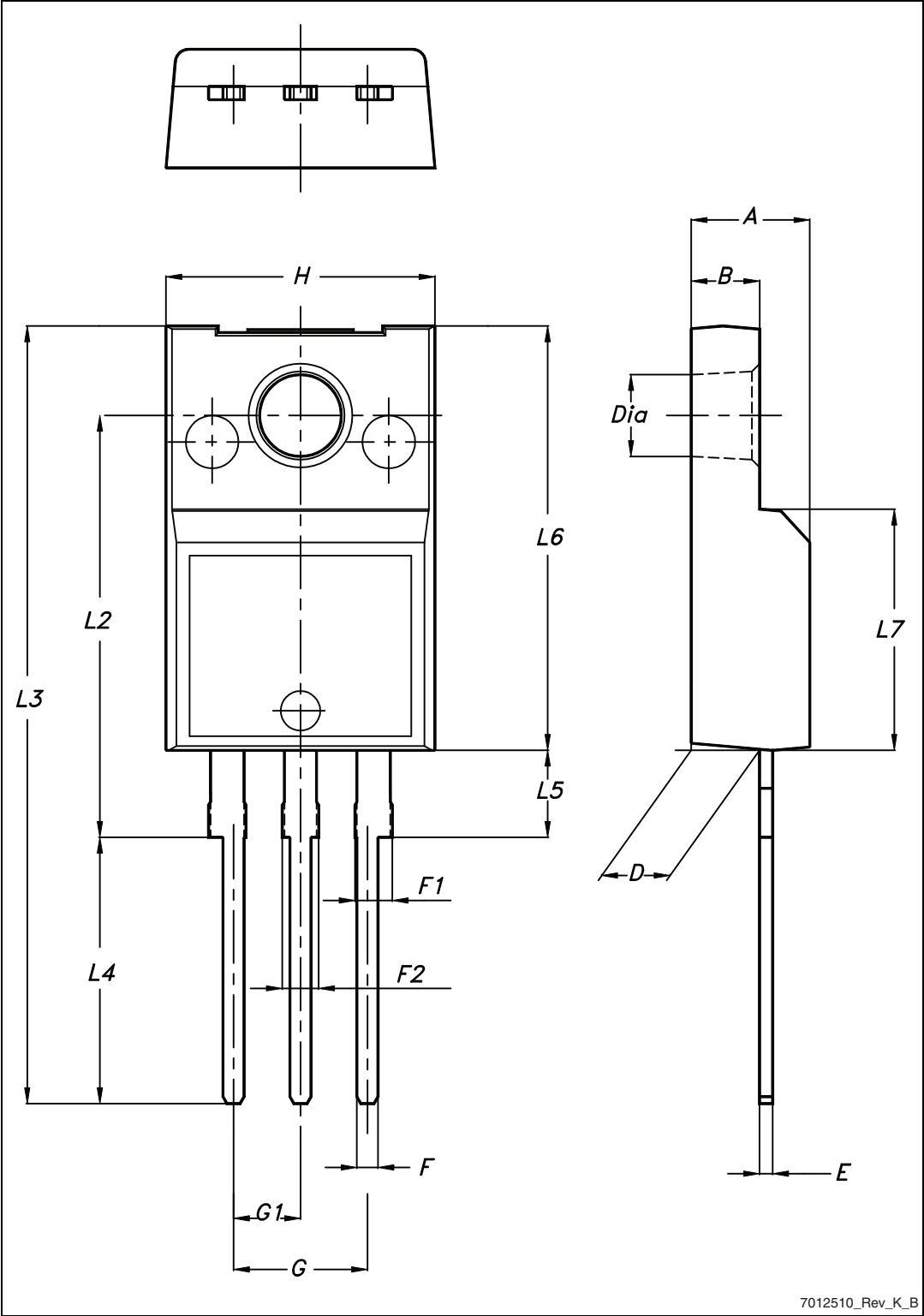
Figure 19. Switching time waveform



4 Package mechanical data

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Figure 20. TO-220FP drawing



7012510_Rev_K_B

Table 9. TO-220FP mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Ø	3		3.2

5 Revision history

Table 10. Document revision history

Date	Revision	Changes
09-May-2014	1	First release.

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