Datasheet

SL917 NCP Module

Version 0.7

Revision History

Version	Date	Notes	Contributors	Approver
0.7	19 Feb 2025	Initial Release	Dave Drogowski Dave Neperud	Andy Ross

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SL917 Wi-Fi® and Bluetooth® LE Network Co-Processor Connectivity Module Datasheet

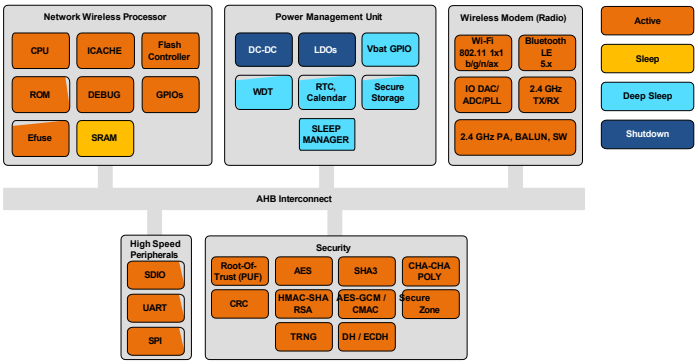
Ezurio's SL917 Network Co-Processor Connectivity module is based on the Silicon Labs SiWN917M, which is our lowest power Wi-Fi 6 silicon, ideal for ultra-low power IoT wireless devices using Wi-Fi®, Bluetooth, and IP networking for secure cloud connectivity. It has an integrated built-in wireless subsystem, advanced security, and integrated power- management. It has a multi-threaded Network Wireless Processor (NWP) running up to 160 MHz. All the networking and wireless stacks run on independent threads of the multi-threaded processor. The SL917 includes an ultra-low power Wi-Fi 6 plus Bluetooth Low Energy (LE) 5.4 wireless CPU subsystem, baseband digital signal processing, analog front end, 2.4 GHz RF transceiver and integrated power amplifier, embedded SRAM, FLASH and power management subsystem all in a single 16 x 21.1 x 2.3 mm PCB module package thus providing a fully integrated solution that is ready for a wide range of embedded wireless IoT applications. The SL917 module is a complete solution offered with robust and fully-upgradeable software stacks, global regulatory certifications, advanced development and debugging tools, and documentation that simplifies and minimizes the development cycle of your end-product, helping to accelerate its time-to-market. The modules come with modular radio type approvals for various countries, including USA (FCC), Canada (IC/ISED) and Japan (MIC), and are in compliance with the relevant EN standards (including EN 300 328 v2.2.2) for the conformity with the directives and regulations in EU and UK.

SL917 applications include:

- Smart Home
- Security Cameras
- HVAC
- Smart Sensors
- Smart Appliances
- Health and Fitness
- Pet Tracker
- Smart Cities
- Smart Meters
- Industrial Wearable
- Smart Buildings
- Asset Tracking
- Smart hospitals

KEY FEATURES

- Wi-Fi 6 Single Band 2.4 GHz 20MHz 1x1 stream IEEE 802.11 b/g/n/ax
- Bluetooth LE 5.4
- Wi-Fi 6 Benefits: TWT for improved efficiency and longer battery life, MU-MIMO/OFDMA for Higher Throughput, network capacity and low latency
- Best in Class Device and Wireless Security
- WLAN Tx power up to +17.5 dBm with integrated PA
- Bluetooth LE Tx power up to +17 dBm with integrated PA
- WLAN Rx sensitivity as low as -95 dBm
- Wi-Fi Standby Associated mode current: 78 µA @ 1-second beacon listen interval
- In-package Flash up to 4MB,
- Embedded Wi-Fi, Bluetooth LE and networking stacks supporting wireless coexistence
- Operating temperature: -40 ºC to +85 ºC
- Operating supply range: 3.0 V - 3.63 V
- Supply voltage for GPIOs: 1.71 V to 3.63 V



1. Feature List

- **Memory**
  - Embedded Static Random Access Memory (SRAM) up to 672 KB total for multi-threaded processor
  - Flash up to 4 MB (embedded)
- **Security**
  - Secure Boot
  - Secure firmware upgrade through boot-loader, Secure OTA.
  - Secure Key storage and HW device identity with PUF
  - Secure Zone
  - Secure XIP (Execution in place) from flash
  - Secure Attestation
  - Hardware Accelerators: Advanced Encryption Standard (AES) 128/256/192, Secure Hash Algorithm (SHA) 256/384/512, Hash Message Authentication Code (HMAC), Random Number Generator (RNG), Cyclic Redundancy Check (CRC), SHA3, AES-Galois Counter Mode (GCM)/ Cipher based Message Authentication Code (CMAC), ChaCha-poly, True Random Number Generator (TRNG)
  - Software Accelerators: RSA, ECC
  - Programmable Secure Hardware Write protect for Flash sectors
  - Anti Rollback
  - Debug Lock
- **Wi-Fi**[1]
  - Compliant to single-spatial stream IEEE 802.11 b/g/n/ax with single band (2.4 GHz) support
  - Support for 20 MHz channel bandwidth for 802.11n and 802.11ax
  - Operating Modes: Wi-Fi 4 STA, Wi-Fi 6 (802.11ax) STA, Wi-Fi 4 AP, Enterprise STA, Wi-Fi 6 STA + Wi-Fi 4 AP, Wi- Fi + BLE
  - Support for 802.11ax 20 MHz non-AP STA mandatory features (such as OFDMA, MU-MIMO) and optional features of individual Target wake-up time (iTWT), Broadcast TWT (bTWT)[3], Intra PPDU power save[3], SU extended range (ER), DCM (Dual Carrier Modulation). DL MU-MIMO, DL/UL OFDMA, MBSSID, BFRP, Spatial Re-use , BSS Coloring, and NDP feedback upto 4 antennas
  - Transmit power up to +17.5 dBm with integrated PA
  - Receive sensitivity as low as -95 dBm
  - Data Rates: 802.11b: 1, 2, 5.5, 11; 802.11g: 6, 9, 12, 18, 24, 36, 48, 54Mbps ; 802.11n: MCS0 to MCS7; 802.11ax: MCS0 to MCS7
  - Operating Frequency Range [MHz]: 2412-2462 (North America, default), 2412-2472 (Europe, and other countries where applicable), 2412-2484 (Japan)
  - PTA Coexistence with Zigbee/Thread/Bluetooth
- **Intelligent Power Management**
  - Power optimizations leveraging multiple power domains and partitioned sub systems
  - Many system-, component-, and circuit-level innovations and optimizations
  - Different Power Modes
  - Deep sleep mode with only timer active – with and without RAM retention

- **Bluetooth**
  - Transmit power up to +17 dBm with integrated PA
  - Receive sensitivity — LE: -93 dBm, LR 125 Kbps: -104.5 dBm
  - Operating Frequency Range — 2.402 GHz - 2.480 GHz
  - Supports Bluetooth® Low Energy (LE): High Speed (1 Mbps and 2 Mbps) and Long Range (LE Coded PHYs, 125 Kbps and 500 Kbps; these are referred to as "LR" throughout this data sheet)
  - Advertising extensions
  - Data length extensions
  - LL privacy
  - LE dual role
  - BLE acceptlist
  - 2 Simultaneous BLE Connections (2 Peripheral, 2 Central, or 1 Central & 1 Peripheral)[3]
- **RF Features**
  - Integrated baseband processor with calibration memory
  - Integrated RF transceiver, high-power amplifier, balun and T/R switch
- **Embedded Wi-Fi Stack**[1]
  - Support for Embedded Wi-Fi STA mode, Wi-Fi Access point mode and Concurrent (AP+STA) mode
  - Supports advanced Wi-Fi Security features: WPA Personal, WPA2 Personal, WPA3 Personal, WPA/WPA2/WPA3 Enterprise in STA mode
  - Networking: Integrated IPv4/IPv6 stack, TCP, UDP, ICMP, ICMPv6, ARP, DHCP Client/Server, DHCPv6 Client, DNS Client, SSL3.0/TLS1.3 Client, SNTP, SNI
  - Applications: HTTP/s Client, HTTP/s Server[3], MQTT/s Client, AWS Client, Azure Client[3]
  - Sockets: BSD Sockets, IoT Sockets
  - Over-the-Air (OTA) Wireless firmware update
  - Provisioning using Wi-Fi AP[3] or BLE
- **Embedded Bluetooth Stack**
  - Support GAP profile
  - Support GATT profile
  - Support SMP
  - Support LE L2CAP
- **Wireless Sub-System Power Consumption**
  - Wi-Fi 4 Standby Associated mode current: 78 µA @ 1-second beacon listen interval
  - Wi-Fi 1 Mbps Listen current: 14 mA
  - Wi-Fi LP mode Rx current: 21 mA
  - Deep sleep current 5 µA, Standby current (352K RAM retention) 12.5 µA
- **Operating Conditions**
  - Operating supply range : 3.0 V to 3.63 V
  - Supply voltage for GPIOs: 1.71 V to 3.63 V
  - Operating temperature: -40 ºC to +85 ºC

- **Software and Regulatory Certifications**
  - Wi-Fi Alliance: Wi-Fi 4[3], Wi-Fi 6[3]
  - Bluetooth SIG Qualification[3]
  - Regulatory certifications: [FCC (USA), IC/ISED (Canada), CE (EU), UKCA (UK), MIC (Japan), KC (South Korea), NCC (Taiwan), SRRC (China), ACMA (Australia), RSM (New Zealand)][3]

Note:

1. For a detailed list of software features and available profiles, refer to the Software Reference Manuals or contact Ezurio for availability.
2. All power and performance numbers are under ideal conditions.
3. For information about Software roadmap features and additional certification information, contact Ezurio for availability and timeline. Currently, we have certifications for FCC (USA), IC/ISED (Canada), CE (EU), UKCA (UK), MIC (Japan), ACMA (Australia), RSM (New Zealand), but not yet for KC (South Korea), NCC (Taiwan), SRRC (China). These last three are pending.

2. Ordering Information

Part #	Description
453-00219R	Module, Veda SL917, 4MB Flash, NCP, Trace Pad, Tape and Reel
453-00219C	Module, Veda SL917, 4MB Flash, NCP, Trace Pad, Cut Tape
453-00221R	Module, Veda SL917, 4MB Flash, NCP, Integrated Antenna, Tape and Reel
453-00221C	Module, Veda SL917, 4MB Flash, NCP, Integrated Antenna, Cut Tape

Veda Click Boards (from MIKROE.com)

Part #	Description	Link
Veda SL917 Click (Integrated Antenna)	Click Board - Veda SL917 NCP Module – Integrated Antenna	See at MIKROE.com
Veda SL917 Click (RF Trace Pad or External Antenna)	Click Board - Veda SL917 NCP Module – RF Trace Pad + FlexPIFA (MHF4)	See at MIKROE.com

3. Applications

Smart Home

Smart Locks, Motion/Entrance Sensors, Water Leak sensors, Smart plugs/switches, Light Emitting Diode (LED) lights, Door-bell cameras, Washers/Dryers, Refrigerators, Thermostats, Consumer Security cameras, Voice Assistants, etc.

Other Consumer Applications

Toys, Anti-theft tags, Smart dispensers, Weighing scales, Fitness Monitors, Smart Glasses, Blood pressure monitors, Blood sugar monitors, Portable cameras, etc.

Other Applications (Medical, Industrial, Retail, Agricultural, Smart City, etc.)

Healthcare Tags, Industrial Wearables, Infusion pumps, Sensors/actuators in Manufacturing, Electronic Shelf labels, Agricultural sensors, Product tracking tags, Smart Meters, Parking sensors, Street LED lighting, Automotive After-market, Security Cameras, Gate- ways, etc.

4. Block Diagrams

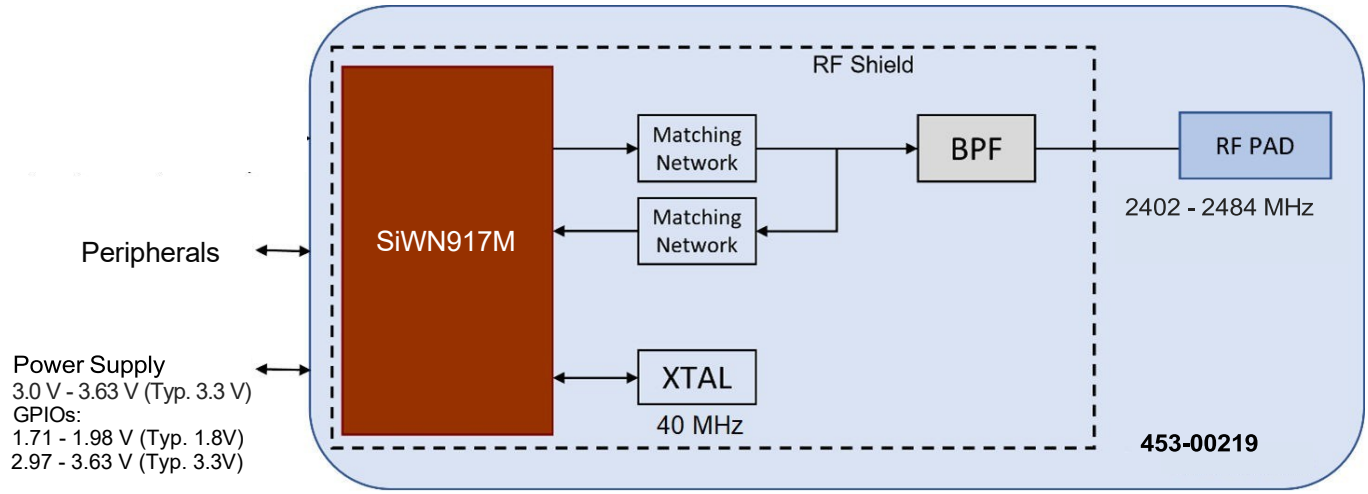


Figure 4.1. 453-00219 (Without Antenna) Module Block Diagram

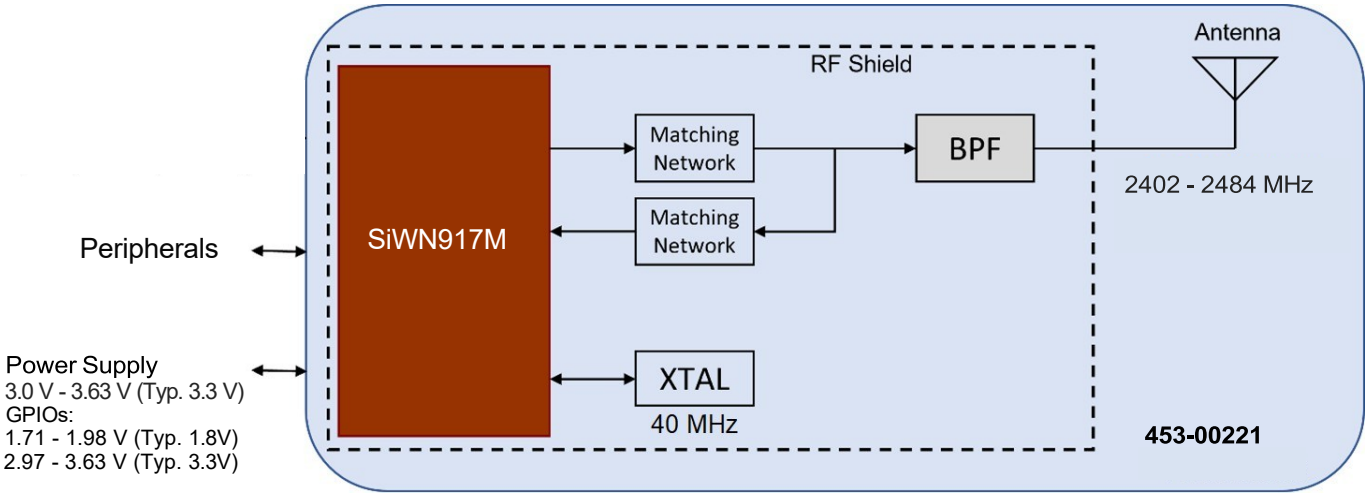


Figure 4.2. 453-00221 (With Antenna) Module Block Diagram

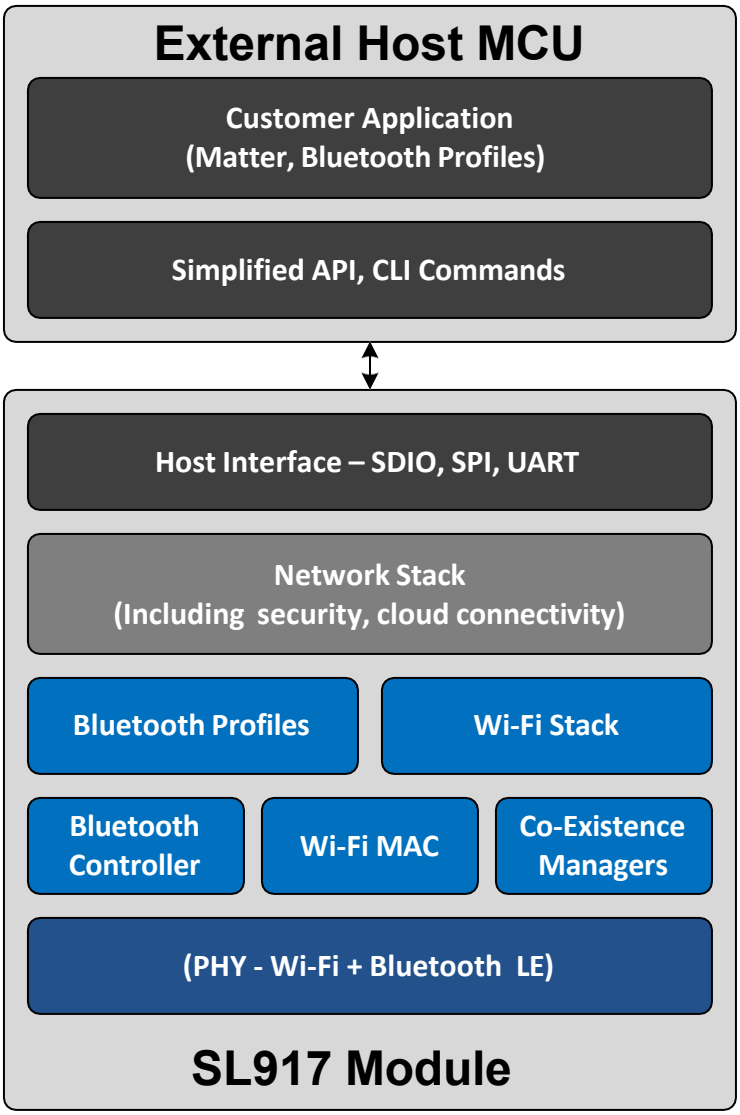


Figure 4.3. SL917 NCP Software Architecture

Note: Customer can connect multiple hosts, but only one host interface can be active after power-on.

5. System Overview

5.1 Introduction

An SL917 module running the NCP mode of operation includes a Network Wireless Processor (NWP) 4-Threaded processor running up to 160 MHz. All the networking and wireless stacks run on independent threads of the NWP. In addition, the NWP subsystem also acts as the secure processing domain and takes care of secure boot, secure firmware update and provides access to security accelerators and secure peripherals through pre-defined APIs. The NWP based "Networking, Security and Wireless subsystem" have power, clocks/ PLLs, bus-matrices, and memory.

5.2 WLAN

- Compliant to single-spatial stream IEEE 802.11 b/g/n/ax with single band (2.4 GHz) support
- Support for 20 MHz channel bandwidth for 802.11n and 802.11ax.
- Operating Modes: Wi-Fi 4 STA, Wi-Fi 6 (802.11ax) STA, Wi-Fi 4 AP, Enterprise STA, Wi-Fi 6 STA + Wi-Fi 4 AP, Wi-Fi + BLE
- Wi-Fi 6 Features: Individual Target wake-up time (iTWT), Broadcast TWT (bTWT),SU extended range (ER), DCM (Dual Carrier Modulation), DL MU-MIMO, DL/UL OFDMA, MBSSID, BFRP, Spatial Re-use, BSS Coloring, and NDP feedback up to 4 antennas
- Integrated PA
- Data Rates—802.11b: up to 11 Mbps; 802.11g: up to 54 Mbps; 802.11n: MCS0 to MCS7; 802.11ax: MCS0 to MCS7
- Operating Frequency Range [MHz]: 2412-2462 (North America, default), 2412-2472 (Europe, and other countries where applicable), 2412-2484 (Japan)

5.2.1 MAC

- Conforms to IEEE 802.11b/g/n/ax standards for MAC
- Hardware accelerators for AES
- WPA, WPA2, WPA3 and WMM support
- AMPDU aggregation for high performance
- Firmware downloaded from host based on application
- Hardware accelerators for DH (for WPS) and ECDH

5.2.2 Baseband Processing

- Supports 11b: DSSS for 1, 2 Mbps and CCK for 5.5, 11 Mbps
- Supports all OFDM data rates:
  - 802.11g: 6, 9, 12, 18, 24, 36, 48, 54 Mbps
  - 802.11ax, 802.11n: MCS 0 to MCS 7
- High-performance multipath handling in OFDM, DSSS, and CCK modes

5.3 Bluetooth

Key Features

- Transmit power up to +17 dBm with integrated PA
- Receive sensitivity — LE: -93 dBm, LR 125 Kbps: -104.5 dBm
- Operating Frequency Range — 2.402 GHz - 2.480 GHz
- Supports Bluetooth® Low Energy (LE): High Speed (1 Mbps and 2 Mbps) and Long Range (LE Coded PHYs, 125 Kbps and 500 Kbps)
- Advertising extensions
- Data length extensions
- LL privacy
- LE dual role
- BLE acceptlist
- Two simultaneous BLE connections (2 peripheral or 2 central, or 1 central and 1 peripheral)

5.3.1 MAC

Link Manager

- Creation, modification & release of physical links
- Connection establishment between Link managers of two Bluetooth devices
- Link supervision is implemented in Link Manager
- Link power control is done depending on the inputs from Link Controller
- Enabling & disabling of encryption & decryption on logical links
- AES hardware acceleration

Link Controller

- Encodes and decodes header of BLE packets
- Manages flow control, acknowledgment, re-transmission requests, etc.
- Stores the last packet status for all physical transports
- Indicates the success status of packet transmission to upper layers
- Indicates the link quality to the LMP layer

Device Manager

- Executes HCI Commands
- Controls Scan & Connection processes
- Controls all BLE Device operations except data transport operations
- BLE Controller state transition management
- Anchor point synchronization & management
- Scheduler

5.3.2 Baseband Processing

- Supports BLE 1Mbps, 2Mbps and long range 125kbps, 500kbps

5.4 RF Transceiver

- The SL917 features two highly configurable RF transceivers supporting WLAN 11b/g/n/ax and Bluetooth LE wireless protocols. Both RF transceivers together operating in multiple modes covering High Performance (HP) and Low Power (LP) operations. List of operating modes are given in next section.
- It contains two fully integrated fractional-N frequency synthesizers having reference from internal oscillator with 40 MHz crystal. One of the synthesizer is a low power architecture which also caters single-bit data modulation feature for Bluetooth LE protocols.

5.4.1 Receiver and Transmitter Operating Modes

The available radio operating modes are as follows:

- WLAN HP TX - WLAN High-Performance Transmitter
- WLAN HP RX - WLAN High-Performance Receiver
- WLAN LP RX - WLAN Low-Power Receiver
- BLE HP TX - Bluetooth LE High-Performance Transmitter
- BLE HP RX - Bluetooth LE High-Performance Receiver
- BLE LP TX - Bluetooth LE Low-Power Transmitter
- BLE LP RX - Bluetooth LE Low-Power Receiver

Note: All the TX / RX modes are automatically controlled by radio firmware and not individually selectable.

5.5 Security Features

- Secure Boot
- Secure OTA Firmware update
- TRNG : Generates high-entropy random numbers based on RF noise, increasing the effort/time needed to expose secret keys
- Secure Zone
- Secure Key storage : HW device identity and key storage with PUF
- Debug Lock
- Anti Rollback : Firmware downgrade to a lower version is prohibited through OTP to prevent the use of older, potentially vulnerable FW version
- Encrypted XIP from flash with XTS/CTR mode
- Secure Attestation : Allows a device to authenticate its identity using a cryptographically signed token and exchange of secret keys
- Hardware Accelerators: AES128/256/192, SHA256/384/512, HMAC, RNG, CRC, SHA3, AES-GCM/ CMAC, ChaCha-poly
- Software Implementation: RSA and ECC

5.6 Embedded Wi-Fi Software

- The wireless software package supports Embedded Wi-Fi (802.11 b/g/n/ax) Client mode, Wi-Fi Access point mode (up to 4 clients), and Enterprise Security in client mode.
- The software package includes complete firmware and application profiles.
- It has a wireless coexistence manager to arbitrate between protocols.

5.6.1 Security

Wireless software supports multiple levels of security capabilities available for the development of IoT devices.

- Accelerators: AES128/256
- WPA/WPA2/WPA3-Personal, WPA/WPA2/WPA3 Enterprise for Client

5.7 Power Architecture

The Power Control Hardware implements the control sequences for transitioning between different power states (Active/Standby/Sleep/ Shutdown).

5.7.1 Highlights

- Two integrated buck switching regulators (High performance and ULP) to enable efficient Voltage Scaling across wide operating mode currents ranging from <1 µA to 250 mA
- Multiple voltage domains with Independent voltage scaling of each domain.
- Fine grained power-gating including peripherals, buses and pads, thereby reducing power consumption when the peripheral/buses/ pads are inactive.
- Flexible switching between different Active states with controls from Software.
- Hardware based wakeup from Standby/Sleep/Shutdown states.
- All the peripherals are clock gated by default thereby reducing the power consumption in inactive state.
- Low wakeup times as configurable by Software.

5.7.2 Power Management

The SL917 NCP modules have an internal power management subsystem, including DC-DC converters and linear regulators. This subsystem generates all the voltages required by the module to operate from a wide variety of input sources.

- Input voltage (3.3 V) on pin VBATT
- Input voltage (1.8 V or 3.3 V) on pin IO_VDD, SDIO_IO_VDD and ULP_IO_VDD
- Input voltage (1.8 V) on pin FLASH_IO_VDD
- Nominal Output - 1.8 V and 48 mA maximum load on pin 1V8_LDO

5.8 Memory Architecture

There are on chip Read Only Memory(ROM), Random Access Memory(RAM) and in-package flash connectivity. Sizes of ROM/RAM/ flash will vary depending on the chip configuration.

The NWP processor has the following memory:

- Embedded SRAM up to 672 KB total
- 448 KB of ROM which holds the Secure primary bootloader, Network Stack, Wireless stacks and security functions
- 16 KB of Instruction cache (I cache)
- Flash up to 4 MB (in-package)
- eFuse of 1024 bytes (used to store primary boot configuration, security and calibration parameters)

5.9 Low Power Modes

It supports Ultra-low power consumption with multiple power modes to reduce system energy consumption.

- Voltage and Frequency Scaling
- Deep sleep (ULP) mode with only the sleep timer active – with and without RAM retention
- Wi-Fi standby associated mode with automatic periodic wake-up
- Automatic clock gating of the unused blocks or transit the system from Normal to ULP mode.

5.9.1 ULP Mode

In Ultra Low Power mode, the deep sleep manager has control over the processors and subsystems and controls their active and sleep states. During deep sleep, the always-on logic domain operates on a lowered supply and a 32 kHz low-frequency clock to reduce power consumption. The ULP mode supports the following wake-up options:

- Timeout wakeup - Exit sleep state after programmed timeout value.
- GPIO Based Wakeup: Exit sleep state when GPIO goes High/Low based on programmed polarity.

6. Pinout and Pin Description

6.1 Pin Diagram

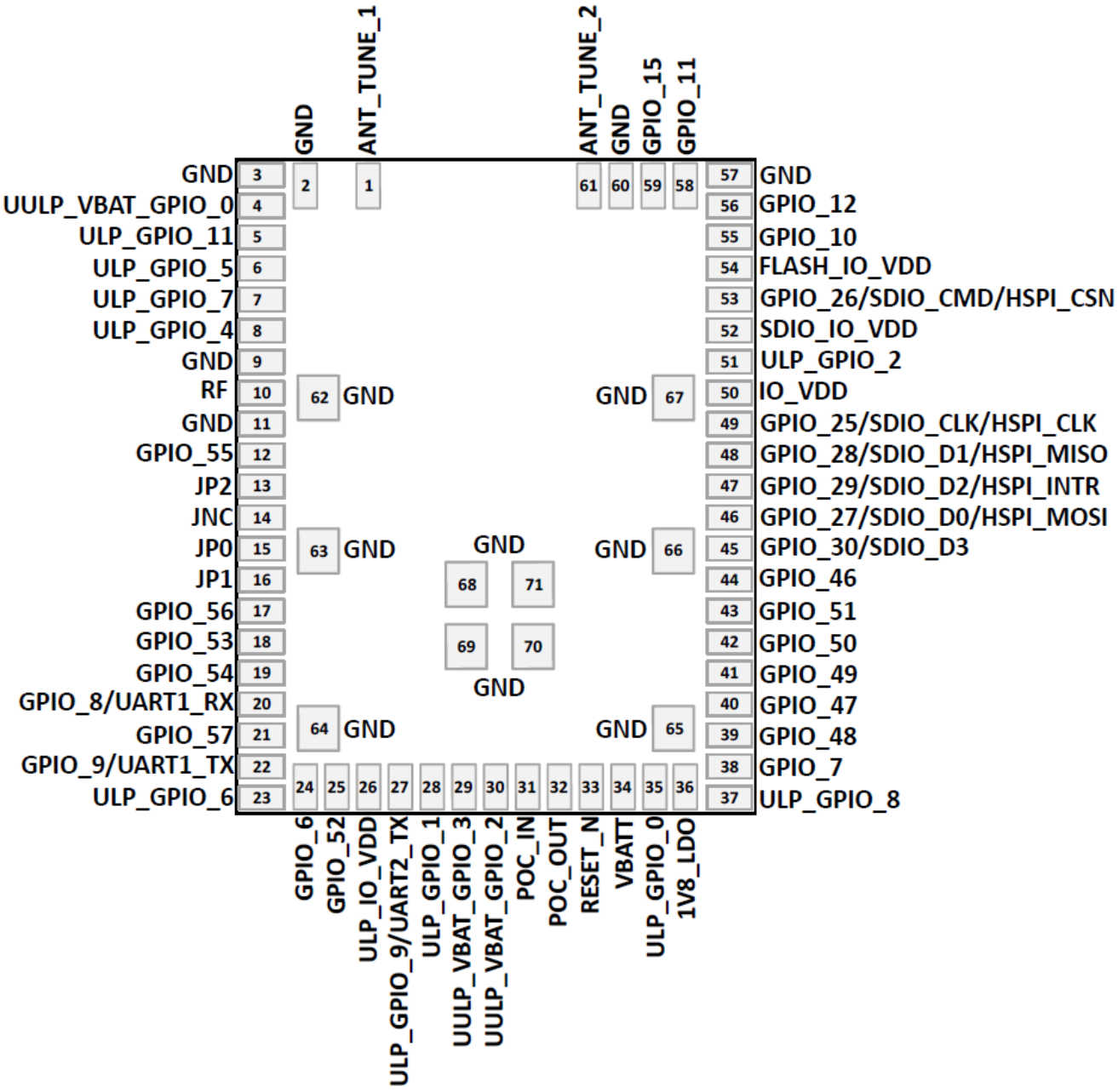


Figure 6.1. SL917 NCP Pin Diagram

6.2 Pin Description

Table 6.1. List of Pins in IC (SiWN917M), Not Available in the Modules

Pin Name	QFN I/O Supply Domain	Direction	Initial State (Power up, Active Reset)	Description
RF_BLETX	RF_AVDD	Output	NA	BLE 8 dBm RF Output
ULP_GPIO_10	ULP_IO_VDD	Inout	HighZ	Default: HighZ Sleep: HighZ
XTAL_32KHZ_P	NA	Inout	NA	Analog Pin. 32KHZ XTAL Connection
XTAL_32KHZ_N	NA	Inout	NA	Analog Pin. 32KHZ XTAL Connection
UULP_VBAT_GPIO_1	VBATT	Inout	HighZ	Default: High Sleep: High

6.2.1 RF and Control Interfaces

Table 6.2. Chip Packages - RF and Control Interfaces

Pin Name	Pin No.	I/O Supply Do-main	Direction	Initial State (Power up Active Reset)	Description
ANT_TUNE_1	1	N/A	Input	N/A	**453-00221:** External fine-tuning option for the integral antenna; connect same tun- ing circuit on both ANT_TUNE1 and ANT_TUNE2 pins; leave floating if no fine-tuning is desired on the integral antenna; **453-00219:** leave this pin floating
RF	10	VBATT	Inout	N/A	Connect to antenna with a 50-Ω impedance as per the reference schematics
POC_IN	31	VBATT	Input	NA	This is an input to the chip which resets all analog and digital blocks in the device. It should be made high only after supplies are valid.
POC_OUT	32	VBATT	Output	NA	This is internally generated. Initially, it is low. But it becomes high when the supply (VBATT) is valid.
RESET_N	33	VBATT	Inout	NA	Active-low reset asynchronous reset signal, which resets only digital blocks. RESET_N will be pulled low if POC_IN is low.
ANT_TUNE_2	61	N/A	Input	N/A	**453-00221:** External fine-tuning option for the integral antenna; connect same tun- ing circuit on both ANT_TUNE1 and ANT_TUNE2 pins; leave floating if no fine-tuning is desired on the integral antenna; **453-00219:** leave this pin floating

6.2.2 Power and Ground Pins

Table 6.3. Chip Packages - Power and Ground Pins

Pin Name	Pin No.	Type	Direction	Description
ULP_IO_VDD	26	Power	Input	I/O supply for ULP I/Os.
VBATT	34	Power	Input	Power supply for the module.
1V8_LDO	36	Power	Output	Output of 1.8V LDO which is used for Flash supply.
IO_VDD	50	Power	Input	I/O Supply for GPIOs. Refer to GPIOs section for details on which GPIOs have this as the I/O supply.
SDIO_IO_VDD	52	Power	Input	I/O Supply for SDIO I/Os. Refer to GPIOs section for details on which GPIOs have this as the I/O supply.
FLASH_IO_VDD	54	Power	Input	I/O Supply for module embedded flash. Connect to 1V8_LDO as per Reference Schematics.
GND	2, 3, 9, 11, 57, 60, 62-71	Ground		Common ground pins.

6.2.3 Peripheral Interfaces

Table 6.4. Chip Packages - Perpheral Interfaces

Pin Name	Pin No.	I/O Supply Domain	Direction	Initial State (Power up Active Reset)	Description
UULP_VBAT_GPIO_0	4	VBATT	Output	High	**Default**: High **Sleep**: High This pin can be configured by software to be any of the following. • SLEEP_IND_FROM_DEV: This signal is used to send an indication to the Host processor. An indication is sent when the chip enters (logic low) and exits (logic high) the ULP Sleep mode.
ULP_GPIO_11	5	ULP_IO_VDD	Inout	HighZ	**Default**: HighZ **Sleep**: HighZ
ULP_GPIO_5	6	ULP_IO_VDD	Inout	HighZ	**Default**: HighZ **Sleep**: HighZ
ULP_GPIO_7	7	ULP_IO_VDD	Inout	HighZ	**Default**: HighZ **Sleep**: HighZ
ULP_GPIO_4	8	ULP_IO_VDD	Inout	HighZ	**Default**: HighZ **Sleep**: HighZ
GPIO_55	12	IO_VDD	Inout	HighZ	**Default**: HighZ **Sleep**: HighZ
JP2	13	IO_VDD	Input	Pullup	**Default:** JP2 **Sleep**: HighZ JP2 - Reserved. Connect to a test point for debugging purposes
JNC	14	IO_VDD	Output	Pullup	**Default:** JNC **Sleep**: HighZ JNC - Reserved. Connect to a test point for debugging purposes
JP0	15	IO_VDD	Input	Pullup	**Default:** JP0 **Sleep**: HighZ JP0 - Reserved. Connect to a test point for debugging purposes
JP1	16	IO_VDD	Input	Pullup	**Default:** JP1 **Sleep**: HighZ JP1 - Reserved. Connect to a test point for debugging purposes

<table>
<tr><th>Pin Name</th><th>Pin No.</th><th>I/O Supply Domain</th><th>Direction</th><th>Initial State (Power up Active Reset)</th><th>Description</th></tr>
<tr><td>GPIO_56</td><td>17</td><td>IO_VDD</td><td>Inout</td><td>HighZ</td><td>Default: HighZ
Sleep: HighZ</td></tr>
<tr><td>GPIO_53</td><td>18</td><td>IO_VDD</td><td>Inout</td><td>HighZ</td><td>Default: HighZ
Sleep: HighZ</td></tr>
<tr><td>GPIO_54</td><td>19</td><td>IO_VDD</td><td>Inout</td><td>HighZ</td><td>Default: HighZ
Sleep: HighZ</td></tr>
<tr><td>GPIO_8/UART1_RX</td><td>20</td><td>IO_VDD</td><td>Inout</td><td>HighZ</td><td><table><tr><th>Host</th><th>Default</th><th>Sleep</th></tr><tr><td>UART</td><td>UART1_RX - UART Host interface serial input.</td><td>HighZ</td></tr><tr><td>Non UART</td><td>HighZ</td><td>HighZ</td></tr></table></td></tr>
<tr><td>GPIO_57</td><td>21</td><td>IO_VDD</td><td>Inout</td><td>HighZ</td><td>Default: HighZ
Sleep: HighZ</td></tr>
<tr><td>GPIO_9/UART1_TX</td><td>22</td><td>IO_VDD</td><td>Inout</td><td>HighZ</td><td><table><tr><th>Host</th><th>Default</th><th>Sleep</th></tr><tr><td>UART</td><td>UART1_TX - UART Host interface serial output.</td><td>HighZ</td></tr><tr><td>Non UART</td><td>HighZ</td><td>HighZ</td></tr></table></td></tr>
<tr><td>ULP_GPIO_6</td><td>23</td><td>ULP_IO_VDD</td><td>Inout</td><td>HighZ</td><td>Default: HighZ
Sleep: HighZ
This pin can be configured by software to be any of the following.
PTA_PRIO: "PTA Priority" input signal is part of 3-wire coexistence (Packet Traffic Arbitration) interface.</td></tr>
<tr><td>GPIO_6</td><td>24</td><td>IO_VDD</td><td>Inout</td><td>HighZ</td><td>Default: HighZ
Sleep: HighZ</td></tr>
<tr><td>GPIO_52</td><td>25</td><td>IO_VDD</td><td>Inout</td><td>HighZ</td><td>Default: HighZ
Sleep: HighZ</td></tr>
<tr><td>ULP_GPIO_9/ UART2_TX</td><td>27</td><td>ULP_IO_VDD</td><td>Inout</td><td>HighZ</td><td>Default: UART2_TX- Debug UART Interface serial output
Sleep: HighZ</td></tr>
</table>

Pin Name	Pin No.	I/O Supply Domain	Direction	Initial State (Power up Active Reset)	Description
ULP_GPIO_1	28	ULP_IO_VDD	Inout	HighZ	**Default:** HighZ **Sleep**: HighZ This pin can be configured by software to be any of the following • PTA_REQ: "PTA Request" input signal is part of 3-wire coexistence (Packet Traffic Arbitration) interface.
UULP_VBAT_GPIO_3	29	VBATT	Inout	HighZ	**Default:** HighZ **Sleep:** EXT_32KHZ_IN This pin can be configured by software to be any of the following. • EXT_32KHZ_IN: This pin can be used to feed external clock from a host processor or from external crystal oscillator.
UULP_VBAT_GPIO_2	30	VBATT	Inout	HighZ	**Default:** HighZ **Sleep:** ULP_WAKEUP This pin can be configured by software to be any of the following. • HOST_BYP_ULP_WAKEUP: This signal has two functionalities – one during the bootloading process and one after the bootloading. During bootloading, this signal is an active-high input to indicate that the bootloader should bypass any inputs from the Host processor and continue to load the default firmware from Flash. After bootloading, this signal is an active-high input to indicate that the module should wakeup from its Ultra Low Power (ULP) sleep mode.
ULP_GPIO_0	35	ULP_IO_VDD	Inout	HighZ	**Default**: HighZ **Sleep**: HighZ
ULP_GPIO_8	37	ULP_IO_VDD	Inout	HighZ	**Default**: HighZ **Sleep**: HighZ
GPIO_7	38	IO_VDD	Inout	HighZ	**Default:**HighZ **Sleep**: HighZ This pin can be configured by software to be any of the following. PTA_GRANT: "PTA Grant" output signal is part of 3-wire coexistence (Packet Traffic Arbitration) interface.
GPIO_48	39	IO_VDD	Inout	HighZ	**Default:** HighZ **Sleep**: HighZ
GPIO_47	40	IO_VDD	Inout	HighZ	**Default:** HighZ **Sleep**: HighZ

<table>
<tr><th>Pin Name</th><th>Pin No.</th><th>I/O Supply Domain</th><th>Direction</th><th>Initial State (Power up Active Reset)</th><th>Description</th></tr>
<tr><td>GPIO_49</td><td>41</td><td>IO_VDD</td><td>Inout</td><td>HighZ</td><td>Default: HighZ
Sleep: HighZ</td></tr>
<tr><td>GPIO_50</td><td>42</td><td>IO_VDD</td><td>Inout</td><td>HighZ</td><td>Default: HighZ
Sleep: HighZ</td></tr>
<tr><td>GPIO_51</td><td>43</td><td>IO_VDD</td><td>Inout</td><td>HighZ</td><td>Default: HighZ
Sleep: HighZ</td></tr>
<tr><td>GPIO_46</td><td>44</td><td>IO_VDD</td><td>Inout</td><td>HighZ</td><td>Default: HighZ
Sleep: HighZ</td></tr>
<tr><td>GPIO_30/SDIO_D3</td><td>45</td><td>SDIO_IO_VDD</td><td>Inout</td><td>Pullup</td><td><table><tr><th>Host</th><th>Default</th><th>Sleep</th></tr><tr><td>SDIO</td><td>SDIO_D3 - SDIO interface Data3 signal</td><td>HighZ</td></tr><tr><td>Non SDIO,SPI</td><td>HighZ</td><td>HighZ</td></tr></table></td></tr>
<tr><td>GPIO_27/SDIO_D0/ HSPI_MOSI</td><td>46</td><td>SDIO_IO_VDD</td><td>Inout</td><td>HighZ</td><td><table><tr><th>Host</th><th>Default</th><th>Sleep</th></tr><tr><td>SDIO</td><td>SDIO_D0 - SDIO interface Data0 signal</td><td>HighZ</td></tr><tr><td>SPI</td><td>HSPI_MOSI - SPI Slave interface Master-Out-Slave-In signal</td><td>HighZ</td></tr><tr><td>Non SDIO,SPI</td><td>HighZ</td><td>HighZ</td></tr></table></td></tr>
<tr><td>GPIO_29/SDIO_D2/ HSPI_INTR</td><td>47</td><td>SDIO_IO_VDD</td><td>Inout</td><td>HighZ</td><td><table><tr><th>Host</th><th>Default</th><th>Sleep</th></tr><tr><td>SDIO</td><td>SDIO_D2 - SDIO interface Data2 signal</td><td>HighZ</td></tr><tr><td>SPI</td><td>HSPI_INTR - SPI Slave interface Interrupt Signal to the Host</td><td>HighZ</td></tr><tr><td>Non SDIO,SPI</td><td>HighZ</td><td>HighZ</td></tr></table></td></tr>
</table>

<table>
<tr><th>Pin Name</th><th>Pin No.</th><th>I/O Supply Domain</th><th>Direction</th><th>Initial State (Power up Active Reset)</th><th>Description</th></tr>
<tr><td>GPIO_28/SDIO_D1/ HSPI_MISO</td><td>48</td><td>SDIO_IO_VDD</td><td>Inout</td><td>HighZ</td><td>
<table>
<tr><th>Host</th><th>Default</th><th>Sleep</th></tr>
<tr><td>SDIO</td><td>SDIO_D1 - SDIO interface Data1 signal</td><td>HighZ</td></tr>
<tr><td>SPI</td><td>HSPI_MISO - SPI Slave interface Master-In-Slave-Out signal</td><td>HighZ</td></tr>
<tr><td>Non SDIO,SPI</td><td>HighZ</td><td>HighZ</td></tr>
</table>
</td></tr>
<tr><td>GPIO_25/SDIO_CLK/ HSPI_CLK</td><td>49</td><td>SDIO_IO_VDD</td><td>Inout</td><td>HighZ</td><td>
<table>
<tr><th>Host</th><th>Default</th><th>Sleep</th></tr>
<tr><td>SDIO</td><td>SDIO_CLK - SDIO interface clock</td><td>HighZ</td></tr>
<tr><td>SPI</td><td>HSPI_CLK - SPI Slave interface clock</td><td>HighZ</td></tr>
<tr><td>Non SDIO,SPI</td><td>HighZ</td><td>HighZ</td></tr>
</table>
</td></tr>
<tr><td>ULP_GPIO_2</td><td>51</td><td>ULP_IO_VDD</td><td>Input</td><td>HighZ</td><td>Default: HighZ
Sleep: HighZ</td></tr>
<tr><td>GPIO_26/SDIO_CMD/ SPI_CSN</td><td>53</td><td>SDIO_IO_VDD</td><td>Inout</td><td>HighZ</td><td>
<table>
<tr><th>Host</th><th>Default</th><th>Sleep</th></tr>
<tr><td>SDIO</td><td>SDIO_CMD - SDIO interface CMD signal</td><td>HighZ</td></tr>
<tr><td>SPI</td><td>HSPI_CSN - Active-low Chip Select signal of SPI Slave interface</td><td>HighZ</td></tr>
<tr><td>Non SDIO,SPI</td><td>HighZ</td><td>HighZ</td></tr>
</table>
</td></tr>
</table>

Pin Name	Pin No.	I/O Supply Domain	Direction	Initial State (Power up Active Reset)	Description
GPIO_10	55	IO_VDD	Inout	HighZ	**Default:** HighZ **Sleep:** HighZ This pin can be configured by software to be any of the following. • HOST_WAKEUP_IND: This is used as indication from host to dev that host is ready to take the packet and device can transfer the packet to host. This is supported only in UART host mode. • It is part of Wake-on-Wireless functionality. Please check with Silabs for availability of this functionality
GPIO_12	56	IO_VDD	Inout	HighZ	**Default:** HighZ **Sleep**: HighZ This pin can be configured by software to be any of the following. • UART1_RTS - UART interface Request to Send, if UART Host Interface flow control is enabled.
GPIO_11	58	IO_VDD	Inout	HighZ	**Default:** HighZ **Sleep:** HighZ This pin can be configured by software to be any of the following. • WAKEUP_FROM_DEV: Used as a wakeup indication to host from device. • It is part of Wake-on-Wireless functionality. It is recommended that one use an external weak pull-down resistor on this pin and software has to be configured suitably. • Please check with Silabs for availability of this functionality.
GPIO_15	59	IO_VDD	Inout	HighZ	**Default:** HighZ **Sleep**: HighZ This pin can be configured by software to be any of the following. • UART1_CTS - UART interface Clear to Send, if UART Host Interface flow control is enabled.

7. Electrical Specifications

7.1 Absolute Maximum Ratings

Stresses beyond those listed below may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions beyond those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. For more information on the available quality and reliability data, see the Quality and Reliability Monitor Report at https://www.silabs.com/about-us/quality.

Note: All the specifications are preliminary and subject to change.

Table 7.1. Absolute Maximum Ratings

Parameter	Symbol	Test Conditon	Min	Typ	Max	Unit
Storage temperature	T_{store}		-40	—	125	°C
Maximum junction temperature	$T_{j(max)}$			—	125	°C
3.3V power supply for the on-chip Buck, RF circuit, and UULP IOs	VBATT		-0.5	—	3.63	V
I/O supply for GPIOs	IO_VDD		-0.5	—	3.63	V
I/O supply for SDIO I/Os	SDIO_IO_VDD		-0.5	—	3.63	V
I/O supply for QSPI flash signals	FLASH_IO_VDD		-0.5	—	3.63	V
I/O supply for ULP I/Os	ULP_IO_VDD		-0.5	—	3.63	V
DC voltage on any I/O pin [1]	V_{IO_PIN}		-0.5	—	VDD + 0.5	V
Total average max current into chip	I_{pmax}		—	—	500	mA
Current per I/O pin	I_{IOMAX}	Sink	—	—	100	mA
		Source	—	—	100	mA

Note:
1. VDD = I/O supply domain pin. Refer to pin description tables for supply domain associated with each I/O.

7.2 Recommended Operating Conditions

Note: The device may operate continuously at the maximum allowable ambient $T_{ambient}$ rating as long as the maximum junction $T_{junction(max)}$ is not exceeded. For an application with significant power dissipation, the allowable $T_{ambient}$ may be lower than the maximum $T_{ambient}$ rating. $T_{ambient}$ = $T_{junction(max)}$ - (Θ_{JA} x Power Dissipation). Refer to the Thermal Characteristics table for Θ_{JA}.

Table 7.2. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Units
Ambient temperature	$T_{ambient}$		-40	25	85	°C
Junction temperature	$T_{junction}$				105	°C
3.3V power supply for the on-chip Buck, RF Power Amplifier, UULP I/Os	VBATT		3.0	3.3	3.63	V
I/O supply for Flash	FLASH_IO_VDD		1.71	1.8	1.98	V
I/O supply for GPIOs	IO_VDD[1]	1.8 V nominal operation	1.71	1.8	1.98	V
		3.3 V nominal operation	2.97	3.3	3.63	
I/O supply for SDIO I/Os	SDIO_IO_VDD[1]	1.8 V nominal operation	1.71	1.8	1.98	V
		3.3 V nominal operation	2.97	3.3	3.63	
I/O supply for ULP I/Os	ULP_IO_VDD[1]	1.8 V nominal operation	1.71	1.8	1.98	V
		3.3 V nominal operation	2.97	3.3	3.63	

Note:

1. Supplies can operate at a nominal 3.3 V or 1.8 V level independent of the other supplies in the system.

7.3 DC Characteristics

7.3.1 RESET_N Pin

Table 7.3. RESET_N Pin

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
High level input voltage	V_{IH}	RESET_N pin, VBATT = 3.3 V	0.8 * VBATT	—	—	V
Low level input voltage	V_{IL}	RESET_N pin, VBATT = 3.3 V	—	—	0.3 * VBATT	V

7.3.2 Power On Control (POC) and Reset

There are three signals involved in power-on control and reset of the device:

- POC_IN: When pulled low, POC_IN will reset all of the internal blocks in the device. The POC_IN signal can be controlled either by external circuitry, by POC_OUT, or both.
- RESET_N: RESET_N is an open-drain signal which will be pulled low during a chip reset. It is released after POC_IN is high. RESET_N should be connected to an RC circuit to fulfill the timing requirements shown in Figure 7.1 Power Up Sequence on page 27.
- POC_OUT: The POC_OUT signal is the output of the internal blackout supply monitor. POC_OUT is distributed to all I/O cells to prevent the I/O cells from powering up in an undesired configuration and is also used inside the IC to place the IC in a safe state until a valid supply is available for proper operation. During power up, POC_OUT stays low until the VBATT reaches 1.6 V. After the VBATT supply exceeds 1.6 V, POC_OUT becomes high and normal operation begins. If VBATT becomes lower than the blackout threshold voltage, POC_OUT will return low. POC_OUT can be used to provide chip reset by connecting to POC_IN in a loopback configuration.

The recommended schematic for the reset signals is shown in Figure 8.4 Reset Configuration on page 50.

Figure 7.1 Power Up Sequence on page 27 shows the signal timing when POC_OUT, POC_IN, and RESET_N are connected per the recommended schematic. The POC_IN-to-RESET_N delay will occur when POC_IN transitions from low to high.

In this configuration the system only has to control the supply (VBATT) during power-up and power down and need not control POC_IN externally. On power-up the chip will be reset internally. The power-down sequence will follow VBATT and external control of POC_IN is not required.

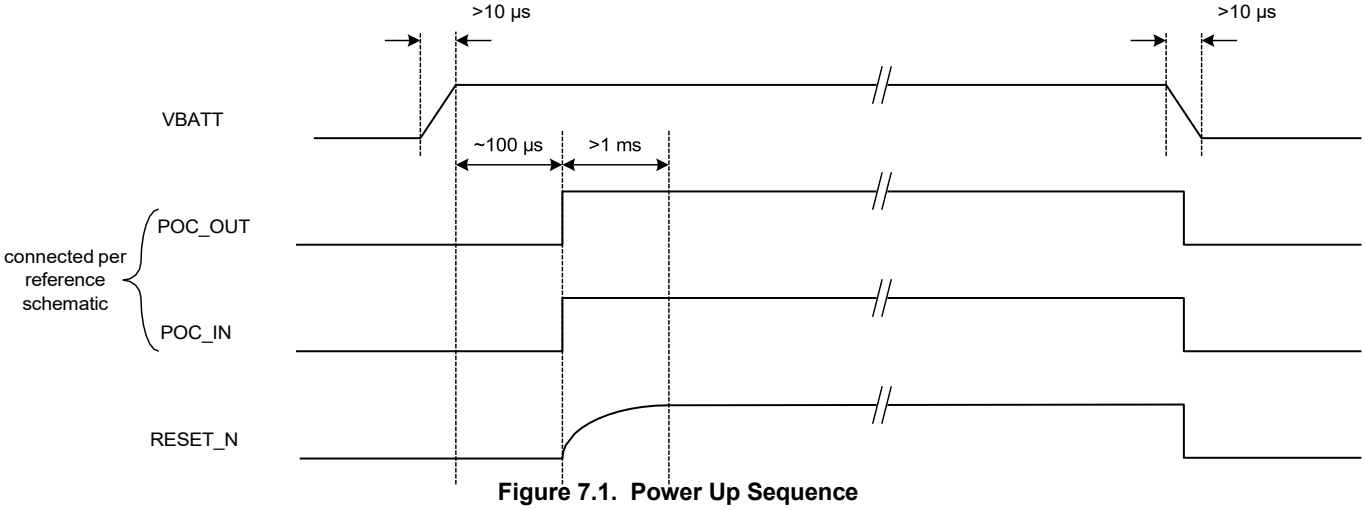


Figure 7.1. Power Up Sequence

If the chip is to be reset from an external host device while powered up, the POC_IN signal should be pulled low for at least 10 ms as shown in Figure 7.2 External Reset via POC_IN on page 27. Upon release of POC_IN, the POC_IN-to-RESET_N delay will occur.

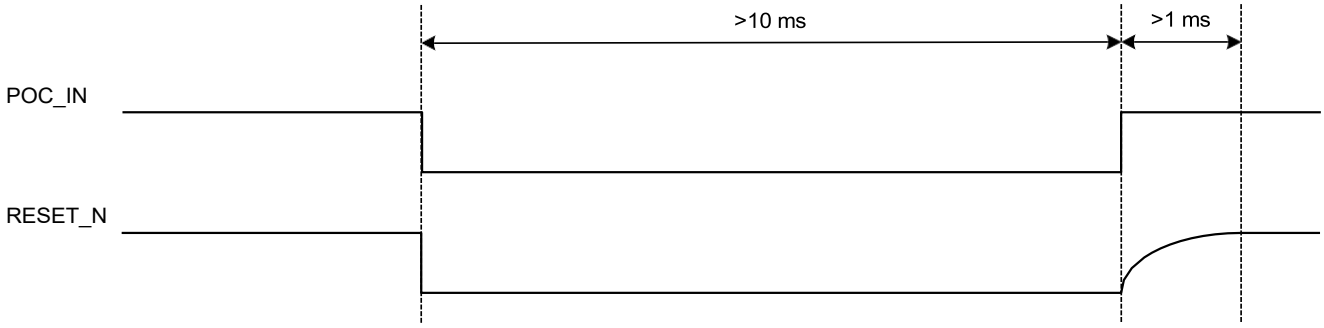


Figure 7.2. External Reset via POC_IN

In the above timing diagrams, it is assumed that all supplies including VBATT are connected together. If they are not connected together and independently controlled, then the guidance below must be followed.

- **Case1**: POC is looped back and there is no external control for POC_IN
  - All supplies can be enabled at the same time, if possible
  - If supplies cannot be enabled at the same time, the VBATT supplies should be powered up first and all other supplies should be powered on at least 1 ms before RESET_N is high. The RC circuit controlling RESET_N must be adjusted to provide the appropriate delay.
  - While powering down, supplies can be powered off simultaneously, or with VBATT the last to be disabled.
- **Case2**: POC is looped back and there is external control for POC_IN during power-up / power-down.
  - All supplies can be enabled at the same time, or VBATT may be enabled before other supplies.
  - POC_IN should be kept low for at least 600 us after all the supplies have settled.
  - On power-down, POC_IN can be driven low before disabling the supplies. Supplies can be powered off simultaneously, or with VBATT the last to be disabled.

7.3.3 Digital I/O Signals

Table 7.4. Digital I/O Signals

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
High level input voltage	V_{IH}	IO_VDDx = 3.3 V	2	—	—	V
		IO_VDDx = 1.8 V	1.17	—	—	V
Low level input voltage	V_{IL}	IO_VDDx = 3.3 V	—	—	0.8	V
		IO_VDDx = 1.8 V	—	—	0.63	V
Low level output voltage	V_{OL}		—	—	0.4	V
High level output voltage	V_{OH}		IO_VDDx - 0.4	—	—	V
Low level output current	I_{OL}	GPIO_* and ULP_GPIO_* pins	2	4	12	mA
		UULP_GPIO_*	1	—	2	mA
High level output current	I_{OH}	GPIO_* and ULP_GPIO_* pins	2	4	12	mA
		UULP_GPIO_*	1	—	2	mA

7.3.4 Flash LDO Electrical Specifications - Regulation Mode

Table 7.5. Flash LDO Electrical Specifications - Regulation Mode

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input Supply Voltage (VBATT)	V_{in}	Flash LDO in Regulation Mode	2.97	3.3	3.63	V
Output Voltage Range (VBATT)	V_{out}		—	1.8	—	V
Load current	I_{load}		—	—	48	mA
Line Regulation	REG_{line}	V_{in} Changed from 2.97 V to 3.63 V	—	—	0.6	%
Load Regulation	REG_{load}	I_{load} changed from 0 mA to 48 mA	—	—	1.4	%

7.4 AC Characteristics

7.4.1 Clock Specifications

The SL917 NCP module includes the following clock options:

- Low frequency clock options for sleep manager and RTC
  - Internal 32 kHz RC oscillator (for applications with low timing accuracy requirements only, typical accuracy is +/- 1.2%)
  - 32.768 kHz LVCMOS rail-to-rail external oscillator input pin UULP_VBAT_GPIO_3 for external oscillator or host clock
- High frequency 40 MHz clock for NWP, Cortex-M4, baseband subsystem and the radio
  - 40 MHz clock is integrated inside the module, and no external clock needs to be provided

The chipsets have integrated internal oscillators including crystal oscillators to generate the required clocks. Integrated crystal oscillators enable the use of low-cost passive crystal components. Additionally, in a system where an external clock source is already present, the clock can be reused. The following are the recommended options for the clocks for different functionalities:

32 kHz External Sources:

Note:

1. For WiFi, BLE, and Co-Ex power saving use cases, Ezurio mandates an external clock to be used on UULP_VBAT_GPIO_3 pin for the low-frequency clock source to maintain timing accuracy requirements and optimize power consumption.

Option 1: From Host MCU/MPU LVCMOS rail to rail clock input on UULP_VBAT_GPIO_3

Option 2: External clock oscillator providing LVCMOS rail to rail clock input on UULP_VBAT_GPIO_3 (Nano-drive clock should not be supplied)."

7.4.1.1 Low Frequency Clock

Low-frequency clock selection can be done through software. The RC oscillator clock is not suited for high timing accuracy applications and may increase overall system current consumption in duty-cycled power modes.

32 kHZ Internal RC Oscillator

Table 7.6. 32 kHz RC Oscillator

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Oscillator Frequency	F_{osc}			32.0		kHz
Frequency Variation with Temp and Voltage	F_{osc_Acc}			1.2		%

32.768 kHz External Oscillator

An external 32.768 kHz low-frequency clock can be fed through UULP_VBAT_GPIO_3.

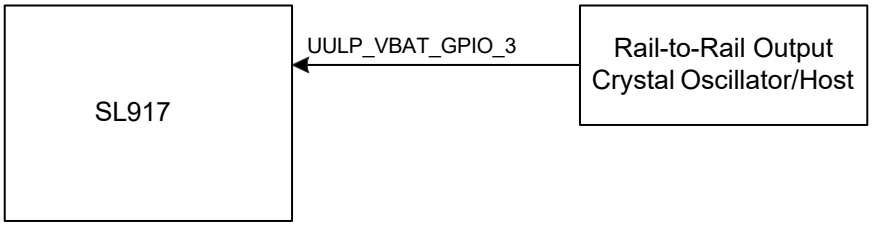


Figure 7.3. External 32.768 kHz Oscillator -

Rail to Rail Table 7.7. 32.768 kHz External

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Oscillator Frequency	f_{osc}		—	32.768	—	kHz
Frequency Variation with Temp and Voltage	f_{osc_Acc}		-100	—	100	ppm
Input duty cycle	DC_{in}		30	50	70	%
Input AC peak-peak voltage swing at input pin.	V_{AC}		-0.3	—	VBATT +/- 10%	Vpp

7.4.2 SDIO 2.0 Secondary

7.4.2.1 Full Speed Mode

Table 7.8. SDIO 2.0 Secondary Full Speed Mode

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SDIO_CLK	f_{sdio_clk}		—	—	25	MHz
SDIO_DATA, SDIO_CMD input setup time	t_s		4	—	—	ns
SDIO_DATA, SDIO_CMD input hold time	t_h		1.2	—	—	ns
SDIO_DATA, clock to output delay	t_{od}		—	—	13	ns
Output Load	C_L		5	—	10	pF

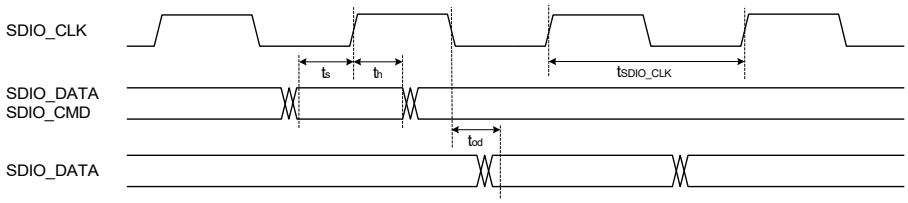


Figure 7.4. Interface Timing Diagram for SDIO 2.0 Secondary Full Speed Mode

7.4.2.2 High Speed Mode

Table 7.9. SDIO 2.0 Secondary High Speed Mode

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SDIO_CLK	f_{sdio_clk}		25	—	50	MHz
SDIO_DATA, input setup time	t_s		4	—	—	ns
SDIO_DATA, input hold time	t_h		1.2	—	—	ns
SDIO_DATA, clock to output delay	t_{od}		2.5	—	13	ns
Output Load	C_L		5	—	10	pF

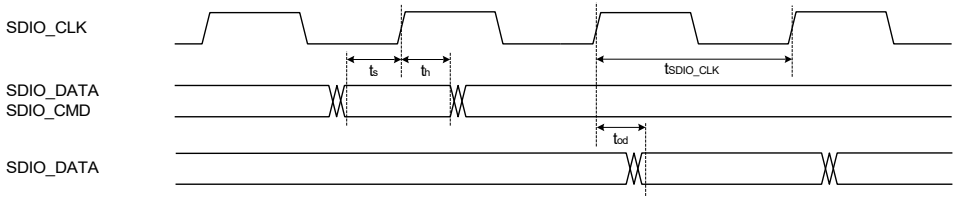


Figure 7.5. Interface Timing Diagram for SDIO 2.0 Secondary High Speed Mode

7.4.3 HSPI Secondary

7.4.3.1 Low Speed Mode

Table 7.10. HSPI Secondary Low Speed Mode

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
HSPI_CLK	f_{hspi}		0	—	25	MHz
HSPI_CSN to output delay	t_{cs}		—	—	7.5	ns
HSPI_CSN to input setup time	t_{cst}		4.5	—	—	ns
HSPI_MOSI, input setup time	t_s		1.4	—	—	ns
HSPI_MOSI, input hold time	t_h		1.5	—	—	ns
HSPI_MISO, clock to output delay	t_{od}		—	—	8.75	ns
Output Load	C_L		5	—	10	pF

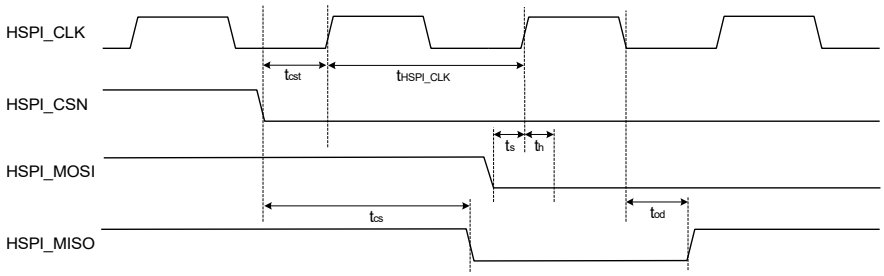


Figure 7.6. Interface Timing Diagram for HSPI Secondary Low Speed Mode

In low speed mode, HSPI_MISO data is driven on the falling edge of HSPI_CLK, and HSPI_MOSI is read on the rising edge of HSPI_CLK.

7.4.3.2 High Speed Mode

Table 7.11. HSPI Secondary High Speed Mode

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
HSPI_CLK	f_{hspi}		25	—	80	MHz
HSPI_CSN to output delay	t_{cs}		—	—	7.5	ns
HSPI_CSN to input setup time	t_{cst}		4.5	—	—	ns
HSPI_MOSI, input setup time	t_s		1.4	—	—	ns
HSPI_MOSI, input hold time	t_h		1.4	—	—	ns
HSPI_MISO, clock to output delay	t_{od}		1.5	—	8.75	ns
Output Load	C_L		5	—	10	pF

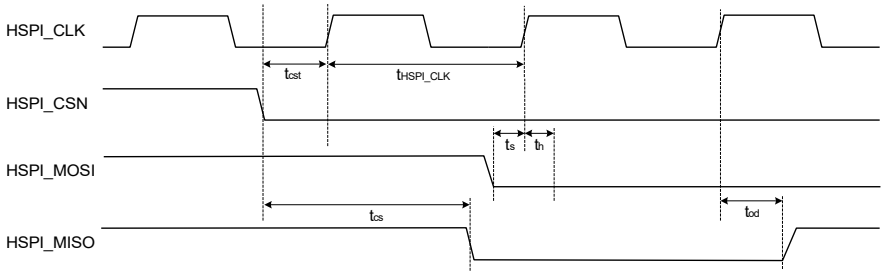


Figure 7.7. Interface Timing Diagram for HSPI Secondary High Speed Mode

In high speed mode, HSPI_MISO data is driven on the rising edge of HSPI_CLK, and HSPI_MOSI is read on the rising edge of HSPI_CLK.

7.4.3.3 Ultra High Speed Mode

Table 7.12. HSPI Secondary Ultra High Speed Mode

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
HSPI_CLK	f_{hspi}		80	—	100	MHz
HSPI_MOSI, input setup time	t_s		1.4	—	—	ns
HSPI_MOSI, input hold time	t_h		1.4	—	—	ns
HSPI_MISO, clock to output delay	t_{od}		1.5	—	8.75	ns
Output Load	C_L		5	—	10	pF

Note:

1. In ultra high-speed modes, the data on HSPI_MISO is driven on the rising edge of the SPI_CLK. The data on SPI_MOSI is read on the rising edge of the SPI_CLK.

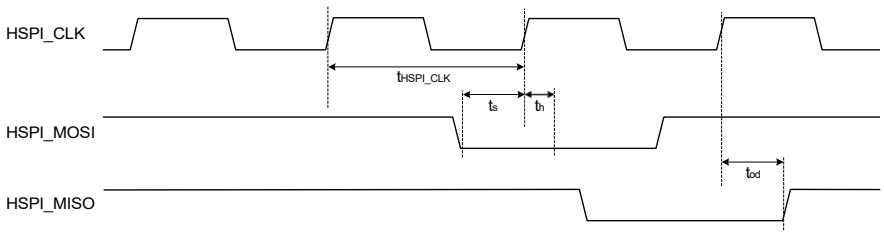


Figure 7.8. Interface Timing Diagram for HSPI Secondary Ultra High Speed Mode

In ultra high speed mode, HSPI_MISO data is driven on the rising edge of HSPI_CLK, and HSPI_MOSI is read on the rising edge of HSPI_CLK.

7.4.4 GPIO Pins

Table 7.13. GPIO Pins

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Rise time	t_{rf}	Pin configured as output	1	—	5	ns
Fall time	t_{ff}	Pin configured as output	0.9	—	5	ns
Rise time	t_r	Pin configured as input	0.3	—	1.3	ns
Fall time	t_f	Pin configured as input	0.2	—	1.2	ns

7.4.5 In-Package Flash Memory

Table 7.14. In-Package Flash Memory

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Endurance	N_{endu}	Sector erase/program	10000	—	—	cycles
		Page erase/program, page in large sector	10000	—	—	cycles
		Page erase/program, page in small sector	10000	—	—	cycles
Retention time	t_{ret}	Powered	10	—	—	years
		Unpowered	10	—	—	years
Block Erase time (32 KB)	t_{er}	Page, sector or multiple consecutive sectors	—	150	1400	ms
Page programming time	t_{prog}		—	0.5	3	ms
Chip Erase time	t_{ce}		—	20	65	s

7.5 RF Characteristics

In the sub-sections below,

- All numbers are measured at T_A = 25°C, VBATT = 3.3 V
- Please refer to 8. Reference Schematics, BOM and Layout Guidelines. The integrated RF front end includes the matching network, RF switch, and a band-pass filter.
- Supported WLAN channels for different regions include:
  - US: Channels 1 (2412 MHz) through 11 (2462 MHz)
  - Europe: Channels 1 (2412 MHz) through 13 (2472 MHz)
  - Japan: Channels 1 (2412 MHz) through 14 (2484 MHz), Channel 14 supports 1 and 2 Mbps data rates only

7.5.1 WLAN 2.4 GHz Transmitter Characteristics

7.5.1.1 Transmitter Characteristics with 3.3V Supply

Unless otherwise indicated, typical conditions are: TA = 25°C, VBATT = 3.3V. Remaining supplies are at typical operating conditions. Parameters are referred at antenna port.

Table 7.15. WLAN 2.4 GHz Transmitter Characteristics with 3.3 V Supply

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Transmit Power for 20 MHz Bandwidth, with EVM limits [1, 2, 5]	POUT	802.11b 1 Mbps DSSS, EVM< -9 dB	—	17	—	dBm
		802.11b 11 Mbps CCK, EVM< -9 dB	—	17	—	dBm
		802.11g 6 Mbps OFDM, EVM< -5 dB [3]	—	17.5	—	dBm
		802.11g 54 Mbps OFDM, EVM< -25 dB [3]	—	13.5	—	dBm
		802.11n HT20 MCS0 Mixed Mode, EVM< -5 dB[3]	—	17	—	dBm
		802.11n HT20 MCS7 Mixed Mode, EVM< -27 dB[3]	—	12.5	—	dBm
		802.11ax HE20 MCS0 SU, EVM< -5 dB[3, 4]	—	16	—	dBm
		802.11ax HE20 MCS7 SU, EVM< -27 dB[3, 4]	—	11	—	dBm
Power variation across channels	$POUT_{VAR\_CH}$		—	2	—	dB

Note:

1. Transmit power listed in this table is average power across all channels.
2. TX power in edge channels will be limited by Restricted band edge in the FCC region.
3. 11g/n/ax TX power in edge channels will be limited by Unwanted Emissions in MIC region.
4. 11ax TX power will be limited by PSD in the ETSI region.
5. Channels 1 (2412 MHz) through 11 (2462 MHz) are supported for North America (FCC, ISED). Channels 1 (2412 MHz) through 13 (2472 MHz) are supported for Europe and Japan (CE, MIC). Channel 14 (2484 MHz) is additionally supported for Japan.

7.5.2 WLAN 2.4 GHz Receiver Characteristics on High-Performance (HP) Mode

Unless otherwise indicated, typical conditions are: TA = 25 °C. VBATT = 3.3 V. Remaining supplies are at typical operating conditions. Parameters are referred at antenna port.

Table 7.16. WLAN 2.4 GHz Receiver Characteristics on HP Mode

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Sensitivity for 20 MHz Bandwidth [1, 2]	SENS	802.11b 1 Mbps DSSS [3]	—	-95	—	dBm
		802.11b 11 Mbps CCK [3]	—	-86	—	dBm
		802.11g 6 Mbps OFDM [4]	—	-90.5	—	dBm
		802.11g 54 Mbps OFDM [4]	—	-74	—	dBm
		802.11n HT20 MCS0 Mixed Mode [5]	—	-89.5	—	dBm
		802.11n HT20 MCS7 Mixed Mode [5]	—	-69.5	—	dBm
		802.11ax HE20 MCS0 SU [6]	—	-89	—	dBm
		802.11ax HE20 MCS7 SU [6]	—	-68.5	—	dBm
		802.11ax HE20 MCS0 ER [6]	—	-91	—	dBm
Maximum Input Level for PER below 10%	RX_{SAT}	802.11b	—	5	—	dBm
		802.11g	—	0	—	dBm
		802.11n	—	0	—	dBm
		802.11ax	—	0	—	dBm
RSSI Accuracy Range	$RSSI_{RNG}$		—	+4/-5	—	dB
Adjacent Channel Interference [7]	ACI	802.11b 1 Mbps DSSS [3 8]	—	51	—	dB
		802.11b 11 Mbps CCK [3 8]	—	34	—	dB
		802.11g 6 Mbps OFDM [4 9]	—	43	—	dB
		802.11g 54 Mbps OFDM [4 9]	—	26	—	dB
		802.11n HT20 MCS0 Mixed Mode [5 9]	—	33	—	dB
		802.11n HT20 MCS7 Mixed Mode [5 9]	—	12	—	dB
		802.11ax HE20 MCS0 SU [6 9]	—	21	—	dB
		802.11ax HE20 MCS7 SU [6 9]	—	6	—	dB

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Alternate Adjacent Channel Interference [7]	AACI	802.11b 1 Mbps DSSS [3] [8]	—	54	—	dB
		802.11b 11 Mbps CCK [3] [8]	—	37	—	dB
		802.11g 6 Mbps OFDM [4] [9]	—	54	—	dB
		802.11g 54 Mbps OFDM [4] [9]	—	34	—	dB
		802.11n HT20 MCS0 Mixed Mode [5] [9]	—	53	—	dB
		802.11n HT20 MCS7 Mixed Mode [5] [9]	—	33	—	dB
		802.11ax HE20 MCS0 SU [6] [9]	—	53	—	dB
		802.11ax HE20 MCS7 SU [6] [9]	—	33	—	dB

Note:

1. RX Sensitivity Variation is up to 3 dB for channels (1, 2, 3, 4, 5, 9, and 10) at typical / room temperature.
2. RX Sensitivity may be degraded up to 4 dB for channels (6, 7, 8, 11, 12, 13 and 14) at typical / room temperature.
3. 802.11b, Packet size is 1024 bytes, < 8% PER limit, Carrier modulation is non-DCM
4. 802.11g, Packet size is 1024 bytes, < 10% PER limit, Carrier modulation is non-DCM
5. 802.11n, Packet size is 4096 bytes, < 10% PER limit, Carrier modulation is non-DCM
6. 802.11ax, Packet size is 4096 bytes, < 10% PER limit, Carrier modulation is non-DCM
7. ACI / AACI is calculated as Interferer Power(dBm)- Inband power(dBm)
8. Desired signal power is 6 dB above standard defined sensitivity level
9. Desired signal power is 3 dB above standard defined sensitivity level

7.5.3 WLAN 2.4 GHz Receiver Characteristics on Low-Power (LP) Mode

Unless otherwise indicated, typical conditions are: TA = 25 °C. VBATT = 3.3 V. Remaining supplies are at typical operating conditions. Parameters are referred at antenna port.

Table 7.17. WLAN 2.4 GHz Receiver Characteristics on LP Mode

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Sensitivity for 20 MHz Bandwidth [1] [2]	SENS	802.11b 1 Mbps DSSS [3]	—	-95	—	dBm
		802.11b 11 Mbps CCK [3]	—	-86	—	dBm
		802.11g 6 Mbps OFDM [4]	—	-90	—	dBm
		802.11g 36 Mbps OFDM [4]	—	-79	—	dBm
		802.11n HT20 MCS0 Mixed Mode [5]	—	-88	—	dBm
		802.11n HT20 MCS4 Mixed Mode [5]	—	-77	—	dBm
Maximum Input Level for PER below 10%	RX_{SAT}	802.11b	—	-2.5	—	dBm
		802.11g	—	1.5	—	dBm
		802.11n	—	0.5	—	dBm
RSSI Accuracy Range	$RSSI_{RNG}$		—	+4/-6	—	dB
Adjacent Channel Interference [6]	ACI	802.11b 1 Mbps DSSS [3] [7]	—	52	—	dB
		802.11b 11 Mbps CCK [3] [7]	—	33	—	dB
		802.11g 6 Mbps OFDM [4] [8]	—	44	—	dB
		802.11g 36 Mbps OFDM [4] [8]	—	29	—	dB
		802.11n HT20 MCS0 Mixed Mode [5] [8]	—	33	—	dB
		802.11n HT20 MCS4 Mixed Mode [5] [8]	—	20	—	dB
Alternate Adjacent Channel Interference [6]	AACI	802.11b 1 Mbps DSSS [3] [7]	—	53	—	dB
		802.11b 11 Mbps CCK [3] [7]	—	37	—	dB
		802.11g 6 Mbps OFDM [4] [8]	—	53	—	dB
		802.11g 36 Mbps OFDM [4] [8]	—	37	—	dB
		802.11n HT20 MCS0 Mixed Mode [5] [8]	—	52	—	dB
		802.11n HT20 MCS4 Mixed Mode [5] [8]	—	36	—	dB

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit

Note:

1. RX Sensitivity Variation is up to 3 dB for channels (1, 2, 3, 4, 5, 9, and 10) at typical / room temperature
2. RX Sensitivity may be degraded up to 4 dB for channels (6, 7, 8, 11, 12, 13 and 14) at typical / room temperature
3. 802.11b, Packet size is 1024 bytes, < 8% PER limit, Carrier modulation is non-DCM
4. 802.11g, Packet size is 1024 bytes, < 10% PER limit, Carrier modulation is non-DCM
5. 802.11n, Packet size is 4096 bytes, < 10% PER limit, Carrier modulation is non-DCM
6. ACI / AACI is calculated as Interferer Power(dBm)- Inband power(dBm)
7. Desired signal power is 6 dB above standard defined sensitivity level
8. Desired signal power is 3 dB above standard defined sensitivity level

7.5.4 Bluetooth Transmitter Characteristics on High-Performance (HP) Mode

Unless otherwise indicated, typical conditions are: TA = 25 °C, VBATT = 3.3 V, and remaining supplies are at typical operating conditions. Parameters are referred at antenna port.

Table 7.18. Bluetooth Transmitter Characteristics on HP Mode 3.3 V

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Transmit Power [1] [2]	POUT	LE 1 Mbps	—	17	—	dBm
		LE 2 Mbps [3]	—	17	—	dBm
		LR 500 kbps	—	17	—	dBm
		LR 125 kbps	—	17	—	dBm
Power variation across channels	$POUT_{VAR\_CH}$		—	2	—	dB
Adjacent Channel Power |M-N| = 2	ACP_{eq2}	LE	—	-33	—	dBm
Adjacent Channel Power |M-N| > 2	ACP_{gt2}	LE	—	-40	—	dBm
BLE Modulation Characteristics at 1 Mbps	MOD_{CHAR}	Δf1 Avg	—	248	—	kHz
		Δf2 Max	—	250	—	kHz
		Δf2 Avg/Δf1 Avg	—	1.43	—	

Note:

1. ETSI Max Power is limited to 10 dBm/MHz EIRP to meet PSD requirements, because device falls under DTS.
2. In FCC, LR 125kbps Max Power is limited to 11 dBm to meet PSD requirement, because device falls under DTS.
3. In MIC Max power is limited to 7 dBm to meet 10 dBm/MHz limit

7.5.5 Bluetooth Transmitter Characteristics on Low-Power (LP) 0 dBm RF Mode

Unless otherwise indicated, typical conditions are: TA = 25 °C, VBATT = 3.3 V, and remaining supplies are at typical operating conditions. Parameters are referred at antenna port.

Table 7.19. Bluetooth Transmitter Characteristics on Low-Power (LP) 0 dBm RF Mode

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Transmit Power	POUT	LE 1 Mbps	—	-2	—	dBm
		LE 2 Mbps	—	-2	—	dBm
		LR 500 kbps	—	-2	—	dBm
		LR 125 kbps	—	-2	—	dBm
Adjacent Channel Power |M-N| = 2	ACP_{eq2}	LE	—	-42	—	dBm
Adjacent Channel Power |M-N| > 2	ACP_{gt2}	LE	—	-51	—	dBm
BLE Modulation Characteristics	MOD_{CHAR}	Δf1 Avg	—	248	—	kHz
		Δf2 Max	—	250	—	kHz
		Δf2 Avg/Δf1 Avg	—	1.3	—	kHz

7.5.6 Bluetooth Receiver Characteristics for 1 Mbps Data Rate

Unless otherwise indicated, typical conditions are: TA = 25 °C, VBATT = 3.3 V, remaining supplies are at typical operating conditions, packet length is 37 bytes, and parameters are referred at antenna port. Unless otherwise indicated, specifications apply to both HP and LP modes.

Table 7.20. Bluetooth Receiver Characteristics for 1 Mbps Data Rate

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Max usable receiver input level	RX_{SAT}	Signal is reference signal, 255 byte payload, BER = 0.017%, HP Mode	—	5	—	dBm
		Signal is reference signal, 255 byte payload, BER = 0.017%, LP Mode	—	1.5	—	dBm
Sensitivity [1]	SENS	Signal is reference signal, 37 byte payload, BER = 0.1%	—	-93	—	dBm
		Signal is reference signal, 255 byte payload, BER = 0.017%	—	-91	—	dBm
Signal to co-channel interferer [2]	C/I_{CC}	(see notes)[3 4]	—	-10	—	dB
N ± 1 Adjacent channel selectivity [2]	C/I_1	Interferer is reference signal at +1 MHz offset[3 4 5 6]	—	4	—	dB
		Interferer is reference signal at -1 MHz offset[3 4 5 6]	—	-4	—	dB
N ± 2 Alternate channel selectivity [2]	C/I_2	Interferer is reference signal at +2 MHz offset[3 4 5 6]	—	26	—	dB
		Interferer is reference signal at -2 MHz offset[3 4 5 6]	—	23	—	dB
N ± 3 Alternate channel selectivity [2]	C/I_3	Interferer is reference signal at +3 MHz offset[3 4 5 6]	—	39	—	dB
		Interferer is reference signal at -3 MHz offset[3 4 5 6]	—	28	—	dB
Selectivity to image frequency [2]	C/I_{IM}	Interferer is reference signal at image frequency[3 4 6]	—	39	—	dB
Selectivity to image frequency ± 1 MHz [2]	C/I_{IM_1}	Interferer is reference signal at image frequency +1 MHz[3 4 6]	—	39	—	dB
		Interferer is reference signal at image frequency -1 MHz[3 4 6]	—	36	—	dB

Note:

1. There is up to 3 dB sensitivity degradation for channels 18, 35, and 37 .
2. C/I is calculated as Interferer Power (dBm) - Inband power (dBm)
3. 0.1% BER, 37 byte packet size
4. Desired signal = -67 dBm
5. Desired frequency 2402 MHz ≤ Fc ≤ 2480 MHz
6. With allowed exceptions

7.5.7 Bluetooth Receiver Characteristics for 2 Mbps Data Rate

Unless otherwise indicated, typical conditions are: TA = 25 °C, VBATT = 3.3 V, remaining supplies are at typical operating conditions, packet length is 37 bytes, and parameters are referred at antenna port. Unless otherwise indicated, specifications apply to both HP and LP modes.

Table 7.21. Bluetooth Receiver Characteristics for 2 Mbps Data Rate

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Max usable receiver input level	RX_{SAT}	Signal is reference signal, 255 byte payload, BER = 0.017%, HP mode	—	0	—	dBm
		Signal is reference signal, 255 byte payload, BER = 0.017%, LP mode	—	-2.5	—	dBm
Sensitivity	SENS	Signal is reference signal, 37 byte payload, BER = 0.1%	—	-90.5	—	dBm
		Signal is reference signal, 255 byte payload, BER = 0.017%	—	-88.5	—	dBm
Signal to co-channel interferer [1]	C/I_{CC}	(see notes)[2 3]	—	-7	—	dB
N ± 1 Adjacent channel selectivity [1]	C/I_1	Interferer is reference signal at +2 MHz offset[2 4 3 5]	—	4	—	dB
		Interferer is reference signal at -2 MHz offset[2 4 3 5]	—	6	—	dB
N ± 2 Alternate channel selectivity [1]	C/I_2	Interferer is reference signal at +4 MHz offset[2 4 3 5]	—	22	—	dB
		Interferer is reference signal at -4 MHz offset[2 4 3 5]	—	16	—	dB
Selectivity to image frequency [1]	C/I_{IM}	Interferer is reference signal at image frequency[2 3 5]	—	16	—	dB
Selectivity to image frequency ± 2 MHz [1]	C/I_{IM_1}	Interferer is reference signal at image frequency +2 MHz[2 3 5]	—	37	—	dB
		Interferer is reference signal at image frequency -2 MHz[2 3 5]	—	28	—	dB

Note:

1. C/I is calculated as Interferer Power (dBm) - Inband power (dBm)
2. 0.1% BER, 37 byte packet size
3. Desired signal = -67 dBm
4. Desired frequency 2402 MHz ≤ Fc ≤ 2480 MHz
5. With allowed exceptions

7.5.8 Bluetooth Receiver Characteristics for 125 kbps Data Rate

Unless otherwise indicated, typical conditions are: TA = 25 °C, VBATT = 3.3 V, remaining supplies are at typical operating conditions, packet length is 37 bytes, and parameters are referred at antenna port. Unless otherwise indicated, specifications apply to both HP and LP modes.

Table 7.22. Bluetooth Receiver Characteristics for 125 kbps Data Rate

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Max usable receiver input level	RX_{SAT}	Signal is reference signal, 255 byte payload, BER = 0.017%, HP mode	—	5	—	dBm
		Signal is reference signal, 255 byte payload, BER = 0.017%, LP mode	—	3.5	—	dBm
Sensitivity [1]	SENS	Signal is reference signal, 37 byte payload, BER = 0.1%	—	-104.5	—	dBm
		Signal is reference signal, 255 byte payload, BER = 0.017%	—	-103.5	—	dBm

Note:
1. BLE, LR: Sensitivities for channels 19, 39 are up to 2 dB lower performance

7.5.9 Bluetooth Receiver Characteristics for 500 kbps Data Rate

Unless otherwise indicated, typical conditions are: TA = 25 °C, VBATT = 3.3 V, remaining supplies are at typical operating conditions, packet length is 37 bytes, and parameters are referred at antenna port. Unless otherwise indicated, specifications apply to both HP and LP modes.

Table 7.23. Bluetooth Receiver Characteristics for 500 kbps Data Rate

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Max usable receiver input level	RX_{SAT}	Signal is reference signal, 255 byte payload, BER = 0.017%, HP Mode	—	5	—	dBm
		Signal is reference signal, 255 byte payload, BER = 0.017%, LP Mode	—	3.5	—	dBm
Sensitivity [1]	SENS	Signal is reference signal, 37 byte payload, BER = 0.1%	—	-100	—	dBm
		Signal is reference signal, 255 byte payload, BER = 0.017%	—	-98.5	—	dBm

Note:
1. BLE, LR: Sensitivities for channels 19, 39 are up to 2 dB lower performance

7.6 Typical Current Consumption

Figure 7.9 Supply Connection for Current Measurements on page 45 shows the supply connection and measurement point for supply current numbers in this section.

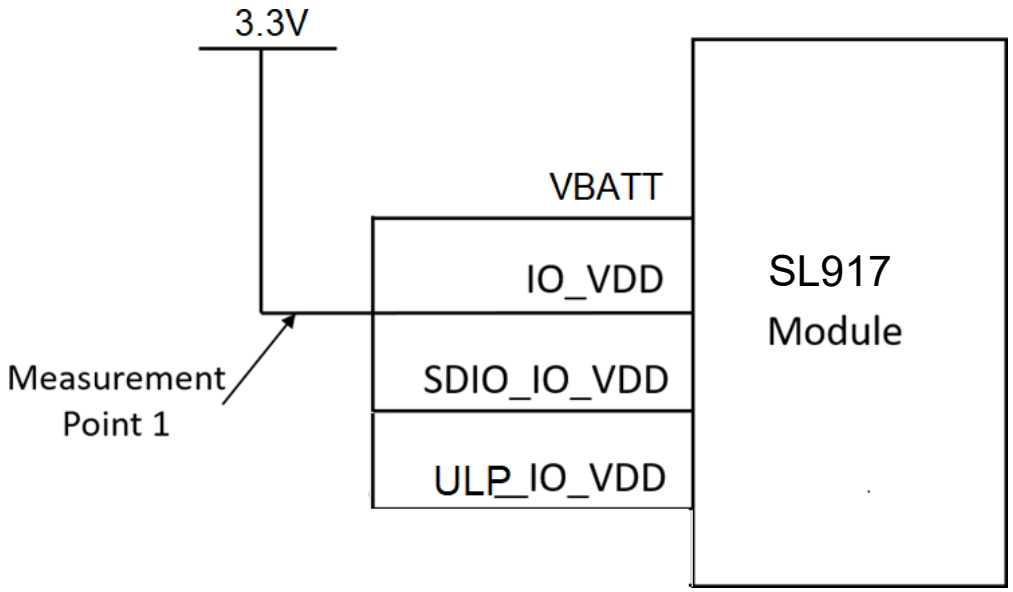


Figure 7.9. Supply Connection for Current Measurements

7.6.1 WLAN 2.4 GHz

T_A = 25 °C. VBATT = 3.3 V. Remaining supplies are at typical operating conditions. NWP clock running at 80 MHz.

Table 7.24. WLAN 2.4 GHz 3.3 V Current Consumption

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Listen current	I_{RX_LISTEN}	LP mode, 1 Mbps Listen	—	14	—	mA
Active Receive Current	I_{RX_ACTIVE}	1 Mbps RX Active, LP mode	—	21	—	mA
		HT20 MCS0, HP mode	—	54	—	mA
		HT20 MCS7, HP mode	—	55	—	mA
		HE20 MCS0, HP mode	—	55	—	mA
		HE20 MCS7, HP mode	—	55	—	mA
Transmit Current	I_{TX}	1 Mbps, HP mode	—	223	—	mA
		HT20 MCS0, HP mode	—	231	—	mA
		HT20 MCS7, HP mode	—	175	—	mA
		HE20 MCS0, HP mode	—	212	—	mA
		HE20 MCS7, HP mode	—	169	—	mA
Deep Sleep	I_{SLEEP}	No RAM retained	—	5	—	µA
		352 KB RAM retained	—	12.5	—	µA
Standby Associated, DTIM = 10	I_{STBY_ASSOC}	WLAN Keep Alive Every 30 s with 352 KB RAM Retained, Without TCP Keep Alive	—	78	—	µA
11ax TWT, Auto Config Ena- bled, Without TCP Keep Alive	I_{STBY_AX}	RX latency 2 s with 8 ms wakeup duration, WLAN Keep Alive Every 30 s with 352 KB RAM Retained	—	97	—	µA
		RX latency 30 s with 8 ms wakeup duration, WLAN Keep Alive Every 30 s with 352 KB RAM Retained	—	37	—	µA
		RX latency 60 s with 8 ms wakeup duration, WLAN Keep Alive Every 60 s with 352 KB RAM Retained	—	27	—	µA
11ax TWT, Auto Config Ena- bled, With TCP Keep Alive Every 240 s	$I_{STBY\_AX\_TCP}$	RX latency 2 s with 8 ms wakeup duration, WLAN Keep Alive Every 30 s with 352 KB RAM Retained	—	101	—	µA
		RX latency 30 s with 8 ms wakeup duration, WLAN Keep Alive Every 30 s with 352 KB RAM Retained	—	43	—	µA
		RX latency 60 s with 8 ms wakeup duration, WLAN Keep Alive Every 60 s with 352 KB RAM Retained	—	32	—	µA

Note:

1. The absolute maximum device current when transmitting at highest transmit power will not exceed 400 mA.

7.6.2 Bluetooth LE

T_A = 25 °C. VBATT = 3.3 V. Remaining supplies are at typical operating conditions. NWP clock running at 80 MHz.

Table 7.25. Bluetooth LE Current Consumption

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
TX Active Current	I_{TX}	LP mode, Tx Power = 0 dBm	—	11	—	mA
		LP mode, Tx Power = Max TX power	—	11	—	mA
RX Active Current	I_{RX}	LP mode	—	11	—	mA
Advertising, Unconnectable	I_{ADV_UC}	Advertising on all 3 channels, 37 Byte payload, Interval = 1.28 s, Tx Power = 0 dBm, LP mode	—	35	—	µA
Advertising, Connectable	I_{ADV_CN}	Advertising on all 3 channels, 37 Byte payload, Interval = 1.28 s, Tx Power = 0 dBm, LP mode	—	41	—	µA
Connected	I_{CONN}	Connection Interval = 200 ms, No data, Tx Power = 0 dBm, LP mode	—	138	—	µA

8. Reference Schematics, BOM and Layout Guidelines

Note:

1. Customers should include provision for programming or updating the firmware at manufacturing.
   a. If using UART, we recommend bringing out the SPI or SDIO lines to test points, so designers could use the faster interface for programming the firmware as needed.
   b. If using SPI or SDIO as host interface, then firmware programming or update can be done through the host MCU, or if design- er prefers to program standalone at manufacturing, then it is recommended to have test points on the SPI or SDIO signals.
2. 3.3 V/1.8 V/VBATT must be supplied by external source.
3. VBATT, SDIO_IO_VDD, IO_VDD, ULP_IO_VDD must be powered using External/On-board Power.
4. FLASH_IO_VDD is powered by 1V8_LDO output.
5. Place all the Caps closer to the corresponding Module pins.

8.1 SL917 NCP Schematics for Parts with RF Pin

8.1.1 System Supplies

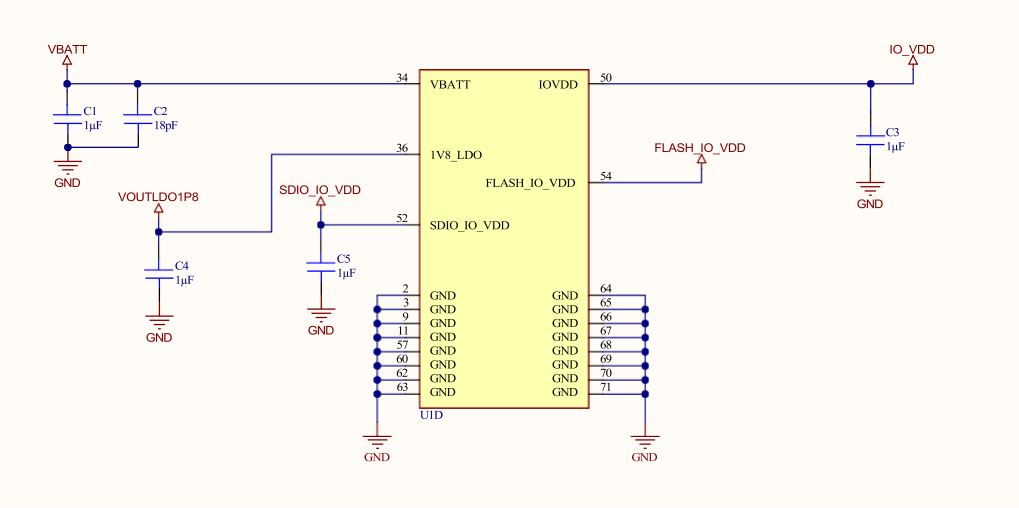


Figure 8.1. System Power Supplies

Note:

1. Place all the decoupling capacitors close to the module pins.
2. IO_VDD, SDIO_IO_VDD, ULP_IO_VDD can be powered independently by different voltage sources based on their corresponding signals voltage levels requirements. Voltages must be as per Table 7.2 Recommended Operating Conditions on page 26.
3. Even if GPIOs are not used, their respective IO domains must still be connected to the power supply.

8.1.2 RF, Debug, and Reset Connection

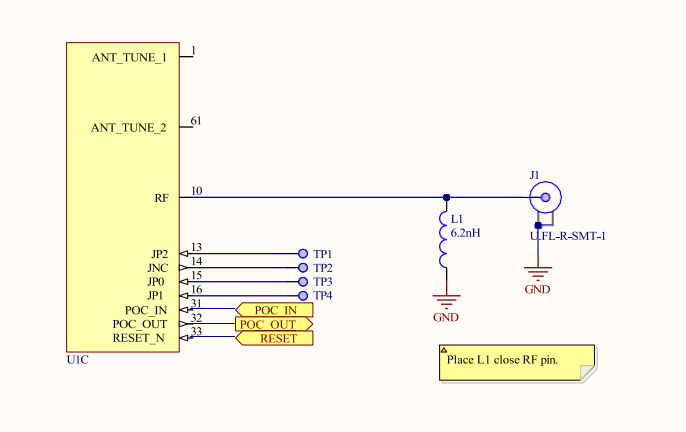


Figure 8.2. RF, Debug, and Reset Connection

Note:

1. Place L1 close to the RF pin.
2. It is mandatory to follow the reference schematics for optimal RF performance.
3. Maintain 50 ohm characteristic impedance for RF traces.
4. J1: In-built antenna or an external antenna (with RF connector) can be used.
5. It is recommended to add microwave coaxial switch connector (Example : Murata's MM8430-2610RA1) or MHF4 connector for conducted measurements.
6. Additional matching circuit to be provided near the antenna, based on antenna used and location on the board.

8.1.3 GPIO Connection

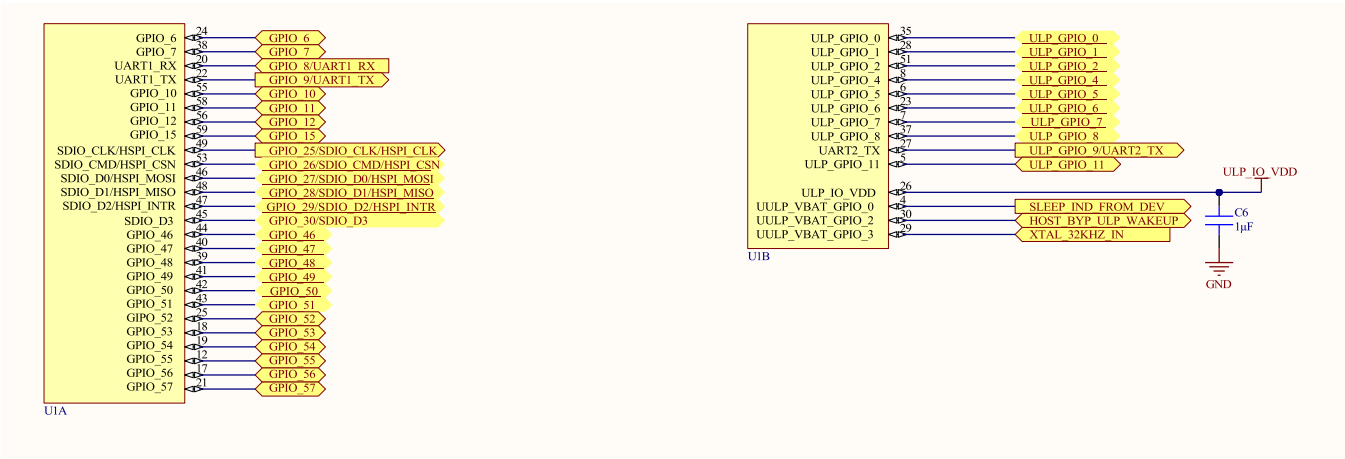


Figure 8.3. GPIO Connection

Note:

1. Place all the decoupling capacitors close to the module pins.
2. IO_VDD, SDIO_IO_VDD, ULP_IO_VDD can be powered independently by different voltage sources based on their corresponding signals voltage levels requirements. Voltages must be as per Table 7.2 Recommended Operating Conditions on page 26.
3. Even if GPIOs are not used, their respective IO domains must still be connected to the power supply.
4. R5 to R10 are optional resistors for signal integrity.
5. 33 ohm on SDIO_CLK/HSPI_CLK has to be near the source of the clock, and not near the module.

8.1.4 Reset

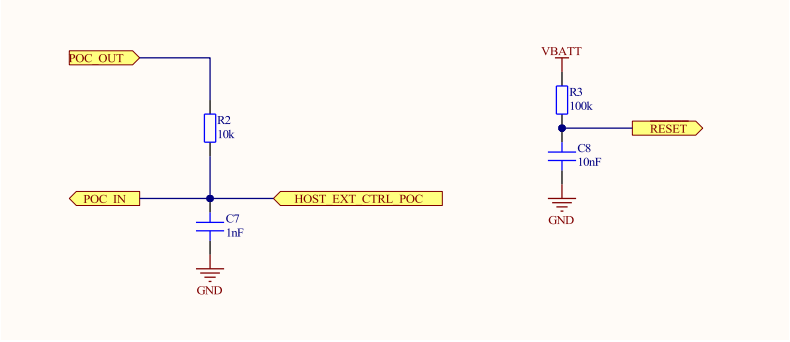


Figure 8.4. Reset Configuration

Note:

1. The configuration shown allows for blackout monitor functionality along with external reset of the embedded SiWN917M IC.
2. The POC_IN signal connects to the POC_IN pin on the SiWN917M. POC_IN resets all the internal blocks of the IC.
3. The Si917_RESET signal connects to the RESET_N pin on the SiWN917M. It is recommended to use the RC filter as shown. RESET_N is an open-drain output pin that will be pulled low when POC_IN goes low.
4. The POC_OUT signal connects to the POC_OUT pin on the SiWN917M. POC_OUT is an active-low, push-pull output from the internal blackout monitor. In this configuration, it is isolated from the external HOST_EXT_CTRL_POC signal with a series resistor. In applications without external host control (HOST_EXT_CTRL_POC), POC_OUT may be directly connected to POC_IN. Without external host control to the POC_IN pin, the IC cannot be reset multiple times after power-on.
5. The HOST_EXT_CTRL_POC signal connects to a GPIO of an external host processor. In this configuration, HOST_EXT_CTRL_POC must be an open-drain output to allow POC_OUT to control POC_IN.
6. HOST_EXT_CTRL_POC must be at the same voltage level as the VBATT supply pin.

8.1.5 LF Clock Option

Note: For WiFi, BLE, and Co-Ex power saving use cases, Ezurio mandates an external clock to be used on UULP_VBAT_GPIO_3 pin for the low-frequency clock source to maintain timing accuracy requirements and optimize power consumption.

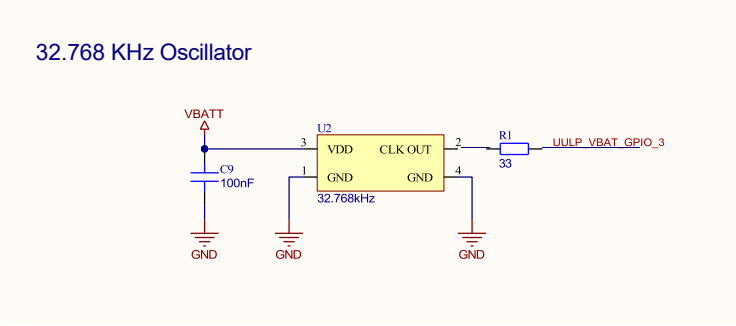


Figure 8.5. 32.768 kHz Clock Oscillator

8.1.6 Flash Memory Configurations

Figure 8.6. In-Package Flash Powered From On-Chip LDO Supply

8.1.7 Host Interface

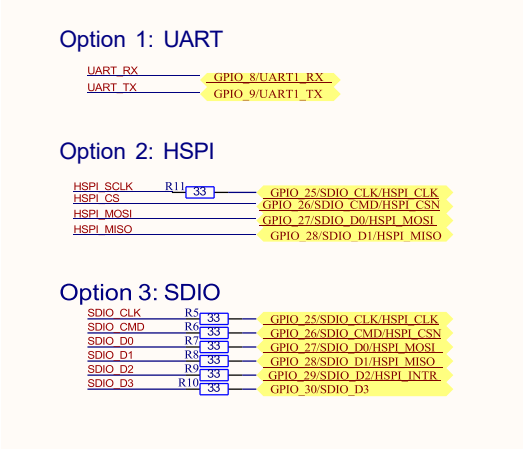


Figure 8.7. Host Interface Options

Note:

1. In UART mode, ensure that the input signals, UART_RX and UART_CTS are not floating when the device is powered up and reset is de-asserted. This can be done by ensuring that the host processor configures its signals (outputs) before de-asserting the reset.
2. In HSPI mode, ensure that the input signals, HSPI_CSN and HSPI_CLK are not floating when the device is powered up and reset is de-asserted. This can be done by ensuring that the external Host processor configures its signals (outputs) before de-asserting the reset. HSPI_INTR is the interrupt signal driven by the secondary device. This signal may be configured as Active-high or Active-low. If it is active-high, an external pull-down resistor is required. If it is active-low, an external pull-up resistor is required. The following actions can be carried out by the host processor during power-up of the device, and before/after ULP Sleep mode.
   a. To use the signal in the Active-high or Active-low mode, ensure that during the power up of the device, the Interrupt is disabled in the Host processor before de-asserting the reset. After de-asserting the reset, the Interrupt needs to be enabled only after the HSPI initialization is done and the Interrupt mode is programmed to either Active-high or Active-low mode as required.
   b. The Host processor needs to disable the interrupt before the ULP Sleep mode is entered and enable it after HSPI interface is reinitialized upon wakeup from ULP Sleep.
3. In SDIO mode, pull-up resistors should be present on SDIO_CMD & SDIO Data lines as per the SDIO physical layer specification version 2.0.
4. 33ohm on SDIO_CLK/HSPI_CLK has to be near the source of the clock, and not near the module.
5. R5 to R11 are optional resistors for Signal Integrity.

8.1.8 Bill of Materials

Line No	Quantity	Designator	Value	Description	Manufac-turer	Manufac-turer PN	Toler-ance	Rating
1	5	C1, C3, C4, C5, C6	1uF	CAP CER 0402 X5R 1uF 10V 10%	-	-	10%	10 V
2	1	C2	18pF	CAP CER 0201 C0G 18pF 25V 2%	-	-	2%	25V
3	1	C7	1nF	CAP CER 0402 X7R 1nF 16V 10%	-	-	10%	16V
4	1	C8	10nF	CAP CER 0402 X7R 10nF 16V 10%	-	-	10%	16V
5	1	C9	100nF	CAP CER 0402 X7R 100nF 50V 10%	-	-	10%	50V
6	1	J1	U.FL-R- SMT-1	CONN RF 500HM UFL_2.6x2.6 SMD	-	-		
7	1	L1	6.2 nH	IND Fixed 0201 6.2nH 300mA 600mOhm 3%	-	-	3%	300mA
8	8	R1, R5, R6, R7, R8, R9, R10, R11	33	RES 0402 33R 1/16W 1% 100ppm	-	-	1%	62.5 mW
9	1	R2	10k	RES 0402 10K 1/16W 5% 200ppm	-	-	5%	63mW
10	1	R3	100k	RES 0402 100K 1/16W 1% 100ppm	-	-	1%	63mW
11	1	U2	32.768 kHz	SiTIME CRYSTAL CSPBGA 32.768kHz 10pF 100ppm	SiTIME	SiT1532AI-J4-DCC-32.768		
12	1	U1	453-00219	SL917 Module based on SiW917Y1GN	Ezurio			

8.2 SL917 NCP Schematics for parts with Integral Antenna

8.2.1 System Supplies

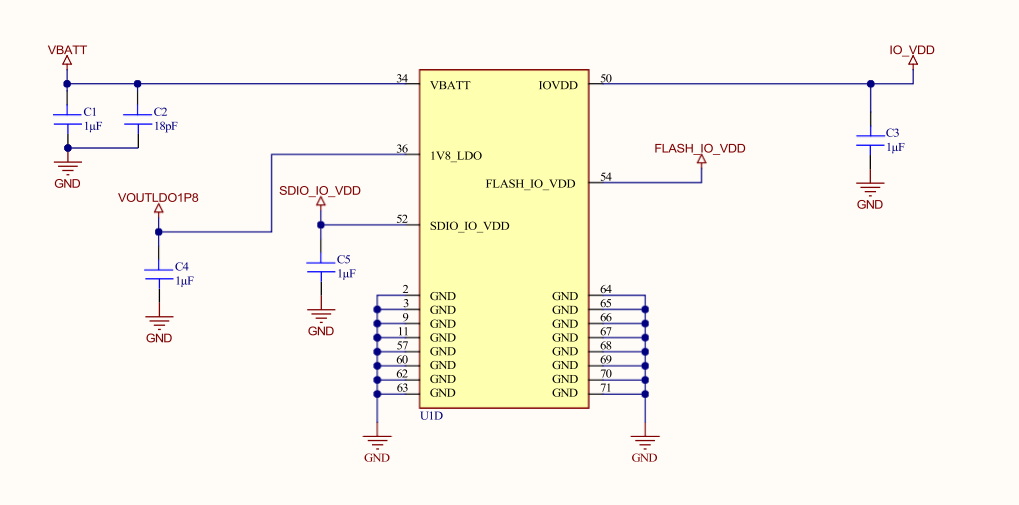


Figure 8.8. System Power Supplies

Note:

1. Place all the decoupling capacitors close to the module pins.
2. IO_VDD, SDIO_IO_VDD, ULP_IO_VDD can be powered independently by different voltage sources based on their corresponding signals voltage levels requirements. Voltages must be as per Table 7.2 Recommended Operating Conditions on page 26.
3. Even if GPIOs are not used, their respective IO domains must still be connected to the power supply.

8.2.2 RF, Debug, and Reset Connection

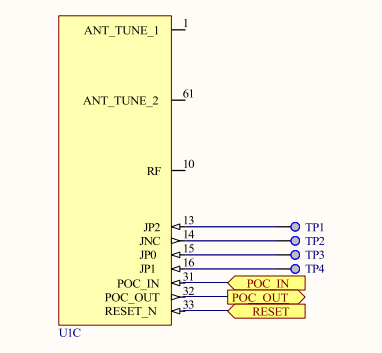


Figure 8.9. RF, Debug, and Reset Connection

Note:

1. It is mandatory to follow the reference schematics for optimal RF performance.

8.2.3 GPIO Connection

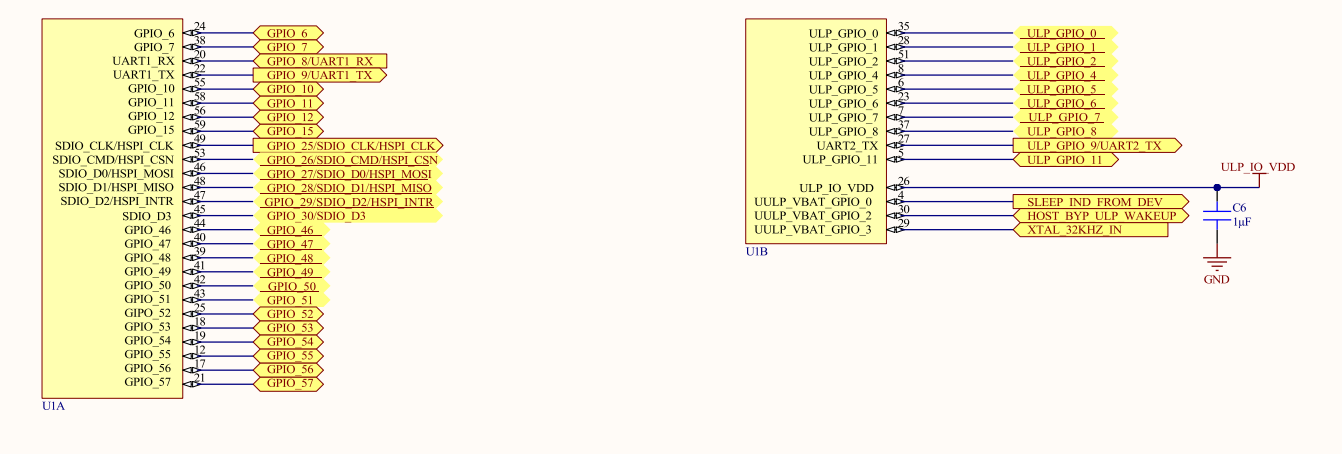


Figure 8.10. GPIO Connection

Note:

1. Place all the decoupling capacitors close to the module pins.
2. IO_VDD, SDIO_IO_VDD, ULP_IO_VDD can be powered independently by different voltage sources based on their corresponding signals voltage levels requirements. Voltages must be as per Table 7.2 Recommended Operating Conditions on page 26.
3. Even if GPIOs are not used, their respective IO domains must still be connected to the power supply.
4. R5 through R10 are optional resistors for signal integrity.
5. R5 33ohm on SDIO_CLK/HSPI_CLK has to be near the source of the clock.

8.2.4 Reset

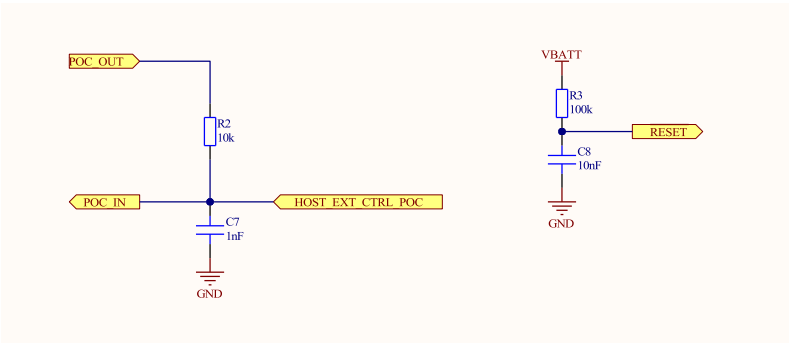


Figure 8.11. Reset Configuration

Note:

1. The configuration shown allows for blackout monitor functionality along with external reset of the embedded SiWN917M IC.
2. The POC_IN signal connects to the POC_IN pin on the SiWN917M. POC_IN resets all the internal blocks of the IC.
3. The Si917_RESET signal connects to the RESET_N pin on the SiWN917M. It is recommended to use the RC filter as shown. RE- SET_N is an open-drain output pin that will be pulled low when POC_IN goes low.
4. The POC_OUT signal connects to the POC_OUT pin on the SiWN917M. POC_OUT is an active-low, push-pull output from the internal blackout monitor. In this configuration, it is isolated from the external HOST_EXT_CTRL_POC signal with a series resistor. In applications without external host control (HOST_EXT_CTRL_POC), POC_OUT may be directly connected to POC_IN. Without external host control to the POC_IN pin, the IC cannot be reset multiple times after power-on.
5. The HOST_EXT_CTRL_POC signal connects to a GPIO of an external host processor. In this configuration, HOST_EXT_CTRL_POC must be an open-drain output to allow POC_OUT to control POC_IN.
6. HOST_EXT_CTRL_POC must be at the same voltage level as the VBATT supply pin.

8.2.5 LF Clock Option

Note: For WiFi, BLE, and Co-Ex power saving use cases, Ezurio mandates an external clock to be used on UULP_VBAT_GPIO_3 pin for the low-frequency clock source to maintain timing accuracy requirements and optimize power consumption.

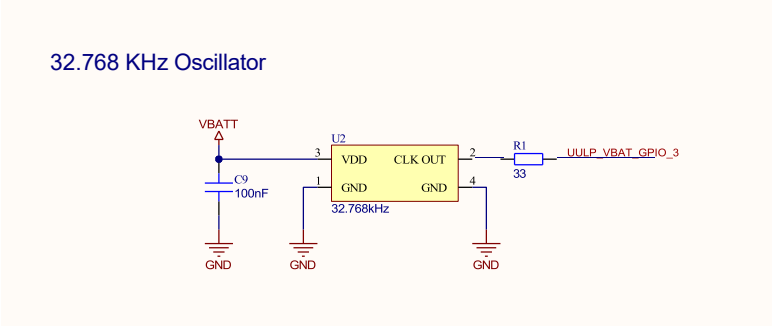


Figure 8.12. 32.768 kHz Clock Oscillator

8.2.6 Flash Memory Configurations

Figure 8.13. In-Package Flash Powered From On-Chip LDO Supply

8.2.7 Host Interface

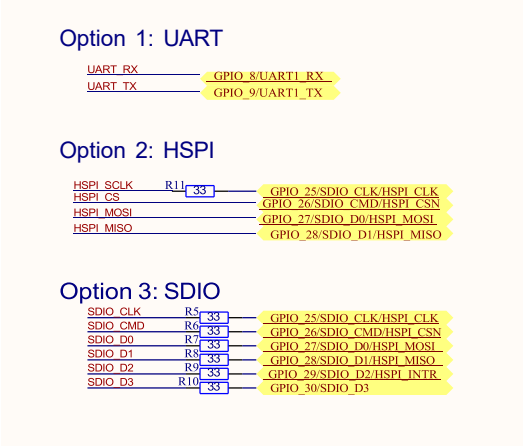


Figure 8.14. Host Interface Options

1. In UART mode, ensure that the input signals, UART_RX and UART_CTS are not floating when the device is powered up and reset is de-asserted. This can be done by ensuring that the host processor configures its signals (outputs) before de-asserting the reset.
2. In HSPI mode, ensure that the input signals, HSPI_CSN and HSPI_CLK are not floating when the device is powered up and reset is de-asserted. This can be done by ensuring that the external Host processor configures its signals (outputs) before de-asserting the reset. HSPI_INTR is the interrupt signal driven by the secondary device. This signal may be configured as Active-high or Active-low. If it is active-high, an external pull-down resistor is required. If it is active-low, an external pull-up resistor is required. The following actions can be carried out by the host processor during power-up of the device, and before/after ULP Sleep mode.
    a. To use the signal in the Active-high or Active-low mode, ensure that during the power up of the device, the Interrupt is disabled in the Host processor before de-asserting the reset. After de-asserting the reset, the Interrupt needs to be enabled only after the HSPI initialization is done and the Interrupt mode is programmed to either Active-high or Active-low mode as required.
    b. The Host processor needs to disable the interrupt before the ULP Sleep mode is entered and enable it after HSPI interface is reinitialized upon wakeup from ULP Sleep.
3. In SDIO mode, pull-up resistors should be present on SDIO_CMD & SDIO Data lines as per the SDIO physical layer specification version 2.0.
4. 33ohm on SDIO_CLK has to be near the source of the clock, and not near the module.
5. R5 to R11 are optional resistors for Signal Integrity.

8.2.8 Bill of Materials

Line No	Quantity	Designator	Value	Description	Manufac-turer	Manufac-turer PN	Toler-ance	Rating
1	5	C1, C3, C4, C5, C6	1uF	CAP CER 0402 X5R 1uF 10V 10%	-	-	10%	10 V
2	1	C2	18pF	CAP CER 0201 C0G 18pF 25V 2%	-	-	2%	25V
3	1	C7	1nF	CAP CER 0402 X7R 1nF 16V 10%	-	-	10%	16V
4	1	C8	10nF	CAP CER 0402 X7R 10nF 16V 10%	-	-	10%	16V
5	1	C9	100nF	CAP CER 0402 X7R 100nF 50V 10%	-	-	10%	50V
6	1	J1	U.FL-R- SMT-1	CONN RF 500HM UFL_2.6x2.6 SMD	-	-		
7	1	L1	6.2 nH	IND Fixed 0201 6.2nH 300mA 600mOhm 3%	-	-	3%	300mA
8	8	R1, R5, R6, R7, R8, R9, R10, R11	33	RES 0402 33R 1/16W 1% 100ppm	-	-	1%	62.5 mW
9	1	R2	10k	RES 0402 10K 1/16W 5% 200ppm	-	-	5%	63mW
10	1	R3	100k	RES 0402 100K 1/16W 1% 100ppm	-	-	1%	63mW
11	1	U2	32.768 kHz	SiTIME CRYSTAL CSPBGA 32.768kHz 10pF 100ppm	SiTIME	SiT1532AI-J4-DCC-32.768		
12	1	U1	453-00221	SL917 Module based on SiW917Y1GA	Ezurio			

8.3 Layout Guidelines

1. The RF (Module Pin No. 10) signal may be directly connected to an on-board chip antenna or terminated in an RF pin connector of any form factor for enabling the use of external antennas. RF pin can be left floating if not used.
2. Antenna clearance area is not necessary if you are using an external antenna attached to the RF pin.
3. The RF pin trace on RF pin should have a characteristic impedance of 50 Ohms. Any standard 50 Ohms RF pin trace (Microstrip or Coplanar wave guide) may be used. The width of the 50 Ohms line depends on the PCB stack, e.g., the dielectric of the PCB, thickness of the copper, thickness of the dielectric and other factors. Consult the PCB fabrication unit to get these factors right.
4. To evaluate transmit and receive performance like Tx Power, and EVM and Rx sensitivity, an RF pin connector would be required. A suggestion is to place a ‘microwave coaxial connector with switch’ between RF pin and the antenna.
5. Each GND pin must have a separate GND via. Place the ground vias as close to the ground pads as possible.
6. All decoupling capacitors placement must be as much close as possible to the corresponding power pins, and the trace lengths as short as possible.
7. Ensure all power supply traces widths are sufficient enough to carry corresponding currents.
8. Add GND copper pour underneath IC/Module in all layers, for better thermal dissipation.
9. Add solid GND copper pour underneath Module for better emission performance.

8.3.1 Installation Guide for SL917 RF Trace NCP Module (453-00219)

Figure 8.15 on page 58 below shows the recommended layout for SL917 NCP when using an RF connector (MHF4 recommended) for an external antenna. The short RF trace from the RF pad of the module to the pad of the RF connector must be 50 ohm and exactly the same width as the RF pad of the module, i.e., 700 µm. Figure 8.15 SL917 RF Trace Top Layer Application Layer with RF Connector on page 58 shows two examples on practical implementations of such a trace. The widths S is fixed to 700 um. The height h depends on the PCB stackup, and the gap width W is adjusted until the impedance of the trace is exactly 50 ohm. Online calculators for coplanar waveguide with ground can be used to calculate the width W for any specific PCB stack-up. The integrator must consider using a unique connector, such as a “reverse polarity SMA” or “reverse thread SMA”, if detachable antenna is offered with the host chassis.

Ground vias underneath the module must be used extensively especially around the rectangular GND pins to enable heat transfer from the bottom of the module to the GND plane of the host board. Routing signal lines elsewhere underneath the module is acceptable.

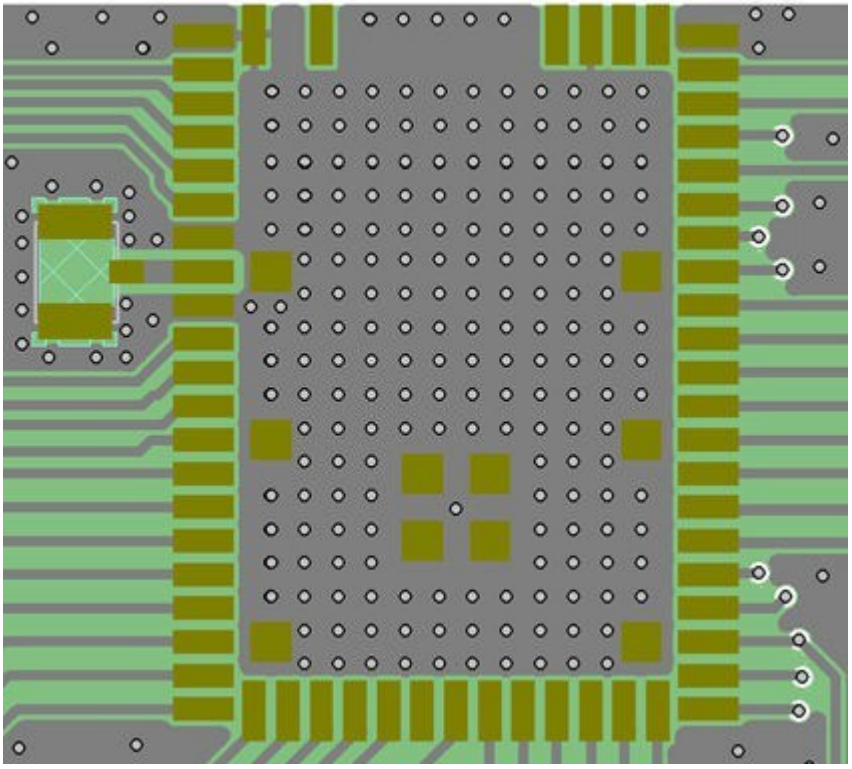


Figure 8.15. SL917 RF Trace Top Layer Application Layer with RF Connector

The typical permittivity of PCB laminate is 4.6. If assuming permittivity of 4.6, in the example shown in Figure 8.16 on page 59 the dimensions would be:

S = 700 um

h = 420 um W = 332 um

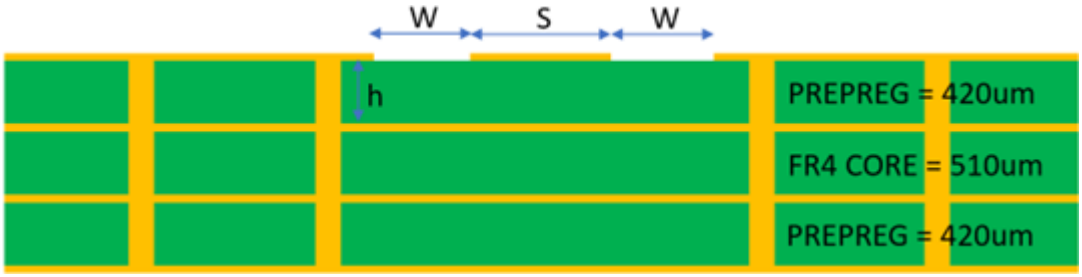


Figure 8.16. Example Implementation of a Co-planar Wave Guide with Ground and Thick Prepeg

Similarly, if assuming permittivity of 4.6, in the example shown in Figure 8.16 on page 59 the dimensions would be:

S = 700 um

h = 730 um W = 132 um

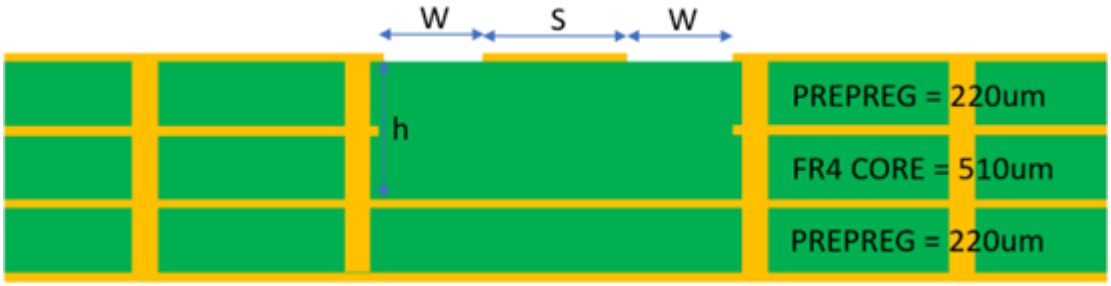
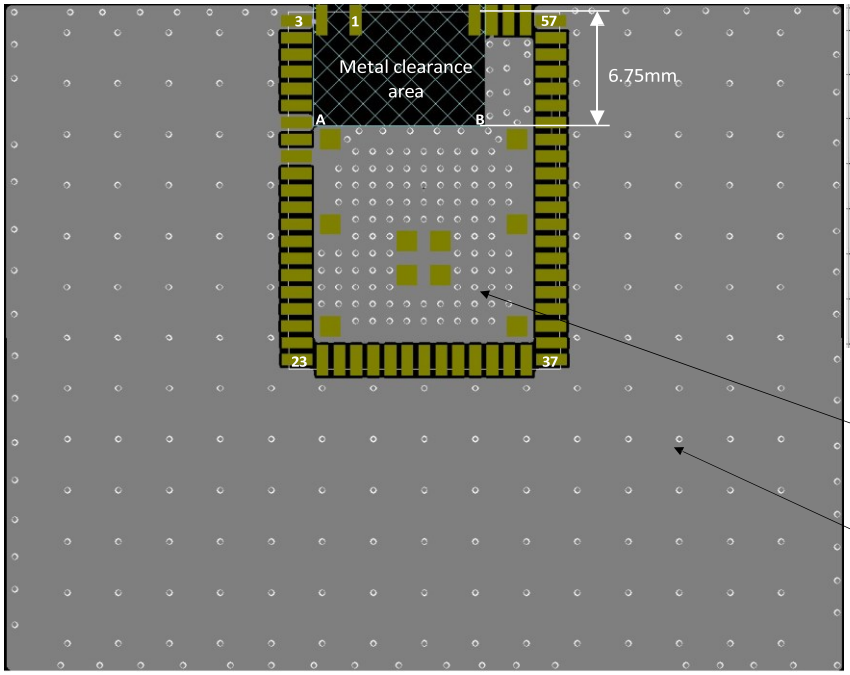


Figure 8.17. Example Implementation of a Co-planar Wave Guide with Ground and Thin Prepeg

8.3.2 Installation Guide for SL917 Integrated Antenna NCP Module (453-00221)



	X-cordinate (mm)	Y-cordinate (mm)
A (Corner of the metal clearance)	-6.5	3.8
B (Corner of the metal clearance)	3.6	3.8
1 (Center point of PAD1)	-4	10.05
3 (Center point of PAD3)	-7.5	10
23 (Center point of PAD23)	-7.5	-10
37 (Center point of PAD37)	7.5	-10
57 (Center point of PAD 57)	7.5	10

Figure 8.18. Application Layout of SL917 Integrated Antenna NCP Module

For optimal performance of the SL917 Integrated Antenna Module:

- Place the module aligned to the edge of the application PCB, as illustrated in Figure 8.18 on page 60.
- Leave the antenna clearance area void of any traces, components, or copper on all layers of the application PCB.
- Connect all ground pads directly to a solid ground plane.
- Place the ground vias as close to the ground pads as possible.
- Avoid plastic or any other dielectric material in direct contact with the antenna.

Figure 8.19 Figure on page 61 shows example layout scenarios which will lead to degraded performance and possible EMC issues with the module.

Ground vias underneath the module must be used extensively especially around the rectangular GND pins to enable heat transfer from the bottom of the module to the GND plane of the host board. Routing signal lines elsewhere underneath the module is acceptable.

Antennas are by nature affected by the surrounding PCB design and in particular the size and shape of the ground surrounding the antenna. The wide band antenna of SL917 Integrated Antenna module is designed to operate in various size/shape application boards and the antenna is not sensitive to dielectric material near the antenna. However, in certain extreme circumstances, such as extremely small board or narrow board, the antenna can be detuned enough to have an impact to the range, EVM characteristics and in-band emissions. In such cases it is possible to fine tune the antenna by using one or two external capacitors or inductors connected between the ANT_TUNE1 and GND and/or ANT_TUNE2 and GND. An example is shown in the Figure 8.20 Figure on page 61. Finding the correct value for these components requires empirical testing and measuring the antenna return loss. (See the note below on modular certification.)

The best antenna performance is achieved when the board width is 50mm and the antenna is placed at the center of the board edge. Having wider or narrower PCB will have up to 25% impact to the range. If the board is narrower than 35mm or wider than 100 mm, it is possible that external fine tuning becomes necessary to maintain the EVM performance.

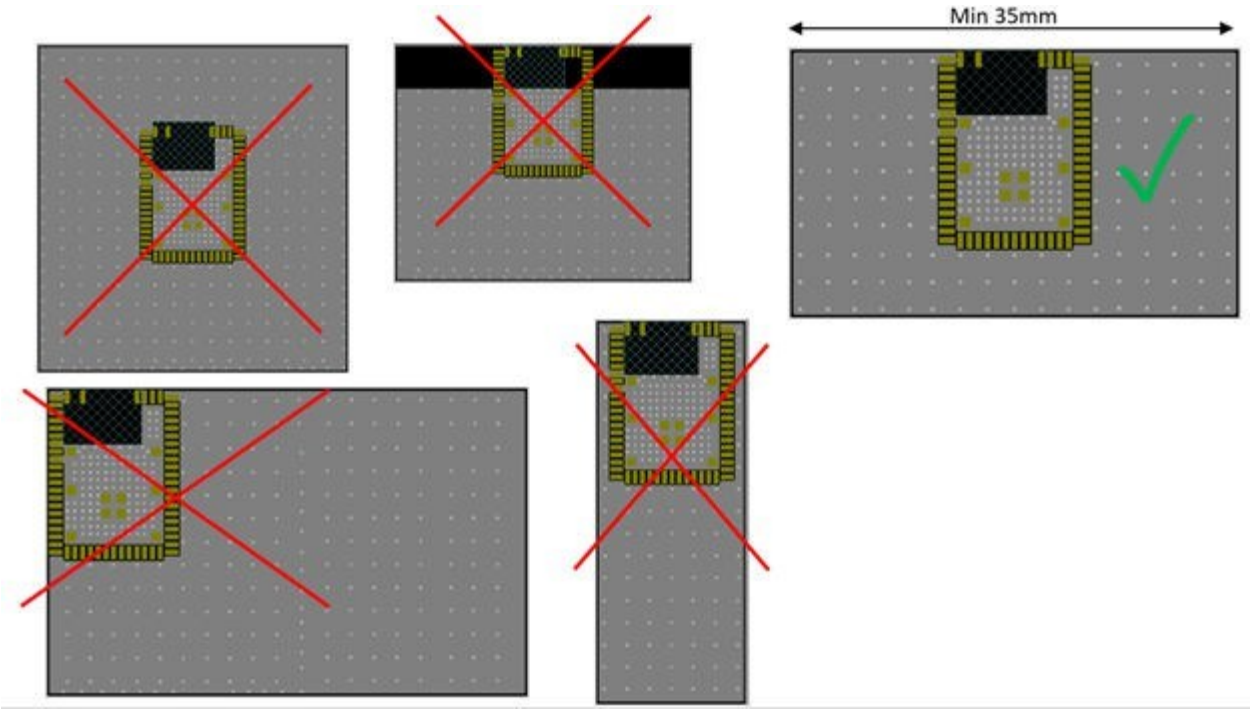


Figure 8.19. Layout Examples

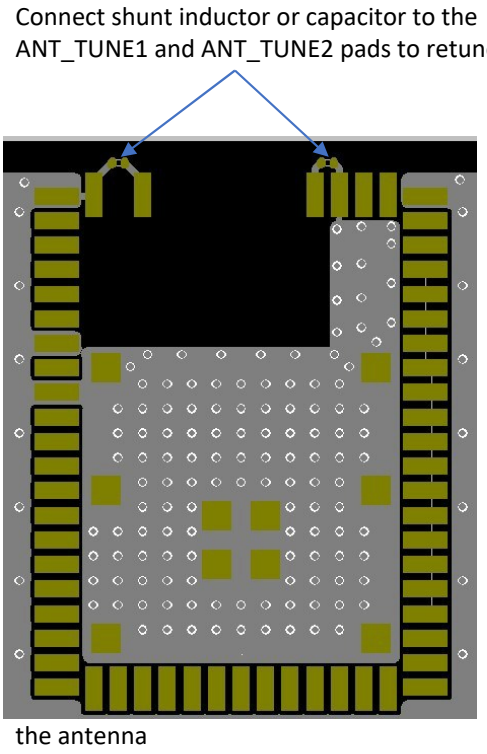


Figure 8.20. External Antenna Fine Tuning Option

8.4 SL917 Integrated Antenna (453-00221) Antenna Radiation and Efficiency

Typical radiation patterns for the built-in antenna under optimal operating conditions are plotted in the figures that follow.

Table 8.1. Antenna Efficiency and Peak Gain

Parameter	With optimal layout	Note
Efficiency	-1 dB	Antenna gain and radiation patterns have a strong dependence on the size and shape of the application PCB the module is mounted on, as well as on the proximity of any mechanical design to the antenna. Refer to 8.3.2 Installation Guide for SL917 Integrated Antenna Module for recommendations to achieve optimal antenna performance.
Peak gain	2.26 dBi	

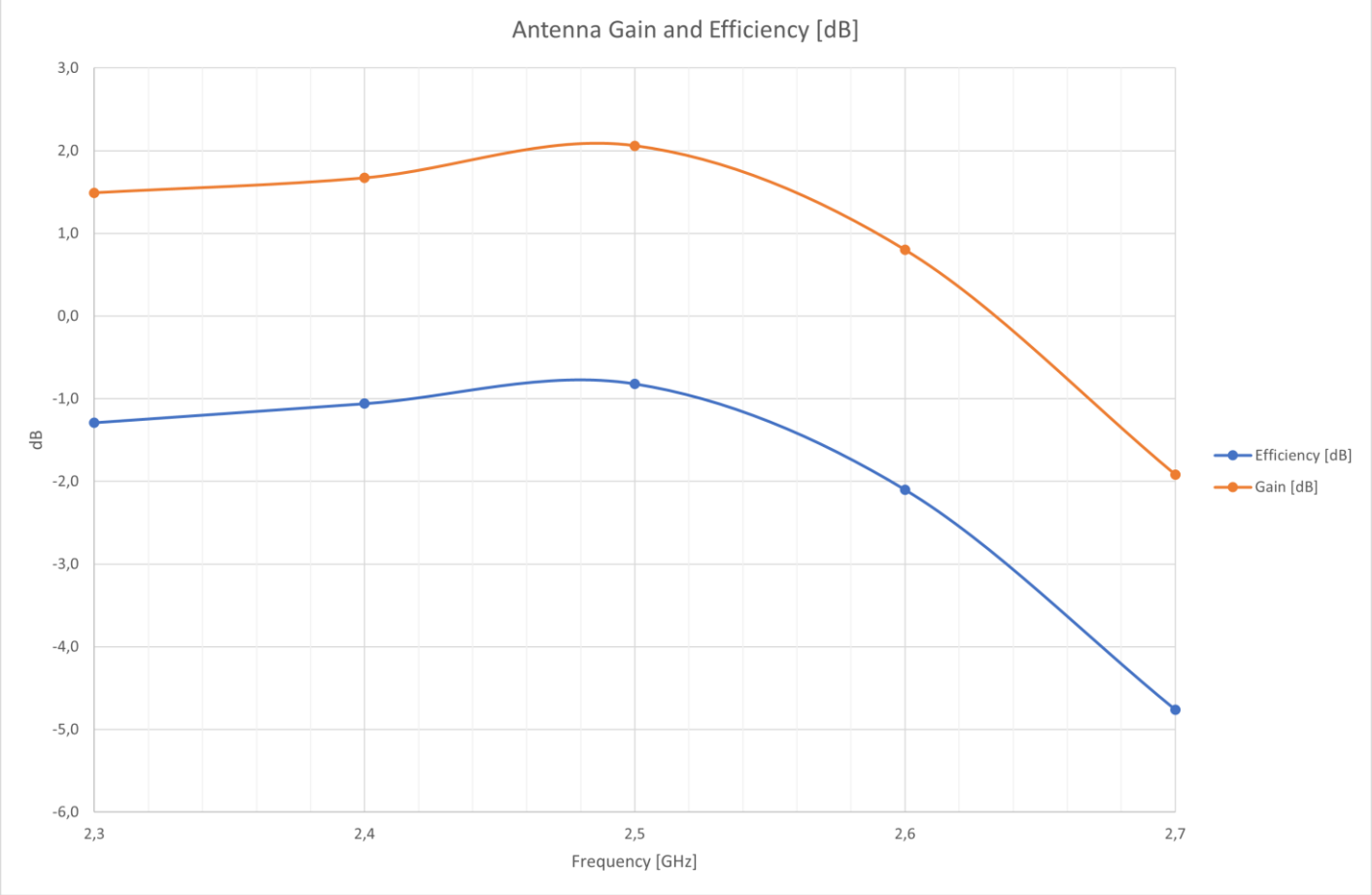


Figure 8.21. Efficiency and Gain of the Built-in Antenna

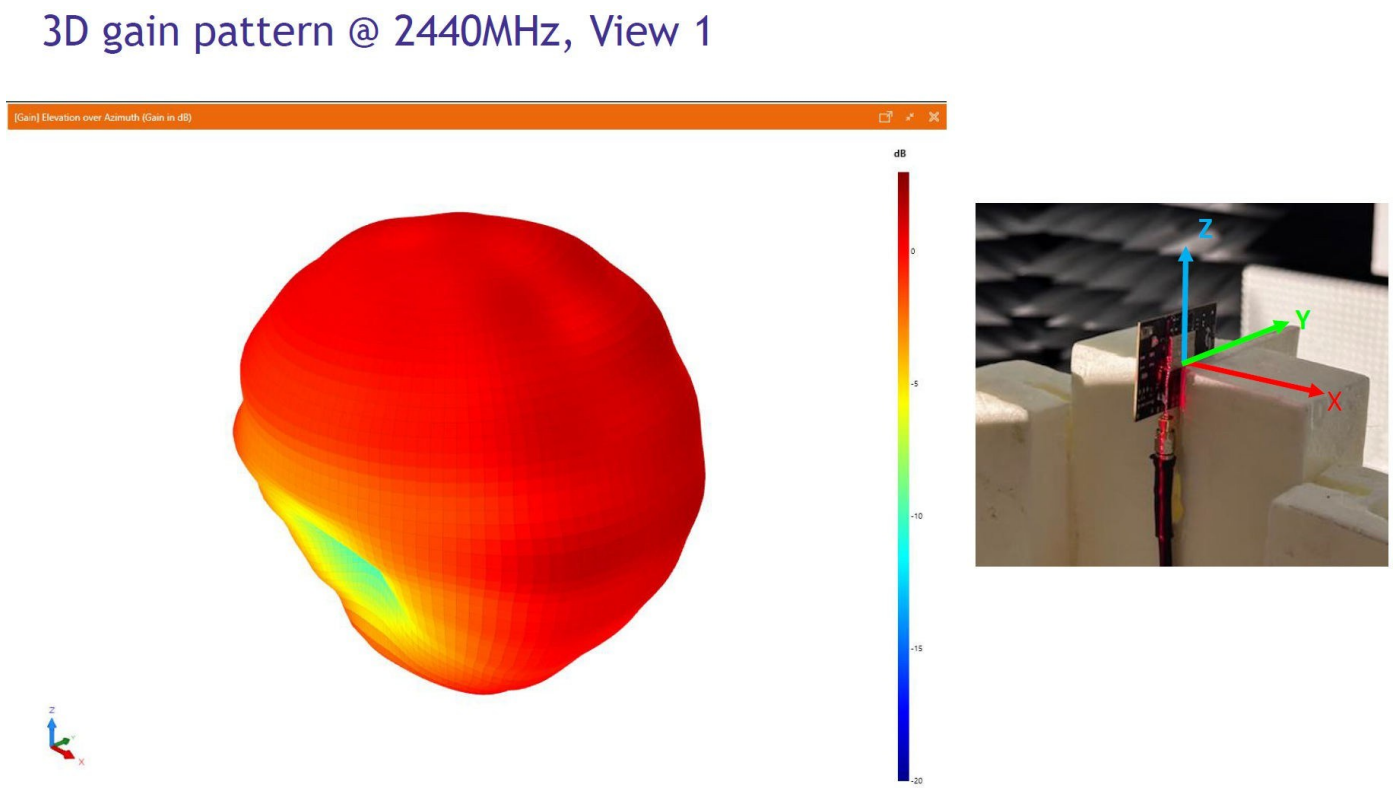


Figure 8.22. 3D Radiation Pattern of the Build-In Antenna

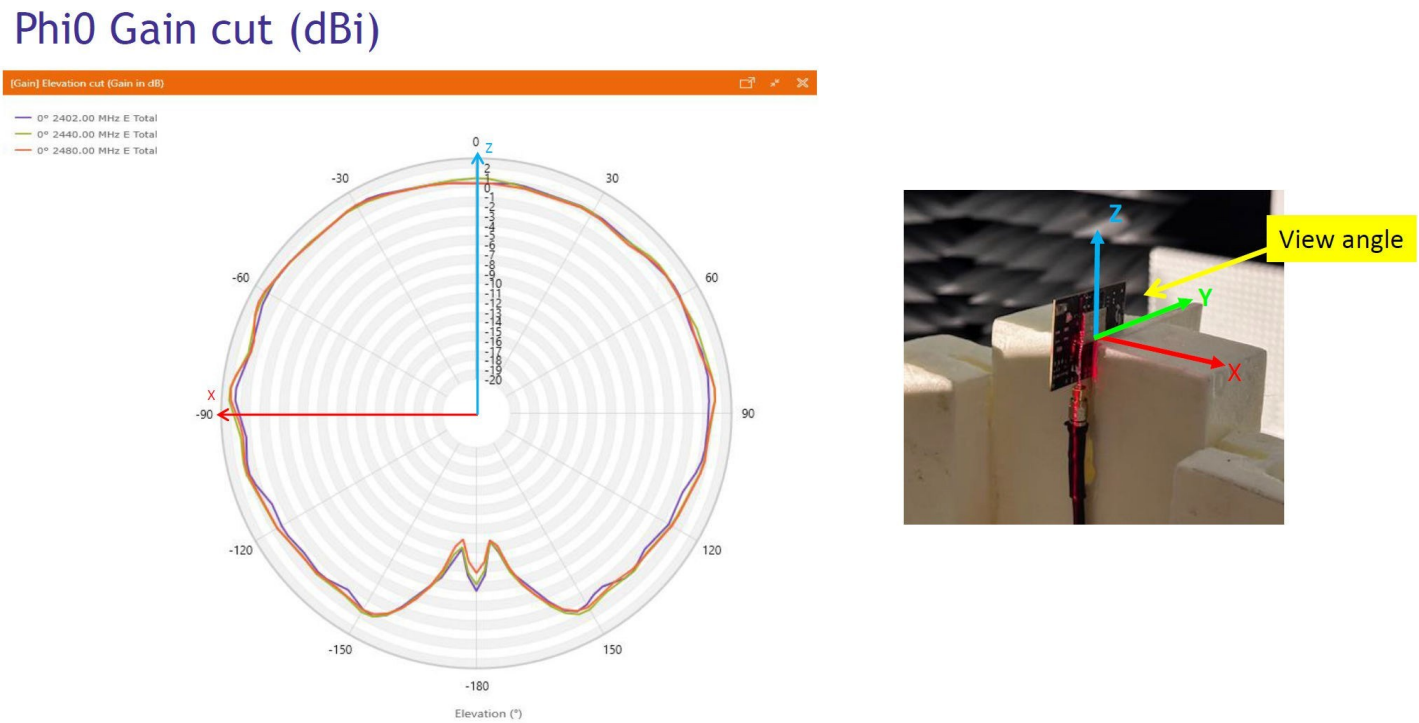


Figure 8.23. Typical 2D Antenna Radiation Patterns - Phi 0º (Side View) Gain (dBi)

Phi90 Gain cut

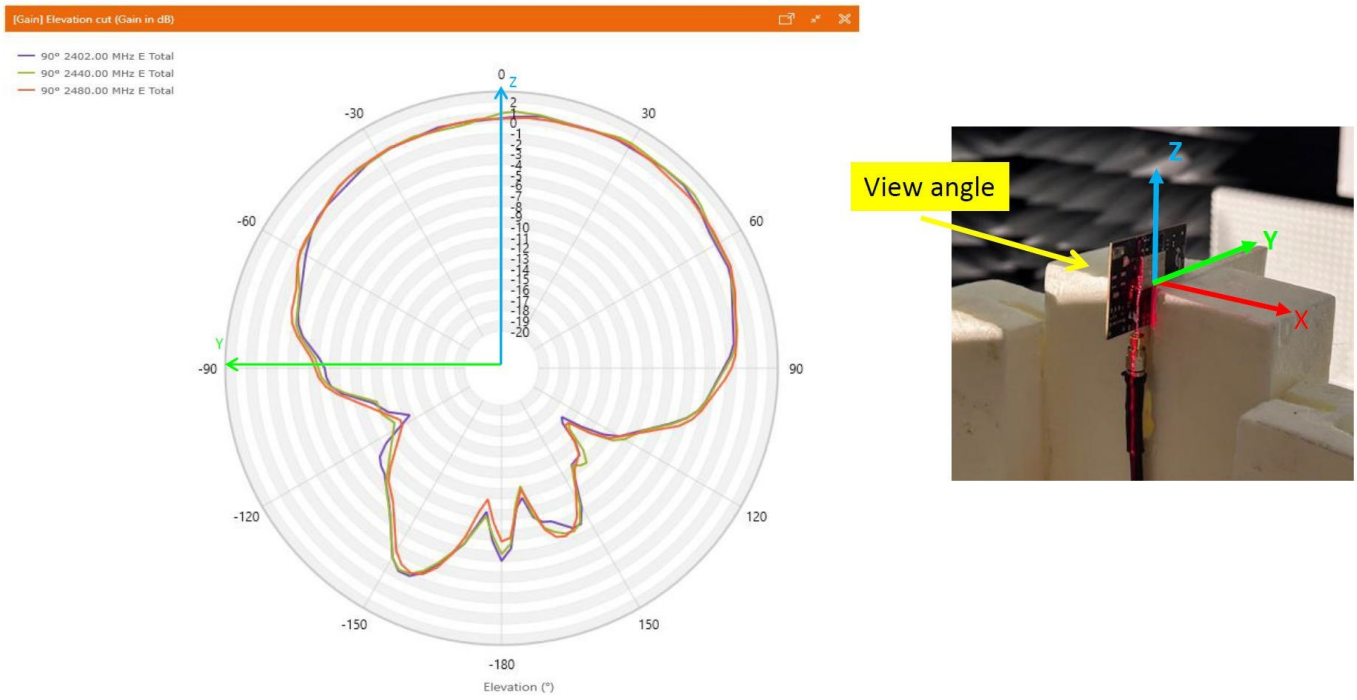


Figure 8.24. Typical 2D Antenna Radiation Patterns - Phi 90º (Top View) Gain (dBi)

Theta90 Gain cut

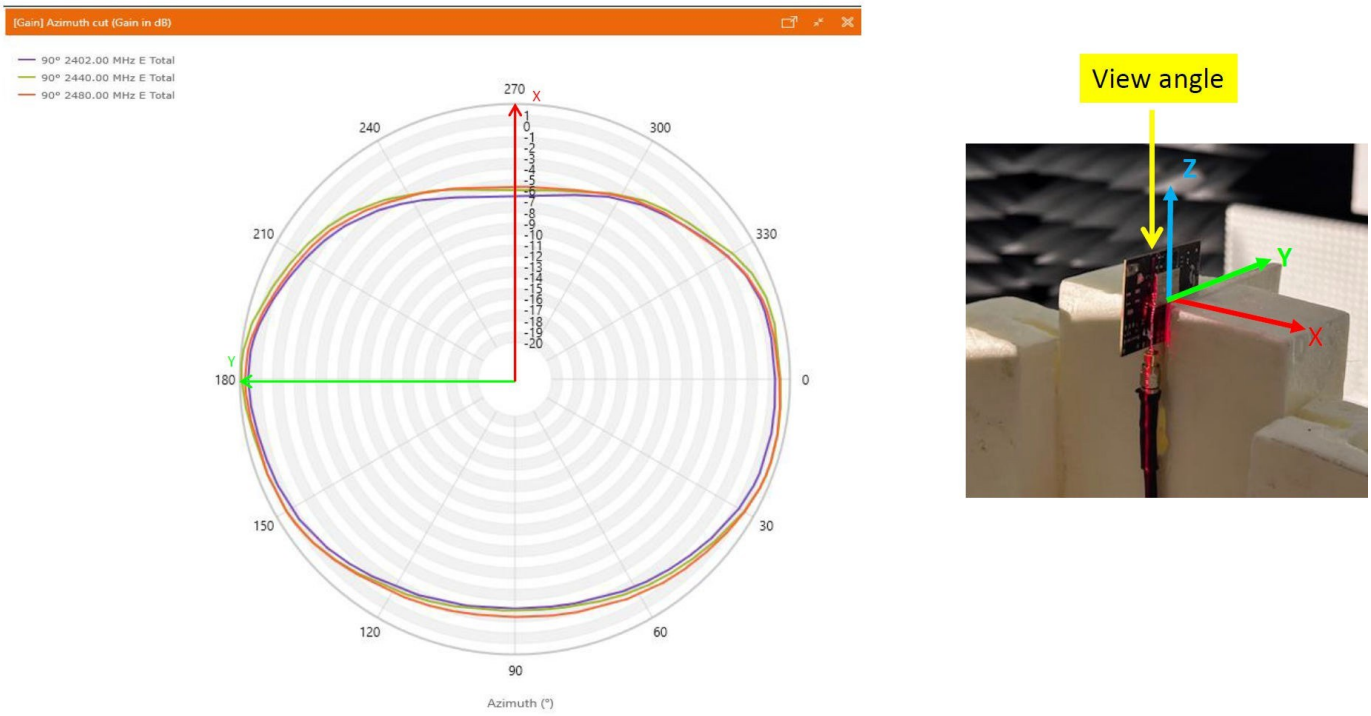


Figure 8.25. Typical 2D Antenna Radiation Patterns - Theta 90º (Front View) Gain (dBi)

8.4.1 Proximity to Other Materials

Avoid placing plastic or any other dielectric material in close proximity to the antenna. Conformal coating and other thin dielectric layers are acceptable directly on top of the antenna region, but this will also negatively impact antenna efficiency and reduce range.

Any metallic objects in close proximity to the antenna will prevent the antenna from radiating freely. The minimum recommended distance of metallic and/or conductive objects is 10 mm in any direction from the antenna except in the directions of the application PCB ground planes.

8.4.2 Proximity to Human Body

Placing the module in contact with or very close to the human body will negatively impact antenna efficiency and reduce range.

Note: When it comes to modular certifications, following the manufacturer's design guidelines is critical for ensuring that compliance is maintained and modular approvals remain valid, in particular with regards to the carrier (host) PCB size, thickness, relative permittivity, and/or module placement. A modular certification is still valid if no antenna tuning is applied to compensate for reduced performance in terms of range, which may result from sub-optimal carrier PCB size, thickness, relative permittivity, module placement, and/or proximity to other materials such as assembly housing. Conversely, a custom antenna tuning might invalidate a modular certification, unless it is done to compensate for the degradation caused by a printed circuit board deviating from the manufacturer’s best-case reference design in terms of size, thickness, relative permittivity, and/or module placement. In such case, a Permissive Change to a modular approval might become necessary, depending on the resulting performance of the end-product relative to the certified module's test reports, in particular with regards to spurious emission levels, as found during spot-checking. For example, in the FCC case, a Class 1 Permissive Change (C1PC) is considered if the host PCB modifications do not increase emissions. Class 2 Permissive Change (C2PC) is considered if the modifications degrade the emissions but remain below regulatory limits. Whether antenna tuning is applied or not, it is strongly recommended that spot-checking is performed in any case with the end-product having the transmitter(s) operating, to confirm that the host product meets all regulatory requirements under any circumstance. In the end, the emission levels established in the mod- ule certification are limits for the end device too and determine whether or not a Permissive Change should be considered. Since this is evaluated on a case-by-case basis, integrators must consult with the company providing certification services for their final product to identify the best approach.

9. Package Specifications

9.1 Dimensions

Table 9.1. Module Dimensions

Parameter	Value (LxWxH)	Units
Module Dimensions	21.10 x 16 x 2.32	mm
Tolerance	±0.2	mm

9.2 Package Outline

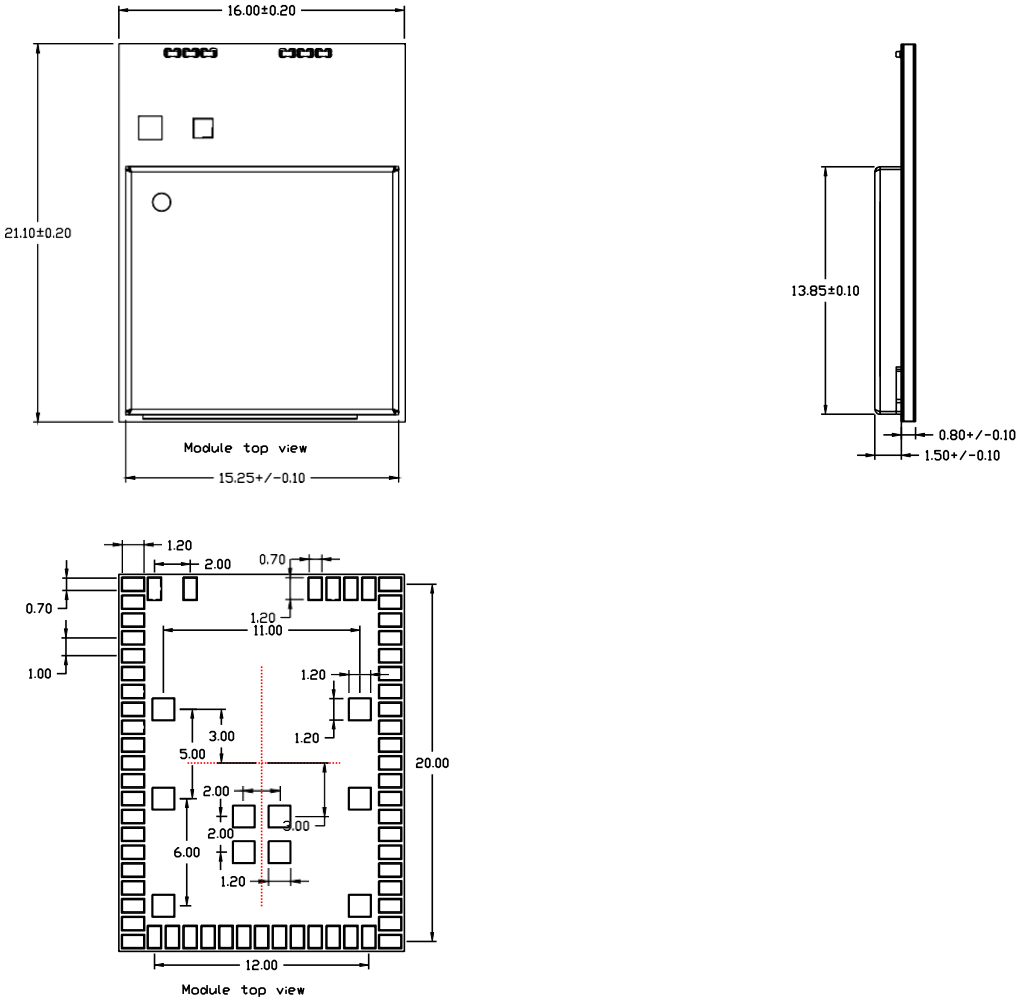


Figure 9.1. Package Outline

9.2.1 Pin Locations

Note: All coordinates in Table 9.2 Pin Locations on page 68 are in millimeters, and in TOP VIEW.

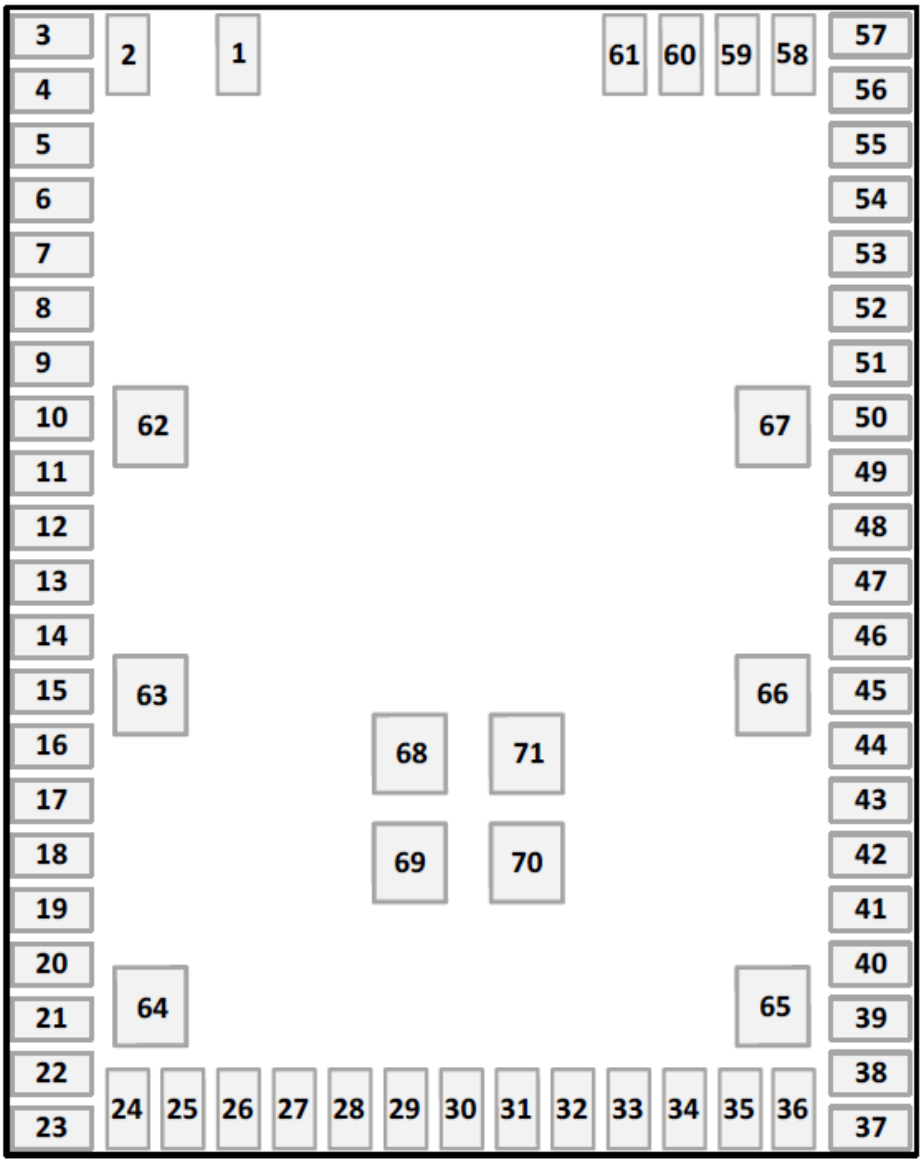


Figure 9.2. Pin Numbering

Table 9.2. Pin Locations

PAD X-Y Coordinates			
Pad #	**X**	**Y**	**Pad Size**
1	-4	9.75	(1.2 x 0.7) mm
2	-6	9.75	
3	-7.2	10	
23	-7.2	-10	
24	-6	-9.75	
36	6	-9.75	
37	7.2	-10	
57	7.2	-10	
58	6	9.75	
61	3	9.75	
62	-5.5	3	(1.2 x 1.2) mm
63	-5.5	-2	
64	-5.5	-8	
65	5.5	-8	
66	5.5	-2	
67	5.5	3	
68	-1	-3	
69	-1	-5	
70	1	-5	
71	1	-3	

9.3 PCB Landing Pattern

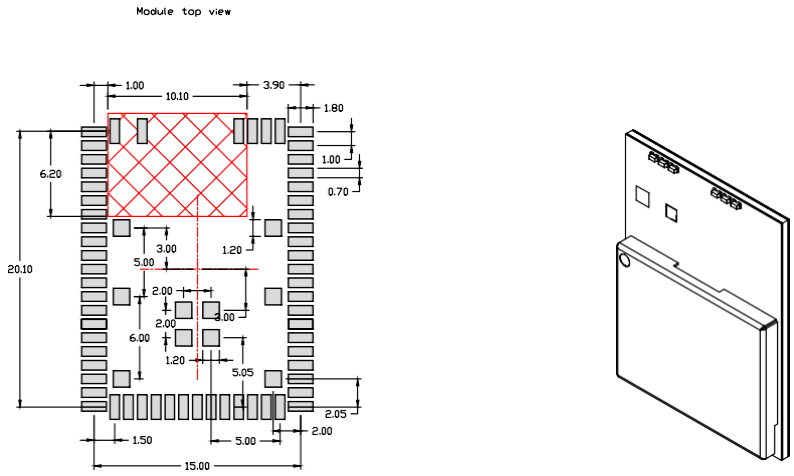


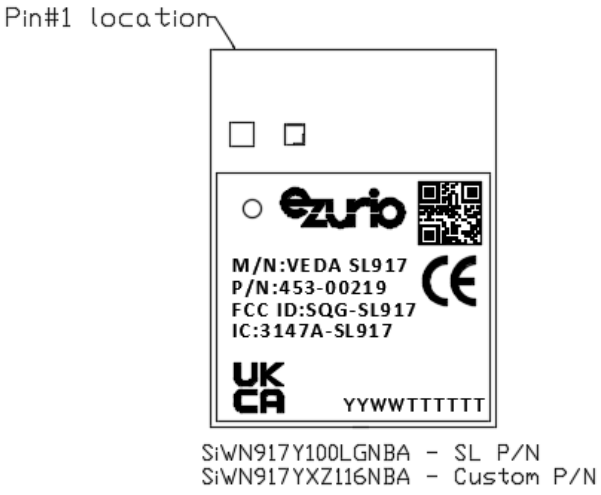
Figure 9.3. PCB Landing Pattern

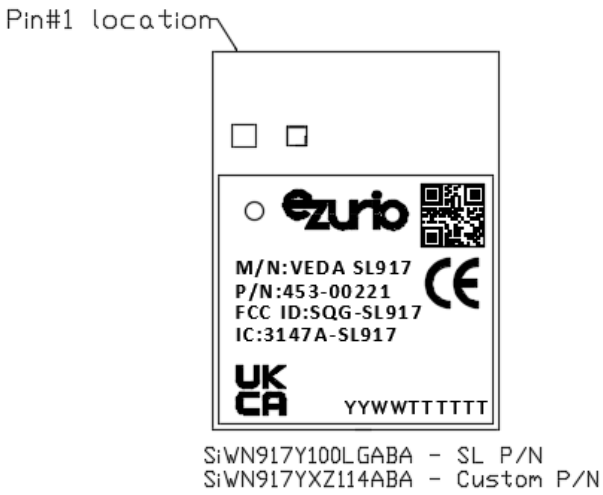
Table 9.3. PCB Landing Pattern Pin Locations

PAD X-Y Coordinates			
Pad #	**X**	**Y**	**Pad Size**
1	-4	10.05	(1.8 x 0.7) mm
2	-6	10.05	
3	-7.5	10	
23	-7.5	-10	
24	-6	-10.05	
36	6	-10.05	
37	7.5	-10	
57	7.5	10	
58	6	10.05	
61	3	10.05	

PAD X-Y Coordinates			
Pad #	**X**	**Y**	**Pad Size**
62	-5.5	3	(1.2 x 1.2) mm
63	-5.5	-2	
64	-5.5	-8	
65	5.5	-8	
66	5.5	-2	
67	5.5	3	
68	-1	-3	
69	-1	-5	
70	1	-5	
71	1	-3	

9.4 Module Marking Information





9.5 Moisture Sensitivity Level

SL917 NCP modules are rated MSL3 (Moisture Sensitivity Level 3). Reels are delivered in packing which conforms to MSL3 requirements.

10. Soldering Recommendations

It is recommended that final PCB assembly of the SL917 NCP Module follows the industry standard as identified by the Institute for Printed Circuits (IPC). This product is assembled in compliance with the J-STD-001 requirements and the guidelines of IPC-AJ-820. Surface mounting of this product by the end user is recommended to follow IPC-A-610 to meet or exceed class 2 requirements.

CLASS 1 General Electronic Products

Includes products suitable for applications where the major requirement is function of the completed assembly.

CLASS 2 Dedicated Service Electronic Products

Includes products where continued performance and extended life is required, and for which uninterrupted service is desired but not critical. Typically the end-use environment would not cause failures.

CLASS 3 High Performance/Harsh Environment Electronic Products

Includes products where continued high performance or performance-on-demand is critical, equipment downtime cannot be tolerated, end-use environment may be uncommonly harsh, and the equipment must function when required, such as life support or other critical systems.

Note: General SMT application notes are provided in AN1223: LGA Manufacturing Guidance.

11. Tape and Reel

The SL917 NCP modules are delivered to the customer in cut tape (100 pcs) or reel (1000 pcs) packaging having the dimensions below. All dimensions are given in mm unless otherwise indicated.

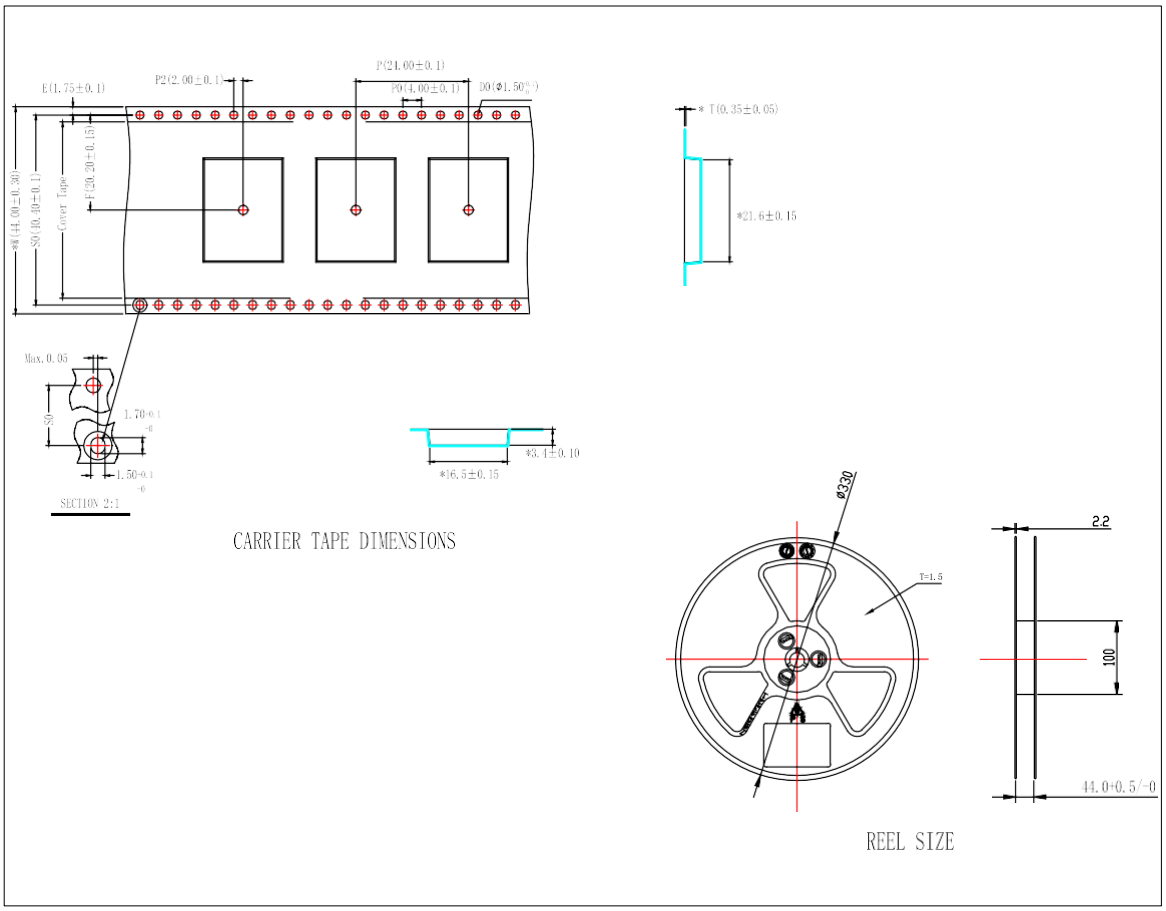


Figure 11.1. Carrier Tape Dimensions

12. Certifications

Note: For complete regulatory information, refer to the Veda SL917 Regulatory Information document which will be available on the Veda SL917 product page.

The Veda SL917 holds current certifications in the following countries (all pending):

Country/Region	Regulatory ID
USA (FCC)	PENDING
Canada (ISED)	PENDING
UK (UKCA)	*No Regulatory ID required
EU	*No Regulatory ID required
China (SRRC)	PENDING
Japan (MIC)	PENDING
Taiwan (NCC)	PENDING
Korea (KC)	PENDING
Australia (AS)	*No Regulatory ID required
New Zealand (NZS)	*No Regulatory ID required

12.1 Qualified Antennas

The Veda SL917 NCP modules have been tested and certified for the use with respectively the built-in integral antenna and a reference external antenna attached to the module's RF pin denoted as RF_PORT. The intended antenna impedance is 50 Ω.

Performance characteristics for the built-in antenna are presented in 8.4 SL917 Integrated Antenna Radiation and Efficiency. The details of the qualified external antenna(s) are summarized in Table 12.1 Qualified External Antenna(s) for the SL917 RF Trace NCP Modules. The qualified external antenna(s) is(are) meant to be directly connected to the module's RF pin, with no active/non-linear component(s) along the RF path in between.

Table 12.1. Qualified External Antenna(s) for the SL917 RF Trace NCP Modules

Manufacturer and Model	Type	Peak Gain	Impedance
TE Connectivity Ltd. (previously Linx Technologies Inc.), ANT-2.4-CW-CT-RPS	Connectorized Coaxial Dipole	+2.8 dBi	50 Ω

Any external antenna of the same general type and of equal or less peak directional gain compared to the one listed in the above table, and having similar in-band and out-of-band characteristics, can be used in the regulatory areas that have modular radio approvals, such as USA and Canada, as long as spot-check testing of the host is performed to verify that no performance changes compromising compliance have been introduced. In the particular FCC case, in order to comply with e-CFR Title 47, Part 15, Subpart C, Section 15.203, the module integrator using an external antenna must ensure it has a unique connector or it is nondetachable.

When using instead an external antenna of a different type (such as a chip antenna, a host PCB trace antenna, or a patch) or having non-similar in-band and out-of-band characteristics, but still with a gain less than or equal to the maximum gain listed in the table above, in principle it can be added to the existing modular grant/certificate by mean of a permissive change, for example with FCC and ISED. Typically, some radiated emission testing is demanded, but no modular or end-product re-certification is required. Please consult your certification house and/or a certification body and/or the module manufacturer for a confirmation of the correct procedures and for any authorization to perform permissive changes.

On the other hand, all products designed to be used with an external antenna having more gain than the maximum gain listed in the table above are very likely to require a full new end-product certification. Since the exact permissive change or registration or re-certification procedure is chosen on a case-by-case basis, please consult your certification house and/or a certification body for understand- ing the correct approach based on your unique design. You might also want or need to

get in touch with Ezurio for any authorization letter that your certification body might ask for.

In countries applying the ETSI standards, where manufacturers issue a self-Declaration of Conformity before placing their end-products in the market, like in the EU countries (and in the UK), the radiated emissions are always evaluated with the end-product and the external antenna type is not critical, but antennas with higher gain may violate some of the EIRP regulatory limits.

For Japan, where compliance testing is done conductively, the allowed external antennas are listed in the certificate and/or test re- port(s). Any other external antenna will have to be formally added to the list of approved antennas by the certificate holder: in this case, please reach out to the module manufacturer to discuss such addition, or consider certifying the end-product itself as an alternative.

12.2 Bluetooth Qualification

Overview

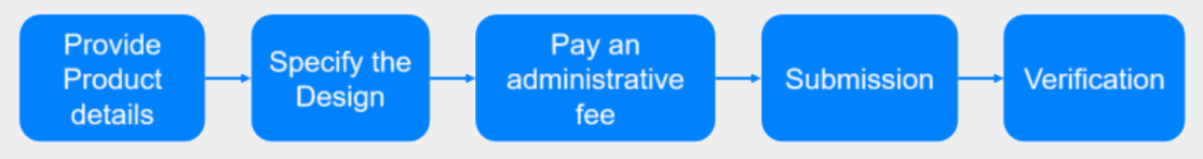
The Bluetooth Qualification Process promotes global product interoperability and reinforces the strength of the Bluetooth® brand and ecosystem to the benefit of all Bluetooth SIG members. The Bluetooth Qualification Process helps member companies ensure their products that incorporate Bluetooth technology comply with the Bluetooth Patent & Copyright License Agreement and the Bluetooth Trademark License Agreement (collectively, the Bluetooth License Agreement) and Bluetooth Specifications.

The Bluetooth Qualification Process is defined by the Qualification Program Reference Document (QPRD) v3.

To demonstrate that a product complies with the Bluetooth Specification(s), each member must for each of its products:

- Identify the product, the design included in the product, the Bluetooth Specifications that the design implements, and the features of each implemented specification
- Complete the Bluetooth Qualification Process by submitting the required documentation for the product under a user account belonging to your company

The Bluetooth Qualification Process consists of the phases shown below:



To complete the Qualification Process the company developing a Bluetooth End Product shall be a member of the Bluetooth SIG. To start the application please use the following link: Apply for Adopter Membership

Scope

This guide is intended to provide guidance on the Bluetooth Qualification Process for End Products that reference multiple existing designs, that have not been modified, (refer to Section 3.2.2.1 of the Qualification Program Reference Document v3).

For a Product that includes a new Design created by combining two or more unmodified designs that have DNs or QDIDs into one of the permitted combinations in Table 3.1 of the QPRDv3, a Member must also provide the following information:

- DNs or QDIDs for Designs included in the new Design
- The desired Core Configuration of the new Design (if applicable, see Table 3.1 below)
- The active TCRL Package version used for checking the applicable Core Configuration (including transport compatibility) and evaluating test requirements

Any included Design must not implement any Layers using withdrawn specification(s).

When creating a new Design using Option 2a, the Inter-Layer Dependency (ILD) between Layers included in the Design will be checked based on the latest TCRL Package version used among the included Designs.

For the purposes of this document, it is assumed that the member is combining unmodified Core-Controller Configuration and Core-Host Configuration designs, to complete a Core-Complete Configuration.

Qualification Steps When Referencing multiple existing designs, (unmodified) – Option 2a in the QPRDv3

For this qualification option, follow these steps:

1. To start a listing, go to: https://qualification.bluetooth.com/
2. Select **Start the Bluetooth Qualification Process**.

3. Product Details to be entered:
    - Project Name (this can be the product name or the Bluetooth Design name).
    - Product Description
    - Model Number
    - Product Publication Date (the product publication date may not be later than 90 days after submission)
    - Product Website (optional)
    - Internal Visibility (this will define if the product will be visible to other users prior to publication)
    - If you have multiple End Products to list then you can select 'Import Multiple Products', firstly downloading and completing the template, then by 'Upload Product List'. This will populate Qualification Workspace with all your products.
4. Specify the Design:
    - Do you include any existing Design(s) in your Product? Answer Yes, I do.
    - Enter the multiple DNs or QDIDs used in your, (for Option 2a two or more DNs or QDIDs must be referenced)
    - Select 'I'm finished entering DN's
    - Once the DNs or QDIDs are selected they will appear on the left-hand side, indicating the layers covered by the design (should show Core-Controller and Core Host Layers covered).
    - What do you want to do next? Answer, 'Combine unmodified Designs'.
    - The Qualification Workspace Tool will indicate that a new Design will be created and what type of Core-Complete configuration is selected.
    - An active TCRL will be selected for the design.
    - Perform the Consistency Check, which should result in no inconsistencies
    - If there are any inconsistencies these will need to be resolved before proceeding
    - Save and go to Test Plan and Documentation
5. Test Plan and Documentation
    a. As no modifications have been made to the combined designs the tool should report the following message: *'No test plan has been generated for your new Design. Test declarations and test reports do not need to be submitted. You can continue to the next step.'*
    b. Save and go to Product Qualification fee
6. Product Qualification Fee:
    - It's important to make sure a Prepaid Product Qualification fee is available as it is required at this stage to complete the Qualification Process.
    - Prepaid Product Qualification Fee's will appear in the available list so select one for the listing.
    - If one is not available select 'Pay Product Qualification Fee', payment can be done immediately via credit card, or you can pay via Invoice. Payment via credit will release the number immediately, if paying via invoice the number will not be released until the invoice is paid.
    - Once you have selected the Prepaid Qualification Fee, select 'Save and go to Submission'
7. Submission:
    - Some automatic checks occur to ensure all submission requirements are complete.
    - To complete the listing any errors must be corrected
    - Once you have confirmed all design information is correct, tick all of the three check boxes and add your name to the signature page.

- Now select ‘Complete the Submission’.
- You will be asked a final time to confirm you want to proceed with the submission, select ‘Complete the Submission’.
- Qualification Workspace will confirm the submission has been submitted. The Bluetooth SIG will email confirmation once the submission has been accepted, (normally this takes 1 working day).

8. Download Product and Design Details (SDoC):
    a. You can now download a copy of the confirmed listing from the design listing page and save a copy in your Compliance Folder

For further information, please refer to the following webpage:

https://www.bluetooth.com/develop-with-bluetooth/qualification-listing/

Example Design Combinations

The following gives an example of a design possible under option 2a:

Ezurio Controller Subsystem + BlueZ 5.50 Host Stack (Ezurio Veda SL917-based design)

Design Name	Owner	Declaration ID	QD ID	Link to listing on the SIG website
TBD				
TBD				

Qualify More Products

If you develop further products based on the same design in the future, it is possible to add them free of charge. The new product must not modify the existing design i.e add ICS functionality, otherwise a new design listing will be required.

To add more products to your design, select ‘Manage Submitted Products’ in the Getting Started page, Actions, Qualify More Products. The tool will take you through the updating process.

13. Documentation and Support

Ezurio offers a set of documents which provide further information required for evaluating, and developing products and applications using the Veda SL917. These documents will be available on the Ezurio website. The documents include information related to Software releases, Evaluation Kits, User Guides, Programming Reference Manuals, Application Notes, and others.

See the Veda SL917 webpage for all supporting documentation:

https://www.ezurio.com/veda-sl917

For further assistance, you can contact Ezurio technical support.

14. Revision History

Revision 0.7

November, 2024

- Updated Cover page
- Updated 1. Feature List
- Updated 3. Applications
- Removed Host Interfaces
- Updated 6.2 Pin Description
- Updated 6.2.3 Peripheral Interfaces
- Updated the following Electrical Specifications:
  - 7.1 Absolute Maximum Ratings
  - 7.2 Recommended Operating Conditions
  - 7.3.1 RESET_N Pin
  - 7.3.2 Power On Control (POC) and Reset
  - 7.3.3 Digital I/O Signals
  - 7.4.2 SDIO 2.0 Secondary
  - 7.4.3 HSPI Secondary
  - Removed UART
  - 7.4.4 GPIO Pins
  - 7.4.5 In-Package Flash Memory
  - Removed SGPIO/MC-PWM/QEI/SCT Timer/SIO Interfaces and USART
- Added Note to 8.4.2 Proximity to Human Body

Revision 0.52

October, 2024

- Updated Notes for 1. Feature List
- Updated 2. Ordering Information
- Reformatted all the tables in Section
- Updated Section 7.5 RF Characteristics
- Updated Table 12.2 Minimum Separation Distances for SAR Evaluation Exemption on page 84
- Updated 12.11 Bluetooth Qualification

Revision 0.5

June, 2024

- Updated Features List
- Updated Ordering Information
- Updated Block Diagrams
- Updated System Overview
- Updated Pin Definitions
- Updated Electrical Specifications
- Updated Reference Schematics, BOM and Layout Guidelines
- Added Certifications

Revision 0.1

September, 2023

- Preliminary version.

15. Additional Information

Please contact your local sales representative or our support team for further assistance:

Headquarters	Ezurio 50 S. Main St. Suite 1100 Akron, OH 44308 USA
Website	http://www.ezurio.com
Technical Support	http://www.ezurio.com/resources/support
Sales Contact	http://www.ezurio.com/contact

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