TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC74LCXR163245FT

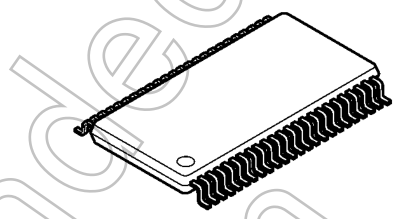
16-Bit Dual Supply Bus Transceiver with Series Resistor

The TC74LCXR163245FT is a dual supply, advanced high-speed CMOS 16-bit dual supply voltage interface bus transceiver fabricated with silicon gate CMOS technology.

Designed for use as an interface between a 3.3-V or a 2.5-V bus and a 5-V bus in mixed 3.3-V or 2.5-V / 5-V supply systems, it achieves high-speed operation while maintaining the CMOS low power dissipation.

It is intended for two-way asynchronous communication between data busses. The direction of data transmission is determined by the level of the DIR input. The enable input ($\overline{OE}$) can be used to disable the device so that the buses are effectively isolated.

The B-port interfaces with the 3.3 V or 2.5 V bus, the A-port with the 5 V bus.



TSSOP48-P-0061-0.50A

Weight: 0.25 g (typ.)

The 26-Ω series resistor helps reducing output overshoot and undershoot without external resistor.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

Features (Note 1) (Note 2)

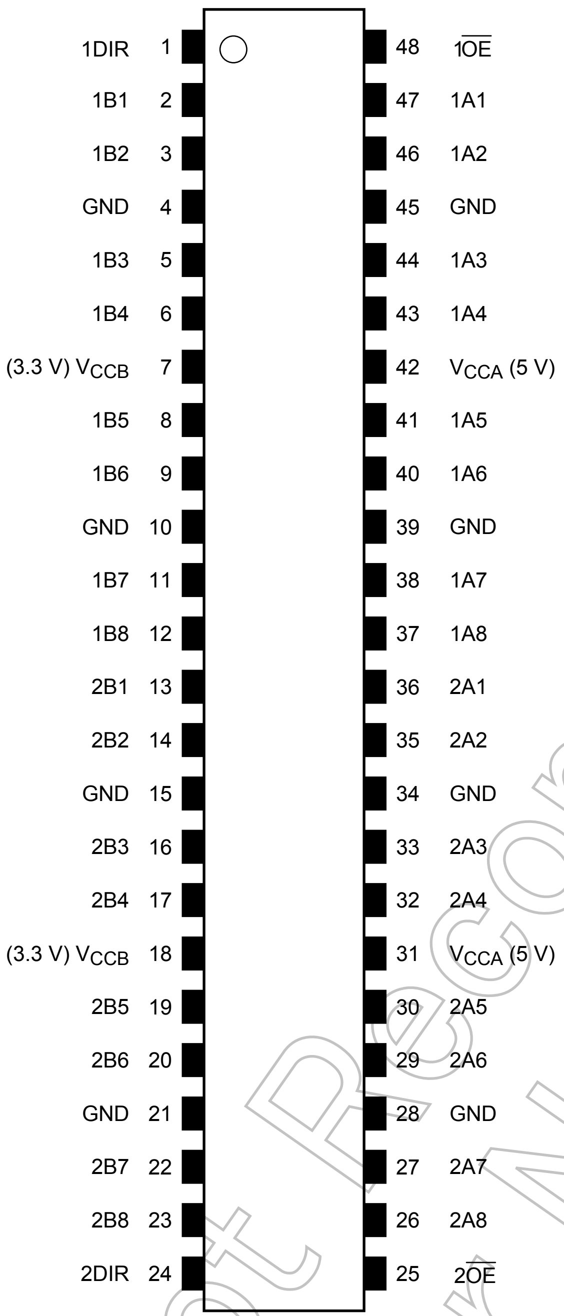
- Bidirectional interface between 3.3 V or 2.5 V buses and 5 V buses
- 26-Ω series resistors on outputs
- High-speed operation: t_{pd} = 8.5 ns (max)
  (V_{CCB} = 3.3 ± 0.3 V / V_{CCA} = 5 ± 0.5 V, Ta = −40 to 85°C)
- Low-voltage operation: I_{CC} = 80 μA (max) (Ta = −40 to 85°C)
- Symmetrical output impedance: I_{OUTB} = ±12 mA (min)
  I_{OUTA} = ±12 mA (min)
  (V_{CCB} = 3.0 V / V_{CCA} = 4.5 V)
- Power-down protection provided on all inputs and outputs
- Allows A port and V_{CCA} to float simultaneously in high state at $\overline{OE}$ pin
- Latch-up performance: −500 mA
- ESD performance: Machine model > ±200 V (Note 2)
- Package: TSSOP

Note 1: Do not apply a signal to any bus pins when it is in the output mode. Damage may result.
All floating (high impedance) bus pins must have their input fixed by means of pull-up or pull-down resistors.

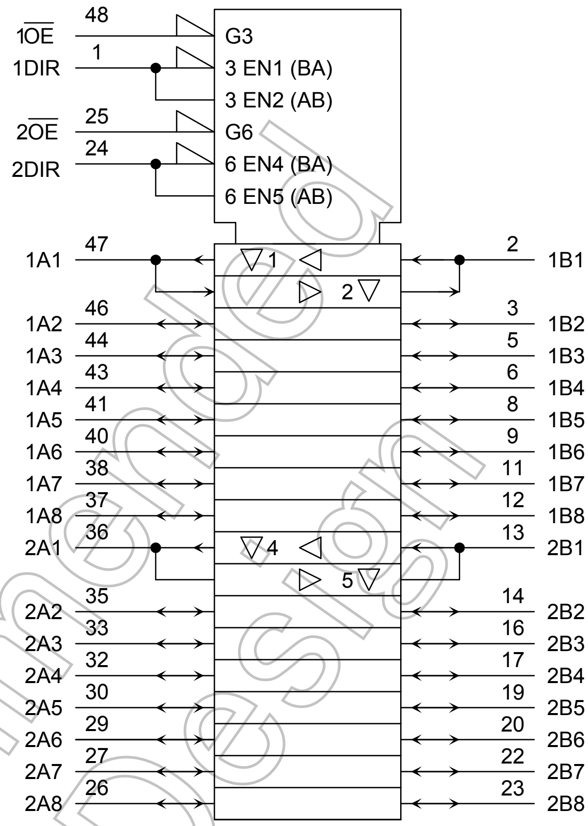
Note 2: This device is electrostatic sensitivity (human body model > 1 kV).
Please handle with caution.

Start of commercial production
1999-03

Pin Assignment (top view)



IEC Logic Symbol



Truth Table

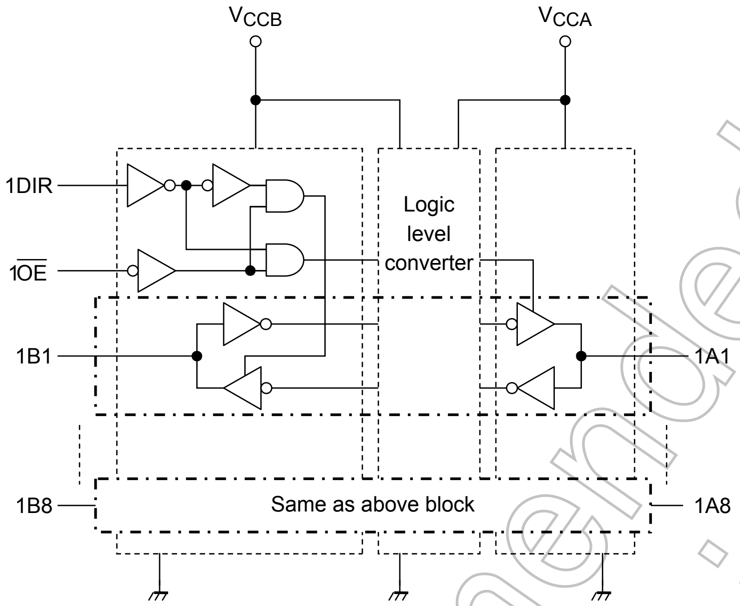
Inputs		Function		Outputs
$1\overline{OE}$	1DIR	Bus 1A1-1A8	Bus 1B1-1B8	
L	L	Output	Input	A = B
L	H	Input	Output	B = A
H	X	Z		Z

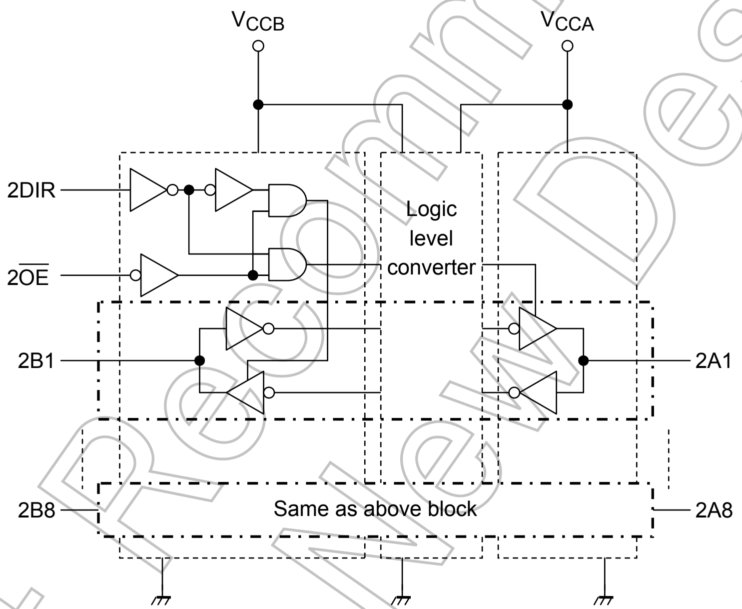
Inputs		Function		Outputs
$2\overline{OE}$	2DIR	Bus 2A1-2A8	Bus 2B1-2B8	
L	L	Output	Input	A = B
L	H	Input	Output	B = A
H	X	Z		Z

X: Don't care

Z: High impedance

Block Diagram





Absolute Maximum Ratings (Note 1)

Characteristics	Symbol	Rating	Unit
Power supply voltage (Note 2)	V_{CCB}	−0.5 to 7.0	V
	V_{CCA}	−0.5 to 7.0	
DC input voltage (DIR, $\overline{OE}$)	V_{IN}	−0.5 to 7.0	V
DC bus I/O voltage	$V_{I/OB}$	−0.5 to 7.0 (Note 3)	V
		−0.5 to V_{CCB} + 0.5 (Note 4)	
	$V_{I/OA}$	−0.5 to 7.0 (Note 3)	
		−0.5 to V_{CCA} + 0.5 (Note 4)	
Input diode current	I_{IK}	−50	mA
Output diode current	$I_{I/OK}$	±50 (Note 5)	mA
DC output current	I_{OUTB}	±50	mA
	I_{OUTA}	±50	
DC V_{CC}/ground current per supply pin	I_{CCB}	±100	mA
	I_{CCA}	±100	
Power dissipation	P_D	400	mW
Storage temperature	T_{stg}	−65 to 150	°C

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.
Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 2: Don't supply a voltage to V_{CCA} terminal when V_{CCB} is in the off-state.

Note 3: Output in OFF state

Note 4: High or low state. I_{OUT} absolute maximum rating must be observed.

Note 5: V_{OUT} < GND, V_{OUT} > V_{CC}

Operating Ranges (Note 1)

Characteristics	Symbol	Rating	Unit
Power supply voltage (Note 2)	V_{CCB}	2.3 to 3.6	V
	V_{CCA}	4.5 to 5.5	
Input voltage (DIR, $\overline{OE}$)	V_{IN}	0 to 5.5	V
DC bus I/O voltage	$V_{I/OB}$	0 to 5.5 (Note 3)	V
		0 to V_{CCB} (Note 4)	
	$V_{I/OA}$	0 to 5.5 (Note 3)	
		0 to V_{CCA} (Note 4)	
Output current	I_{OUTB}	±12 (Note 5)	mA
		±4 (Note 6)	
	I_{OUTA}	±12 (Note 7)	
Operating temperature	T_{opr}	−40 to 85	°C
Input rise and fall time	dt/dv	0 to 10 (Note 8)	ns/V

Note 1: The operating ranges must be maintained to ensure the normal operation of the device. Unused inputs must be tied to either V_{CC} or GND. Please connect both bus inputs and the bus outputs with V_{CC} or GND when the I/O of the bus terminal changes by the function. In this case, please note that the output is not short-circuited.

Note 2: Don't use in $V_{CCB} > V_{CCA}$.

Note 3: Output in OFF state

Note 4: High or low state

Note 5: $V_{CCB} = 3.0$ to 3.6 V

Note 6: $V_{CCB} = 2.3$ to 2.7 V

Note 7: $V_{CCA} = 4.5$ to 5.5 V

Note 8: $V_{INB} = 0.8$ to 2.0 V, $V_{CCB} = 3.0$ V
$V_{INA} = 0.8$ to 2.0 V, $V_{CCA} = 5.0$ V

Electrical Characteristics

DC Characteristics

Characteristics	Symbol	Test Condition		V_{CCB} (V)	V_{CCA} (V)	Ta = −40 to 85°C Min	Ta = −40 to 85°C Max	Unit
H-level input voltage	V_{IHB}	DIR, $\overline{OE}$, Bn		2.5 ± 0.2	5.0 ± 0.5	1.7	—	V
				3.3 ± 0.3	5.0 ± 0.5	2.0	—	
	V_{IHA}	An		2.3 to 3.6	5.0 ± 0.5	2.0	—	
L-level input voltage	V_{ILB}	DIR, $\overline{OE}$, Bn		2.5 ± 0.2	5.0 ± 0.5	—	0.7	V
				3.3 ± 0.3	5.0 ± 0.5	—	0.8	
	V_{ILA}	An		2.3 to 3.6	5.0 ± 0.5	—	0.8	
H-level output voltage	V_{OHB}	$V_{INA} = V_{IHA}$ or V_{ILA}, $V_{INB} = V_{IHB}$ or V_{ILB}	$I_{OHB} = -100$ μA	2.3 to 3.6	5.0 ± 0.5	$V_{CCB} - 0.2$	—	V
			$I_{OHB} = -12$ mA	3.0	5.0 ± 0.5	2.2	—	
			$I_{OHB} = -4$ mA	2.3	5.0 ± 0.5	1.8	—	
	V_{OHA}		$I_{OHA} = -100$ μA	2.3 to 3.6	5.0 ± 0.5	$V_{CCA} - 0.2$	—	
			$I_{OHA} = -12$ mA	2.3 to 3.6	4.5	3.7	—	
L-level output voltage	V_{OLB}	$V_{INA} = V_{IHA}$ or V_{ILA}, $V_{INB} = V_{IHB}$ or V_{ILB}	$I_{OLB} = 100$ μA	2.3 to 3.6	5.0 ± 0.5	—	0.2	V
			$I_{OLB} = 12$ mA	3.0	5.0 ± 0.5	—	0.8	
			$I_{OLB} = 4$ mA	2.3	5.0 ± 0.5	—	0.6	
	V_{OLA}		$I_{OLA} = 100$ μA	2.3 to 3.6	5.0 ± 0.5	—	0.2	
			$I_{OLA} = 12$ mA	2.3 to 3.6	4.5	—	0.7	
3-state output OFF state current	I_{OZB}	$V_{IN} = V_{IHB}$ or V_{ILB}, $V_{I/OB} = V_{CCB}$ or GND		2.3 to 3.6	5.0 ± 0.5	—	±5.0	μA
	I_{OZA}	$V_{IN} = V_{IHB}$ or V_{ILB}, $V_{I/OA} = V_{CCA}$ or GND		2.3 to 3.6	5.0 ± 0.5	—	±5.0	
Input leakage current	I_{IN}	V_{IN} (DIR, $\overline{OE}$) = V_{CCB} or GND		3.6	5.5	—	±5.0	μA
Power-off leakage current	I_{OFF}	V_{INA}/V_{INB} = 0 to 5.5 V		0	0	—	10	μA
Quiescent supply current	I_{CCB1}	$V_{I/OA}$ = Open, V_{CCA} = Open, $V_{\overline{OE}} = V_{CCB}$, DIR = GND		3.6	Open	—	50	μA
	I_{CCB2}	$V_{INA} = V_{CCA}$ or GND, $V_{INB} = V_{CCB}$ or GND		3.6	5.5	—	50	
	I_{CCA}	$V_{INA} = V_{CCA}$ or GND, $V_{INB} = V_{CCB}$ or GND		3.6	5.5	—	80	
	I_{CCTB}	$V_{INB} = V_{CCB} - 0.6$ V per input		3.6	5.0 ± 0.5	—	500	
	I_{CCTA}	V_{INA} = 3.4 V per input		2.3 to 3.6	5.5	—	2.0	mA

AC Characteristics (input: $t_r = t_f = 2.5$ ns, $R_L = 500\ \Omega$)

$V_{CCB} = 3.3 \pm 0.3$ V

Characteristics	Symbol	Test Condition	CL (pF)	V_{CCA} (V)	Ta = –40 to 85°C Min	Ta = –40 to 85°C Max	Unit
Propagation delay time (Bn → An)	t_{pLH} t_{pHL}	Input: Bn Output: An (DIR = "L")	50	5.0 ± 0.5	1.0	7.5	ns
3-state output enable time ($\overline{OE}$ → An)	t_{pZL} t_{pZH}		50	5.0 ± 0.5	1.0	9.5	
3-state output disable time ($\overline{OE}$ → An)	t_{pLZ} t_{pHZ}		50	5.0 ± 0.5	1.0	9.5	
Propagation delay time (An → Bn)	t_{pLH} t_{pHL}	Input: An Output: Bn (DIR = "H")	50	5.0 ± 0.5	1.0	8.5	ns
3-state output enable time ($\overline{OE}$ → Bn)	t_{pZL} t_{pZH}		50	5.0 ± 0.5	1.0	9.5	
3-state output disable time ($\overline{OE}$ → Bn)	t_{pLZ} t_{pHZ}		50	5.0 ± 0.5	1.0	9.5	
Output to output skew	t_{osLH} t_{osHL}	(Note)	50	5.0 ± 0.5	—	1.0	ns

Note: Parameter guaranteed by design.
($t_{osLH} = |t_{pLHm} - t_{pLHn}|$, $t_{osHL} = |t_{pHLm} - t_{pHLn}|$)

$V_{CCB} = 2.5 \pm 0.2$ V

Characteristics	Symbol	Test Condition	CL (pF)	V_{CCA} (V)	Ta = –40 to 85°C Min	Ta = –40 to 85°C Max	Unit
Propagation delay time (Bn → An)	t_{pLH} t_{pHL}	Input: Bn Output: An (DIR = "L")	50	5.0 ± 0.5	1.0	9.0	ns
3-state output enable time ($\overline{OE}$ → An)	t_{pZL} t_{pZH}		50	5.0 ± 0.5	1.0	13.0	
3-state output disable time ($\overline{OE}$ → An)	t_{pLZ} t_{pHZ}		50	5.0 ± 0.5	1.0	14.0	
Propagation delay time (An → Bn)	t_{pLH} t_{pHL}	Input: An Output: Bn (DIR = "H")	30	5.0 ± 0.5	1.0	9.5	ns
3-state output enable time ($\overline{OE}$ → Bn)	t_{pZL} t_{pZH}		30	5.0 ± 0.5	1.0	12.5	
3-state output disable time ($\overline{OE}$ → Bn)	t_{pLZ} t_{pHZ}		30	5.0 ± 0.5	1.0	10.0	
Output to output skew	t_{osLH} t_{osHL}	(Note)	30 or 50	5.0 ± 0.5	—	1.0	ns

Note: Parameter guaranteed by design.
($t_{osLH} = |t_{pLHm} - t_{pLHn}|$, $t_{osHL} = |t_{pHLm} - t_{pHLn}|$)

Capacitive Characteristics (Ta = 25°C)

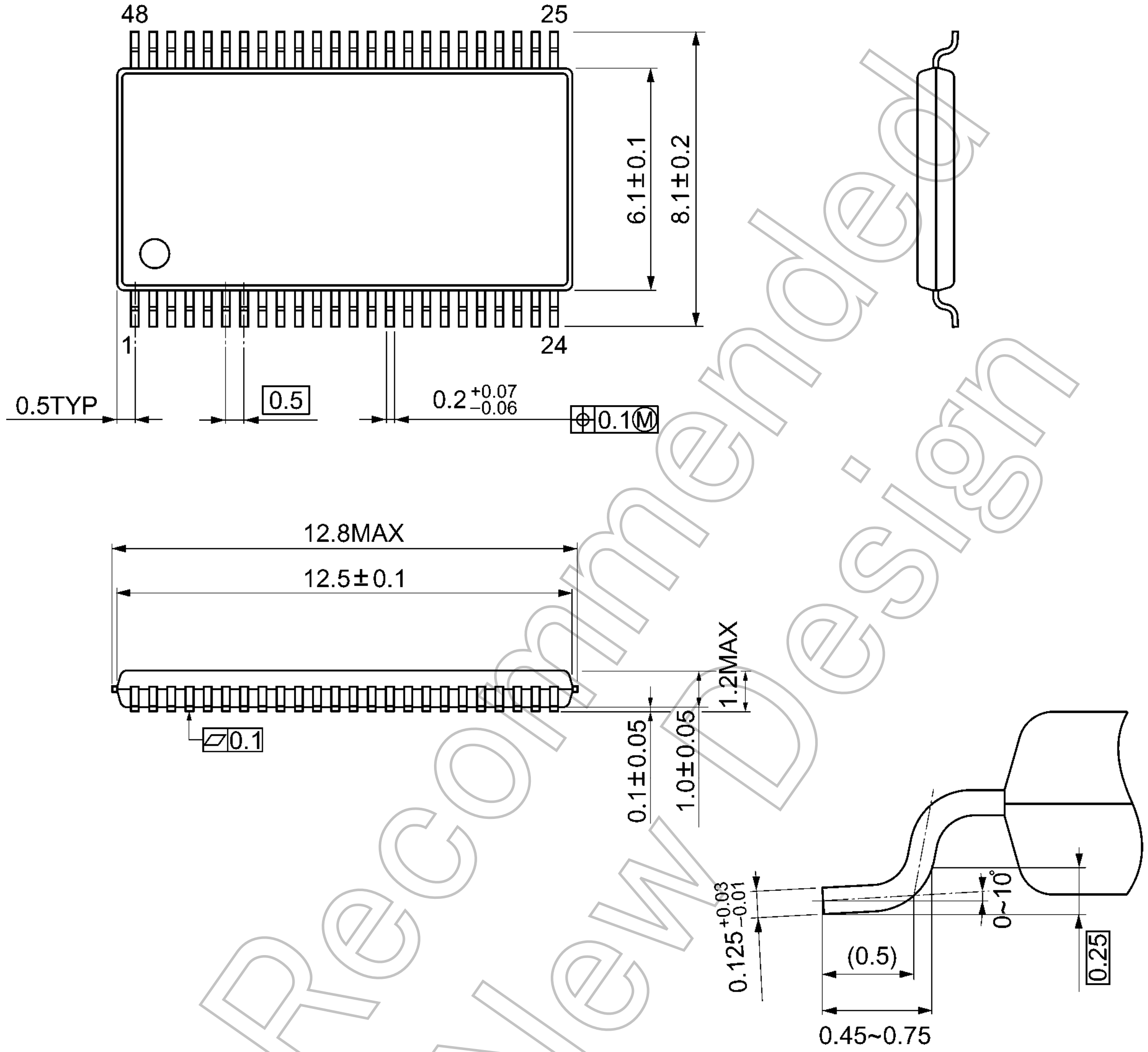
V_{CCB} = 2.5, 3.3 V

Characteristics	Symbol	Test Circuit	Test Condition	V_{CCA} (V)	Typ.	Unit
Input capacitance	C_{IN}	—	DIR, $\overline{OE}$	5.0	7	pF
Output capacitance	$C_{I/O}$	—	An, Bn	5.0	8	pF
Power dissipation capacitance (Note)	C_{PDA}	—	A ⇒ B (DIR = "H")	5.0	20	pF
			B ⇒ A (DIR = "L")	5.0	66	
	C_{PDB}	—	A ⇒ B (DIR = "H")	5.0	34	pF
			B ⇒ A (DIR = "L")	5.0	4	

Note: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:
$I_{CC\ (opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$ / 16 (per bit)

Package Dimensions

TSSOP48-P-0061-0.50A Unit: mm



Weight: 0.25 g (typ.)

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