APPLICATION MANUAL

RV-3029-C2

Real Time Clock / Calendar Module with Temperature Compensation and I2C-Interfcae

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Real Time Clock / Calendar Module RV-3029-C2

Ultra Low Power serial I/O 32 kHz RTC

1 Description

The RV3029/49 is Ultra Low Power CMOS real-time clock IC with possibility one of the serial interfaces: I2C, SPI or 3-wires. The choice of the interface is fixed according to the chip version.

A clock is obtained from 32768 Hz crystal oscillator. A thermal compensation of the frequency is based on the temperature measurement and calculation of a correction value. The temperature can be measured internally or written by an external application to the register.

The chip provides clock and calendar information in BCD format with alarm possibility. An actual contents are latched at the beginning of a transaction and afterwards data are read without clock counter data corruption.

An integrated 16-bit timer can run in Zero-Stop or Auto-Reload mode.

An interrupt can be provided through INT/ pad due to events coming from Alarm, Timer, Voltage detector and Digital Self-Recovery system.

An integrated Trickle Charger allows recharging Backup Supply V_{Back} from the Main Supply Voltage Vcc through internal resistor(s).

The device supply will switchover V_{cc} when V_{cc} is higher than V_{Back}.

The device operates over a wide 1.3 V to 5.5 V supply range and requires only 980nA at 5 V. It's possible to detect internally two voltage levels.

Only decoupling capacitor needed.

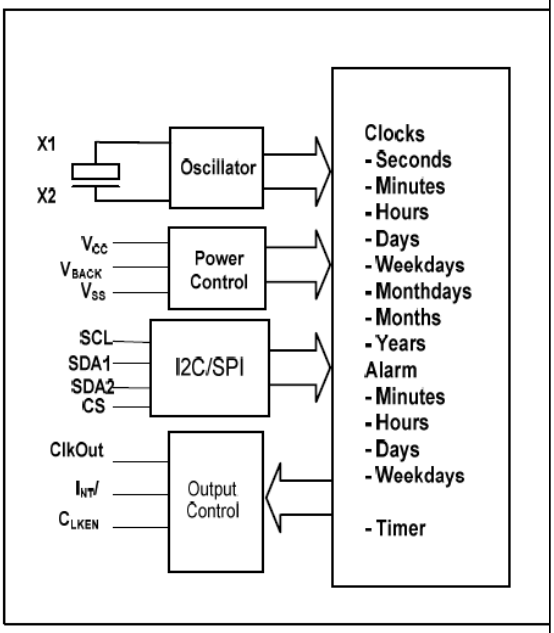
Applications

- Utility meters
- Battery operated and portable equipment
- Consumer electronics
- White/brown goods
- Pay phones
- Cash registers
- Personal computers
- Programmable controller systems
- Automotive systems
- Data loggers

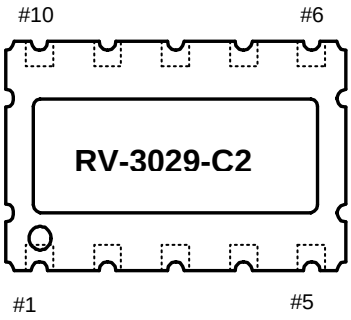
Features

- Supply current typically 900 nA at 1.3V
- Fully operational from 1.8 V to 5.5V
- Trickle Charger to preserve Battery Discharge and Data Integrity
- Low Voltage Detection
- Supply switchover
- Serial communication via I2C, SPI or 3-wires
- No busy states and no risk of corrupted data while accessing
- Oscillator stability 0.3 ppm / volt
- Thermal compensated crystal frequency deviation.
- Counts Seconds, minutes, hours, day of week, date month, year, in BCD format + alarm
- Leap year compensation
- Timer peripheral included
- Digital Self-Recovery system
- 1 hour periodical refresh of EEPROM registers
- Standard Temperature Range: -40℃ to +85℃
- Extended Temperature Range: -40℃ to +125℃
- Packages: SON10

Block Diagram

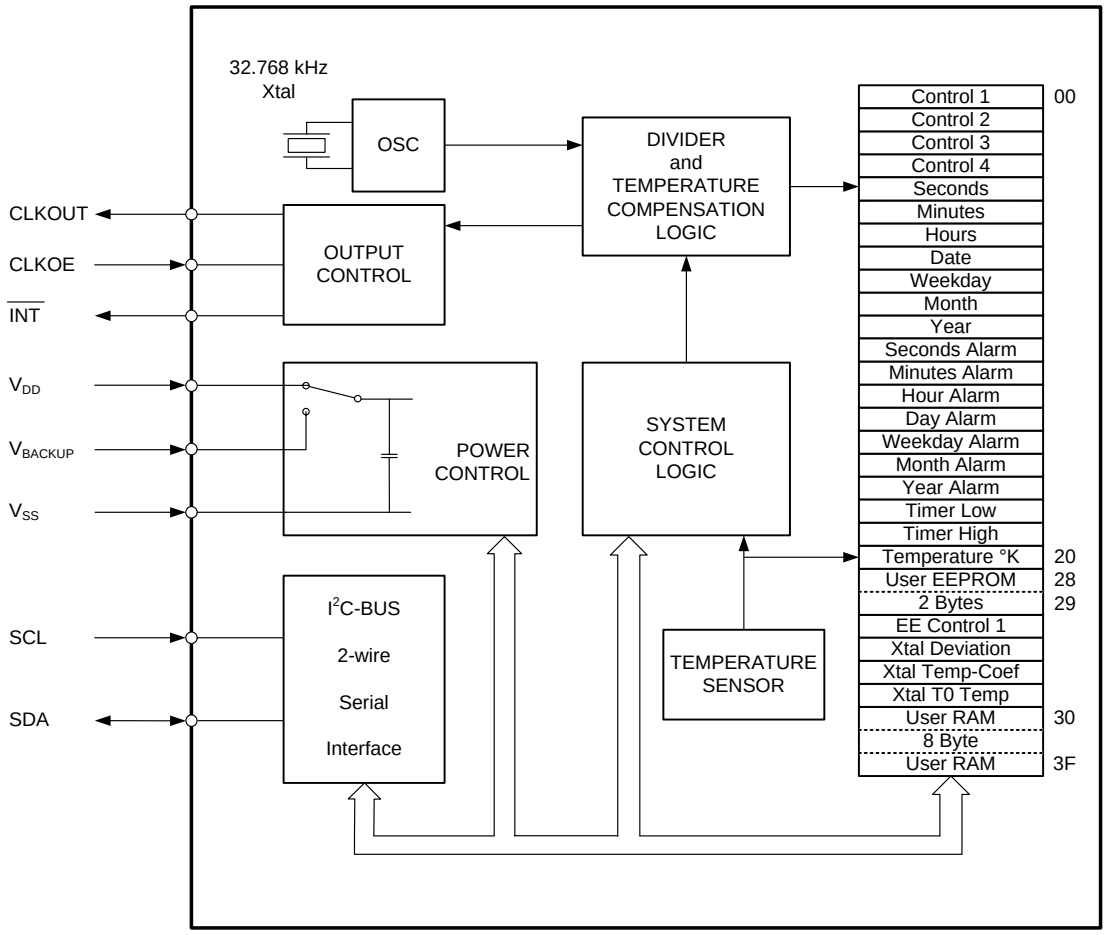


2.1 PINOUT



# 1	V_{DD}	# 10	CLKOE
# 2	CLKOUT	# 9	N.C.
# 3	N.C	# 8	V_{BACKUP}
# 4	SCL	# 7	$\overline{INT}$
# 5	SDA	# 6	V_{SS}

2.0 BLOCK DIAGRAM



4 Absolute Maximum Ratings

Parameter	Symbol	Conditions
Maximum voltage at V_{CC}	V_{CCmax}	V_{SS} + 6.0V
Minimun voltage at V_{CC}	V_{CCmin}	V_{SS} – 0.3V
Maximum voltage at any signal pin	V_{max}	V_{CC} + 0.3V
Minimum voltage at any signal pin	V_{min}	V_{SS} – 0.3V
Maximum storage temperature	T_{STOmax}	+150℃
Minimum storage temperature	T_{STOmin}	-65℃
Electrostatic discharge maximum to MIL-STD-883C method 3015.7 with ref. to V_{SS}	V_{Smax}	2000V

Table 1

Stresses above these listed maximum ratings may cause permanent damages to the device. Exposure beyond specified operating conditions may affect device reliability or cause malfunction.

4.1 Handling Procedures

This device has built-in protection against high static voltages or electric fields; however, anti-static precautions must be taken as for any other CMOS component. Unless otherwise specified, proper operation can only occur when all terminal voltages are kept within the voltage range. Unused inputs must always be tied to a defined logic voltage level.

4.2 Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Operating temperature	T_A	-40		+125	℃
Supply voltage	V_{CC} or V_{BACK}	1.3	5.0	5.5	V
Supply voltage dv/dt (power-up & power-down)	dv/dt	0.06		6	V/µs
Decoupling capacitor	C_D		100		nF

Table 2

4.3 Crystal characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Frequency	f		32.768		kHz
Load capacitance	C_L	7	8.2	12.5	pF
Series resistance	R_S		70	110	kΩ

Table 3

4.4 EEPROM characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Read voltage	V_{read}	1.3			V
Programming voltage (allowed temp -40 to +85℃)	V_{prog}	2.3			V
Cycling			5000		cycles

Table 4

5 Electrical Characteristics

5.1 Electrical Characteristics, standard temperature range.

V_{CC}= 1.3V, V_{SS} = 0V and T_A=-40 to +85℃, unless otherwise specified

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Total static supply	I_{SS}	All outputs open, all inputs at V_{CC}, SDA and SCL at V_{CC},Rs< 70 kΩ		0.25	0.5	µA
Dynamic current	I_{DD}	SCL= 100 kHz			300	µA
Low Supply Detection2	Vlow2	Voltage applied on VCC or Vback	1.30		1.35	V
Switchover Hysteresis	Vhyst	VCC wrt Vback	50			mV
Input / Output						
Input logic low	V_{IL}	Inputs level low			0.3	V
Input logic high	V_{IH}	Inputs level high	0.9			V
Output logic low	V_{OL}	I_{OL} = 0.4 mA			0.2	V
Output logic high	V_{OH}	I_{OH} = 0.1mA	1.0			V
Input leakage	I_{IN}	0.0 < V_{IN} < 1.3V		0.1	1	µA
Output tri-state leakage on I/Opin	I_{TS}	CS low		0.1	1	µA
Oscillator						
Starting voltage	V_{STA}		1.2			V
Input capacitance on XI	C_{IN}	T_A = +25℃		13		pF
Output capacitance on XO	C_{OUT}	T_A = +25℃		9		pF
Start-up time	T_{STA}			1		s
Frequency stability	Δf/f	1.5 ≤ V_{CC} ≤ 5.5V, T_A = +25℃		0.2	2	ppm/V

Table 5

5.2 Electrical Characteristics, standard temperature range.

V_{CC}= 5.0V, V_{SS} = 0V and T_A=-40 to +85℃, unless otherwise specified

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Total static supply	I_{SS}	All outputs open, all inputs at V_{SS} V_{CC} = 5.0V,Vback=3V Rs< 70 kΩ SCl at Vcc		0.6	1	µA
Dynamic current	I_{DD}	SCL = 200k			300	µA
Low Supply Detection1	Vlow1	Voltage applied on VCC or Vback	1.8		1.85	V
Low Supply Detection2	Vlow2	Voltage applied on VCC or Vback	1.3		1.35	V
Switchover Hysteresis	Vhyst	VCC wrt Vback	50			mV
Input / Output						
Input logic low	V_{IL}	Inputs level low			0.5	V
Input logic high	V_{IH}	Inputs level high	3.0			V
Output logic low	V_{OL}	I_{OL} = 6 mA			0.4	V
Output logic high	V_{OH}	I_{OH} = 2 mA	3.5			V
Input leakage	I_{IN}	0.0 < V_{IN} < 5.0V		0.1	1	µA
Output tri-state leakage on I/Opin	I_{TS}	CS low		0.1	1	µA
Oscillator						
Starting voltage	V_{STA}		1.2			V
Input capacitance on XI	C_{IN}	T_A = +25℃		13		pF
Output capacitance on XO	C_{OUT}	T_A = +25℃		9		pF
Start-up time	T_{STA}			1		S
Frequency stability	Δf/f	1.5 ≤ V_{CC} ≤ 5.5V, T_A = +25℃		0.2	2	ppm/V

Table 6

5.3 Electrical Characteristics, extended temperature range.

V_{CC}= 1.3V, V_{SS} = 0V and T_A=-40 to +125℃, unless otherwise specified

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Total static supply	I_{SS}	All outputs open, all inputs at V_{SS}, Rs< 70 kΩ		0.4	0.8	µA
Dynamic current	I_{DD}	SCL = 100 kHz			300	µA
Low supply Detection	Vlow		1.30		1.35	V
Switchover Hysteresis	Vhyst	VCC wrt Vback	50			mV
Input / Output						
Input logic low	V_{IL}	Inputs level low			0.3	V
Input logic high	V_{IH}	Inputs level high	1.0			V
Output logic low	V_{OL}	I_{OL} = 0.4 mA			0.2	V
Output logic high	V_{OH}	I_{OH} = 0.1 mA	1.1			V
Input leakage	I_{IN}	0.0 < V_{IN} < 1.3V		0.1	1	µA
Output tri-state leakage on I/O's	I_{TS}	I/O pins in Hi-Z mode		0.1	1	µA
Oscillator						
Starting voltage	V_{STA}		1.2			V
Supply voltage dV/dt (power-up & power-down)			0.06		6	V/µs
Input capacitance on XI	C_{IN}	T_A = +25℃		13		pF
Output capacitance on XO	C_{OUT}	T_A = +25℃		9		pF
Start-up time	T_{STA}	T_A = +125℃ (note 1)		10		s
Frequency stability	Δf/f	2.0 ≤ V_{CC} ≤ 5.5V, T_A = +25℃		0.2	2	ppm/V

Table 7

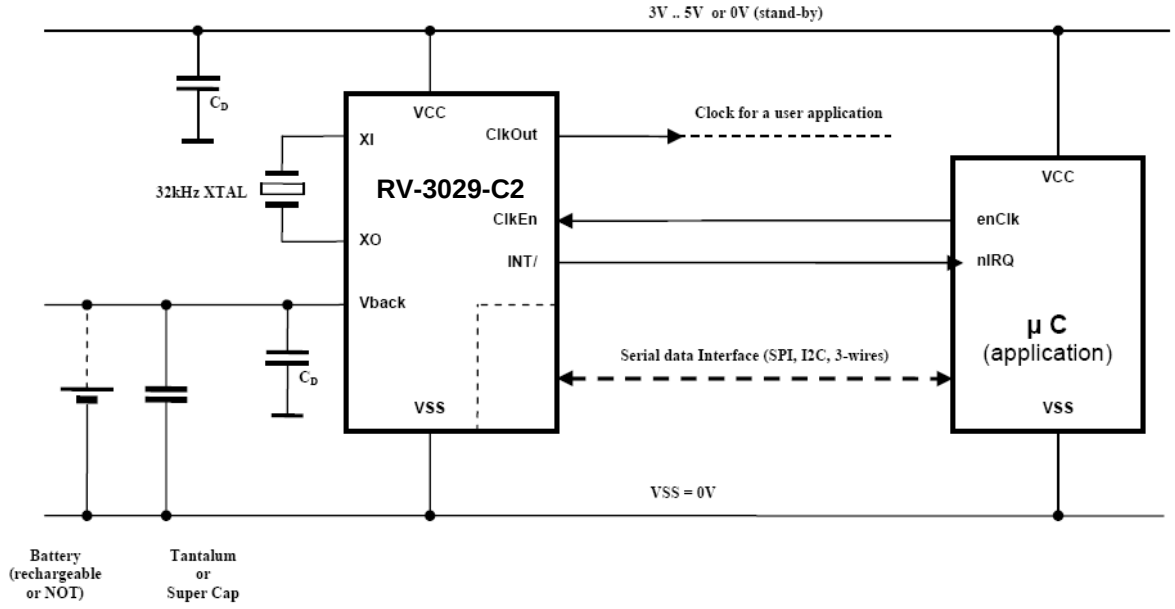
5.4 Electrical Characteristics, extended temperature range

V_{CC}= 5.0V, V_{SS} = 0V and T_A=-40 to +125℃, unless otherwise specified

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Total static supply	I_{SS}	All outputs open, all inputs at V_{ss} V_{CC} = 5.0V, Rs< 70 kΩ,		0.8	1.2	µA
Dynamic current	I_{DD}	I/O to V_{SS} through 1MΩ SCL, SDA = 2 MHz			300	µA
Low supply Detection1	Vlow1	Voltage applied on VCC or Vback	1.8		1.85	V
Low supply Detection2	Vlow2	Voltage applied on VCC or Vback	1.3		1.35	V
Switchover Hysteresis	Vhyst	VCC wrt Vback	50			mV
Input / Output						
Input logic low	V_{IL}	Inputs level low			0.5	V
Input logic high	V_{IH}	Inputs level high	3.0			V
Output logic low	V_{OL}	I_{OL} = 6 mA			0.4	V
Output logic high	V_{OH}	I_{OH} = 2 mA	3.5			V
Input leakage	I_{IN}	0.0 < V_{IN} < 5.0V		0.1	1	µA
Output tri-state leakage on I/O's	I_{TS}	I/O pins in Hi-Z mode		0.1	1	µA
Oscillator						
Starting voltage	V_{STA}		1.2			V
Supply voltage dV/dt (power-up & power-down)			0.06		6	V/µs
Input capacitance on XI	C_{IN}	T_A = +25℃		13		pF
Output capacitance on XO	C_{OUT}	T_A = +25℃		9		pF
Start-up time	T_{STA}	T_A = +125℃ (note 1)		10		s
Frequency stability	Δf/f	2.0 ≤ V_{CC} ≤ 5.5V, T_A = +25℃		0.2	2	ppm/V

Table 8

6 Application schematic



6.1 AC characteristics – I2C

V_{CC} = 1.8V to 5.5V, T_A=-40℃ to +125℃

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCL Clock Frequency	f_{SCL}	Fast mode	100		400	kHz
		Standard mode			100	
Bus Free Time Between STOP and START Condition	t_{BUF}	Fast mode	1.3			µs
		Standard mode	4.7			
Hold Time (Repeated) START Condition	$t_{HD:STA}$	Fast mode	0.6			µs
		Standard mode	4.0			
LOW Period of SCL Clock	t_{LOW}	Fast mode	1.3			µs
		Standard mode	4.7			
HIGH Period of SCL Clock	t_{HIGH}	Fast mode	0.6			µs
		Standard mode	4.0			
Setup Time (Repeated) START Condition	$t_{SU:STA}$	Fast mode	0.6			µs
		Standard mode	4.7			
Data Hold Time	$t_{HD:DAT}$	Fast mode	0		0.9	µs
		Standard mode	0			
Data Setup Time	$t_{SU:DAT}$	Fast mode	100			ns
		Standard mode	250			
Rise Time of Both SDA and SCL Signals	t_R	Fast mode	$20+0.1C_B$		300	ns
		Standard mode	$20+0.1C_B$		1000	
Fall Time of Both SDA and SCL Signals	t_F	Fast mode	$20+0.1C_B$		300	ns
		Standard mode	$20+0.1C_B$		300	
Setup Time (Repeated) STOP Condition	$t_{SU:STO}$	Fast mode	0.6			µs
		Standard mode	4.0			
Capacitive Load For Each Bus Line	C_B				400	pF
I/O Capacitance (SDA, SCL)	$C_{I/O}$				10	pF
SCK Pull-Up	R_{PU}			100		kΩ

Table 9

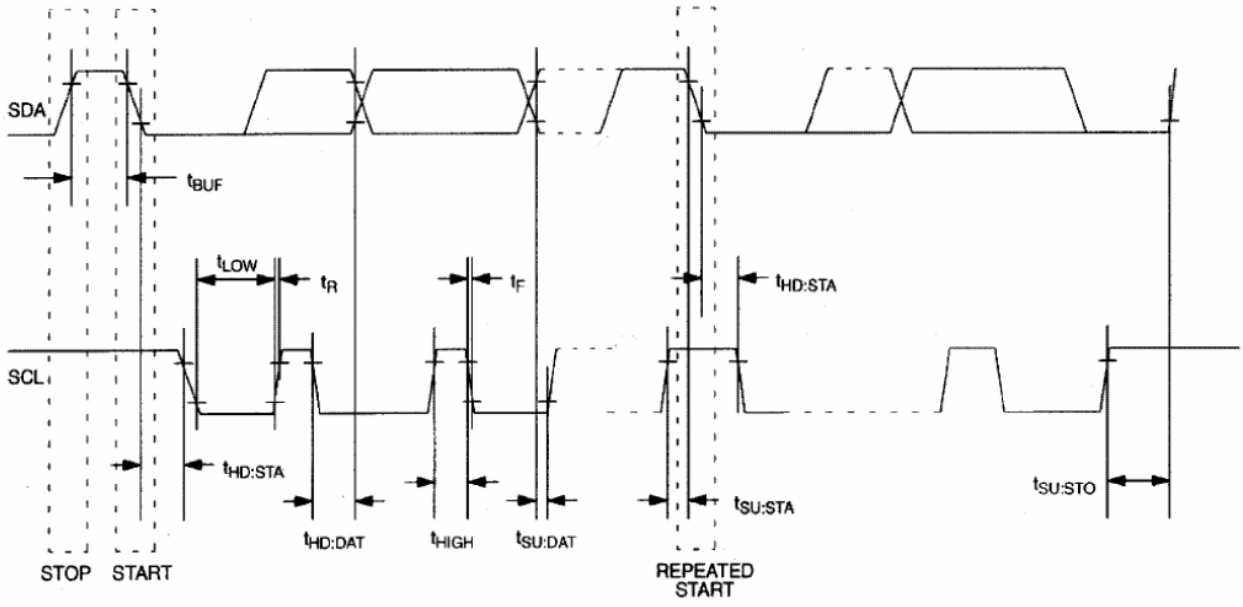


Figure 1 : Timing - I2C

6.2 AC characteristics – SPI

V_{CC}= 5.0V, V_{SS} = 0V and T_A=-40 to +125°C, unless otherwise specified

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCK Clock Frequency	f_{SCK}	2.7V ≤ V_{CC} ≤ 5.5V			2	MHz
		1.71V ≤ V_{CC} ≤ 1.89V			1	
Data to SCK Setup	t_{DC}		30			ns
SCK to Data Hold	t_{CDH}		30			ns
SCK to Data Valid	t_{CDD}	2.7V ≤ V_{CC} ≤ 5.5V			80	ns
		1.71V ≤ V_{CC} ≤ 1.89V			160	
SCK Low Time	t_{CL}	2.7V ≤ V_{CC} ≤ 5.5V	210			ns
		1.71V ≤ V_{CC} ≤ 1.89V	400			
SCK High Time	t_{CH}	2.7V ≤ V_{CC} ≤ 5.5V	210			ns
		1.71V ≤ V_{CC} ≤ 1.89V	400			
SCK Rise and Fall	t_R , t_F				200	ns
CS to SCK Setup	t_{CC}		400			ns
SCK to CS Hold	t_{CCH}		200			ns
CS Inactive Time	t_{CWL}	2.7V ≤ V_{CC} ≤ 5.5V	400			ns
		1.71V ≤ V_{CC} ≤ 1.89V	500			
CS to Output High Impedance	t_{CDZ}				100 ??	ns

Table 10

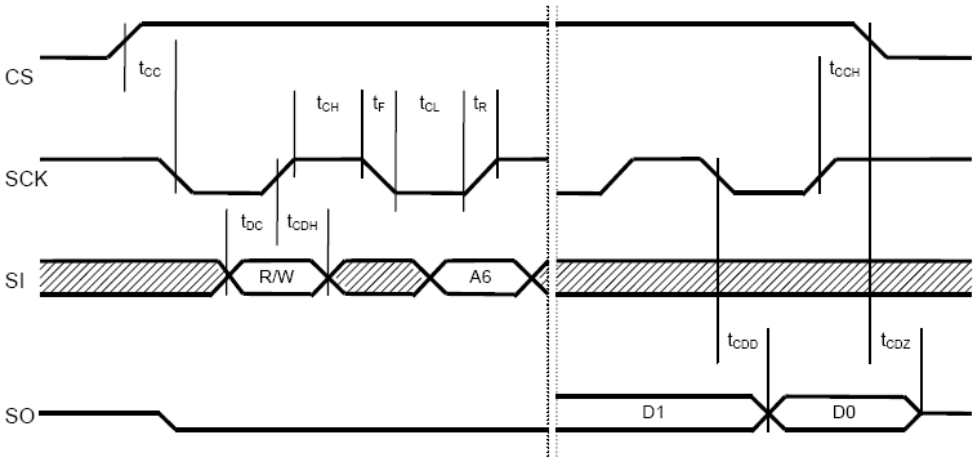


Figure 2 : Timing - SPI read

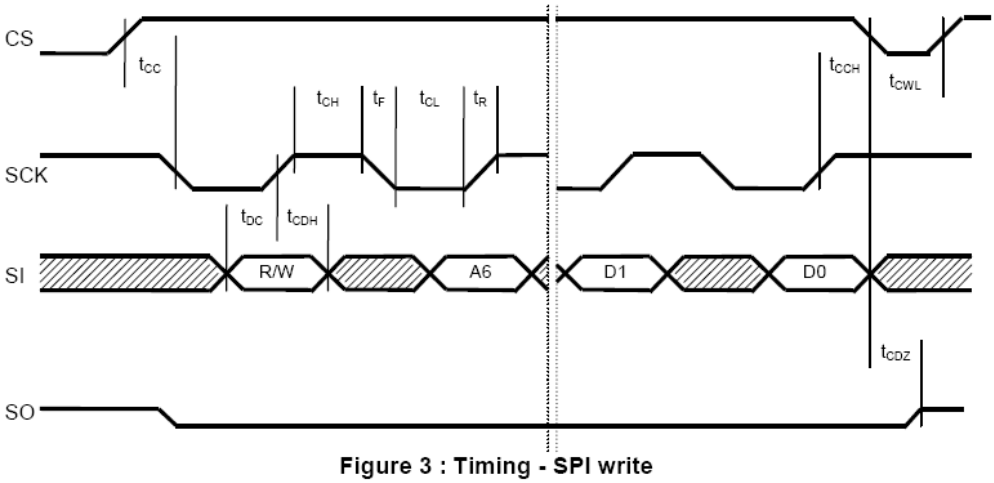


Figure 3 : Timing - SPI write

7 Crystal thermal behaviour

A frequency of the real crystal is dependent on the temperature concurring with the following diagram:

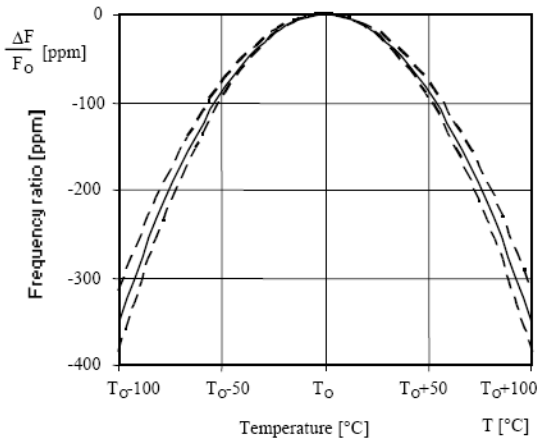


Figure 6 – crystal thermal behaviour

T_O – turnover temperature in [℃]
F_O – crystal frequency when T_O

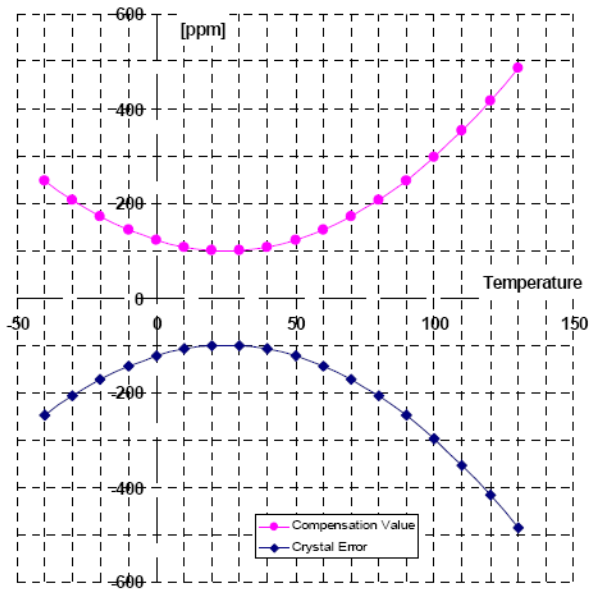
The following expression expresses a correction value to be used during compensation.

$$COMP\_val = Qcoef \times (T - To)^2 - XtalOffset$$

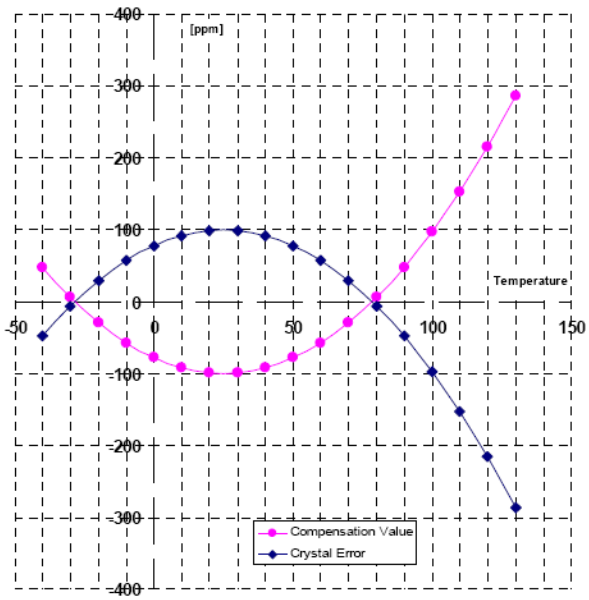
Qcoef	– thermal quadratic coefficient
T	– actual temperature in [℃]
T_O	– turnover temperature in [℃]
XtalOffset	– crystal offset at T_O
COMP_val	– compensation value result in [ppm]

The Oscillator Frequency is adjusted, according to the equation above by using coefficients located in the EEPROM control page and a temperature.
The actual temperature can be obtained from the internal thermometer or from the register updated externally by an application.
A principle of the frequency compensation is based on the adding-removing pulses.

Example 1: Qcoef=0.035; T_O=25; XtalOffset=–100



Example 2: Qcoef=0.035; T_O=25; XtalOffset=+100



8 Memory Mapping

Address			Description	Range	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Page [7..3]	Addr [2..0]	Hex										
Control Page												
00000	000	0x00	OnOffCtrl	----	Clk/Int	TD1	TD0	SROn	EERefOn	TROn	TiOn	WaOn
					1	*0*	*0*	*1*	*1*	*0*	*0*	*1*
	001	0x01	IRQctrl	----				SRIntE	V2IntE	V1IntE	TIntE	AIntE
								0	*0*	*0*	*0*	*0*
	010	0x02	IRQflags	----				SRF	V2F	V1F	TF	AF
	011	0x03	Status	----	EEBusy			SR	VLOW2	VLOW1		
	100	0x04	RstCtrl	----				SYSRes				ALLRes
Watch Page												
00001	000	0x08	w_seconds	0 – 59		4	2	1	8	4	2	1
	001	0x09	w_minutes	0 – 59		4	2	1	8	4	2	1
	010	0x0A	w_hours	0 – 23		S12/24	2/pm	1	8	4	2	1
	011	0x0B	w_date	1 – 31			2	1	8	4	2	1
	100	0x0C	w_days	1 – 7						4	2	1
	101	0x0D	w_months	1 – 12				1	8	4	2	1
	110	0x0E	w_years	0 – 79		4	2	1	8	4	2	1
Alarm Page												
00010	000	0x10	a_seconds	0 – 59	SecEq	4	2	1	8	4	2	1
	001	0x11	a_minutes	0 – 59	MinEq	4	2	1	8	4	2	1
	010	0x12	a_hours	0 – 23	HourEq		2	1	8	4	2	1
	011	0x13	a_date	1 – 31	DateEq		2/pm	1	8	4	2	1
	100	0x14	a_days	1 – 7	DayEq					4	2	1
	101	0x15	a_months	1 – 12	MonthEq			1	8	4	2	1
	110	0x16	a_years	0 – 79	YearEq	4	2	1	8	4	2	1
Timer Page												
00011	000	0x18	TimLow	255–0	128	64	32	16	8	4	2	1
	001	0x19	TimHigh	255–0	128	64	32	16	8	4	2	1
Temperature Page												
00100	000	0x20	Temp	-60-195 °C	128	64	32	16	8	4	2	1
EEPROM Data Page												
00101	000	0x28	EEData	----	EEPROM user data (2 bytes)							
	001	0x29										
EEPROM Control Page												
00110	000	0x30	EEctrl	----	R80k	R20k	R5k	R1k	FD1	FD0	ThEn	ThPer
	001	0x31	XtalOffset	±127	sign	64	32	16	8	4	2	1
	010	0x32	Qcoef	----	128	64	32	16	8	4	2	1
	011	0x33	TurnOver	4-67 °C			32	16	8	4	2	1
RAM Page (User data RAM)												
00111	000-111	0x38-0x3F	RAMdata	----	8 bytes of data							

Note1: Only pages 0 to 7 are used. Unused pages are dedicated for a future use and test purposes.
Note2: The XtalOffset must be limited to ± 127 ppm.
Note3: Zero values are read from unused locations.
Note4: Watch, Alarm, Timer pages have to be initialised by an application before use.
Note5: The 8th bit of the address is ignored.

8.1 Definitions of terms in the memory mapping

Control Page - Register *OnOffCtrl*

Clk/Int	Selects if clock or interrupt is applied onto the IRQ/Clk pad ('0' – IRQ; '1' – Clk) (Clk after reset)
TD0, TD1	Selects decrement rates for Timer (32 Hz after reset)
SROn	Enables Self-Recovery function (ON after reset)
EERefOn	Enables EEPROM regular refresh each 1 hour (ON after reset);
TROn	Enables Timer Auto-reload mode ('0' – reload disabled; '1' – reload enabled)
TiOn	Enables Timer (OFF after reset)
WaOn	Enables 1 Hz clock for Watch (ON after initialisation)

Control Page - Register *IRQctrl*

SRIntE	Self-Recovery interrupt enable
V2IntE	vlow2 interrupt enable
V1IntE	vlow1 interrupt enable
TIntE	Timer interrupt enable
AIntE	Alarm interrupt enable

Control Page - Register *IRQflags*

SRF	Self-Recovery interrupt flag (bit is set to '1' when Self-Recovery reset is generated)
V2F	vlow2 interrupt flag (bit is set to '1' when power drops below vlow2)
V1F	vlow1 interrupt flag (bit is set to '1' when power drops below vlow1)
TF	Timer interrupt flag (bit is set to '1' when Timer reaches ZERO)
AF	Alarm interrupt flag (bit is set to '1' when Watch matches Alarm)

NOTE: Flags can be cleared by '0' writing.

Control Page - Register *Status*

EEBusy	EEPROM is busy (bit is set to '1' when EEPROM write or regular refresh is in progress) (ReadOnly)
SR	Self-Recovery reset detected (clear by '0' writing)
Vlow2	Voltage drop below Vlow2 (clear by '0' writing)
Vlow1	Voltage drop below Vlow1 (clear by '0' writing)

Control Page - Register *RstCtrl*

SYSRes	One shot register; writing '1' will initiate restart of the logic (watch part excluded)
ALLRes	One shot register; writing '1' will initiate restart of the logic (watch part included)

Watch Page - Registers *w_seconds, w_minutes, w_hours, w_date, w_days, w_months, w_years*

Watch information (BCD format)

Alarm Page - Registers *a_seconds, a_minutes, a_hours, a_date, a_days, a_months, a_years*

Alarm information (BCD format)

Timer Page - Registers *TimLow, TimHigh*

TimLow	Timer value (Low byte)
TimHigh	Timer value (High byte)

Temperature Page - Register *Temp*

Temp	Temperature (range from -60°C to 190°C with 0°C corresponding to a content of 60)

EEPROM Data Page - Register *EEData*

EEData	EEPROM data used for user general purposes (2 bytes)

EEPROM Control Page - Register *EECtrl*

R80k, R20k, R5k, R1k	Selects Trickle resistor between V_{CC} and V_{BACK}
FD0, FD1	Selects clocks frequency at IRQ/Clk pad.
ThEn	Thermometer Enable
ThPer	Selects the thermometer scan period, voltage detector scan period ('0' – 1 second; '1' – 16 seconds)

EEPROM Control Page - Register *XtalOffset*

XtalOffset	Crystal frequency deviation at T_O in [ppm]

EEPROM Control Page - Register *Qcoef*

Qcoef	Thermal quadratic coefficient of the crystal; example: value 151 is related to 0.035 ppm/°C²; 4096x(1.05 x 0.035 ppm/°C ^{2})

EEPROM Control Page - Register *TurnOver*

TurnOver	Turn over temperature of the crystal (values 0 to 63 are related to temperature 4 to 67 °C)

RAM Page - Register *RAMdata*

RAMdata	RAM data used for user general purposes

9 Serial communication

Any serial communication with the chip starts with a "Transaction START" and terminates with the "Transaction STOP".

"Transaction START"

I2C – START bit
SPI – CS goes to active
3-wires – CS goes to active

"Transaction STOP"

I2C – STOP bit
SPI – CS goes to inactive
3-wires – CS goes to inactive

At the same moment the **"Transaction START"** is detected a copy of Watch, Timer, Temperature content is created (copying to a cache memory). A following communication is provided through the cache memory.
Data in the cache for reading are stable until the **"Transaction STOP"**.
At the same moment the **"Transaction STOP"** is detected contents of the cache memory is copied into Watch, Timer, Temperature according to the "page address" when write was initiated.

9.1 How to perform READ/WRITE through I2C

The I2C protocol is a bidirectional protocol using 2 wires for master-slave communication. SCL (clock) and SDA (data) signals are used. This protocol allows a connection of more slaves through a bus. The bus is pulled-up (externally by resistors) and drivers are realised by open drain drivers. This chip can work as slave only.
The communication is controlled by the master. At the beginning of each transaction a start bit is sent (transaction START). A slave address follows with last bit which selects if READ or WRITE is initiated. If slave address sent by the master is equal to the slave address of the slave then slave continues to communicate with the master. Each slave address, address or data byte is finished by an acknowledge bit (ACK).It's possible to WRITE/READ the whole "page" during one transaction with automatic address increment feature. Only three less specified bits of the address are incremented.
In case of WRITE transaction the address byte is sent to the slave and data bytes can follow (MSb first order is used). A less significant part of the address is incremented after each data byte is received. The "page address" is fixed until a new address is received.
In case of READ transaction the slave sends data bytes. An address is defined by the last address change (WRITE transaction or a last increment). The "page address" can be changed only by WRITE transaction. A less significant part of the address is incremented also after each ACK received from the master. If ACK is not received then data are read from the same address.
At the end of each transaction a stop bit is send (transaction STOP).

I2C: Write transaction

	Slave Address	R/W										
S	**6543210**	**0**	**As**	**Address**	**As**	**Data Byte (1)**	**As**	**Data Byte (n-1)**	**As**	**Data Byte (n)**	**As**	**P**
	1010110	**0**	the slave address is 0ACh for write in									

I2C: Read transaction

	Slave Address	R/W						Slave Address	R/W						
S	**6543210**	**0**	**As**	**Address**	**As**	**P**	**S**	**6543210**	**1**	**As**	**Data byte (1)**	**Am**	**Data byte (n)**	**Am**	**P**
	1010110	**0**	0ACh for write					**1010110**	**1**	0ADh for read					

Note : the slave address is 0ACh for write in , and 0ADh for read out.

S ... a start bit sent by a master
As ... an acknowledge from the slave
Am ... an acknowledge from the master
R/W ... read/write select
P ... a stop bit

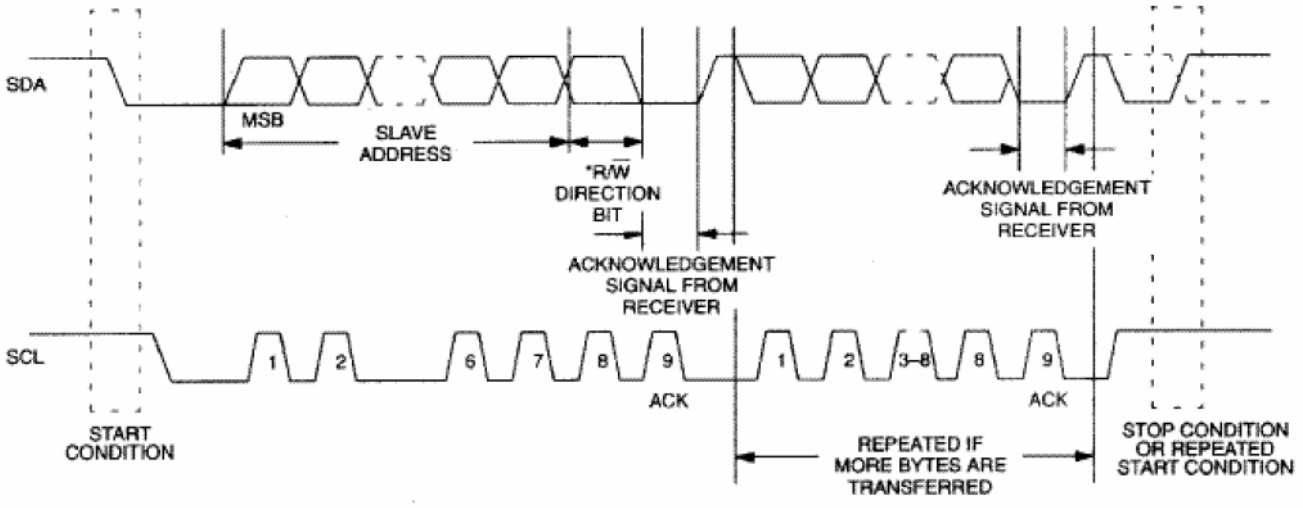


Figure 7 – I2C communication

9.2 How to perform READ/WRITE through SPI

The SPI protocol is used to connect master and slaves.
4 wires are used: CS (Chip Select), SCK (serial clock), SI (input data) and SO (output data). This chip can work as slave only.
SPI is byte oriented protocol (MSb first order is used). Data are changing on SCK falling edge and sampled on the rising edge.
It's possible to WRITE/READ the whole "page" during one transaction with automatic address increment feature. Only three less specified bits of the address are incremented.
At the beginning of the transaction Chip Select goes to active. First bit of data selects if READ or WRITE operation will follow after an address. The address is composed of 7 bits.

If WRITE transaction is initiated then master continues with data sending byte by byte. A less significant part of the address is automatically incremented after each data byte is received. The "page address" is fixed until a new transaction is started. SO data output stays at '0' during the whole transaction.
If READ transaction is initiated then data are send after the address by the slave. A less significant part of the address is automatically incremented after each data byte sent. The "page address" is not changing until a new transaction is started. SI data input is not cared.
SO is in tristate when CS inactive.

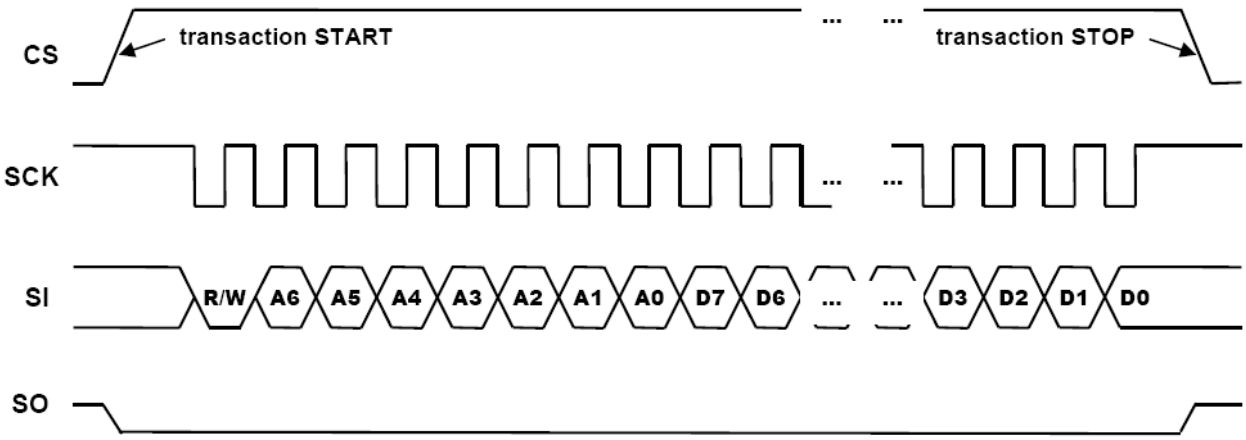


Figure 8 – SPI write transaction

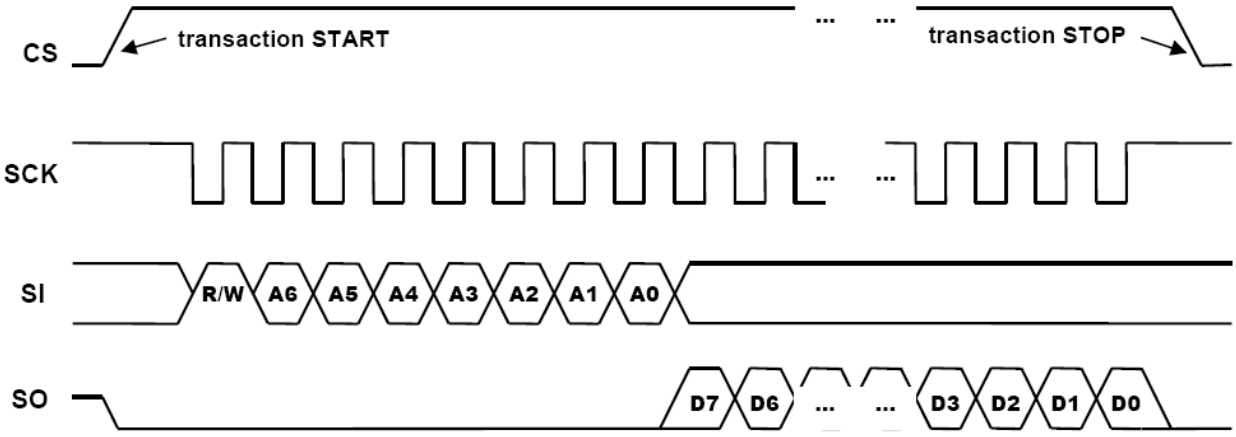


Figure 9 – SPI read transaction

9.3 How to perform READ/WRITE through 3-wires

The 3-wires protocol is used to connect master and slaves.
3 wires are used: CS (Chip Select), SCK (serial clock) and SIO (input/output data). This chip can work as slave only. SPI is byte oriented protocol (LSb first order is used). Data are changing on SCK falling edge and sampled on the rising edge.
It's possible to WRITE/READ the whole "page" during one transaction with automatic address increment feature. Only three less specified bits of the address are incremented.
At the beginning of the transaction Chip Select goes to active. First 7-bits is the address in LSb first order. The next bit of data selects if READ or WRITE operation.

If WRITE transaction is initiated then master continues with data sending byte by byte. A less significant part of the address is incremented after each data byte is received. The "page address" is fixed until a new transaction is started.
If READ transaction is initiated then data are send after the address by the slave. A less significant part of the address is incremented after each data byte sent. The "page address" is fixed until a new transaction is started.
SIO is in tristate when CS inactive.

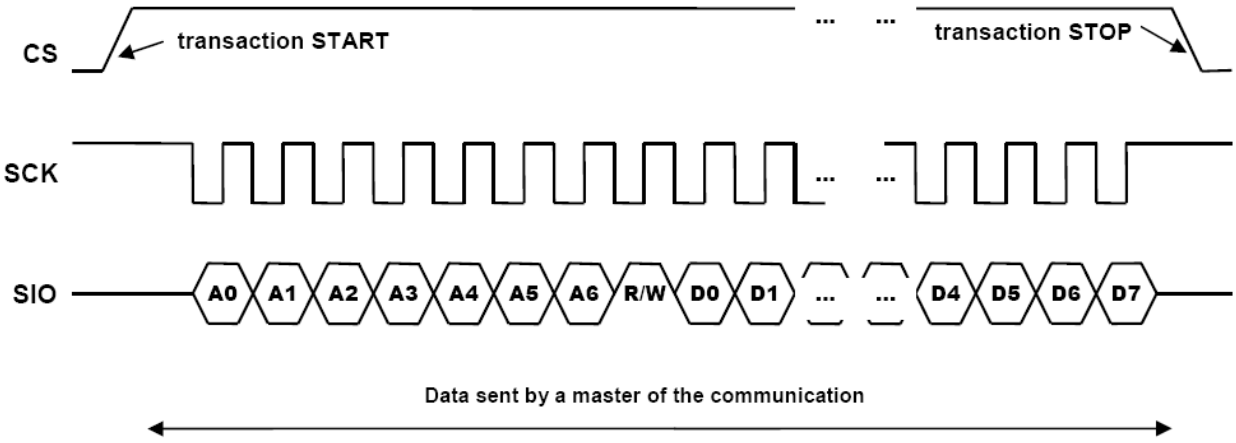


Figure 10 – 3-wires write transaction

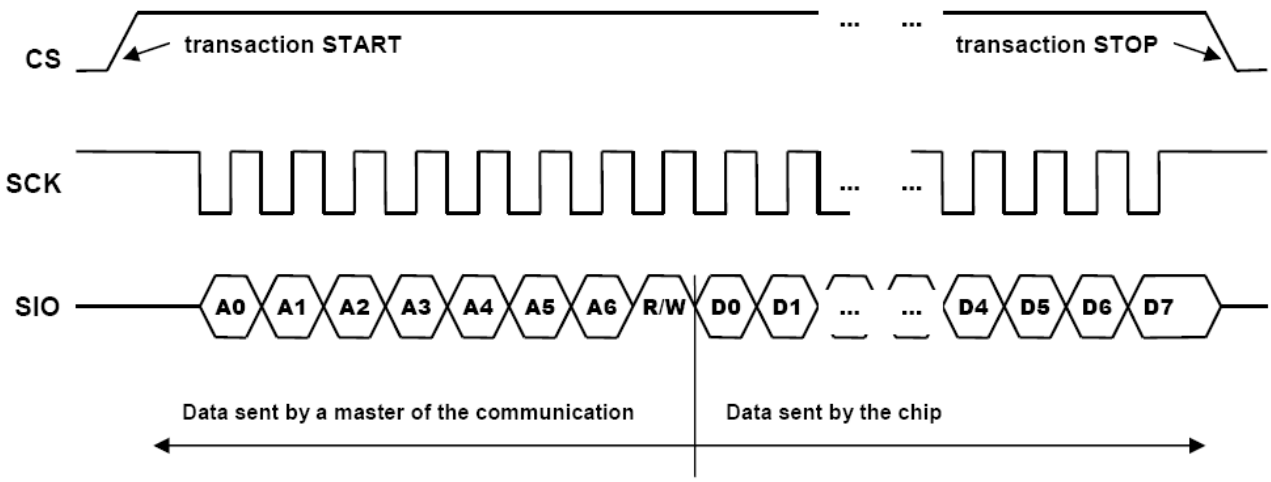


Figure 11 – 3-wires read transaction

10 Detailed Functional Description

10.1 Start after power-up

The chip is in a reset state when voltage is below minimum voltage level. When the reset is released then the chip is starting its functionality with steps described below.

1. crystal oscillator start – It's necessary to have available clock for Watch part and main control part
2. detection of VLOW2 – The voltage has to be above VLOW2 to guarantee minimum EEPROM read voltage
3. read initialisation – The configuration is read from EEPROM
4. go to Normal Mode

10.2 Normal Mode functionality

The chip provides following functionality during the Normal Mode:

1. **Voltage detection –** The voltage detection is provided each 1 or 16 seconds (ThPer bit)
2. **Temperature compensation –** It's executed if voltage is above VLOW1 and thermometer is enabled (ThEn bit)
3. **EEPROM regular refresh –** It's provided each hour to guarantee correct content of configuration registers (voltage must be above VLOW2)
4. **Watch/Alarm** – normal mode (enabled)
5. **Timer** – disabled
6. **Self-Recovery system** – enabled
7. **Serial interface** – enabled

10.3 Watch and Alarm functionality

A Watch part provides information in BCD format. The value is incremented each one second. It's composed of seconds, minutes, hours, date, weekdays, months, years.
The Watch part setup is provided by Write transaction into the Watch Page. At the end of transaction ("Transaction STOP") the Watch is restarted. A first clock will increment Watch counting part just after 1s.

There is possibility to use Alarm functionality by setting and enabling alarm registers. Each cipher has its own enable bit. Allowed possibilities of enables are described in the table below.

SecEq	MinEq	HourEq	DayEq	DateEq	YearEq
1	0	0	0	0	0
1	1	0	0	0	0
1	1	1	0	0	0
1	1	1	1	0	0
1	1	1	0	1	0
1	1	1	1	0	1

Table 12 – Alarm Period selection

NOTE: Both Watch and Alarm parts must be setup by an application before use.

10.4 Timer functionality

The 16-bit count down timer can be enabled/disabled by TiOn bit.
It's possible to select timer frequency by TD1, TD0 bits according to the following table:

TD1	TD0	Timer frequency
0	0	32 Hz
1	0	8 Hz
0	1	1 Hz
1	1	0.5 Hz

Table 13 – Timer Frequency selection

The timer can run in Zero-Stop or Auto-Reload mode (TROn bit; '0' – Zero-Stop mode, '1' – Auto-Reload mode).

When TROn = '0' then it's possible to read current value of the timer. If TROn = '1' then last written value is read from cache memory. The value in the cache memory is used as a new value during reloading (Auto-Reload).
Timer values (TimLow, TimHigh), frequency selection (TD1, TD0) and mode selection (TROn) can be provided only when the timer is stopped (TiOn = '0')

NOTE: The "Timer Page" can be used also as well as a common purposed registers when the timer function is not used.

10.5 Temperature compensation

The temperature compensation is provided continuously when thermometer is enabled (ThEn = '1') or just once after Temp register is written and thermometer is disabled (ThEn = '0'). After power-up the correction value is zero. A temperature correction value is computed according to the equation described in **chapter 7**.
Thermometer period is selectable by ThPer bit according to the table below:

ThPer	Period in Seconds
0	1 s
1	16 s

Table 14 – Thermometer Period

The thermometer is automatically disabled when VLOW1 status bit is at '1'. The correction value is frozen.

Temp register uses also a cache memory to keep stable value during a whole transaction (read/write).

10.6 EEPROM memory

Before any EEPROM access (read/write), the bit EERefOn has to be reset by the application. Then the application has to read EEBusy bit and if EEBusy = '0' then EEPROM access can be provided (started).
After write command ("Transaction STOP") a progress of EEPROM writing is detected by EEBusy register bit at '1'. EEBusy goes to '0' when EEPROM writing is finished.

NOTE: (V_{CC} >V_{prog}) VCC must be connected during whole EEPROM write (serial interface connected).

10.6.1 EEPROM Control Page

This part is composed of 4 bytes purposed for functionality control and for crystal compensation constants.
EEctrl byte contains: trickle change selectors (R80k, R20k, R5k, R1k); output clock frequency selector (FD1, FD0); thermometer enable and thermometer period selector.

FD1	FD0	Select Clocks Out
0	0	32768 Hz (without correction)
0	1	1024 Hz
1	0	32 Hz
1	1	1 Hz

Table 15 – Output Clock frequency selector

10.6.2 EEPROM user memory

This part of the memory is dedicated for the application. 2 bytes are available.

10.7 RAM user memory

RAM memory size is 8 bytes. The state of RAM part after power-up is undefined.

10.8 Status register

The purpose of EEBusy bit is to inform users about current status of the EEPROM operations.

EEBusy – status of EEPROM controller (if EEBusy = '1' then EEPROM regular refresh or EEPROM write in progress)

The purpose of the following status bits is to record history of Voltage and Self-Recovery system behavioural.

VLOW1 – status of Vlow1 voltage detection (if bit is once set then it can be cleared only by '0' writing)
VLOW2 – status of Vlow2 voltage detection (if bit is once set then it can be cleared only by '0' writing)
SR – status of the Self-Recovery system (if bit is once set then it can be cleared only by '0' writing)

10.9 Interrupts

There are several interrupt sources which can generate interrupt on (INT/ and/or ClkOut) pads (active at '0' – open drain). The interrupt is generated when at least one of IRQflags goes to '1' (OR function).

AF – interrupt is provided when Watch reaches Alarm settings
TF – interrupt is provided when Timer reaches ZERO
V1F – interrupt is provided when Voltage detects Voltage below Vlow1 (VLOW1 status "rising edge")
V2F – interrupt is provided when Voltage detects Voltage below Vlow2 (VLOW2 status "rising edge")
SRF – interrupt is provided when Self-Recovery system invoked internal reset (SR status "rising edge")

Each interrupt source has its own interrupt enable (AintE, TintE, V1IntE, V2IntE, SRIntE). When the enable is '0' then the appropriate interrupt source is blocked.
Interrupt bits are cleared by '0' writing into the appropriate bit. It's necessary to clear also status bits after interrupt bits.

10.10 Self-Recovery system function

A purpose of the Self-Recovery system is to generate internal chip reset in case of some EMC problem on the chip. It prevents internal state machine possible deadlock. The Self-Recovery system is automatically enabled after power-up (SROn bit). It can be disabled by an application by writing '0' into the SROn.

10.11 Register Map

Registers in the register map are divided into pages. The page is addressed by the most significant bits of the address. The low significant bits of the address provide addressing inside the page. During address incrementing only low significant bits are changing. The page address part is fixed during whole data transaction.

10.12 Oscillation and Clock Divider

The 32768 Hz Xtal oscillator and the clock divider provide the time base for the all blocks on the chip.
If the temperature increases or decreases apart of the turnover point, the frequency deviation will be corrected and deviation applied. The temperature deviation is computed with temperature coefficients stored in the EEPROM.
The frequency is adjusted by an automatic acquisition (ThEn='1') or after writing into the Temp register (ThEn = '0').
The integrated thermometer has a resolution of 1℃. Thper is used to define the periodicity of the temperature and voltage measurement.

11 Power management

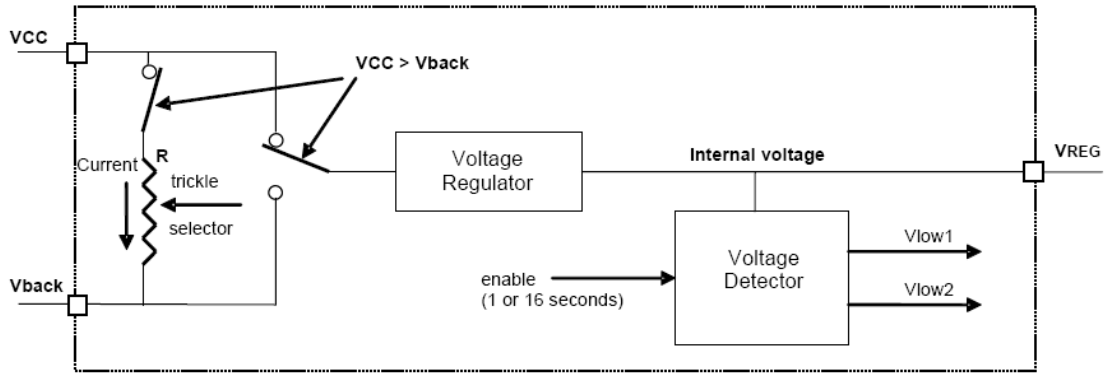


Figure 12 – Power management

11.1 Supply, switchover and Trickle Charge

The device can be supplied through the VCC pad or through the Vback pad.
If the V_{CC} voltage is ON at a potential higher than the V_{back} voltage, resistors can be inserted between VCC and Vback by setting the trickle charger bits. It can be applied also when Vback is provided by a cap or supercap.

11.2 Low Supply Detection

The supply levels Vlow1 and Vlow2 are tested periodically and have built in hysteresis. The period of the detection is defined by ThPer bit (the same as the Thermometer Period) (1 or 16 seconds).

When the voltage drops below Vlow1 then the VLOW1 status bit is set to '1'. It is only possible to clear VLOW1 by increasing the supply voltage above Vlow1 and then writing '0' into the VLOW1 status bit.

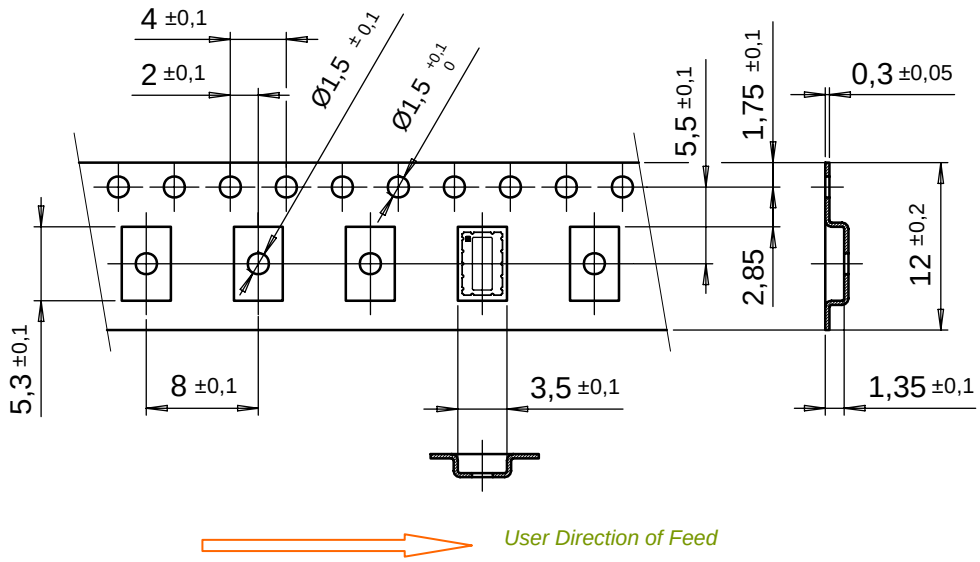
When the VLOW1 bit is at '1' the thermometer is disabled and the automatic thermal compensation inhibited (last computed correction value is used).
The device continues to work until the supply voltage drops below the limit Vlow2 which is the minimum supply voltage of the device.

Then the VLOW2 bit is set and can only be reset by increasing the supply above the level Vlow2 and then writing '0' into the VLOW2 status bit.

Below the Vlow2 level the device functionality is not guaranteed.

11.0 PACKING INFO CARRIER TAPE

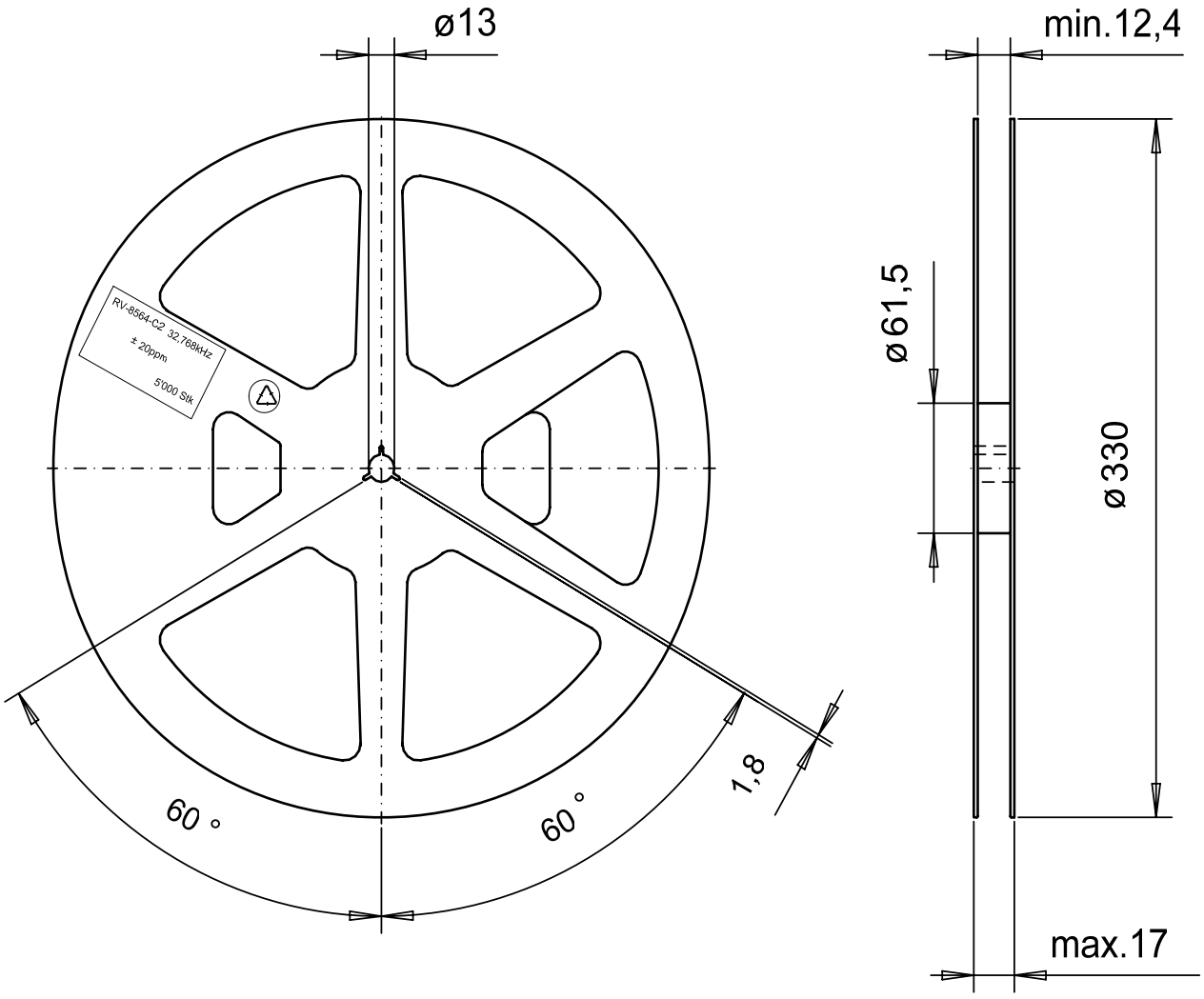
12 mm Carrier-Tape:	Material:	Polystyrene / Butadine or Polystyrol black, conductive
Cover Tape:	Base Material:	Polyester, conductive 0.061 mm
	Adhesive Material:	Pressure-sensitive Synthetic Polymer



Tape Leader and Trailer: 300 mm minimum *All dimensions are in mm*

REELS:	DIAMETER	MATERIAL.	RTC's per REEL.
	7"	Plastic, Polystyrene	1000
	10"	Plastic, Polystyrene	2500
	13"	Plastic, Polystyrol	5000

11.1 REEL 13 INCH FOR 12 mm TAPE



Reel:

Diameter	***Material***
13”	*Plastic, Polystyrol*

12.0 DOCUMENT REVISION HISTORY

Date	Revision #	Revision Details
June 2008	1.0	First release “Preliminary Version”