

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC74VHC367F, TC74VHC367FN, TC74VHC367FT
TC74VHC368F, TC74VHC368FN, TC74VHC368FT

HEX BUS BUFFER

TC74VHC367 F / FN / FT
TC74VHC368 F / FN / FTNON - INVERTED, 3 - STATE OUTPUTS
INVERTED, 3 - STATE OUTPUTS

(Note) The JEDEC SOP (FN) is not available in Japan.

The TC74VHC367 and 368 are advanced high speed CMOS HEX BUS BUFFERs fabricated with silicon gate C²MOS technology.

They achieve the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

They contain six buffers; four buffers are controlled by an enable input ($\overline{G1}$), and the other two buffers are controlled by another enable input ($\overline{G2}$). The outputs of each buffer group are enabled when $\overline{G1}$ and/or $\overline{G2}$ inputs are held low; if held high, these outputs are in a high impedance state.

The TC74VHC367 is a non-inverting output type, while the TC74VHC368 is an inverting output type.

An input protection circuit ensures that 0 to 7V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

FEATURES:

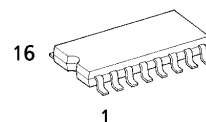
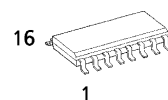
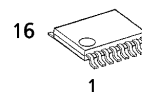
- High Speed..... $t_{pd} = 3.8\text{ns}(\text{typ.})$ at $V_{CC} = 5\text{V}$
- Low Power Dissipation..... $I_{CC} = 4\mu\text{A}(\text{Max.})$ at $T_a = 25^\circ\text{C}$
- High Noise Immunity..... $V_{NIH} = V_{NIL} = 28\% V_{CC}(\text{Min.})$
- Power Down Protection is provided on all inputs.
- Balanced Propagation Delays..... $t_{PLH} \approx t_{PHL}$
- Wide Operating Voltage Range..... $V_{CC}(\text{opr}) = 2\text{V} \sim 5.5\text{V}$
- Low Noise..... $V_{OLP} = 0.8\text{V}(\text{Max.})$
- Pin and Function Compatible with 74ALS367/368

TRUTH TABLE

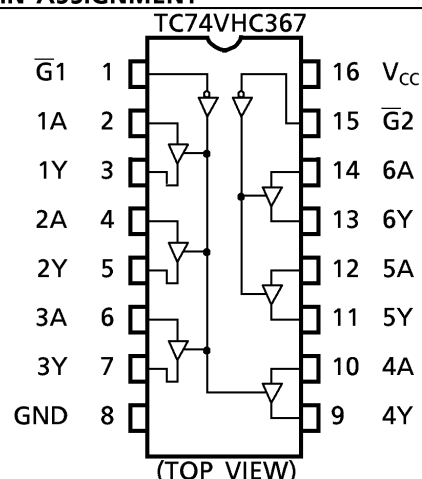
INPUTS		OUTPUTS	
$\overline{G}$	A	Y(367)	$\overline{Y}$ (368)
L	L	L	H
L	H	H	L
H	X	Z	Z

X : Don't Care

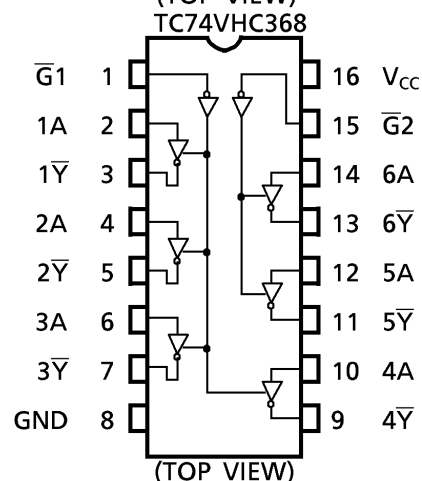
Z : High Impedance

F (SOP16-P-300-1.27)
Weight : 0.18g (Typ.)FN (SOL16-P-150-1.27)
Weight : 0.13g (Typ.)FT (TSSOP16-P-0044-0.65)
Weight : 0.06g (Typ.)

PIN ASSIGNMENT



(TOP VIEW)

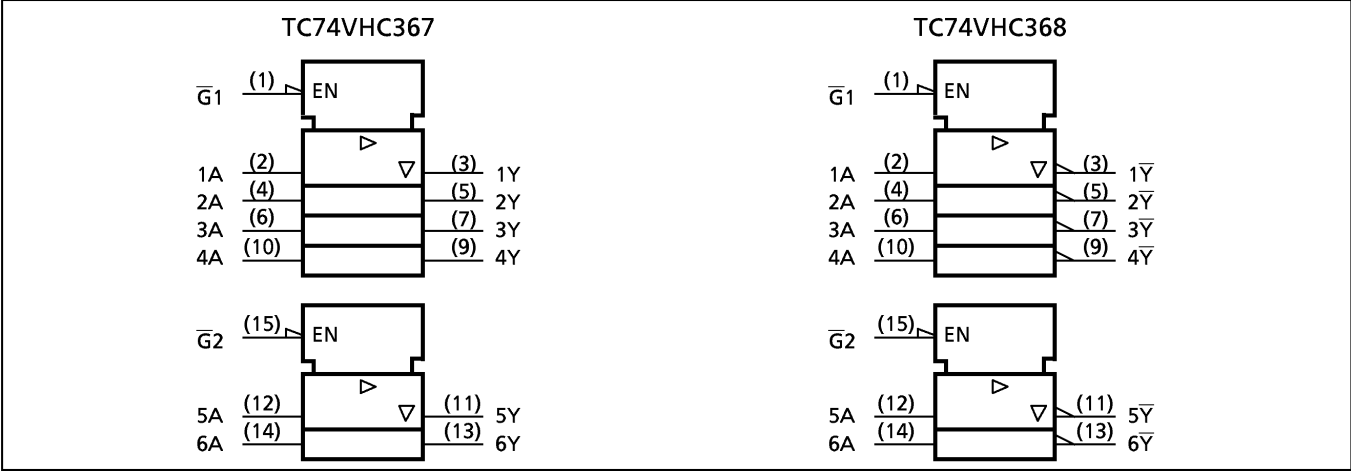


(TOP VIEW)

961001EBA2

● TOSHIBA is continually working to improve the quality and the reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing TOSHIBA products, to observe standards of safety, and to avoid situations in which a malfunction or failure of a TOSHIBA product could cause loss of human life, bodily injury or damage to property. In developing your designs, please ensure that TOSHIBA products are used within specified operating ranges as set forth in the most recent products specifications. Also, please keep in mind the precautions and conditions set forth in the TOSHIBA Semiconductor Reliability Handbook.

IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7.0$	V
DC Input Voltage	V_{IN}	$-0.5 \sim 7.0$	V
DC Output Voltage	V_{OUT}	$-0.5 \sim V_{CC} + 0.5$	V
Input Diode Current	I_{IK}	-20	mA
Output Diode Current	I_{OK}	± 20	mA
DC Output Current	I_{OUT}	± 25	mA
DC V_{CC} /Ground Current	I_{CC}	± 50	mA
Power Dissipation	P_D	180	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2.0~5.5	V
Input Voltage	V_{IN}	0~5.5	V
Output Voltage	V_{OUT}	0~ V_{CC}	V
Operating Temperature	T_{opr}	$-40 \sim 85$	°C
Input Rise and Fall Time	dt / dv	0~100 ($V_{CC} = 3.3 \pm 0.3V$) 0~20 ($V_{CC} = 5 \pm 0.5V$)	ns / V

961001EBA2'

● The products described in this document are subject to foreign exchange and foreign trade control laws.
● The information contained herein is presented only as a guide for the applications of our products. No responsibility is assumed by TOSHIBA CORPORATION for any infringements of intellectual property or other rights of the third parties which may result from its use. No license is granted by implication or otherwise under any intellectual property or other rights of TOSHIBA CORPORATION or others.
● The information contained herein is subject to change without notice.

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V _{CC} (V)	Ta = 25°C			Ta = -40~85°C		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	
High - Level Input Voltage	V _{IH}			2.0 3.0~ 5.5	1.50 V _{CC} × 0.7	— —	— —	1.50 V _{CC} × 0.7	— —	V
Low - Level Input Voltage	V _{IL}			2.0 3.0~ 5.5	— —	— —	0.50 V _{CC} × 0.3	— —	0.50 V _{CC} × 0.3	V
High - Level Output Voltage	V _{OH}	V _{IN} = V _{IH} or V _{IL}	I _{OH} = -50μA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5	— — —	1.9 2.9 4.4	— — —	V
			I _{OH} = -4mA	3.0	2.58	—	—	2.48	—	
			I _{OH} = -8mA	4.5	3.94	—	—	3.80	—	
Low - Level Output Voltage	V _{OL}	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 50μA	2.0 3.0 4.5	— — —	0.0 0.0 0.0	0.1 0.1 0.1	— — —	0.1 0.1 0.1	V
			I _{OL} = 4mA	3.0	—	—	0.36	—	0.44	
			I _{OL} = 8mA	4.5	—	—	0.36	—	0.44	
3 - State Output Off - State Current	I _{OZ}	V _{IN} = V _{IH} or V _{IL} V _{OUT} = V _{CC} or GND		5.5	—	—	±0.25	—	±2.50	μA
Input Leakage Current	I _{IN}	V _{IN} = 5.5V or GND		0~5.5	—	—	±0.1	—	±1.0	
Quiescent Supply Current	I _{CC}	V _{IN} = V _{CC} or GND		5.5	—	—	4.0	—	40.0	

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3\text{ns}$)

PARAMETER	SYMBOL	TEST CONDITION		Ta = 25°C			Ta = − 40~85°C		UNIT	
			V _{CC} (V)	CL (pF)	MIN.	TYP.	MAX.	MIN.		MAX.
Propagation Delay Time (TC74VHC367)	t _{pLH} t _{pHL}		3.3 ± 0.3	15	—	5.9	8.3	1.0	10.0	ns
				50	—	8.4	11.8	1.0	13.5	
			5.0 ± 0.5	15	—	4.1	5.9	1.0	7.0	
				50	—	5.6	7.9	1.0	9.0	
Propagation Delay Time (TC74VHC368)	t _{pLH} t _{pHL}		3.3 ± 0.3	15	—	5.3	7.5	1.0	9.0	
				50	—	7.8	11.0	1.0	12.5	
			5.0 ± 0.5	15	—	3.8	5.5	1.0	6.5	
				50	—	5.3	7.5	1.0	8.5	
3-State Output Enable Time	t _{pZL} t _{pZH}	RL = 1kΩ	3.3 ± 0.3	15	—	6.8	10.5	1.0	12.5	
				50	—	9.3	14.0	1.0	16.0	
			5.0 ± 0.5	15	—	4.8	7.2	1.0	8.5	
				50	—	6.3	9.2	1.0	10.5	
3-State Output Disable Time	t _{pLZ} t _{pHZ}	RL = 1kΩ	3.3 ± 0.3	50	—	9.9	13.6	1.0	15.5	
			5.0 ± 0.5	50	—	6.3	9.2	1.0	10.5	
Output to Output Skew	t _{osLH} t _{osHL}	(Note 1)	3.3 ± 0.3	50	—	—	1.5	—	1.5	
			5.0 ± 0.5	50	—	—	1.0	—	1.0	
Input Capacitance	C _{I N}				—	4	10	—	10	pF
Output Capacitance	C _{OUT}				—	6	—	—	—	
Power Dissipation Capacitance	C _{PD}	(Note 2)			—	19	—	—	—	

Note (1) Parameter guaranteed by design. $t_{\text{osLH}} = t_{\text{pLHm}} - t_{\text{pLHn}}$, $t_{\text{osHL}} = t_{\text{pHLm}} - t_{\text{pHLn}}$

Note (2) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

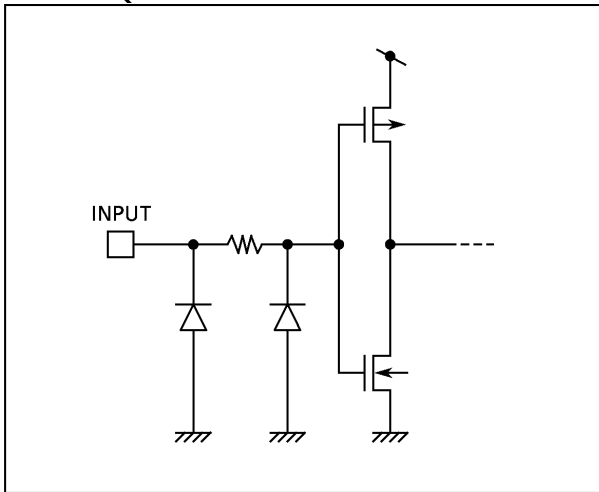
Average operating current can be obtained by the equation :

$$I_{\text{CC(opr.)}} = C_{\text{PD}} \cdot V_{\text{CC}} \cdot f_{\text{IN}} + I_{\text{CC}} / 6 \text{ (per bit)}$$

NOISE CHARACTERISTICS (Input $t_r = t_f = 3\text{ns}$)

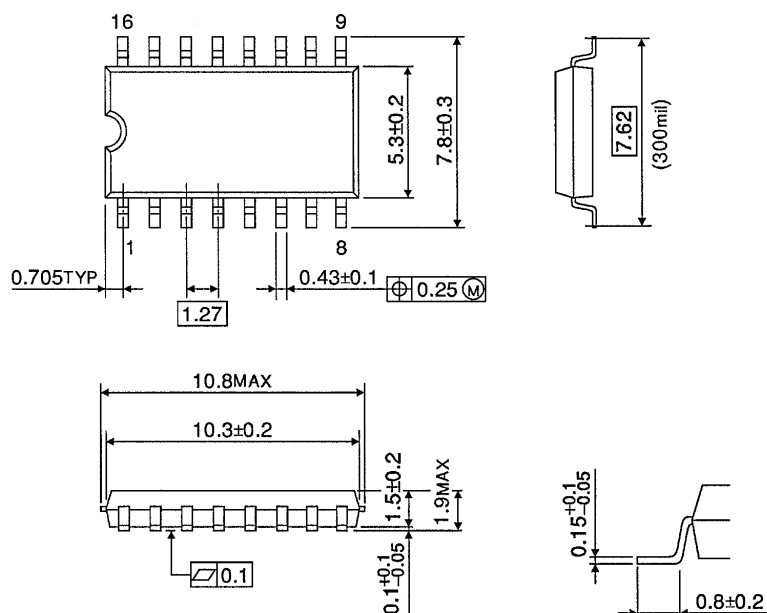
PARAMETER	SYMBOL	TEST CONDITION		Ta = 25°C		UNIT
				V _{CC} (V)	TYP. MAX.	
Quiet Output Maximum Dynamic V _{OL}	V _{OLP}	C _L = 50pF	5.0	0.4	0.8	V
Quiet Output Minimum Dynamic V _{OL}	V _{OLV}	C _L = 50pF	5.0	-0.4	-0.8	V
Minimum High Level Dynamic Input Voltage	V _{IHD}	C _L = 50pF	5.0	—	3.5	V
Maximum Low Level Dynamic Input Voltage	V _{ILD}	C _L = 50pF	5.0	—	1.5	V

INPUT EQUIVALENT CIRCUIT



SOP 16PIN (200mil BODY) OUTLINE DRAWING (SOP16-P-300-1.27)

Unit in mm

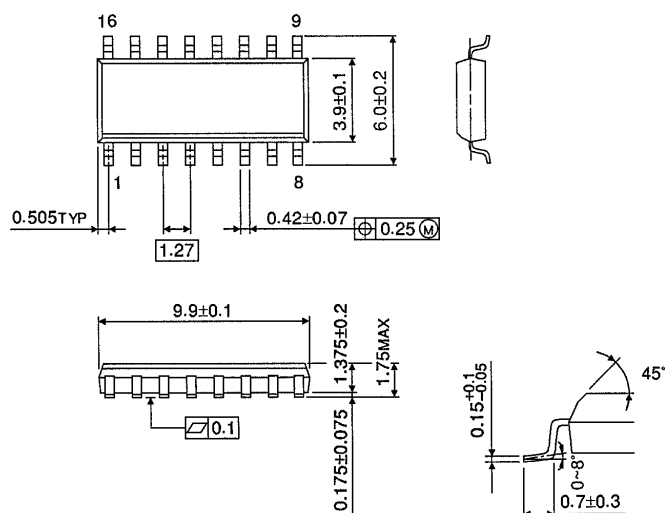


Weight : 0.18g (Typ.)

SOP 16PIN (150mil BODY) OUTLINE DRAWING (SOP16-P-150-1.27)

Unit in mm

(Note) This package is not available in Japan.



Weight : 0.13g (Typ.)

TSSOP 16PIN OUTLINE DRAWING (TSSOP16-P-0044-0.65)

Unit in mm

