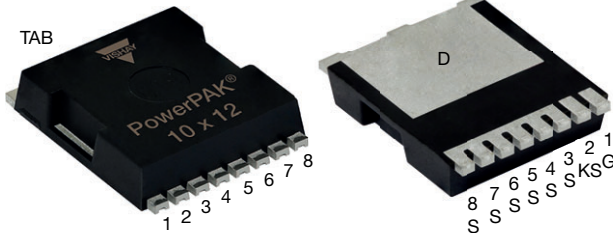


## N-Channel 60 V (D-S) MOSFET

PowerPAK® 10 x 12



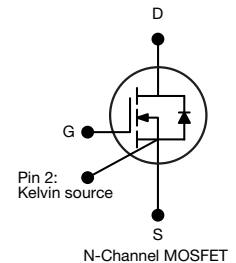
### FEATURES

- TrenchFET® Gen IV power MOSFET
- Leadership  $R_{DS(on)}$  minimizes power loss from conduction
- 100 %  $R_g$  and UIS tested
- Kelvin connection for reduced gate noise
- Enhance power dissipation and lower  $R_{thJC}$
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)


**RoHS**  
 COMPLIANT  
 HALOGEN  
**FREE**

### APPLICATIONS

- Synchronous rectification
- Automation
- OR-ing and hot swap switch
- Power supplies
- Motor drive control
- Battery management



PRODUCT SUMMARY	
$V_{DS}$ (V)	60
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS} = 10$ V	0.0012
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS} = 7.5$ V	0.0014
$Q_g$ typ. (nC)	162
$I_D$ (A) <sup>a</sup>	461
Configuration	Single

ORDERING INFORMATION	
Package	PowerPAK® 10 x 12
Lead (Pb)-free and halogen-free	SiJK4610-T1-GE3

ABSOLUTE MAXIMUM RATINGS ( $T_A = 25$ °C, unless otherwise noted)				
PARAMETER	SYMBOL	LIMIT	UNIT	
Drain-source voltage	$V_{DS}$	60	V	
Gate-source voltage	$V_{GS}$	$\pm 20$		
Continuous drain current ( $T_J = 175$ °C)	$I_D$	$T_C = 25$ °C	461	A
		$T_C = 100$ °C	291	
		$T_A = 25$ °C	77 <sup>b, c</sup>	
		$T_A = 100$ °C	49 <sup>b, c</sup>	
Pulsed drain current ( $V_{GS} = 10$ V, $t = 100$ $\mu$ s)	$I_{DM}$	700		
Continuous source-drain diode current	$I_S$	$T_C = 25$ °C	406	
		$T_A = 25$ °C	11.4 <sup>b, c</sup>	
Single pulse avalanche current	$I_{AS}$	90		
Single pulse avalanche energy	$E_{AS}$	405	mJ	
Maximum power dissipation	$P_D$	$T_C = 25$ °C	446	W
		$T_C = 100$ °C	179	
		$T_A = 25$ °C	12.5 <sup>b, c</sup>	
		$T_A = 100$ °C	5 <sup>b, c</sup>	
Operating junction and storage temperature range	$T_J, T_{stg}$	-55 to +150	°C	
Soldering recommendations (peak temperature) <sup>c</sup>		260		

THERMAL RESISTANCE RATINGS					
PARAMETER	SYMBOL	TYPICAL	MAXIMUM	UNIT	
Maximum junction-to-ambient <sup>b</sup>	$R_{thJA}$	7.8	10	°C/W	
Maximum junction-to-case (drain)	$R_{thJC}$	0.21	0.28		

#### Notes

- $T_C = 25$  °C
- Surface mounted on 1" x 1" FR4 board
- $t = 10$  s
- See solder profile ([www.vishay.com/doc?73257](http://www.vishay.com/doc?73257)). The PowerPAK 10 x 12 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components
- Maximum under steady state conditions is 42 °C/W



SPECIFICATIONS (T <sub>J</sub> = 25 °C, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Static</b>						
Drain-source breakdown voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	60	-	-	V
V <sub>DS</sub> temperature coefficient	ΔV <sub>DS</sub> /T <sub>J</sub>	I <sub>D</sub> = 10 mA	-	32	-	mV/°C
V <sub>GS(th)</sub> temperature coefficient	ΔV <sub>GS(th)</sub> /T <sub>J</sub>	I <sub>D</sub> = 250 μA	-	-8.4	-	
Gate-source threshold voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	2	-	3.5	V
Gate-source leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ± 20 V	-	-	± 100	nA
Zero gate voltage drain current	I <sub>DSS</sub>	V <sub>DS</sub> = 60 V, V <sub>GS</sub> = 0 V	-	-	1	μA
		V <sub>DS</sub> = 60 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 55 °C	-	-	10	
Drain-source on-state resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 20 A	-	0.00088	0.0012	Ω
		V <sub>GS</sub> = 7.5 V, I <sub>D</sub> = 20 A	-	0.00094	0.0014	
Forward transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 25 V, I <sub>D</sub> = 30 A	-	105	-	S
<b>Dynamic <sup>b</sup></b>						
Input capacitance	C <sub>iss</sub>	V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 0 V, f = 1 MHz	-	15 550	-	pF
Output capacitance	C <sub>oss</sub>		-	3540	-	
Reverse transfer capacitance	C <sub>rss</sub>		-	101	-	
Total gate charge	Q <sub>g</sub>	V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 10 V, I <sub>D</sub> = 20 A	-	214	321	nC
Gate-source charge	Q <sub>gs</sub>		-	66	-	
Gate-drain charge	Q <sub>gd</sub>		-	28	-	
Total gate charge	Q <sub>g</sub>	V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 7.5 V, I <sub>D</sub> = 20 A	-	162	243	nC
Output charge	Q <sub>oss</sub>	V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 0 V	-	220	-	
Gate resistance	R <sub>g</sub>	f = 1 MHz	0.2	1.0	2.0	Ω
Turn-on delay time	t <sub>d(on)</sub>	V <sub>DD</sub> = 30 V, R <sub>L</sub> = 3 Ω, I <sub>D</sub> ≅ 10 A, V <sub>GEN</sub> = 10 V, R <sub>g</sub> = 1 Ω	-	30	60	ns
Rise time	t <sub>r</sub>		-	20	40	
Turn-off delay time	t <sub>d(off)</sub>		-	77	160	
Fall time	t <sub>f</sub>		-	27	60	
Turn-on delay time	t <sub>d(on)</sub>	V <sub>DD</sub> = 30 V, R <sub>L</sub> = 3 Ω, I <sub>D</sub> ≅ 10 A, V <sub>GEN</sub> = 7.5 V, R <sub>g</sub> = 1 Ω	-	37	75	ns
Rise time	t <sub>r</sub>		-	24	50	
Turn-off delay time	t <sub>d(off)</sub>		-	69	140	
Fall time	t <sub>f</sub>		-	30	60	
<b>Drain-Source Body Diode Characteristics</b>						
Continuous source-drain diode current	I <sub>S</sub>	T <sub>C</sub> = 25 °C	-	-	406	A
Pulse diode forward current	I <sub>SM</sub>		-	-	700	
Body diode voltage	V <sub>SD</sub>	I <sub>S</sub> = 10 A, V <sub>GS</sub> = 0 V	-	0.7	1.1	V
Body diode reverse recovery time	t <sub>rr</sub>	I <sub>F</sub> = 10 A, di/dt = 100 A/μs, T <sub>J</sub> = 25 °C	-	110	220	ns
Body diode reverse recovery charge	Q <sub>rr</sub>		-	260	520	nC
Reverse recovery fall time	t <sub>a</sub>		-	56	-	ns
Reverse recovery rise time	t <sub>b</sub>		-	54	-	

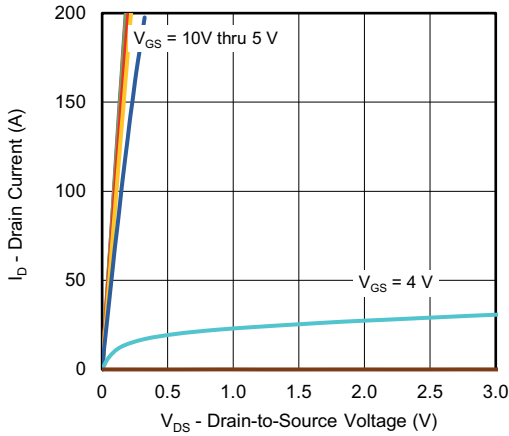
**Notes**

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %
- b. Guaranteed by design, not subject to production testing

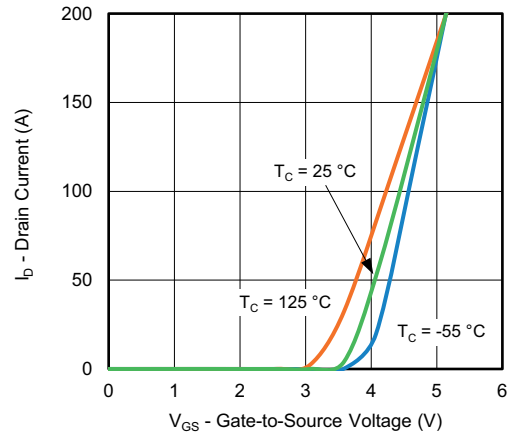
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



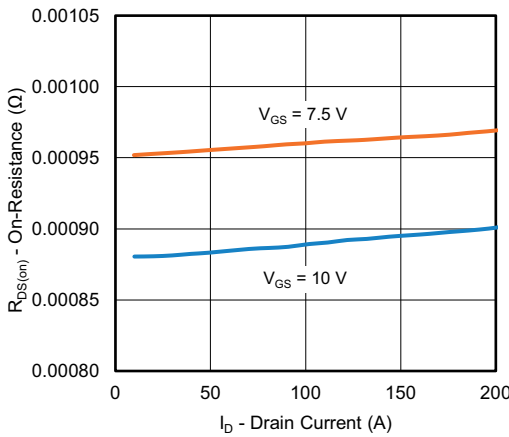
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



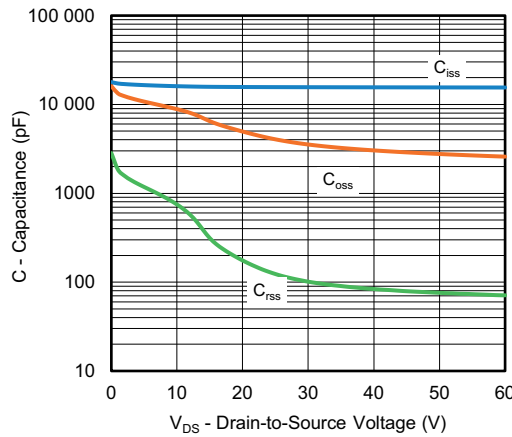
Output Characteristics



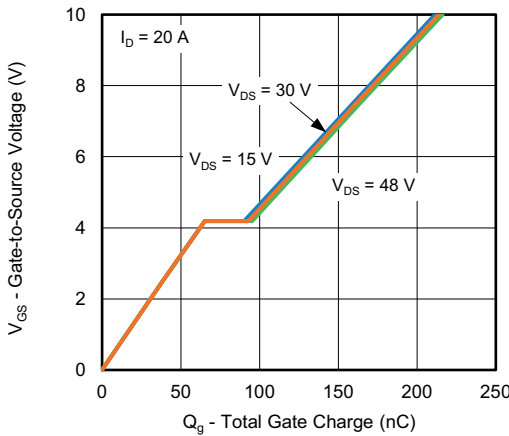
Transfer Characteristics



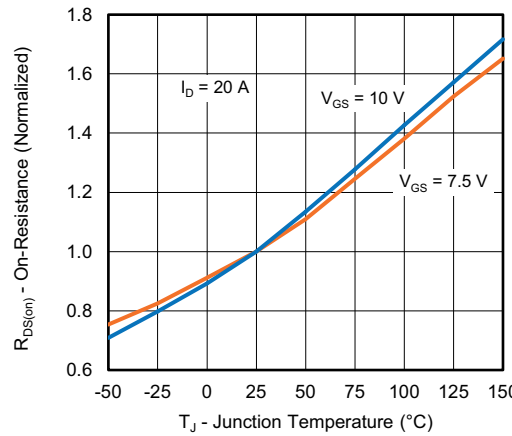
On-Resistance vs. Drain Current and Gate Voltage



Capacitance



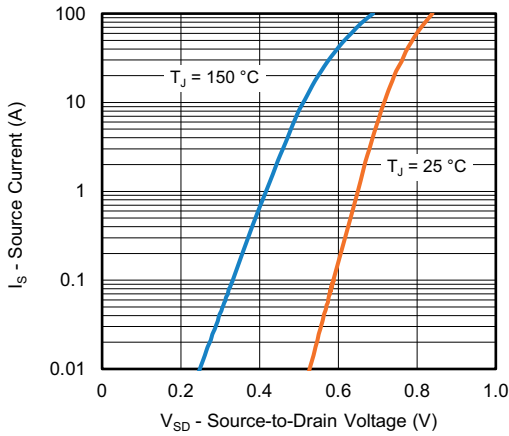
Gate Charge



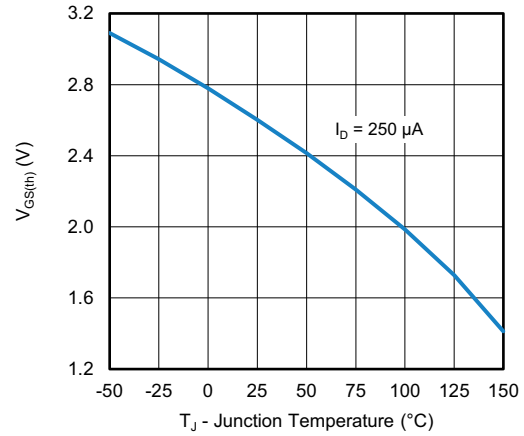
On-Resistance vs. Junction Temperature



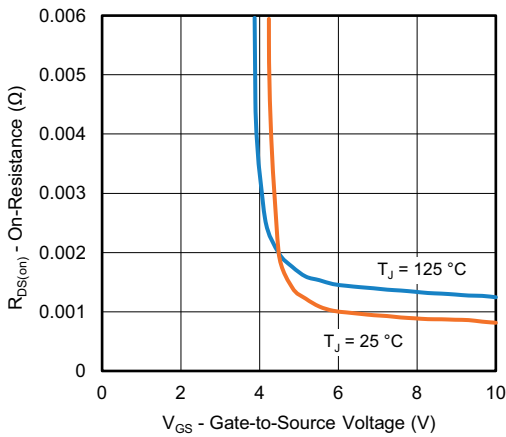
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



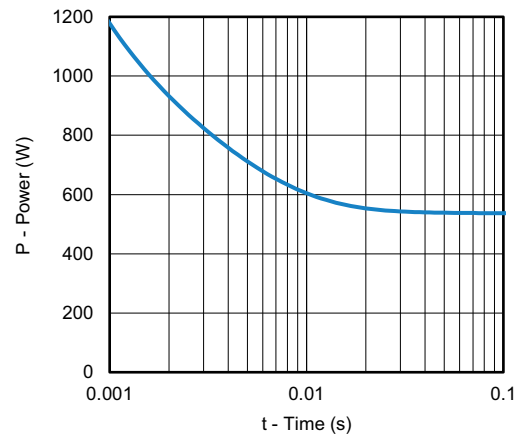
Source-Drain Diode Forward Voltage



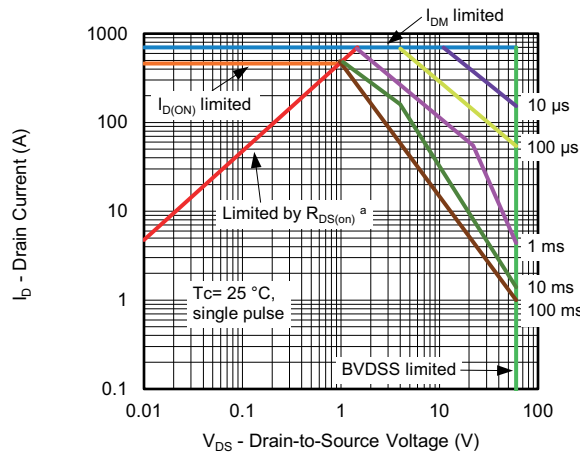
Threshold Voltage



On-Resistance vs. Gate-to-Source Voltage



Single Pulse Power, Junction-to-Case



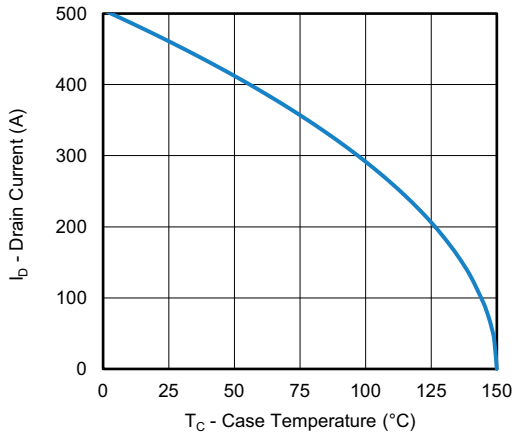
Safe Operating Area, Junction-to-Ambient

Note

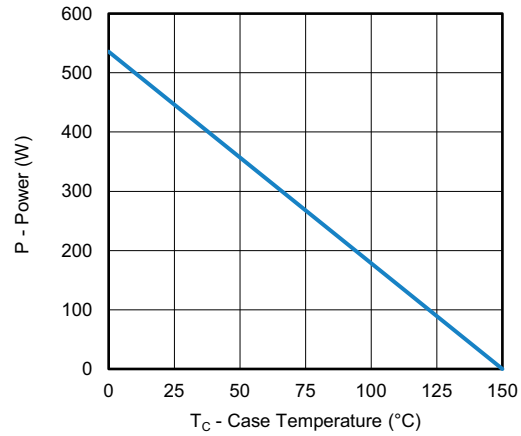
a.  $V_{GS} >$  minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified



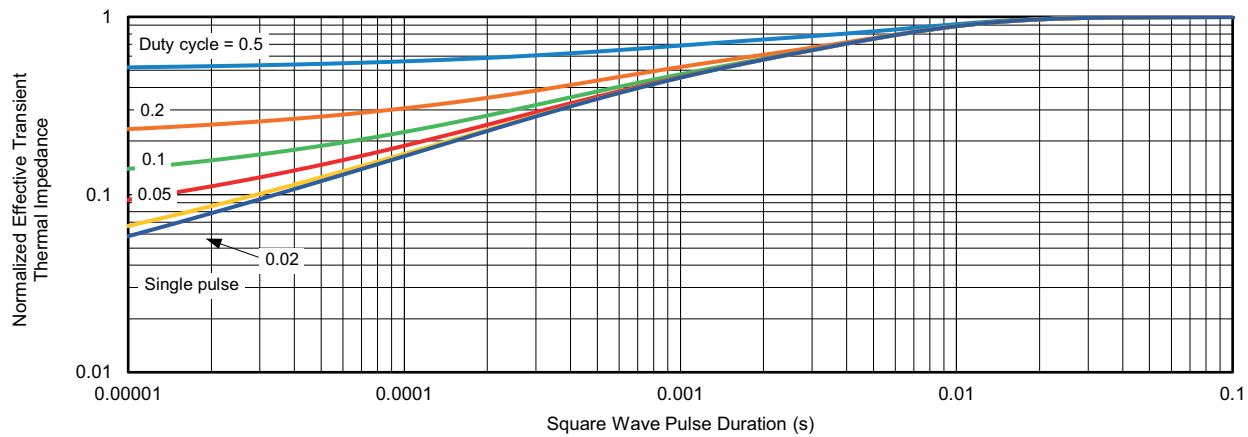
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating <sup>a</sup>



Power, Junction-to-Case



Normalized Thermal Transient Impedance, Junction-to-Case

Note

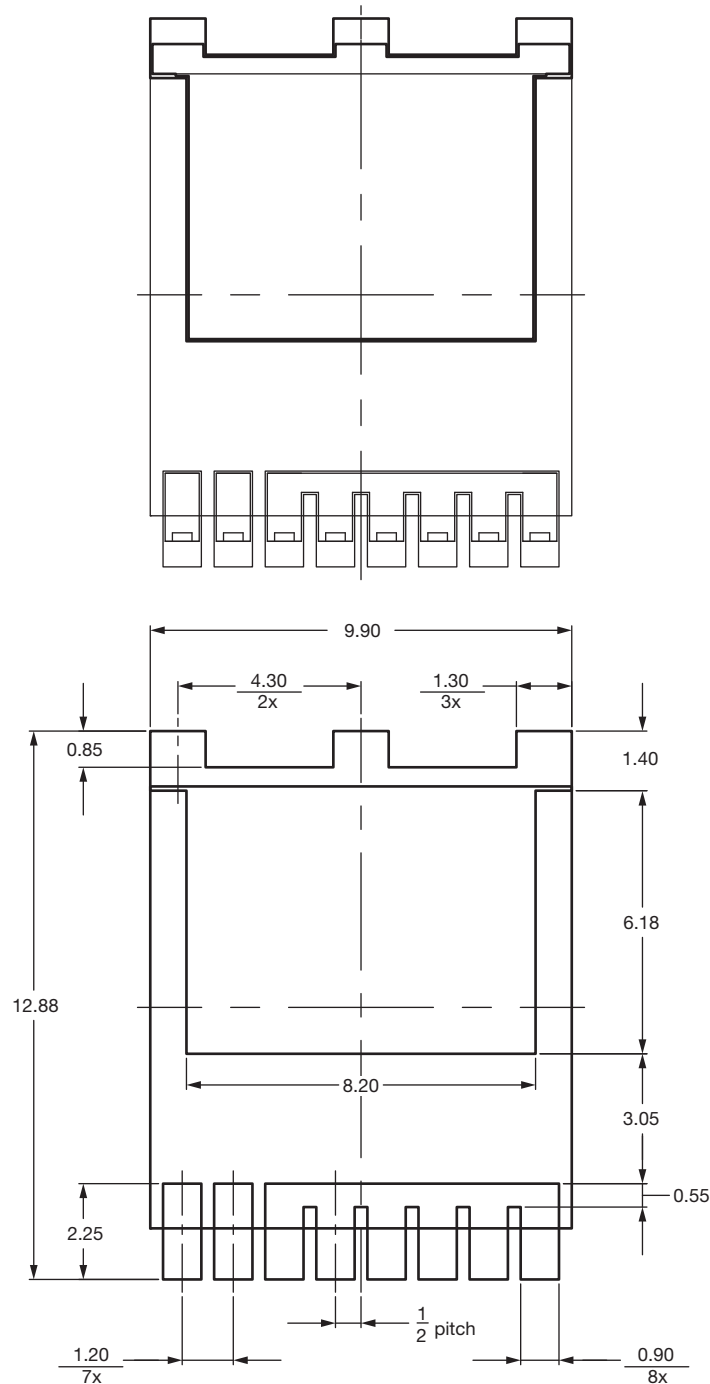
- a. The power dissipation  $P_D$  is based on  $T_J$  max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit

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# Recommended Land Pattern PowerPAK® 10 x 12

## PowerPAK® 10 x 12-1

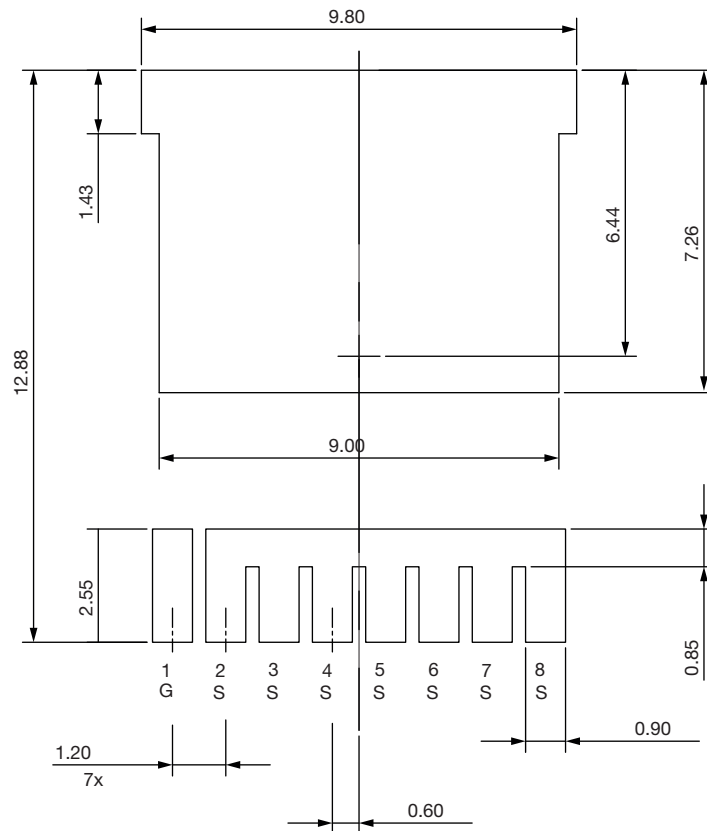
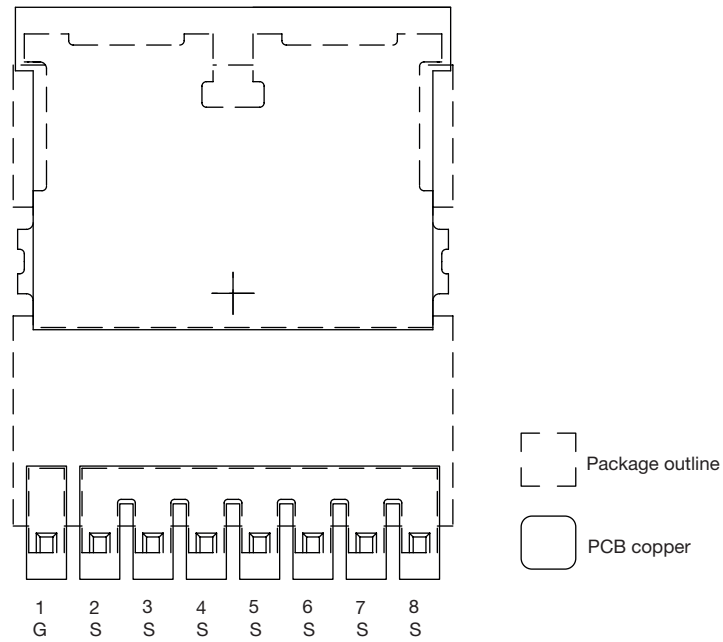


**Note**

- Dimensions in mm



## PowerPAK® 10 x 12-2



### Note

- Dimensions in mm

ECN: S25-0975-Rev. A, 18-Aug-2025  
DWG: 3037



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