

# **FDD6630A**

# 30V N-Channel PowerTrench MOSFET

### **General Description**

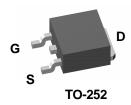
This N-Channel MOSFET has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low RDS(ON) and fast switching speed.

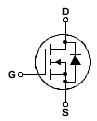
### **Applications**

- DC/DC converter
- Motor drives

#### **Features**

- 21 A, 30 V  $R_{DS(ON)} = 35 \ m\Omega \ @ \ V_{GS} = 10 \ V$   $R_{DS(ON)} = 50 \ m\Omega \ @ \ V_{GS} = 4.5 \ V$
- Low gate charge (5nC typical)
- · Fast switching
- High performance trench technology for extremely low R<sub>DS(ON)</sub>





### **Absolute Maximum Ratings** T<sub>A</sub>=25°C unless otherwise noted

Symbol	Parameter		Ratings	Units
V <sub>DSS</sub>	Drain-Source Voltage		30	V
V <sub>GSS</sub>	Gate-Source Voltage		±20	V
I <sub>D</sub>	Drain Current - Continuous	(Note 3)	21	Α
	- Pulsed	(Note 1a)	100	
P <sub>D</sub>	Power Dissipation	(Note 1)	28	W
		(Note 1a)	3.2	
		(Note 1b)	1.3	
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Junction Temperature Range		-55 to +175	°C

### **Thermal Characteristics**

R <sub>0</sub> JC	Thermal Resistance, Junction-to-Case	(Note 1)	4.5	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	40	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1b)	96	°C/W

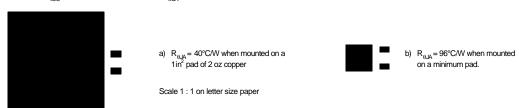
### **Package Marking and Ordering Information**

Device Marking	Device	Reel Size	Tape width	Quantity
FDD6630A	FDD6630A	13"	16mm	2500 units

Symbol	Parameter	Test Conditions	Min	Тур	Max	Units
Drain-Sc	ource Avalanche Ratings (Note	2)				
W <sub>DSS</sub>	Drain-Source Avalanche Energy	Single Pulse, V <sub>DD</sub> = 15 V			55	mJ
l <sub>AR</sub>	Drain-Source Avalanche Current				7.6	Α
Off Char	acteristics			l	l	l
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	30			V
$\frac{\Delta BV_{DSS}}{\Delta T_{J}}$	Breakdown Voltage Temperature Coefficient	$I_D$ = 250 μA, Referenced to 25°C		23		mV/°C
DSS	Zero Gate Voltage Drain Current	$V_{DS} = 24 \text{ V},  V_{GS} = 0 \text{ V}$			1	μΑ
GSSF	Gate-Body Leakage, Forward	$V_{GS} = 20 \text{ V}, \qquad V_{DS} = 0 \text{ V}$			100	nA
IGSSR	Gate-Body Leakage, Reverse	$V_{GS} = -20 \text{ V},  V_{DS} = 0 \text{ V}$			-100	nA
On Char	acteristics (Note 2)					
V <sub>GS(th)</sub>	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250 \mu A$	1	1.7	3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D$ = 250 $\mu$ A, Referenced to 25°C		-4		mV/°C
R <sub>DS(on)</sub>	Static Drain–Source On–Resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 7.6 A V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 6.3 A V <sub>GS</sub> = 10 V, I <sub>D</sub> = 7.6 A, T <sub>I</sub> = 125°C		28 40 44	35 50 58	mΩ
I <sub>D(on)</sub>	On–State Drain Current	$V_{GS} = 10 \text{ V}, I_D = 7.6 \text{ A}, T_J = 125^{\circ}\text{C}$ $V_{GS} = 10 \text{ V}, V_{DS} = 5 \text{ V}$	20			Α
<b>g</b> FS	Forward Transconductance	$V_{DS} = 5 \text{ V}, \qquad I_{D} = 7.6 \text{ A}$		13		S
Dynamic	Characteristics			l	l	l
Ciss	Input Capacitance	$V_{DS} = 15 \text{ V}, \qquad V_{GS} = 0 \text{ V},$		462		pF
Coss	Output Capacitance	f = 1.0 MHz		113		pF
Crss	Reverse Transfer Capacitance			40		pF
Switchin	g Characteristics (Note 2)			I	l	
t <sub>d(on)</sub>	Turn-On Delay Time	$V_{DD} = 15 \text{ V}, \qquad I_D = 1 \text{ A},$		5	11	ns
t <sub>r</sub>	Turn-On Rise Time	$V_{GS} = 10 \text{ V}, \qquad R_{GEN} = 6 \Omega$		8	17	ns
t <sub>d(off)</sub>	Turn-Off Delay Time			17	28	ns
t <sub>f</sub>	Turn-Off Fall Time			13	24	ns
Qg	Total Gate Charge	$V_{DS} = 15 \text{ V}, \qquad I_{D} = 7.6 \text{ A},$		5	7	nC
Q <sub>gs</sub>	Gate-Source Charge	$V_{GS} = 5 V$		2		nC
$Q_{gd}$	Gate-Drain Charge			1.4		nC
Drain-Se	ource Diode Characteristics	and Maximum Ratings				
I <sub>S</sub>	Maximum Continuous Drain-Source				2.7	Α
V <sub>SD</sub>	Drain–Source Diode Forward Voltage	$V_{GS} = 0 \text{ V},  I_S = 2.7 \text{ A}$ (Note 2)		0.8	1.2	V

#### Notes:

1. R<sub>Q,A</sub> is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R<sub>Q,C</sub> is guaranteed by design while R<sub>Q,CA</sub> is determined by the user's board design.



- 2. Pulse Test: Pulse Width <  $300\mu s,$  Duty Cycle < 2.0%
- 3. Maximum current is calculated as:  $\sqrt{\frac{P_D}{R_{DS(CN)}}}$  where  $P_D$  is maximum power dissipation at  $T_C = 25^{\circ}C$  and  $R_{DS(cn)}$  is at  $T_{J(max)}$  and  $V_{GS} = 10V$ . Package current limitation is 21A

# **Typical Characteristics**

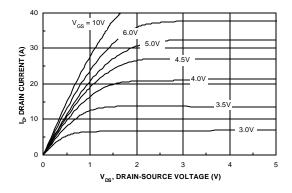
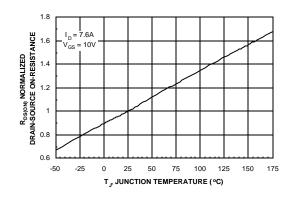


Figure 1. On-Region Characteristics.

Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.



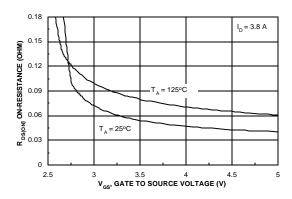
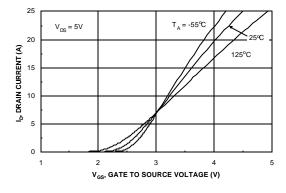


Figure 3. On-Resistance Variation with Temperature.

Figure 4. On-Resistance Variation with Gate-to-Source Voltage.



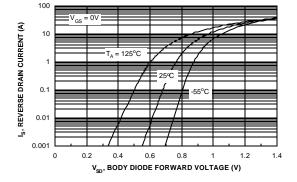
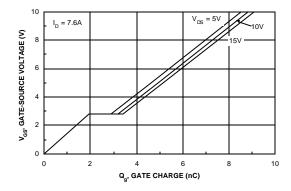


Figure 5. Transfer Characteristics.

Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

# **Typical Characteristics**



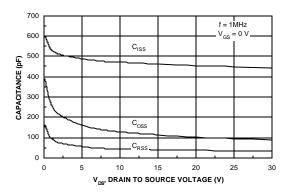
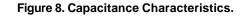
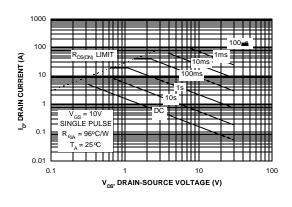


Figure 7. Gate Charge Characteristics.





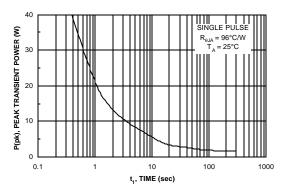


Figure 9. Maximum Safe Operating Area.

Figure 10. Single Pulse Maximum Power Dissipation.

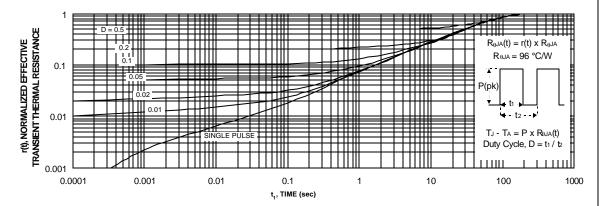


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1b. Transient thermal response will change depending on the circuit board design.





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