

FEATURES

High common-mode transient immunity: 100 kV/μs

High robustness to radiated and conducted noise

Low propagation delay

13 ns maximum for 5 V operation

15 ns maximum for 1.8 V operation

150 Mbps maximum guaranteed data rate

Safety and regulatory approvals (pending)

UL recognition

3000 V rms/3750 V rms for 1 minute per UL 1577

CSA Component Acceptance Notice 5A

VDE certificate of conformity

DIN V VDE V 0884-10 (VDE V 0884-10):2006-12

$V_{IORM} = 849$ V peak

CQC certification per GB4943.1-2011

Backward compatibility

ADuM140E1/ADuM141E1/ADuM142E1 pin-compatible
with **ADuM1400/ADuM1401/ADuM1402**

Low dynamic power consumption

1.8 V to 5 V level translation

High temperature operation: 125°C

Fail-safe high or low options

16-lead, RoHS compliant, SOIC package

APPLICATIONS

General-purpose multichannel isolation

Serial peripheral interface (SPI)/data converter isolation

Industrial field bus isolation

GENERAL DESCRIPTION

The **ADuM140D/ADuM140E/ADuM141D/ADuM141E/ADuM142D/ADuM142E**¹ are quad-channel digital isolators based on Analog Devices, Inc., iCoupler® technology. Combining high speed, complementary metal-oxide semiconductor (CMOS) and monolithic air core transformer technology, these isolation components provide outstanding performance characteristics superior to alternatives such as optocoupler devices and other integrated couplers. The maximum propagation delay is 13 ns with a pulse width distortion of less than 3 ns at 5 V operation. Channel matching is tight at 3.0 ns maximum.

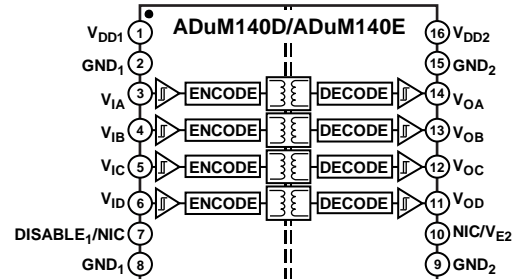
The **ADuM140D/ADuM140E/ADuM141D/ADuM141E/ADuM142D/ADuM142E** data channels are independent and are available in a variety of configurations with a withstand voltage rating of 3.0 kV rms or 3.75 kV rms (see the Ordering Guide). The devices operate with the supply voltage on either side ranging from 1.8 V to 5 V, providing compatibility with lower voltage systems as well as enabling voltage translation functionality across the isolation barrier.

Rev. B

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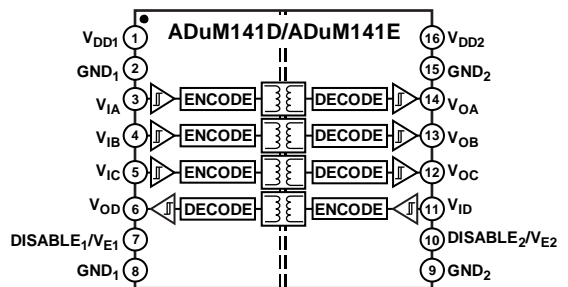
FUNCTIONAL BLOCK DIAGRAMS



NOTES

1. NIC = NO INTERNAL CONNECTION. LEAVE THIS PIN FLOATING.
2. PIN 7 IS DISABLE₁ AND PIN 10 IS NIC FOR THE ADuM140D, AND PIN 7 IS NIC AND PIN 10 IS VE₂ FOR THE ADuM140E.

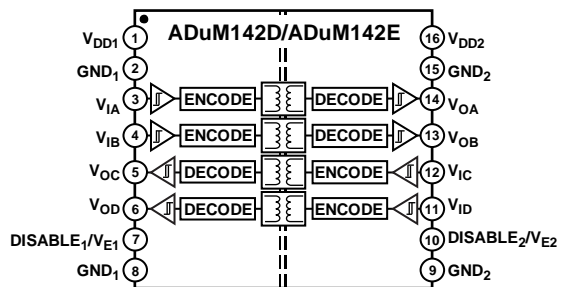
Figure 1. ADuM140D/ADuM140E Functional Block Diagram



NOTES

1. PIN 7 IS DISABLE₁ AND PIN 10 IS DISABLE₂ FOR THE ADuM141D, AND PIN 7 IS VE₁ AND PIN 10 IS VE₂ FOR THE ADuM141E.

Figure 2. ADuM141D/ADuM141E Functional Block Diagram



NOTES

1. PIN 7 IS DISABLE₁ AND PIN 10 IS DISABLE₂ FOR THE ADuM142D, AND PIN 7 IS VE₁ AND PIN 10 IS VE₂ FOR THE ADuM142E.

Figure 3. ADuM142D/ADuM142E Functional Block Diagram

Unlike other optocoupler alternatives, dc correctness is ensured in the absence of input logic transitions. Two different fail-safe options are available, by which the outputs transition to a pre-determined state when the input power supply is not applied or the inputs are disabled. The **ADuM140E1/ADuM141E1/ADuM142E1** are pin-compatible with the **ADuM1400/ADuM1401/ADuM1402**.

¹ Protected by U.S. Patents 5,952,849; 6,873,065; 6,903,578; and 7,075,329. Other patents are pending.

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REVISION HISTORY

11/15—Rev. A to Rev. B

| | |
|---|-----------|
| Added 16-Lead, Narrow Body SOIC Package | Universal |
| Changes to Title, Features Section, and General Description | |
| Section..... | 1 |
| Changes to Table 1..... | 3 |
| Changes to Table 3..... | 5 |
| Changes to Table 5..... | 7 |
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| Added Table 9; Renumbered Sequentially | 11 |
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| Added Table 13 | 12 |
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| Added Table 15 and Figure 4; Renumbered Sequentially | 14 |
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| Added Table 18 | 15 |
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| Updated Outline Dimensions | 25 |
| Changes to Ordering Guide | 26 |

9/15—Rev. 0 to Rev. A

| | |
|--|-----------|
| Added ADuM141D/ADuM141E | Universal |
| Added ADuM142D/ADuM142E | Universal |
| Changes to Features and Figure 1 | 1 |
| Delete Figure 2; Renumbered Sequentially..... | 1 |
| Added Figure 2 and Figure 3; Renumbered Sequentially | 1 |
| Changes to Table 1..... | 3 |
| Changes to Table 2..... | 4 |
| Changes to Table 3..... | 5 |
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| Added Figure 7, Figure 8, and Table 19; Renumbered | |
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| Updated Outline Dimensions | 23 |
| Changes to Ordering Guide | 23 |

4/15—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS—5 V OPERATION

All typical specifications are at $T_A = 25^\circ\text{C}$, $V_{DD1} = V_{DD2} = 5\text{ V}$. Minimum/maximum specifications apply over the entire recommended operation range of $4.5\text{ V} \leq V_{DD1} \leq 5.5\text{ V}$, $4.5\text{ V} \leq V_{DD2} \leq 5.5\text{ V}$, and $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$, unless otherwise noted. Switching specifications are tested with $C_L = 15\text{ pF}$ and CMOS signal levels, unless otherwise noted. Supply currents are specified with 50% duty cycle signals.

Table 1.

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions/Comments |
|--|-----------------------|----------------------|-----------------|----------------------|----------------------|--|
| SWITCHING SPECIFICATIONS | | | | | | |
| Pulse Width | PW | 6.6 | | | ns | Within pulse width distortion (PWD) limit |
| Data Rate ¹ | | 150 | | | Mbps | Within PWD limit |
| Propagation Delay | t_{PHL} , t_{PLH} | 4.8 | 7.2 | 13 | ns | 50% input to 50% output |
| Pulse Width Distortion | PWD | | 0.5 | 3 | ns | $ t_{PLH} - t_{PHL} $ |
| Change vs. Temperature | | | 1.5 | | ps/ $^\circ\text{C}$ | |
| Propagation Delay Skew | t_{PSK} | | | 6.1 | ns | Between any two units at the same temperature, voltage, and load |
| Channel Matching | | | | | | |
| Codirectional | t_{PSKCD} | | 0.5 | 3.0 | ns | |
| Opposing Direction | t_{PSKOD} | | 0.5 | 3.0 | ns | |
| Jitter | | | 490 | | ps p-p | See the Jitter Measurement section |
| | | | 70 | | ps rms | See the Jitter Measurement section |
| DC SPECIFICATIONS | | | | | | |
| Input Threshold Voltage | | | | | | |
| Logic High | V_{IH} | $0.7 \times V_{DDx}$ | | | V | |
| Logic Low | V_{IL} | | | $0.3 \times V_{DDx}$ | V | |
| Output Voltage | | | | | | |
| Logic High | V_{OH} | $V_{DDx} - 0.1$ | V_{DDx} | | V | $I_{Ox}^2 = -20\ \mu\text{A}$, $V_{Ix} = V_{IxH}^3$ |
| | | $V_{DDx} - 0.4$ | $V_{DDx} - 0.2$ | | V | $I_{Ox}^2 = -4\ \text{mA}$, $V_{Ix} = V_{IxH}^3$ |
| Logic Low | V_{OL} | | 0.0 | 0.1 | V | $I_{Ox}^2 = 20\ \mu\text{A}$, $V_{Ix} = V_{IxL}^4$ |
| | | | 0.2 | 0.4 | V | $I_{Ox}^2 = 4\ \text{mA}$, $V_{Ix} = V_{IxL}^4$ |
| Input Current per Channel | I_I | -10 | +0.01 | +10 | μA | $0\text{ V} \leq V_{Ix} \leq V_{DDx}$ |
| V_{E2} Enable Input Pull-Up Current | I_{PU} | -10 | -3 | | μA | $V_{E2} = 0\text{ V}$ |
| DISABLE ₁ Input Pull-Down Current | I_{PD} | | 9 | 15 | μA | DISABLE ₁ = V_{DDx} |
| Tristate Output Current per Channel | I_{OZ} | -10 | +0.01 | +10 | μA | $0\text{ V} \leq V_{Ox} \leq V_{DDx}$ |
| Quiescent Supply Current | | | | | | |
| ADuM140D/ADuM140E | $I_{DD1(Q)}$ | | 1.2 | 2.2 | mA | $V_I^5 = 0$ (E0, D0), 1 (E1, D1) ⁶ |
| | $I_{DD2(Q)}$ | | 2.0 | 2.72 | mA | $V_I^5 = 0$ (E0, D0), 1 (E1, D1) ⁶ |
| | $I_{DD1(Q)}$ | | 12.0 | 20.0 | mA | $V_I^5 = 1$ (E0, D0), 0 (E1, D1) ⁶ |
| | $I_{DD2(Q)}$ | | 2.0 | 2.92 | mA | $V_I^5 = 1$ (E0, D0), 0 (E1, D1) ⁶ |
| ADuM141D/ADuM141E | $I_{DD1(Q)}$ | | 1.6 | 2.46 | mA | $V_I^5 = 0$ (E0, D0), 1 (E1, D1) ⁶ |
| | $I_{DD2(Q)}$ | | 1.9 | 2.62 | mA | $V_I^5 = 0$ (E0, D0), 1 (E1, D1) ⁶ |
| | $I_{DD1(Q)}$ | | 10.0 | 17.0 | mA | $V_I^5 = 1$ (E0, D0), 0 (E1, D1) ⁶ |
| | $I_{DD2(Q)}$ | | 6.0 | 10.0 | mA | $V_I^5 = 1$ (E0, D0), 0 (E1, D1) ⁶ |
| ADuM142D/ADuM142E | $I_{DD1(Q)}$ | | 1.6 | 2.46 | mA | $V_I^5 = 0$ (E0, D0), 1 (E1, D1) ⁶ |
| | $I_{DD2(Q)}$ | | 1.6 | 2.46 | mA | $V_I^5 = 0$ (E0, D0), 1 (E1, D1) ⁶ |
| | $I_{DD1(Q)}$ | | 7.2 | 11.5 | mA | $V_I^5 = 1$ (E0, D0), 0 (E1, D1) ⁶ |
| | $I_{DD2(Q)}$ | | 8.4 | 11.5 | mA | $V_I^5 = 1$ (E0, D0), 0 (E1, D1) ⁶ |
| Dynamic Supply Current | | | | | | |
| Dynamic Input | $I_{DDI(D)}$ | | 0.01 | | mA/Mbps | Inputs switching, 50% duty cycle |
| Dynamic Output | $I_{DDO(D)}$ | | 0.02 | | mA/Mbps | Inputs switching, 50% duty cycle |

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|-----------------|-----|-----|-----|-------------|---|
| Undervoltage Lockout | UVLO | | | | | |
| Positive V_{DDx} Threshold | V_{DDxUV+} | | 1.6 | | V | |
| Negative V_{DDx} Threshold | V_{DDxUV-} | | 1.5 | | V | |
| V_{DDx} Hysteresis | V_{DDxUVH} | | 0.1 | | V | |
| AC SPECIFICATIONS | | | | | | |
| Output Rise/Fall Time | t_{ri}/t_{rf} | | 2.5 | | ns | 10% to 90% |
| Common-Mode Transient Immunity ⁷ | $ CM_H $ | 75 | 100 | | kV/ μ s | $V_{ix} = V_{DDx}$, $V_{CM} = 1000$ V, transient magnitude = 800 V |
| | $ CM_L $ | 75 | 100 | | kV/ μ s | $V_{ix} = 0$ V, $V_{CM} = 1000$ V, transient magnitude = 800 V |

¹ 150 Mbps is the highest data rate that can be guaranteed, although higher data rates are possible.

² I_{Ox} is the Channel x output current, where x = A, B, C, or D.

³ V_{IH} is the input side logic high.

⁴ V_{IL} is the input side logic low.

⁵ V_i is the voltage input.

⁶ E0 is the ADuM140E0/ADuM141E0/ADuM142E0 models, D0 is the ADuM140D0/ADuM141D0/ADuM142D0 models, E1 is the ADuM140E1/ADuM141E1/ADuM142E1 models, and D1 is the ADuM140D1/ADuM141D1/ADuM142D1 models. See the Ordering Guide section.

⁷ $|CM_H|$ is the maximum common-mode voltage slew rate that can be sustained while maintaining the voltage output (V_o) > 0.8 V_{DDx} . $|CM_L|$ is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_o > 0.8$ V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

Table 2. Total Supply Current vs. Data Throughput

| Parameter | Symbol | 1 Mbps | | | 25 Mbps | | | 100 Mbps | | | Unit |
|-----------------------|-----------|--------|------|-----|---------|------|-----|----------|------|-----|------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| SUPPLY CURRENT | | | | | | | | | | | |
| ADuM140D/ADuM140E | | | | | | | | | | | |
| Supply Current Side 1 | I_{DD1} | 6.8 | 10 | | 7.8 | 12 | | 11.8 | 17.4 | | mA |
| Supply Current Side 2 | I_{DD2} | 2.1 | 3.7 | | 3.9 | 5.7 | | 9.2 | 13 | | mA |
| ADuM141D/ADuM141E | | | | | | | | | | | |
| Supply Current Side 1 | I_{DD1} | 5.8 | 10.3 | | 7.0 | 10.9 | | 11.4 | 15.9 | | mA |
| Supply Current Side 2 | I_{DD2} | 4.0 | 6.85 | | 5.5 | 8.5 | | 10.3 | 14.0 | | mA |
| ADuM142D/ADuM142E | | | | | | | | | | | |
| Supply Current Side 1 | I_{DD1} | 4.3 | 7.7 | | 6.0 | 9.3 | | 10.3 | 14.2 | | mA |
| Supply Current Side 2 | I_{DD2} | 5.3 | 8.7 | | 6.7 | 10.1 | | 11.0 | 14.9 | | mA |

ELECTRICAL CHARACTERISTICS—3.3 V OPERATION

All typical specifications are at $T_A = 25^\circ\text{C}$, $V_{DD1} = V_{DD2} = 3.3\text{ V}$. Minimum/maximum specifications apply over the entire recommended operation range: $3.0\text{ V} \leq V_{DD1} \leq 3.6\text{ V}$, $3.0\text{ V} \leq V_{DD2} \leq 3.6\text{ V}$, and $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$, unless otherwise noted. Switching specifications are tested with $C_L = 15\text{ pF}$ and CMOS signal levels, unless otherwise noted. Supply currents are specified with 50% duty cycle signals.

Table 3.

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions/Comments |
|--|-----------------------|----------------------|-----------------|----------------------|---------------|--|
| SWITCHING SPECIFICATIONS | | | | | | |
| Pulse Width | PW | 6.6 | | | ns | Within PWD limit |
| Data Rate ¹ | | 150 | | | Mbps | Within PWD limit |
| Propagation Delay | t_{PHL} , t_{PLH} | 4.8 | 6.8 | 14 | ns | 50% input to 50% output |
| Pulse Width Distortion | PWD | | 0.7 | 3 | ns | $ t_{PLH} - t_{PHL} $ |
| Change vs. Temperature | | | 1.5 | | ps/°C | |
| Propagation Delay Skew | t_{PSK} | | | 7.5 | ns | Between any two units at the same temperature, voltage, and load |
| Channel Matching | | | | | | |
| Codirectional | t_{PSKCD} | | 0.7 | 3.0 | ns | |
| Opposing Direction | t_{PSKOD} | | 0.7 | 3.0 | ns | |
| Jitter | | | 580 | | ps p-p | See the Jitter Measurement section |
| | | | 120 | | ps rms | See the Jitter Measurement section |
| DC SPECIFICATIONS | | | | | | |
| Input Threshold Voltage | | | | | | |
| Logic High | V_{IH} | $0.7 \times V_{DDx}$ | | | V | |
| Logic Low | V_{IL} | | | $0.3 \times V_{DDx}$ | V | |
| Output Voltage | | | | | | |
| Logic High | V_{OH} | $V_{DDx} - 0.1$ | V_{DDx} | | V | $I_{Ox}^2 = -20\text{ }\mu\text{A}$, $V_{Ix} = V_{IxH}^3$ |
| | | $V_{DDx} - 0.4$ | $V_{DDx} - 0.2$ | | V | $I_{Ox}^2 = -2\text{ mA}$, $V_{Ix} = V_{IxH}^3$ |
| Logic Low | V_{OL} | | 0.0 | 0.1 | V | $I_{Ox}^2 = 20\text{ }\mu\text{A}$, $V_{Ix} = V_{IxL}^4$ |
| | | | 0.2 | 0.4 | V | $I_{Ox}^2 = 2\text{ mA}$, $V_{Ix} = V_{IxL}^4$ |
| Input Current per Channel | I_i | -10 | +0.01 | +10 | μA | $0\text{ V} \leq V_{Ix} \leq V_{DDx}$ |
| V_{E2} Enable Input Pull-Up Current | I_{PU} | -10 | -3 | | μA | $V_{E2} = 0\text{ V}$ |
| DISABLE ₁ Input Pull-Down Current | I_{PD} | | 9 | 15 | μA | DISABLE ₁ = V_{DDx} |
| Tristate Output Current per Channel | I_{OZ} | -10 | +0.01 | +10 | μA | $0\text{ V} \leq V_{Ox} \leq V_{DDx}$ |
| Quiescent Supply Current | | | | | | |
| ADuM140D/ADuM140E | | | | | | |
| | $I_{DD1(Q)}$ | | 1.2 | 2.12 | mA | $V_i^5 = 0$ (E0, D0), 1 (E1, D1) ⁶ |
| | $I_{DD2(Q)}$ | | 2.0 | 2.68 | mA | $V_i^5 = 0$ (E0, D0), 1 (E1, D1) ⁶ |
| | $I_{DD1(Q)}$ | | 12.0 | 19.6 | mA | $V_i^5 = 1$ (E0, D0), 0 (E1, D1) ⁶ |
| | $I_{DD2(Q)}$ | | 2.0 | 2.8 | mA | $V_i^5 = 1$ (E0, D0), 0 (E1, D1) ⁶ |
| ADuM141D/ADuM141E | | | | | | |
| | $I_{DD1(Q)}$ | | 1.5 | 2.36 | mA | $V_i^5 = 0$ (E0, D0), 1 (E1, D1) ⁶ |
| | $I_{DD2(Q)}$ | | 1.8 | 2.52 | mA | $V_i^5 = 0$ (E0, D0), 1 (E1, D1) ⁶ |
| | $I_{DD1(Q)}$ | | 9.8 | 16.7 | mA | $V_i^5 = 1$ (E0, D0), 0 (E1, D1) ⁶ |
| | $I_{DD2(Q)}$ | | 5.7 | 9.7 | mA | $V_i^5 = 1$ (E0, D0), 0 (E1, D1) ⁶ |
| ADuM142D/ADuM142E | | | | | | |
| | $I_{DD1(Q)}$ | | 1.6 | 2.4 | mA | $V_i^5 = 0$ (E0, D0), 1 (E1, D1) ⁶ |
| | $I_{DD2(Q)}$ | | 1.6 | 2.4 | mA | $V_i^5 = 0$ (E0, D0), 1 (E1, D1) ⁶ |
| | $I_{DD1(Q)}$ | | 7.2 | 11.2 | mA | $V_i^5 = 1$ (E0, D0), 0 (E1, D1) ⁶ |
| | $I_{DD2(Q)}$ | | 8.4 | 11.2 | mA | $V_i^5 = 1$ (E0, D0), 0 (E1, D1) ⁶ |

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|--------------|-----|------|-----|-------------|--|
| Dynamic Supply Current | | | | | | |
| Dynamic Input | $I_{DD1(D)}$ | | 0.01 | | mA/Mbps | Inputs switching, 50% duty cycle |
| Dynamic Output | $I_{DD0(D)}$ | | 0.01 | | mA/Mbps | Inputs switching, 50% duty cycle |
| Undervoltage Lockout | UVLO | | | | | |
| Positive V_{DDx} Threshold | V_{DDxUV+} | | 1.6 | | V | |
| Negative V_{DDx} Threshold | V_{DDxUV-} | | 1.5 | | V | |
| V_{DDx} Hysteresis | V_{DDxUVH} | | 0.1 | | V | |
| AC SPECIFICATIONS | | | | | | |
| Output Rise/Fall Time | t_r/t_f | | 2.5 | | ns | 10% to 90% |
| Common-Mode Transient Immunity ⁷ | $ CM_H $ | 75 | 100 | | kV/ μ s | $V_{ix} = V_{DDx}$, $V_{CM} = 1000$ V, transient magnitude = 800 V |
| | $ CM_L $ | 75 | 100 | | kV/ μ s | $V_{ix} = 0$ V, $V_{CM} = 1000$ V, transient magnitude = 800 V |

¹ 150 Mbps is the highest data rate that can be guaranteed, although higher data rates are possible.

² I_{Ox} is the Channel x output current, where x = A, B, C, or D.

³ V_{BH} is the input side logic high.

⁴ V_{BL} is the input side logic low.

⁵ V_i is the voltage input.

⁶ E0 is the ADuM140E0/ADuM141E0/ADuM142E0 models, D0 is the ADuM140D0/ADuM141D0/ADuM142D0 models, E1 is the ADuM140E1/ADuM141E1/ADuM142E1 models, and D1 is the ADuM140D1/ADuM141D1/ADuM142D1 models. See the Ordering Guide section.

⁷ $|CM_H|$ is the maximum common-mode voltage slew rate that can be sustained while maintaining the voltage output (V_o) > 0.8 V_{DDx} . $|CM_L|$ is the maximum common-mode voltage slew rate that can be sustained while maintaining V_o > 0.8 V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

Table 4. Total Supply Current vs. Data Throughput

| Parameter | Symbol | 1 Mbps | | | 25 Mbps | | | 100 Mbps | | | Unit |
|-----------------------|-----------|--------|------|------|---------|------|------|----------|------|------|------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| SUPPLY CURRENT | | | | | | | | | | | |
| ADuM140D/ADuM140E | | | | | | | | | | | |
| Supply Current Side 1 | I_{DD1} | | 6.6 | 9.8 | | 7.4 | 11.2 | | 10.7 | 15.9 | mA |
| Supply Current Side 2 | I_{DD2} | | 2.0 | 3.7 | | 3.5 | 5.5 | | 8.2 | 11.6 | mA |
| ADuM141D/ADuM141E | | | | | | | | | | | |
| Supply Current Side 1 | I_{DD1} | | 5.65 | 10.1 | | 6.65 | 10.5 | | 10.4 | 14.9 | mA |
| Supply Current Side 2 | I_{DD2} | | 3.9 | 6.65 | | 5.2 | 8.0 | | 9.4 | 12.8 | mA |
| ADuM142D/ADuM142E | | | | | | | | | | | |
| Supply Current Side 1 | I_{DD1} | | 4.3 | 7.7 | | 5.6 | 9.0 | | 9.1 | 13 | mA |
| Supply Current Side 2 | I_{DD2} | | 5.0 | 8.4 | | 6.2 | 9.6 | | 9.8 | 13.7 | mA |

ELECTRICAL CHARACTERISTICS—2.5 V OPERATION

All typical specifications are at $T_A = 25^\circ\text{C}$, $V_{DD1} = V_{DD2} = 2.5\text{ V}$. Minimum/maximum specifications apply over the entire recommended operation range: $2.25\text{ V} \leq V_{DD1} \leq 2.75\text{ V}$, $2.25\text{ V} \leq V_{DD2} \leq 2.75\text{ V}$, $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$, unless otherwise noted. Switching specifications are tested with $C_L = 15\text{ pF}$ and CMOS signal levels, unless otherwise noted. Supply currents are specified with 50% duty cycle signals.

Table 5.

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions/Comments |
|--|-----------------------|----------------------|-----------------|----------------------|---------------|--|
| SWITCHING SPECIFICATIONS | | | | | | |
| Pulse Width | PW | 6.6 | | | ns | Within PWD limit |
| Data Rate ¹ | | 150 | | | Mbps | Within PWD limit |
| Propagation Delay | t_{PHL} , t_{PLH} | 5.0 | 7.0 | 14 | ns | 50% input to 50% output |
| Pulse Width Distortion | PWD | | 0.7 | 3 | ns | $ t_{PLH} - t_{PHL} $ |
| Change vs. Temperature | | | 1.5 | | ps/°C | |
| Propagation Delay Skew | t_{PSK} | | | 6.8 | ns | Between any two units at the same temperature, voltage, and load |
| Channel Matching | | | | | | |
| Codirectional | t_{PSKCD} | | 0.7 | 3.0 | ns | |
| Opposing Direction | t_{PSKOD} | | 0.7 | 3.0 | ns | |
| Jitter | | | 800 | | ps p-p | See the Jitter Measurement section |
| | | | 190 | | ps rms | See the Jitter Measurement section |
| DC SPECIFICATIONS | | | | | | |
| Input Threshold Voltage | | | | | | |
| Logic High | V_{IH} | $0.7 \times V_{DDx}$ | | | V | |
| Logic Low | V_{IL} | | | $0.3 \times V_{DDx}$ | V | |
| Output Voltage | | | | | | |
| Logic High | V_{OH} | $V_{DDx} - 0.1$ | V_{DDx} | | V | $I_{Ox}^2 = -20\text{ }\mu\text{A}$, $V_{Ix} = V_{IxH}^3$ |
| | | $V_{DDx} - 0.4$ | $V_{DDx} - 0.2$ | | V | $I_{Ox}^2 = -2\text{ mA}$, $V_{Ix} = V_{IxH}^3$ |
| Logic Low | V_{OL} | | 0.0 | 0.1 | V | $I_{Ox}^2 = 20\text{ }\mu\text{A}$, $V_{Ix} = V_{IxL}^4$ |
| | | | 0.2 | 0.4 | V | $I_{Ox}^2 = 2\text{ mA}$, $V_{Ix} = V_{IxL}^4$ |
| Input Current per Channel | I_I | -10 | +0.01 | +10 | μA | $0\text{ V} \leq V_{Ix} \leq V_{DDx}$ |
| V_{E2} Enable Input Pull-Up Current | I_{PU} | -10 | -3 | | μA | $V_{E2} = 0\text{ V}$ |
| DISABLE ₁ Input Pull-Down Current | I_{PD} | | 9 | 15 | μA | DISABLE ₁ = V_{DDx} |
| Tristate Output Current per Channel | I_{OZ} | -10 | +0.01 | +10 | μA | $0\text{ V} \leq V_{Ox} \leq V_{DDx}$ |
| Quiescent Supply Current | | | | | | |
| ADuM140D/ADuM140E | | | | | | |
| | $I_{DD1(Q)}$ | | 1.2 | 2.0 | mA | $V_I^5 = 0$ (E0, D0), 1 (E1, D1) ⁶ |
| | $I_{DD2(Q)}$ | | 2.0 | 2.64 | mA | $V_I^5 = 0$ (E0, D0), 1 (E1, D1) ⁶ |
| | $I_{DD1(Q)}$ | | 1.2 | 19.6 | mA | $V_I^5 = 1$ (E0, D0), 0 (E1, D1) ⁶ |
| | $I_{DD2(Q)}$ | | 2.0 | 2.76 | mA | $V_I^5 = 1$ (E0, D0), 0 (E1, D1) ⁶ |
| ADuM141D/ADuM141E | | | | | | |
| | $I_{DD1(Q)}$ | | 1.46 | 2.32 | mA | $V_I^5 = 0$ (E0, D0), 1 (E1, D1) ⁶ |
| | $I_{DD2(Q)}$ | | 1.75 | 2.47 | mA | $V_I^5 = 0$ (E0, D0), 1 (E1, D1) ⁶ |
| | $I_{DD1(Q)}$ | | 9.7 | 16.6 | mA | $V_I^5 = 1$ (E0, D0), 0 (E1, D1) ⁶ |
| | $I_{DD2(Q)}$ | | 5.67 | 9.67 | mA | $V_I^5 = 1$ (E0, D0), 0 (E1, D1) ⁶ |
| ADuM142D/ADuM142E | | | | | | |
| | $I_{DD1(Q)}$ | | 1.6 | 2.32 | mA | $V_I^5 = 0$ (E0, D0), 1 (E1, D1) ⁶ |
| | $I_{DD2(Q)}$ | | 1.6 | 2.32 | mA | $V_I^5 = 0$ (E0, D0), 1 (E1, D1) ⁶ |
| | $I_{DD1(Q)}$ | | 7.2 | 11.2 | mA | $V_I^5 = 1$ (E0, D0), 0 (E1, D1) ⁶ |
| | $I_{DD2(Q)}$ | | 8.4 | 11.2 | mA | $V_I^5 = 1$ (E0, D0), 0 (E1, D1) ⁶ |
| Dynamic Supply Current | | | | | | |
| Dynamic Input | $I_{DDI(D)}$ | | 0.01 | | mA/Mbps | Inputs switching, 50% duty cycle |
| Dynamic Output | $I_{DDO(D)}$ | | 0.01 | | mA/Mbps | Inputs switching, 50% duty cycle |

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|--------------|-----|-----|-----|-------------|--|
| Undervoltage Lockout | | | | | | |
| Positive V_{DDx} Threshold | V_{DDxUV+} | | 1.6 | | V | |
| Negative V_{DDx} Threshold | V_{DDxUV-} | | 1.5 | | V | |
| V_{DDx} Hysteresis | V_{DDxUVH} | | 0.1 | | V | |
| AC SPECIFICATIONS | | | | | | |
| Output Rise/Fall Time | t_R/t_F | | 2.5 | | ns | 10% to 90% |
| Common-Mode Transient Immunity ⁷ | $ CM_H $ | 75 | 100 | | kV/ μ s | $V_{IX} = V_{DDx}$, $V_{CM} = 1000$ V, transient magnitude = 800 V |
| | $ CM_L $ | 75 | 100 | | kV/ μ s | $V_{IX} = 0$ V, $V_{CM} = 1000$ V, transient magnitude = 800 V |

¹ 150 Mbps is the highest data rate that can be guaranteed, although higher data rates are possible.

² I_{Ox} is the Channel x output current, where x = A, B, C, or D.

³ V_{BH} is the input side logic high.

⁴ V_{BL} is the input side logic low.

⁵ V_i is the voltage input.

⁶ E0 is the ADuM140E0/ADuM141E0/ADuM142E0 models, D0 is the ADuM140D0/ADuM141D0/ADuM142D0 models, E1 is the ADuM140E1/ADuM141E1/ADuM142E1 models, and D1 is the ADuM140D1/ADuM141D1/ADuM142D1 models. See the Ordering Guide section.

⁷ $|CM_H|$ is the maximum common-mode voltage slew rate that can be sustained while maintaining the voltage output (VO) > 0.8 VDDx. $|CM_L|$ is the maximum common-mode voltage slew rate that can be sustained while maintaining VO > 0.8 V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

Table 6. Total Supply Current vs. Data Throughput

| Parameter | Symbol | 1 Mbps | | | 25 Mbps | | | 100 Mbps | | | Unit |
|-----------------------|-----------|--------|------|-----|---------|------|-----|----------|------|-----|------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| SUPPLY CURRENT | | | | | | | | | | | |
| ADuM140D/ADuM140E | | | | | | | | | | | |
| Supply Current Side 1 | I_{DD1} | 6.5 | 9.8 | | 7.3 | 11.1 | | 10.4 | 15.5 | mA | |
| Supply Current Side 2 | I_{DD2} | 2.0 | 3.6 | | 3.3 | 5.2 | | 7.3 | 10.2 | mA | |
| ADuM141D/ADuM141E | | | | | | | | | | | |
| Supply Current Side 1 | I_{DD1} | 5.6 | 10.0 | | 6.4 | 10.4 | | 9.7 | 14.5 | mA | |
| Supply Current Side 2 | I_{DD2} | 3.8 | 6.55 | | 4.8 | 7.7 | | 8.3 | 11.5 | mA | |
| ADuM142D/ADuM142E | | | | | | | | | | | |
| Supply Current Side 1 | I_{DD1} | 4.3 | 7.7 | | 5.4 | 8.8 | | 8.8 | 12.7 | mA | |
| Supply Current Side 2 | I_{DD2} | 5.0 | 8.4 | | 6.1 | 9.5 | | 9.5 | 13.4 | mA | |

ELECTRICAL CHARACTERISTICS—1.8 V OPERATION

All typical specifications are at $T_A = 25^\circ\text{C}$, $V_{DD1} = V_{DD2} = 1.8\text{ V}$. Minimum/maximum specifications apply over the entire recommended operation range: $1.7\text{ V} \leq V_{DD1} \leq 1.9\text{ V}$, $1.7\text{ V} \leq V_{DD2} \leq 1.9\text{ V}$, and $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$, unless otherwise noted. Switching specifications are tested with $C_L = 15\text{ pF}$ and CMOS signal levels, unless otherwise noted. Supply currents are specified with 50% duty cycle signals.

Table 7.

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions/Comments |
|--|-----------------------|----------------------|-----------------|----------------------|---------------|--|
| SWITCHING SPECIFICATIONS | | | | | | |
| Pulse Width | PW | 6.6 | | | ns | Within PWD limit |
| Data Rate ¹ | | 150 | | | Mbps | Within PWD limit |
| Propagation Delay | t_{PHL} , t_{PLH} | 5.8 | 8.7 | 15 | ns | 50% input to 50% output |
| Pulse Width Distortion | PWD | | 0.7 | 3 | ns | $ t_{PLH} - t_{PHL} $ |
| Change vs. Temperature | | | 1.5 | | ps/°C | |
| Propagation Delay Skew | t_{PSK} | | | 7.0 | ns | Between any two units at the same temperature, voltage, and load |
| Channel Matching | | | | | | |
| Codirectional | t_{PSKCD} | | 0.7 | 3.0 | ns | |
| Opposing Direction | t_{PSKOD} | | 0.7 | 3.0 | ns | |
| Jitter | | | 470 | | ps p-p | See the Jitter Measurement section |
| | | | 70 | | ps rms | See the Jitter Measurement section |
| DC SPECIFICATIONS | | | | | | |
| Input Threshold Voltage | | | | | | |
| Logic High | V_{IH} | $0.7 \times V_{DDx}$ | | | V | |
| Logic Low | V_{IL} | | | $0.3 \times V_{DDx}$ | V | |
| Output Voltage | | | | | | |
| Logic High | V_{OH} | $V_{DDx} - 0.1$ | V_{DDx} | | V | $I_{Ox}^2 = -20\text{ }\mu\text{A}$, $V_{Ix} = V_{IxH}^3$ |
| | | $V_{DDx} - 0.4$ | $V_{DDx} - 0.2$ | | V | $I_{Ox}^2 = -2\text{ mA}$, $V_{Ix} = V_{IxH}^3$ |
| Logic Low | V_{OL} | | 0.0 | 0.1 | V | $I_{Ox}^2 = 20\text{ }\mu\text{A}$, $V_{Ix} = V_{IxL}^4$ |
| | | | 0.2 | 0.4 | V | $I_{Ox}^2 = 2\text{ mA}$, $V_{Ix} = V_{IxL}^4$ |
| Input Current per Channel | I_I | -10 | +0.01 | +10 | μA | $0\text{ V} \leq V_{Ix} \leq V_{DDx}$ |
| V_{E2} Enable Input Pull-Up Current | I_{PU} | -10 | -3 | | μA | $V_{E2} = 0\text{ V}$ |
| DISABLE ₁ Input Pull-Down Current | I_{PD} | | 9 | 15 | μA | DISABLE ₁ = V_{DDx} |
| Tristate Output Current per Channel | I_{OZ} | -10 | +0.01 | +10 | μA | $0\text{ V} \leq V_{Ox} \leq V_{DDx}$ |
| Quiescent Supply Current | | | | | | |
| ADuM140D/ADuM140E | | | | | | |
| | $I_{DD1(Q)}$ | | 1.2 | 1.92 | mA | $V_I^5 = 0$ (E0, D0), 1 (E1, D1) ⁶ |
| | $I_{DD2(Q)}$ | | 2.0 | 2.64 | mA | $V_I^5 = 0$ (E0, D0), 1 (E1, D1) ⁶ |
| | $I_{DD1(Q)}$ | | 12.0 | 19.6 | mA | $V_I^5 = 1$ (E0, D0), 0 (E1, D1) ⁶ |
| | $I_{DD2(Q)}$ | | 2.0 | 2.76 | mA | $V_I^5 = 1$ (E0, D0), 0 (E1, D1) ⁶ |
| ADuM141D/ADuM141E | | | | | | |
| | $I_{DD1(Q)}$ | | 1.4 | 2.28 | mA | $V_I^5 = 0$ (E0, D0), 1 (E1, D1) ⁶ |
| | $I_{DD2(Q)}$ | | 1.73 | 2.45 | mA | $V_I^5 = 0$ (E0, D0), 1 (E1, D1) ⁶ |
| | $I_{DD1(Q)}$ | | 9.6 | 16.5 | mA | $V_I^5 = 1$ (E0, D0), 0 (E1, D1) ⁶ |
| | $I_{DD2(Q)}$ | | 5.6 | 9.6 | mA | $V_I^5 = 1$ (E0, D0), 0 (E1, D1) ⁶ |
| ADuM142D/ADuM142E | | | | | | |
| | $I_{DD1(Q)}$ | | 1.6 | 2.28 | mA | $V_I^5 = 0$ (E0, D0), 1 (E1, D1) ⁶ |
| | $I_{DD2(Q)}$ | | 1.6 | 2.28 | mA | $V_I^5 = 0$ (E0, D0), 1 (E1, D1) ⁶ |
| | $I_{DD1(Q)}$ | | 7.2 | 11.2 | mA | $V_I^5 = 1$ (E0, D0), 0 (E1, D1) ⁶ |
| | $I_{DD2(Q)}$ | | 8.4 | 11.2 | mA | $V_I^5 = 1$ (E0, D0), 0 (E1, D1) ⁶ |
| Dynamic Supply Current | | | | | | |
| Dynamic Input | $I_{DDI(D)}$ | | 0.01 | | mA/Mbps | Inputs switching, 50% duty cycle |
| Dynamic Output | $I_{DDO(D)}$ | | 0.01 | | mA/Mbps | Inputs switching, 50% duty cycle |

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|--------------|-----|-----|-----|-------------|--|
| Undervoltage Lockout | UVLO | | | | | |
| Positive V_{DDx} Threshold | V_{DDxUV+} | | 1.6 | | V | |
| Negative V_{DDx} Threshold | V_{DDxUV-} | | 1.5 | | V | |
| V_{DDx} Hysteresis | V_{DDxUVH} | | 0.1 | | V | |
| AC SPECIFICATIONS | | | | | | |
| Output Rise/Fall Time | t_R/t_F | | 2.5 | | ns | 10% to 90% |
| Common-Mode Transient Immunity ⁷ | $ CM_H $ | 75 | 100 | | kV/ μ s | $V_{IX} = V_{DDx}$, $V_{CM} = 1000$ V, transient magnitude = 800 V |
| | $ CM_L $ | 75 | 100 | | kV/ μ s | $V_{IX} = 0$ V, $V_{CM} = 1000$ V, transient magnitude = 800 V |

¹ 150 Mbps is the highest data rate that can be guaranteed, although higher data rates are possible.

² I_{Ox} is the Channel x output current, where x = A, B, C, or D.

³ V_{BH} is the input side logic high.

⁴ V_{BL} is the input side logic low.

⁵ V_i is the voltage input.

⁶ E0 is the ADuM140E0/ADuM141E0/ADuM142E0 models, D0 is the ADuM140D0/ADuM141D0/ADuM142D0 models, E1 is the ADuM140E1/ADuM141E1/ADuM142E1 models, and D1 is the ADuM140D1/ADuM141D1/ADuM142D1 models. See the Ordering Guide section.

⁷ $|CM_H|$ is the maximum common-mode voltage slew rate that can be sustained while maintaining the voltage output (V_o) > 0.8 V_{DDx} . $|CM_L|$ is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_o > 0.8$ V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

Table 8. Total Supply Current vs. Data Throughput

| Parameter | Symbol | 1 Mbps | | | 25 Mbps | | | 100 Mbps | | | Unit |
|-----------------------|-----------|--------|------|------|---------|-----|------|----------|------|------|------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| SUPPLY CURRENT | | | | | | | | | | | |
| ADuM140D/ADuM140E | | | | | | | | | | | |
| Supply Current Side 1 | I_{DD1} | | 6.4 | 9.8 | | 7.2 | 11 | | 10.2 | 15.2 | mA |
| Supply Current Side 2 | I_{DD2} | | 1.9 | 3.5 | | 3.1 | 5.0 | | 6.8 | 10 | mA |
| ADuM141D/ADuM141E | | | | | | | | | | | |
| Supply Current Side 1 | I_{DD1} | | 5.5 | 9.1 | | 6.3 | 10.0 | | 9.6 | 14.0 | mA |
| Supply Current Side 2 | I_{DD2} | | 3.72 | 6.45 | | 4.8 | 7.5 | | 8.4 | 11.2 | mA |
| ADuM142D/ADuM142E | | | | | | | | | | | |
| Supply Current Side 1 | I_{DD1} | | 4.3 | 7.7 | | 5.3 | 8.7 | | 8.6 | 12.6 | mA |
| Supply Current Side 2 | I_{DD2} | | 4.9 | 8.3 | | 6.0 | 9.4 | | 9.3 | 13.3 | mA |

INSULATION AND SAFETY RELATED SPECIFICATIONS

For additional information, see www.analog.com/icouplersafety.

Table 9. R-16 Narrow Body [SOIC_N] Package

| Parameter | Symbol | Value | Unit | Test Conditions/Comments |
|---|---------|-------|--------|--|
| Rated Dielectric Insulation Voltage | | 3000 | V rms | 1-minute duration |
| Minimum External Air Gap (Clearance) | L (I01) | 4.0 | mm min | Measured from input terminals to output terminals, shortest distance through air |
| Minimum External Tracking (Creepage) | L (I02) | 4.0 | mm min | Measured from input terminals to output terminals, shortest distance path along body |
| Minimum Clearance in the Plane of the Printed Circuit Board (PCB Clearance) | L (PCB) | 4.5 | mm min | Measured from input terminals to output terminals, shortest distance through air, line of sight, in the PCB mounting plane |
| Minimum Internal Gap (Internal Clearance) | | 25.5 | µm min | Minimum distance through insulation |
| Tracking Resistance (Comparative Tracking Index) | CTI | >400 | V | DIN IEC 112/VDE 0303 Part 1 |
| Material Group | | II | | Material Group (DIN VDE 0110, 1/89, Table 1) |

Table 10. RW-16 Wide Body [SOIC_W] Package

| Parameter | Symbol | Value | Unit | Test Conditions/Comments |
|---|---------|-------|--------|--|
| Rated Dielectric Insulation Voltage | | 3750 | V rms | 1-minute duration |
| Minimum External Air Gap (Clearance) | L (I01) | 7.8 | mm min | Measured from input terminals to output terminals, shortest distance through air |
| Minimum External Tracking (Creepage) | L (I02) | 7.8 | mm min | Measured from input terminals to output terminals, shortest distance path along body |
| Minimum Clearance in the Plane of the Printed Circuit Board (PCB Clearance) | L (PCB) | 8.3 | mm min | Measured from input terminals to output terminals, shortest distance through air, line of sight, in the PCB mounting plane |
| Minimum Internal Gap (Internal Clearance) | | 25.5 | µm min | Minimum distance through insulation |
| Tracking Resistance (Comparative Tracking Index) | CTI | >400 | V | DIN IEC 112/VDE 0303 Part 1 |
| Material Group | | II | | Material Group (DIN VDE 0110, 1/89, Table 1) |

PACKAGE CHARACTERISTICS**Table 11.**

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions/Comments |
|--|------------------|-----|------------------|-----|------|---|
| Resistance (Input to Output) ¹ | R _{I-O} | | 10 ¹³ | | Ω | |
| Capacitance (Input to Output) ¹ | C _{I-O} | | 2.2 | | pF | f = 1 MHz |
| Input Capacitance ² | C _I | | 4.0 | | pF | |
| IC Junction to Ambient Thermal Resistance | | | | | | |
| R-16 Narrow Body [SOIC_N] Package | θ _{JA} | | 76 | | °C/W | Thermocouple located at center of package underside |
| RW-16 Wide Body [SOIC_W] Package | θ _{JA} | | 45 | | °C/W | Thermocouple located at center of package underside |

¹ The device is considered a 2-terminal device: Pin 1 through Pin 8 are shorted together, and Pin 9 through Pin 16 are shorted together.

² Input capacitance is from any input data pin to ground.

REGULATORY INFORMATION

See Table 18 for the SOIC_N package or Table 19 for the SOIC_N package and the Insulation Lifetime section for details regarding recommended maximum working voltages for specific cross isolation waveforms and insulation levels.

Table 12. R-16 Narrow Body [SOIC_N] Package

| UL (Pending) | CSA (Pending) | VDE (Pending) | CQC (Pending) |
|---|--|---|---|
| Recognized Under UL 1577 Component Recognition Program ¹ Single Protection, 3000 V rms Isolation Voltage Double Protection, 3000 V rms Isolation Voltage | Approved under CSA Component Acceptance Notice 5A CSA 60950-1-07+A1+A2 and IEC 60950-1, second edition, +A1+A2: Basic insulation at 400 V rms (565 V peak) Reinforced insulation at 200 V rms (283 V peak) IEC 60601-1 Edition 3.1: Basic insulation (one means of patient protection (1 MOPP)), 250 V rms (354 V peak) CSA 61010-1-12 and IEC 61010-1 third edition: Basic insulation at 300 V rms mains, 400 V rms secondary (565 V peak) Reinforced insulation at 300 V rms mains, 200 V secondary (282 V peak) | Certified according to DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 ² Reinforced insulation, V _{IORM} = 565 V peak, V _{IOSM} = 6000 V peak Basic insulation, V _{IORM} = 565 V peak, V _{IOSM} = 10 kV peak | Certified under CQC11-471543-2012 GB4943.1-2011: Basic insulation at 770 V rms (1089 V peak) Reinforced insulation at 385 V rms (545 V peak) |
| File E214100 | File 205078 | File 2471900-4880-0001 | File (pending) |

¹ In accordance with UL 1577, each [ADuM140D/ADuM140E/ADuM141D/ADuM141E/ADuM142D/ADuM142E](#) in the R-16 narrow body [SOIC_N] package is proof tested by applying an insulation test voltage ≥ 3600 V rms for 1 sec.

² In accordance with DIN V VDE V 0884-10, each [ADuM140D/ADuM140E/ADuM141D/ADuM141E/ADuM142D/ADuM142E](#) in the R-16 narrow body [SOIC_N] package is proof tested by applying an insulation test voltage ≥ 1059 V peak for 1 sec (partial discharge detection limit = 5 pC). The * marking branded on the component designates DIN V VDE V 0884-10 approval.

Table 13. RW-16 Wide Body [SOIC_W] Package

| UL (Pending) | CSA (Pending) | VDE (Pending) | CQC (Pending) |
|---|--|---|---|
| Recognized Under UL 1577 Component Recognition Program ¹ Single Protection, 3750 V rms Isolation Voltage Double Protection, 3750 V rms Isolation Voltage | Approved under CSA Component Acceptance Notice 5A CSA 60950-1-07+A1+A2 and IEC 60950-1, second edition, +A1+A2: Basic insulation at 780 V rms (1103 V peak) Reinforced insulation at 390 V rms (552 V peak) IEC 60601-1 Edition 3.1: Basic insulation (1 means of patient protection (MOPP)), 490 V rms (693 V peak) CSA 61010-1-12 and IEC 61010-1 third edition: Basic insulation at 300 V rms mains, 780 V secondary (1103 V peak) Reinforced insulation at 300 V rms mains, 390 V secondary (552 V peak) | Certified according to DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 ² Reinforced insulation, V _{IORM} = 849 V peak, V _{IOSM} = 6000 V peak Basic insulation, V _{IORM} = 849 V peak, V _{IOSM} = 10 kV peak | Certified under CQC11-471543-2012 GB4943.1-2011: Basic insulation at 780 V rms (1103 V peak) Reinforced insulation at 390 V rms (552 V peak) |
| File E214100 | File 205078 | File 2471900-4880-0001 | File (pending) |

¹ In accordance with UL 1577, each [ADuM140D/ADuM140E/ADuM141D/ADuM141E/ADuM142D/ADuM142E](#) in the RW-16 wide body [SOIC_W] package is proof tested by applying an insulation test voltage ≥ 4500 V rms for 1 sec.

² In accordance with DIN V VDE V 0884-10, each [ADuM140D/ADuM140E/ADuM141D/ADuM141E/ADuM142D/ADuM142E](#) in the RW-16 wide body [SOIC_W] package is proof tested by applying an insulation test voltage ≥ 1592 V peak for 1 sec (partial discharge detection limit = 5 pC). The * marking branded on the component designates DIN V VDE V 0884-10 approval.

DIN V VDE V 0884-10 (VDE V 0884-10) INSULATION CHARACTERISTICS

These isolators are suitable for reinforced electrical isolation only within the safety limit data. Protective circuits ensure the maintenance of the safety data. The * marking on packages denotes DIN V VDE V 0884-10 approval.

Table 14. R-16 Narrow Body [SOIC_N] Package

| Description | Test Conditions/Comments | Symbol | Characteristic | Unit |
|--|--|-------------|--------------------------------|--------------|
| Installation Classification per DIN VDE 0110 For Rated Mains Voltage ≤ 150 V rms For Rated Mains Voltage ≤ 300 V rms For Rated Mains Voltage ≤ 600 V rms | | | I to IV I to IV I to III | |
| Climatic Classification | | | 40/125/21 | |
| Pollution Degree per DIN VDE 0110, Table 1 | | | 2 | |
| Maximum Working Insulation Voltage | | V_{IORM} | 565 | V peak |
| Input to Output Test Voltage, Method B1 | $V_{IORM} \times 1.875 = V_{pd(m)}$, 100% production test, $t_{ini} = t_m = 1$ sec, partial discharge < 5 pC | $V_{pd(m)}$ | 1059 | V peak |
| Input to Output Test Voltage, Method A | | $V_{pd(m)}$ | | |
| After Environmental Tests Subgroup 1 | $V_{IORM} \times 1.5 = V_{pd(m)}$, $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge < 5 pC | | 848 | V peak |
| After Input and/or Safety Test Subgroup 2 and Subgroup 3 | $V_{IORM} \times 1.2 = V_{pd(m)}$, $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge < 5 pC | | 678 | V peak |
| Highest Allowable Overvoltage | | V_{IOTM} | 4200 | V peak |
| Surge Isolation Voltage Basic | $V_{peak} = 10$ kV, 1.2 μ s rise time, 50 μ s, 50% fall time | V_{IOSM} | 10000 | V peak |
| Surge Isolation Voltage Reinforced | $V_{peak} = 10$ kV, 1.2 μ s rise time, 50 μ s, 50% fall time | V_{IOSM} | 6000 | V peak |
| Safety Limiting Values | Maximum value allowed in the event of a failure (see Figure 4) | | | |
| Maximum Junction Temperature | | T_S | 150 | $^{\circ}$ C |
| Total Power Dissipation at 25 $^{\circ}$ C | | P_S | 1.64 | W |
| Insulation Resistance at T_S | $V_{IO} = 500$ V | R_S | $>10^9$ | Ω |

Table 15. RW-16 Wide Body [SOIC_W] Package

| Description | Test Conditions/Comments | Symbol | Characteristic | Unit |
|---|--|-------------|-------------------------------|--------|
| Installation Classification per DIN VDE 0110 For Rated Mains Voltage ≤ 150 V rms For Rated Mains Voltage ≤ 300 V rms For Rated Mains Voltage ≤ 600 V rms | | | I to IV I to IV I to IV | |
| Climatic Classification | | | 40/125/21 | |
| Pollution Degree per DIN VDE 0110, Table 1 | | | 2 | |
| Maximum Working Insulation Voltage | | V_{IORM} | 849 | V peak |
| Input to Output Test Voltage, Method B1 | $V_{IORM} \times 1.875 = V_{pd(m)}$, 100% production test, $t_{ini} = t_m = 1$ sec, partial discharge < 5 pC | $V_{pd(m)}$ | 1592 | V peak |
| Input to Output Test Voltage, Method A After Environmental Tests Subgroup 1 | $V_{IORM} \times 1.5 = V_{pd(m)}$, $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge < 5 pC | $V_{pd(m)}$ | 1274 | V peak |
| After Input and/or Safety Test Subgroup 2 and Subgroup 3 | $V_{IORM} \times 1.2 = V_{pd(m)}$, $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge < 5 pC | | 1019 | V peak |
| Highest Allowable Overvoltage | | V_{IOTM} | 7000 | V peak |
| Surge Isolation Voltage Basic | V peak = 12.8 kV, 1.2 μs rise time, 50 μs, 50% fall time | V_{IOSM} | 12000 | V peak |
| Surge Isolation Voltage Reinforced | V peak = 12.8 kV, 1.2 μs rise time, 50 μs, 50% fall time | V_{IOSM} | 8000 | V peak |
| Safety Limiting Values | Maximum value allowed in the event of a failure (see Figure 5) | | | |
| Maximum Junction Temperature | | T_S | 150 | °C |
| Total Power Dissipation at 25°C | | P_S | 2.78 | W |
| Insulation Resistance at T_S | $V_{IO} = 500$ V | R_S | >10 ⁹ | Ω |

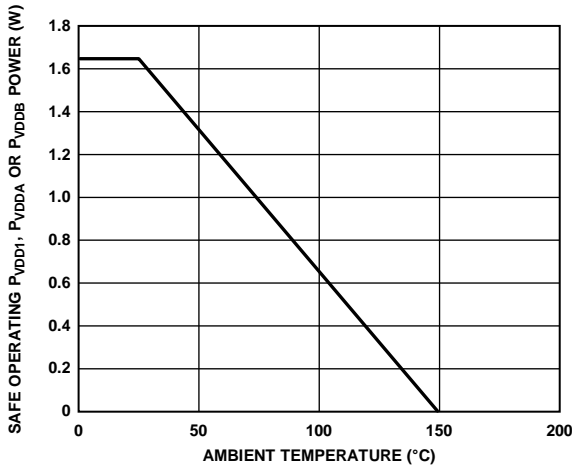


Figure 4. Thermal Derating Curve for R-16 Narrow Body [SOIC_N] Package, Dependence of Safety Limiting Values with Ambient Temperature per DIN V VDE V 0884-10

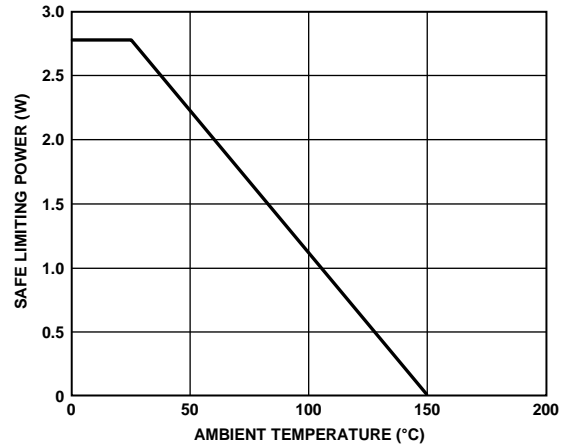


Figure 5. Thermal Derating Curve for RW-16 Wide Body [SOIC_W] Package, Dependence of Safety Limiting Values with Ambient Temperature per DIN V VDE V 0884-10

RECOMMENDED OPERATING CONDITIONS

Table 16.

| Parameter | Symbol | Rating |
|----------------------------------|--------------------|-----------------|
| Operating Temperature | T_A | -40°C to +125°C |
| Supply Voltages | V_{DD1}, V_{DD2} | 1.7 V to 5.5 V |
| Input Signal Rise and Fall Times | | 1.0 ms |

ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 17.

| Parameter | Rating |
|--|--|
| Storage Temperature (T_{ST}) Range | -65°C to $+150^\circ\text{C}$ |
| Ambient Operating Temperature (T_A) Range | -40°C to $+125^\circ\text{C}$ |
| Supply Voltages (V_{DD1} , V_{DD2}) | -0.5 V to $+7.0\text{ V}$ |
| Input Voltages (V_{IA} , V_{IB} , V_{IC} , V_{ID} , V_{E1} , V_{E2} , DISABLE_1 , DISABLE_2) | -0.5 V to $V_{DD1}^1 + 0.5\text{ V}$ |
| Output Voltages (V_{OA} , V_{OB} , V_{OC} , V_{OD}) | -0.5 V to $V_{DDO}^2 + 0.5\text{ V}$ |
| Average Output Current per Pin ³ | |
| Side 1 Output Current (I_{O1}) | -10 mA to $+10\text{ mA}$ |
| Side 2 Output Current (I_{O2}) | -10 mA to $+10\text{ mA}$ |
| Common-Mode Transients ⁴ | $-150\text{ kV}/\mu\text{s}$ to $+150\text{ kV}/\mu\text{s}$ |

¹ V_{DD1} is the input side supply voltage.

² V_{DDO} is the output side supply voltage.

³ See Figure 4 for the R-16 narrow body [SOIC_N] package or Figure 5 for the RW-16 wide body [SOIC_W] package for the maximum rated current values at various temperatures.

⁴ Refers to the common-mode transients across the insulation barrier. Common-mode transients exceeding the absolute maximum ratings may cause latch-up or permanent damage.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

Table 18. Maximum Continuous Working Voltage R-16 Narrow Body [SOIC_N] Package¹

| Parameter | Rating | Constraint ² |
|-----------------------|------------|---|
| AC Voltage | | |
| Bipolar Waveform | | |
| Basic Insulation | 789 V peak | Lifetime limited by package creepage maximum approved working voltage per IEC 60950-1 |
| Reinforced Insulation | 403 V peak | Lifetime limited by package creepage maximum approved working voltage per IEC 60950-1 |
| Unipolar Waveform | | |
| Basic Insulation | 909 V peak | Lifetime limited by package creepage maximum approved working voltage per IEC 60950-1 |
| Reinforced Insulation | 469 V peak | Lifetime limited by package creepage maximum approved working voltage per IEC 60950-1 |
| DC Voltage | | |
| Basic Insulation | 558 V peak | Lifetime limited by package creepage maximum approved working voltage per IEC 60950-1 |
| Reinforced Insulation | 285V peak | Lifetime limited by package creepage maximum approved working voltage per IEC 60950-1 |

¹ Refers to the continuous voltage magnitude imposed across the isolation barrier. See the Insulation Lifetime section for more details.

² Insulation lifetime for the specified test condition is greater than 50 years.

Table 19. Maximum Continuous Working Voltage RW-16 Wide Body [SOIC_W] Package¹

| Parameter | Rating | Constraint ² |
|-----------------------|-------------|---|
| AC Voltage | | |
| Bipolar Waveform | | |
| Basic Insulation | 849 V peak | 50-year minimum insulation lifetime |
| Reinforced Insulation | 768 V peak | Lifetime limited by package creepage maximum approved working voltage per IEC 60950-1 |
| Unipolar Waveform | | |
| Basic Insulation | 1698 V peak | 50-year minimum insulation lifetime |
| Reinforced Insulation | 885 V peak | Lifetime limited by package creepage maximum approved working voltage per IEC 60950-1 |
| DC Voltage | | |
| Basic Insulation | 1092 V peak | Lifetime limited by package creepage maximum approved working voltage per IEC 60950-1 |
| Reinforced Insulation | 543 V peak | Lifetime limited by package creepage maximum approved working voltage per IEC 60950-1 |

¹ Refers to the continuous voltage magnitude imposed across the isolation barrier. See the Insulation Lifetime section for more details.

² Insulation lifetime for the specified test condition is greater than 50 years.

TRUTH TABLES

Table 20. ADuM140D/ADuM141D/ADuM142D Truth Table (Positive Logic)

| V _{ix} Input ^{1, 2} | V _{DISABLEx} Input ^{1, 2} | V _{DDI} State ² | V _{DDO} State ² | Default Low (D0), V _{Ox} Output ^{1, 2, 3} | Default High (D1), V _{Ox} Output ^{1, 2, 3} | Test Conditions/Comments |
|---------------------------------------|---|-------------------------------------|-------------------------------------|--|---|-----------------------------------|
| L | L or NC | Powered | Powered | L | L | Normal operation |
| H | L or NC | Powered | Powered | H | H | Normal operation |
| X | H | Powered | Powered | L | H | Inputs disabled, fail-safe output |
| X ⁴ | X ⁴ | Unpowered | Powered | L | H | Fail-safe output |
| X ⁴ | X ⁴ | Powered | Unpowered | Indeterminate | Indeterminate | |

¹ L means low, H means high, X means don't care, and NC means not connected.

² V_{ix} and V_{Ox} refer to the input and output signals of a given channel (A, B, C, or D). V_{DISABLEx} refers to the input disable signal on the same side as the V_{ix} inputs. V_{DDI} and V_{DDO} refer to the supply voltages on the input and output sides of the given channel, respectively.

³ D0 is the ADuM140D0/ADuM141D0/ADuM142D0 models, and D1 is the ADuM140D1/ADuM141D1/ADuM142D1 models. See the Ordering Guide section.

⁴ Input pins (V_{ix}, DISABLE_{E1}, and DISABLE_{E2}) on the same side as an unpowered supply must be in a low state to avoid powering the device through its ESD protection circuitry.

Table 21. ADuM140E/ADuM141E/ADuM142E Truth Table (Positive Logic)

| V _{ix} Input ^{1, 2} | V _{Ex} Input ^{1, 2} | V _{DDI} State ² | V _{DDO} State ² | Default Low (E0), V _{Ox} Output ^{1, 2, 3} | Default High (E1), V _{Ox} Output ^{1, 2, 3} | Test Conditions/Comments |
|---------------------------------------|---------------------------------------|-------------------------------------|-------------------------------------|--|---|--------------------------|
| L | H or NC | Powered | Powered | L | L | Normal operation |
| H | H or NC | Powered | Powered | H | H | Normal operation |
| X | L | Powered | Powered | Z | Z | Outputs disabled |
| L | H or NC | Unpowered | Powered | L | H | Fail-safe output |
| X ⁴ | L ⁴ | Unpowered | Powered | Z | Z | Outputs disabled |
| X ⁴ | X ⁴ | Powered | Unpowered | Indeterminate | Indeterminate | |

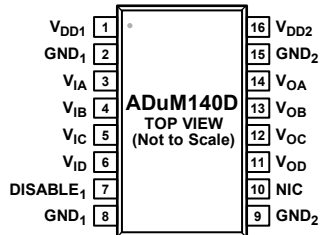
¹ L means low, H means high, X means don't care, NC means not connected, and Z means high impedance.

² V_{ix} and V_{Ox} refer to the input and output signals of a given channel (A, B, C, or D). V_{Ex} refers to the output enable signal on the same side as the V_{Ox} outputs. V_{DDI} and V_{DDO} refer to the supply voltages on the input and output sides of the given channel, respectively.

³ E0 is the ADuM140E0/ADuM141E0/ADuM142E0 models, and E1 is the ADuM140E1/ADuM141E1/ADuM142E1 models. See the Ordering Guide section.

⁴ Input pins (V_{ix}, V_{E1}, and V_{E2}) on the same side as an unpowered supply must be in a low state to avoid powering the device through its ESD protection circuitry.

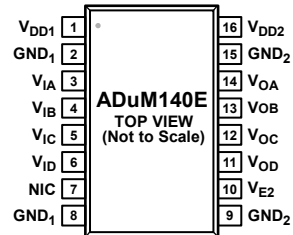
PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS



NOTES
1. NIC = NO INTERNAL CONNECTION. LEAVE THIS PIN FLOATING.

13119-004

Figure 6. ADuM140D Pin Configuration



NOTES
1. NIC = NO INTERNAL CONNECTION. LEAVE THIS PIN FLOATING.

13119-005

Figure 7. ADuM140E Pin Configuration

Table 22. Pin Function Descriptions

| Pin No. ¹ | | Mnemonic | Description |
|----------------------|----------------|----------------------|---|
| ADuM140D | ADuM140E | | |
| 1 | 1 | V _{DD1} | Supply Voltage for Isolator Side 1. |
| 2, 8 | 2, 8 | GND ₁ | Ground Reference for Isolator Side 1. |
| 3 | 3 | V _{IA} | Logic Input A. |
| 4 | 4 | V _{IB} | Logic Input B. |
| 5 | 5 | V _{IC} | Logic Input C. |
| 6 | 6 | V _{ID} | Logic Input D. |
| 7 | Not applicable | DISABLE ₁ | Input Disable 1. This pin disables the isolator inputs. Outputs take on the logic state determined by the fail-safe option shown in the Ordering Guide. |
| 9, 15 | 9, 15 | GND ₂ | Ground Reference for Isolator Side 2. |
| 10 | 7 | NIC | No Internal Connection. Leave this pin floating. |
| Not applicable | 10 | V _{E2} | Output Enable 2. Active high logic input. When V _{E2} is high or disconnected, the V _{OA} , V _{OB} , V _{OC} , and V _{OD} outputs are enabled. When V _{E2} is low, the V _{OA} , V _{OB} , V _{OC} , and V _{OD} outputs are disabled to the high-Z state. |
| 11 | 11 | V _{OD} | Logic Output D. |
| 12 | 12 | V _{OC} | Logic Output C. |
| 13 | 13 | V _{OB} | Logic Output B. |
| 14 | 14 | V _{OA} | Logic Output A. |
| 16 | 16 | V _{DD2} | Supply Voltage for Isolator Side 2. |

¹ Reference the [AN-1109](#) Application Note for specific layout guidelines.

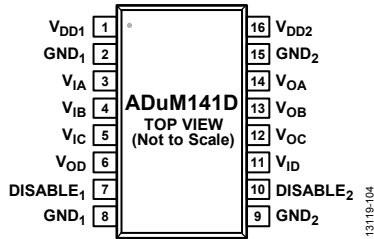


Figure 8. ADuM141D Pin Configuration

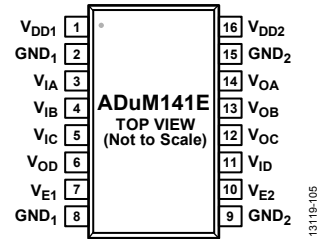


Figure 9. ADuM141E Pin Configuration

Table 23. Pin Function Descriptions

| Pin No. ¹ | | Mnemonic | Description |
|----------------------|----------------|----------------------|---|
| ADuM141D | ADuM141E | | |
| 1 | 1 | V _{DD1} | Supply Voltage for Isolator Side 1. |
| 2, 8 | 2, 8 | GND ₁ | Ground Reference for Isolator Side 1. |
| 3 | 3 | V _{IA} | Logic Input A. |
| 4 | 4 | V _{IB} | Logic Input B. |
| 5 | 5 | V _{IC} | Logic Input C. |
| 6 | 6 | V _{OD} | Logic Output D. |
| 7 | Not applicable | DISABLE ₁ | Input Disable 1. This pin disables the isolator inputs. Outputs take on the logic state determined by the fail-safe option shown in the Ordering Guide. |
| Not applicable | 7 | V _{E1} | Output Enable 1. Active high logic input. When V _{E1} is high or disconnected, the V _{OD} output is enabled. When V _{E1} is low, the V _{OD} output is disabled to the high-Z state. |
| 9, 15 | 9, 15 | GND ₂ | Ground Reference for Isolator Side 2. |
| 10 | Not applicable | DISABLE ₂ | Input Disable 2. This pin disables the isolator inputs. Outputs take on the logic state determined by the fail-safe option shown in the Ordering Guide. |
| Not applicable | 10 | V _{E2} | Output Enable 2. Active high logic input. When V _{E2} is high or disconnected, the V _{OA} , V _{OB} , and V _{OC} outputs are enabled. When V _{E2} is low, the V _{OA} , V _{OB} , and V _{OC} outputs are disabled to the high-Z state. |
| 11 | 11 | V _{ID} | Logic Input D. |
| 12 | 12 | V _{OC} | Logic Output C. |
| 13 | 13 | V _{OB} | Logic Output B. |
| 14 | 14 | V _{OA} | Logic Output A. |
| 16 | 16 | V _{DD2} | Supply Voltage for Isolator Side 2. |

¹ Reference the [AN-1109](#) Application Note for specific layout guidelines.

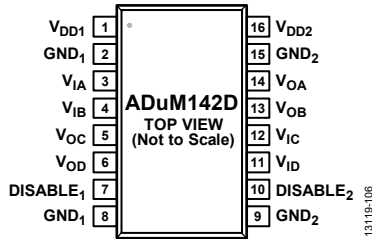


Figure 10. ADuM142D Pin Configuration

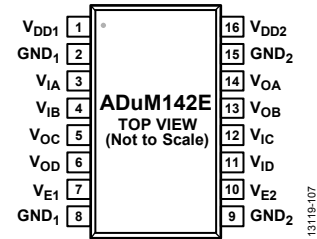


Figure 11. ADuM142E Pin Configuration

Table 24. Pin Function Descriptions

| Pin No. ¹ | | Mnemonic | Description |
|----------------------|----------------|----------------------|---|
| ADuM142D | ADuM142E | | |
| 1 | 1 | V _{DD1} | Supply Voltage for Isolator Side 1. |
| 2, 8 | 2, 8 | GND ₁ | Ground Reference for Isolator Side 1. |
| 3 | 3 | V _{IA} | Logic Input A. |
| 4 | 4 | V _{IB} | Logic Input B. |
| 5 | 5 | V _{OC} | Logic Output C. |
| 6 | 6 | V _{OD} | Logic Output D. |
| 7 | Not applicable | DISABLE ₁ | Input Disable 1. This pin disables the isolator inputs. Outputs take on the logic state determined by the fail-safe option shown in the Ordering Guide. |
| Not applicable | 7 | V _{E1} | Output Enable 1. Active high logic input. When V _{E1} is high or disconnected, the V _{OC} and V _{OD} outputs are enabled. When V _{E1} is low, the V _{OC} and V _{OD} outputs are disabled to the high-Z state. |
| 9, 15 | 9, 15 | GND ₂ | Ground Reference for Isolator Side 2. |
| 10 | Not applicable | DISABLE ₂ | Input Disable 2. This pin disables the isolator inputs. Outputs take on the logic state determined by the fail-safe option shown in the Ordering Guide. |
| Not applicable | 10 | V _{E2} | Output Enable 2. Active high logic input. When V _{E2} is high or disconnected, the V _{OA} and V _{OB} outputs are enabled. When V _{E2} is low, the V _{OA} and V _{OB} outputs are disabled to the high-Z state. |
| 11 | 11 | V _{ID} | Logic Input D. |
| 12 | 12 | V _{IC} | Logic Input C. |
| 13 | 13 | V _{OB} | Logic Output B. |
| 14 | 14 | V _{OA} | Logic Output A. |
| 16 | 16 | V _{DD2} | Supply Voltage for Isolator Side 2. |

¹ Reference the AN-1109 Application Note for specific layout guidelines.

TYPICAL PERFORMANCE CHARACTERISTICS

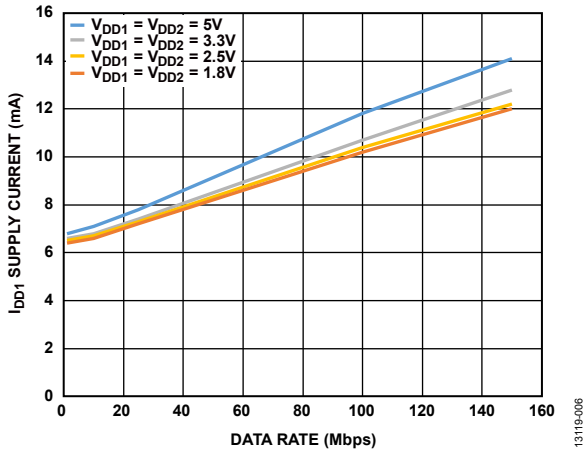


Figure 12. ADuM140D/ADuM140E I_{DD1} Supply Current vs. Data Rate at Various Voltages

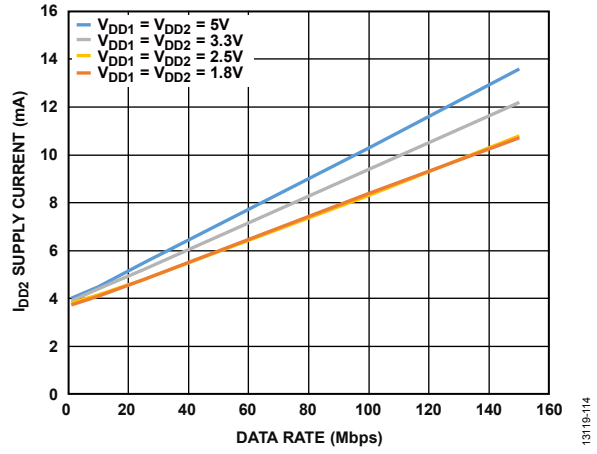


Figure 15. ADuM141D/ADuM141E I_{DD2} Supply Current vs. Data Rate at Various Voltages

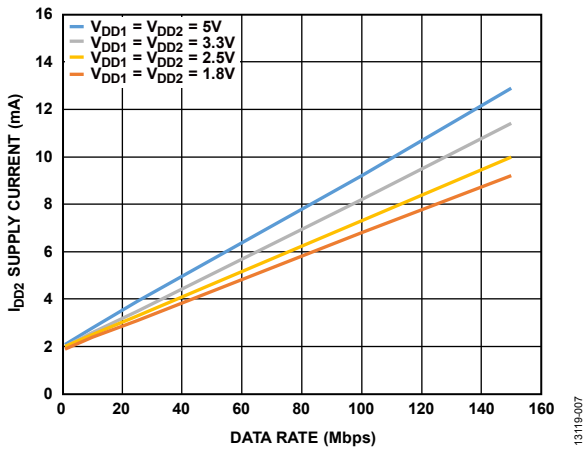


Figure 13. ADuM140D/ADuM140E I_{DD2} Supply Current vs. Data Rate at Various Voltages

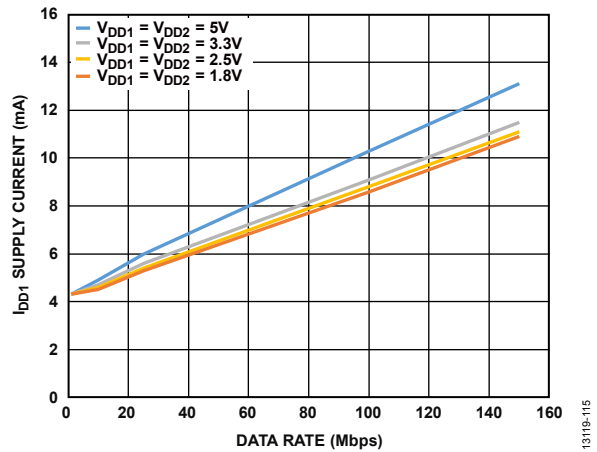


Figure 16. ADuM142D/ADuM142E I_{DD1} Supply Current vs. Data Rate at Various Voltages

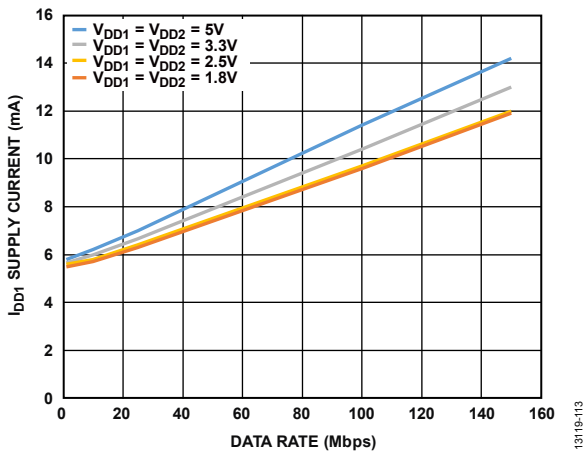


Figure 14. ADuM141D/ADuM141E I_{DD1} Supply Current vs. Data Rate at Various Voltages

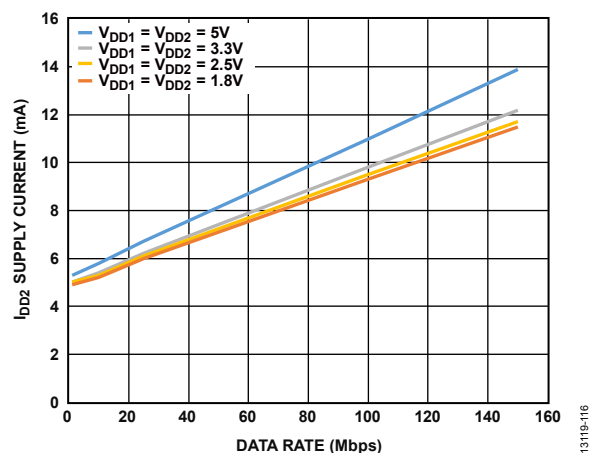


Figure 17. ADuM142D/ADuM142E I_{DD2} Supply Current vs. Data Rate at Various Voltages

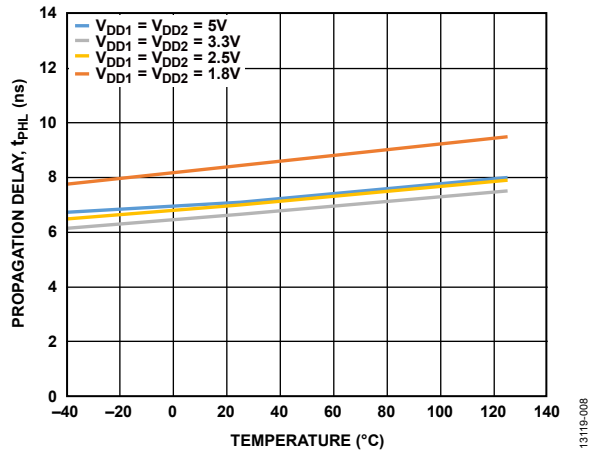


Figure 18. Propagation Delay, t_{PLH} vs. Temperature at Various Voltages

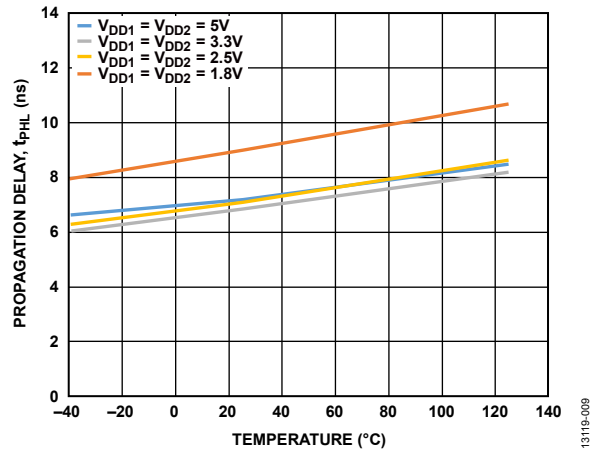


Figure 19. Propagation Delay, t_{PHL} vs. Temperature at Various Voltages

APPLICATIONS INFORMATION

OVERVIEW

The ADuM140D/ADuM140E/ADuM141D/ADuM141E/ADuM142D/ADuM142E use a high frequency carrier to transmit data across the isolation barrier using iCoupler chip scale transformer coils separated by layers of polyimide isolation. Using an on/off keying (OOK) technique and the differential architecture shown in Figure 21 and Figure 22, the ADuM140D/ADuM140E/ADuM141D/ADuM141E/ADuM142D/ADuM142E have very low propagation delay and high speed. Internal regulators and input/output design techniques allow logic and supply voltages over a wide range from 1.7 V to 5.5 V, offering voltage translation of 1.8 V, 2.5 V, 3.3 V, and 5 V logic. The architecture is designed for high common-mode transient immunity and high immunity to electrical noise and magnetic interference. Radiated emissions are minimized with a spread spectrum OOK carrier and other techniques.

Figure 21 illustrates the waveforms for models of the ADuM140D/ADuM140E/ADuM141D/ADuM141E/ADuM142D/ADuM142E that have the condition of the fail-safe output state equal to low, where the carrier waveform is off when the input state is low. If the input side is off or not operating, the low fail-safe output state (ADuM140D0/ADuM140E0/ADuM141D0/ADuM141E0/ADuM142D0/ADuM142E0) sets the output to low. For the ADuM140D/ADuM140E/ADuM141D/ADuM141E/ADuM142D/ADuM142E that have a high fail-safe output state, Figure 22 illustrates the conditions where the carrier waveform is off when the input state is high. When the input side is off or not operating, the fail-safe output state of high (ADuM140D1/ADuM140E1/ADuM141D1/ADuM141E1/ADuM142D1/ADuM142E1) sets the output to high. See the Ordering Guide for the model numbers that have the fail-safe output state of low or the fail-safe output state of high.

PRINTED CIRCUIT BOARD (PCB) LAYOUT

The ADuM140D/ADuM140E/ADuM141D/ADuM141E/ADuM142D/ADuM142E digital isolators require no external interface circuitry for the logic interfaces. Power supply bypassing is strongly recommended at the input and output supply pins (see Figure 20). Bypass capacitors are most conveniently connected between Pin 1 and Pin 2 for V_{DD1} and between Pin 15 and Pin 16 for V_{DD2} . The recommended bypass capacitor value is between 0.01 μ F and 0.1 μ F. The total lead length between both ends of the capacitor and the input power supply pin must not exceed 10 mm. Bypassing between Pin 1 and Pin 8 and between Pin 9 and Pin 16 must also be considered, unless the ground pair on each package side is connected close to the package.

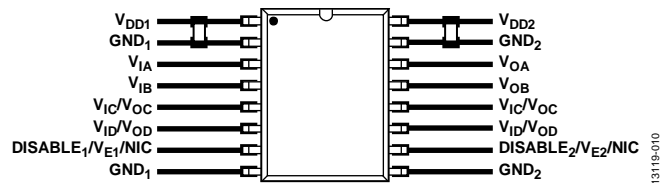


Figure 20. Recommended Printed Circuit Board Layout

In applications involving high common-mode transients, ensure that board coupling across the isolation barrier is minimized. Furthermore, design the board layout such that any coupling that does occur equally affects all pins on a given component side. Failure to ensure this can cause voltage differentials between pins exceeding the Absolute Maximum Ratings of the device, thereby leading to latch-up or permanent damage.

See the AN-1109 Application Note for board layout guidelines.

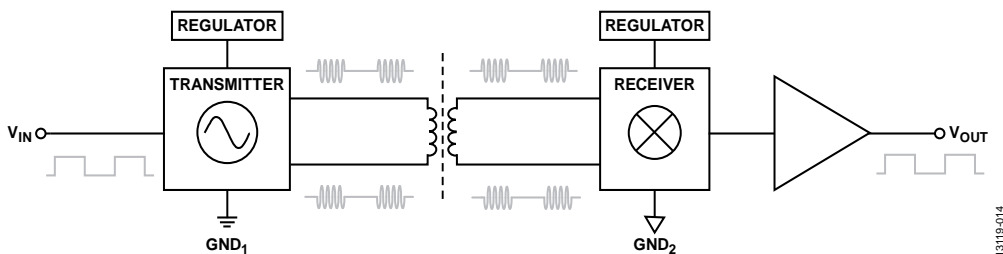


Figure 21. Operational Block Diagram of a Single Channel with a Low Fail-Safe Output State

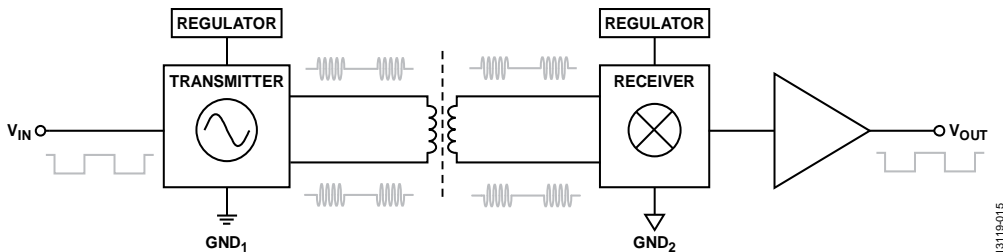


Figure 22. Operational Block Diagram of a Single Channel with a High Fail-Safe Output State

PROPAGATION DELAY RELATED PARAMETERS

Propagation delay is a parameter that describes the time required for a logic signal to propagate through a component. The propagation delay to a Logic 0 output may differ from the propagation delay to a Logic 1 output.

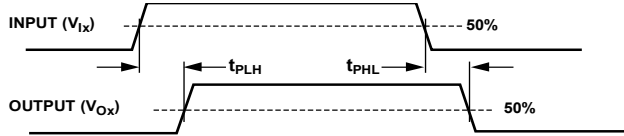


Figure 23. Propagation Delay Parameters

Pulse width distortion is the maximum difference between these two propagation delay values and is an indication of how accurately the timing of the input signal is preserved.

Channel matching is the maximum amount the propagation delay differs between channels within a single [ADuM140D/ADuM140E/ADuM141D/ADuM141E/ADuM142D/ADuM142E](#) component.

Propagation delay skew is the maximum amount the propagation delay that differs between multiple [ADuM140D/ADuM140E/ADuM141D/ADuM141E/ADuM142D/ADuM142E](#) components operating under the same conditions.

JITTER MEASUREMENT

Figure 24 shows the eye diagram for the [ADuM140D/ADuM140E/ADuM141D/ADuM141E/ADuM142D/ADuM142E](#). The measurement was taken using an Agilent 81110A pulse pattern generator at 150 Mbps with pseudorandom bit sequences (PRBS) $2(n - 1)$, $n = 14$, for 5 V supplies. Jitter was measured with the Tektronix Model 5104B oscilloscope, 1 GHz, 10 GSPS with the DPOJET jitter and eye diagram analysis tools. The result shows a typical measurement on the [ADuM140D/ADuM140E/ADuM141D/ADuM141E/ADuM142D/ADuM142E](#) with 490 ps p-p jitter.

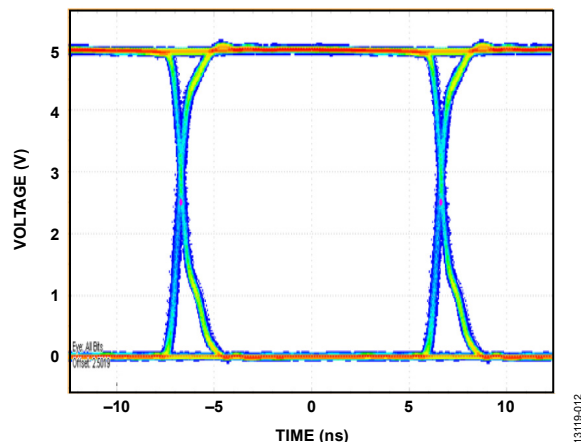


Figure 24. [ADuM140D/ADuM140E/ADuM141D/ADuM141E/ADuM142D/ADuM142E](#) Eye Diagram

INSULATION LIFETIME

All insulation structures eventually break down when subjected to voltage stress over a sufficiently long period. The rate of insulation degradation is dependent on the characteristics of the voltage waveform applied across the insulation as well as on the materials and material interfaces.

The two types of insulation degradation of primary interest are breakdown along surfaces exposed to the air and insulation wear out. Surface breakdown is the phenomenon of surface tracking and the primary determinant of surface creepage requirements in system level standards. Insulation wear out is the phenomenon where charge injection or displacement currents inside the insulation material cause long-term insulation degradation.

Surface Tracking

Surface tracking is addressed in electrical safety standards by setting a minimum surface creepage based on the working voltage, the environmental conditions, and the properties of the insulation material. Safety agencies perform characterization testing on the surface insulation of components that allows the components to be categorized in different material groups. Lower material group ratings are more resistant to surface tracking and, therefore, can provide adequate lifetime with smaller creepage. The minimum creepage for a given working voltage and material group is in each system level standard and is based on the total rms voltage across the isolation, pollution degree, and material group. The material group and creepage for the [ADuM140D/ADuM140E/ADuM141D/ADuM141E/ADuM142D/ADuM142E](#) isolators are presented in Table 9 for the R-16 narrow body [SOIC_N] package or Table 10 for the RW-16 wide body [SOIC_W] package.

Insulation Wear Out

The lifetime of insulation caused by wear out is determined by its thickness, material properties, and the voltage stress applied. It is important to verify that the product lifetime is adequate at the application working voltage. The working voltage supported by an isolator for wear out may not be the same as the working voltage supported for tracking. The working voltage applicable to tracking is specified in most standards.

Testing and modeling have shown that the primary driver of long-term degradation is displacement current in the polyimide insulation causing incremental damage. The stress on the insulation can be broken down into broad categories, such as dc stress, which causes very little wear out because there is no displacement current, and an ac component time varying voltage stress, which causes wear out.

The ratings in certification documents are usually based on 60 Hz sinusoidal stress because this reflects isolation from line voltage. However, many practical applications have combinations of 60 Hz ac and dc across the barrier as shown in Equation 1. Because only the ac portion of the stress causes wear out, the equation can be rearranged to solve for the ac rms voltage, as is shown in Equation 2. For insulation wear out with the polyimide materials used in these products, the ac rms voltage determines the product lifetime.

$$V_{RMS} = \sqrt{V_{AC\ RMS}^2 + V_{DC}^2} \tag{1}$$

or

$$V_{AC\ RMS} = \sqrt{V_{RMS}^2 - V_{DC}^2} \tag{2}$$

where:

$V_{AC\ RMS}$ is the time varying portion of the working voltage.

V_{RMS} is the total rms working voltage.

V_{DC} is the dc offset of the working voltage.

Calculation and Use of Parameters Example

The following example frequently arises in power conversion applications. Assume that the line voltage on one side of the isolation is 240 V ac rms and a 400 V dc bus voltage is present on the other side of the isolation barrier. The isolator material is polyimide. To establish the critical voltages in determining the creepage, clearance and lifetime of a device, see Figure 25 and the following equations.

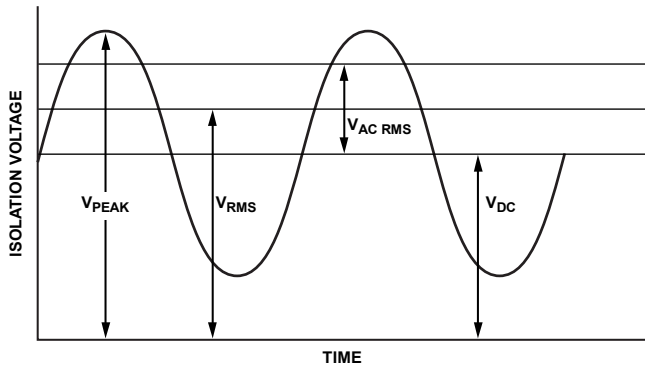


Figure 25. Critical Voltage Example

13119-013

The working voltage across the barrier from Equation 1 is

$$V_{RMS} = \sqrt{V_{AC\ RMS}^2 + V_{DC}^2}$$

$$V_{RMS} = \sqrt{240^2 + 400^2}$$

$$V_{RMS} = 466\text{ V}$$

This V_{RMS} value is the working voltage used together with the material group and pollution degree when looking up the creepage required by a system standard.

To determine if the lifetime is adequate, obtain the time varying portion of the working voltage. To obtain the ac rms voltage, use Equation 2.

$$V_{AC\ RMS} = \sqrt{V_{RMS}^2 - V_{DC}^2}$$

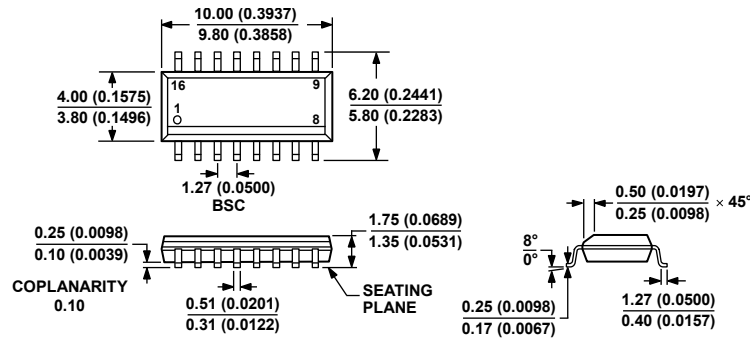
$$V_{AC\ RMS} = \sqrt{466^2 - 400^2}$$

$$V_{AC\ RMS} = 240\text{ V rms}$$

In this case, the ac rms voltage is simply the line voltage of 240 V rms. This calculation is more relevant when the waveform is not sinusoidal. The value is compared to the limits for working voltage in Table 18 for the SOIC_N package or Table 19 for the SOIC_W package, for the expected lifetime, which is less than a 60 Hz sine wave, and it is well within the limit for a 50-year service life.

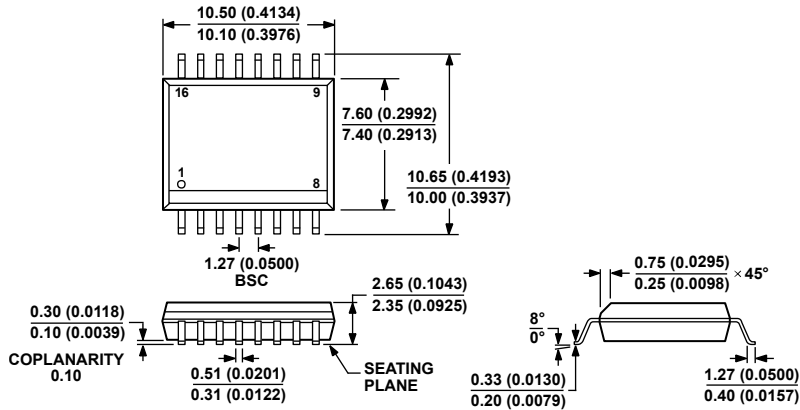
Note that the dc working voltage limit is set by the creepage of the package as specified in IEC 60664-1. This value can differ for specific system level standards.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-012-AC
 CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 26. 16-Lead Standard Small Outline Package [SOIC_N] Narrow Body (R-16)
 Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MS-013-AA
 CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 27. 16-Lead Standard Small Outline Package [SOIC_W] Wide Body (RW-16)
 Dimensions shown in millimeters and (inches)

060606-A

03-27-2007-B

ORDERING GUIDE

| Model ¹ | Temperature Range | No. of Inputs, V _{DD1} Side | No. of Inputs, V _{DD2} Side | Withstand Voltage Rating (kV rms) | Fail-Safe Output State | Input Disable | Output Enable | Package Description | Package Option |
|--------------------|-------------------|--------------------------------------|--------------------------------------|-----------------------------------|------------------------|---------------|---------------|---------------------|----------------|
| ADuM140D1BRZ | -40°C to +125°C | 4 | 0 | 3.0 | High | Yes | No | 16-Lead SOIC_N | R-16 |
| ADuM140D1BRZ-RL7 | -40°C to +125°C | 4 | 0 | 3.0 | High | Yes | No | 16-Lead SOIC_N | R-16 |
| ADuM140D0BRZ | -40°C to +125°C | 4 | 0 | 3.0 | Low | Yes | No | 16-Lead SOIC_N | R-16 |
| ADuM140D0BRZ-RL7 | -40°C to +125°C | 4 | 0 | 3.0 | Low | Yes | No | 16-Lead SOIC_N | R-16 |
| ADuM140E1BRZ | -40°C to +125°C | 4 | 0 | 3.0 | High | No | Yes | 16-Lead SOIC_N | R-16 |
| ADuM140E1BRZ-RL7 | -40°C to +125°C | 4 | 0 | 3.0 | High | No | Yes | 16-Lead SOIC_N | R-16 |
| ADuM140E0BRZ | -40°C to +125°C | 4 | 0 | 3.0 | Low | No | Yes | 16-Lead SOIC_N | R-16 |
| ADuM140E0BRZ-RL7 | -40°C to +125°C | 4 | 0 | 3.0 | Low | No | Yes | 16-Lead SOIC_N | R-16 |
| ADuM140D1BRWZ | -40°C to +125°C | 4 | 0 | 3.75 | High | Yes | No | 16-Lead SOIC_W | RW-16 |
| ADuM140D1BRWZ-RL | -40°C to +125°C | 4 | 0 | 3.75 | High | Yes | No | 16-Lead SOIC_W | RW-16 |
| ADuM140D0BRWZ | -40°C to +125°C | 4 | 0 | 3.75 | Low | Yes | No | 16-Lead SOIC_W | RW-16 |
| ADuM140D0BRWZ-RL | -40°C to +125°C | 4 | 0 | 3.75 | Low | Yes | No | 16-Lead SOIC_W | RW-16 |
| ADuM140E1BRWZ | -40°C to +125°C | 4 | 0 | 3.75 | High | No | Yes | 16-Lead SOIC_W | RW-16 |
| ADuM140E1BRWZ-RL | -40°C to +125°C | 4 | 0 | 3.75 | High | No | Yes | 16-Lead SOIC_W | RW-16 |
| ADuM140E0BRWZ | -40°C to +125°C | 4 | 0 | 3.75 | Low | No | Yes | 16-Lead SOIC_W | RW-16 |
| ADuM140E0BRWZ-RL | -40°C to +125°C | 4 | 0 | 3.75 | Low | No | Yes | 16-Lead SOIC_W | RW-16 |
| ADuM141D1BRZ | -40°C to +125°C | 3 | 1 | 3.0 | High | Yes | No | 16-Lead SOIC_N | R-16 |
| ADuM141D1BRZ-RL7 | -40°C to +125°C | 3 | 1 | 3.0 | High | Yes | No | 16-Lead SOIC_N | R-16 |
| ADuM141D0BRZ | -40°C to +125°C | 3 | 1 | 3.0 | Low | Yes | No | 16-Lead SOIC_N | R-16 |
| ADuM141D0BRZ-RL7 | -40°C to +125°C | 3 | 1 | 3.0 | Low | Yes | No | 16-Lead SOIC_N | R-16 |
| ADuM141E1BRZ | -40°C to +125°C | 3 | 1 | 3.0 | High | No | Yes | 16-Lead SOIC_N | R-16 |
| ADuM141E1BRZ-RL7 | -40°C to +125°C | 3 | 1 | 3.0 | High | No | Yes | 16-Lead SOIC_N | R-16 |
| ADuM141E0BRZ | -40°C to +125°C | 3 | 1 | 3.0 | Low | No | Yes | 16-Lead SOIC_N | R-16 |
| ADuM141E0BRZ-RL7 | -40°C to +125°C | 3 | 1 | 3.0 | Low | No | Yes | 16-Lead SOIC_N | R-16 |
| ADuM141D1BRWZ | -40°C to +125°C | 3 | 1 | 3.75 | High | Yes | No | 16-Lead SOIC_W | RW-16 |
| ADuM141D1BRWZ-RL | -40°C to +125°C | 3 | 1 | 3.75 | High | Yes | No | 16-Lead SOIC_W | RW-16 |
| ADuM141D0BRWZ | -40°C to +125°C | 3 | 1 | 3.75 | Low | Yes | No | 16-Lead SOIC_W | RW-16 |
| ADuM141D0BRWZ-RL | -40°C to +125°C | 3 | 1 | 3.75 | Low | Yes | No | 16-Lead SOIC_W | RW-16 |
| ADuM141E1BRWZ | -40°C to +125°C | 3 | 1 | 3.75 | High | No | Yes | 16-Lead SOIC_W | RW-16 |
| ADuM141E1BRWZ-RL | -40°C to +125°C | 3 | 1 | 3.75 | High | No | Yes | 16-Lead SOIC_W | RW-16 |
| ADuM141E0BRWZ | -40°C to +125°C | 3 | 1 | 3.75 | Low | No | Yes | 16-Lead SOIC_W | RW-16 |
| ADuM141E0BRWZ-RL | -40°C to +125°C | 3 | 1 | 3.75 | Low | No | Yes | 16-Lead SOIC_W | RW-16 |
| ADuM142D1BRZ | -40°C to +125°C | 2 | 2 | 3.0 | High | Yes | No | 16-Lead SOIC_N | R-16 |
| ADuM142D1BRZ-RL7 | -40°C to +125°C | 2 | 2 | 3.0 | High | Yes | No | 16-Lead SOIC_N | R-16 |
| ADuM142D0BRZ | -40°C to +125°C | 2 | 2 | 3.0 | Low | Yes | No | 16-Lead SOIC_N | R-16 |
| ADuM142D0BRZ-RL7 | -40°C to +125°C | 2 | 2 | 3.0 | Low | Yes | No | 16-Lead SOIC_N | R-16 |
| ADuM142E1BRZ | -40°C to +125°C | 2 | 2 | 3.0 | High | No | Yes | 16-Lead SOIC_N | R-16 |
| ADuM142E1BRZ-RL7 | -40°C to +125°C | 2 | 2 | 3.0 | High | No | Yes | 16-Lead SOIC_N | R-16 |
| ADuM142E0BRZ | -40°C to +125°C | 2 | 2 | 3.0 | Low | No | Yes | 16-Lead SOIC_N | R-16 |
| ADuM142E0BRZ-RL7 | -40°C to +125°C | 2 | 2 | 3.0 | Low | No | Yes | 16-Lead SOIC_N | R-16 |
| ADuM142D1BRWZ | -40°C to +125°C | 2 | 2 | 3.75 | High | Yes | No | 16-Lead SOIC_W | RW-16 |
| ADuM142D1BRWZ-RL | -40°C to +125°C | 2 | 2 | 3.75 | High | Yes | No | 16-Lead SOIC_W | RW-16 |
| ADuM142D0BRWZ | -40°C to +125°C | 2 | 2 | 3.75 | Low | Yes | No | 16-Lead SOIC_W | RW-16 |
| ADuM142D0BRWZ-RL | -40°C to +125°C | 2 | 2 | 3.75 | Low | Yes | No | 16-Lead SOIC_W | RW-16 |
| ADuM142E1BRWZ | -40°C to +125°C | 2 | 2 | 3.75 | High | No | Yes | 16-Lead SOIC_W | RW-16 |
| ADuM142E1BRWZ-RL | -40°C to +125°C | 2 | 2 | 3.75 | High | No | Yes | 16-Lead SOIC_W | RW-16 |
| ADuM142E0BRWZ | -40°C to +125°C | 2 | 2 | 3.75 | Low | No | Yes | 16-Lead SOIC_W | RW-16 |
| ADuM142E0BRWZ-RL | -40°C to +125°C | 2 | 2 | 3.75 | Low | No | Yes | 16-Lead SOIC_W | RW-16 |

¹ Z = RoHS Compliant Part.

NOTES