Product Specification | Rev. 1.1 |

G5 Silver

153 Ball - Embedded Multimedia Card

4GB - 32GB

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1 Product Summary

CAPACITY RANGE:	4GB – 32GB
FORM FACTOR:	FBGA 153 (11.5x13.0mm, 0.5mm pitch)
INTERFACE:	eMMC 5.1 Backward compatible eMMC Specification Ver.4.4, 4.41, 4.5, 5.0
BUS MODE:	High-speed eMMC protocol, Clock frequency: 0-200MHz
TRANSFER RATE	Data transfer rate: up to 52Mbyte/s (8 data lines @52 MHz) Single data rate: up to 200Mbyte/s @ 200MHz Dual data rate: up to 400Mbyte/s @ 200MHz
PERFORMANCE	Sequential read: up to 300 MB/s Sequential write: up to 60 MB/s
OPERATION VOLTAGE	VCCQ = 1.7V ~ 1.95V / 2.7V ~ 3.6V VCC = 2.7 V ~ 3.6V
OPERATING TEMPERATURE	Industrial Grade : -40°C ~ 85°C Extended : -25°C ~ 85°C
STORAGE TEMPERATURE	-55°C ~ 95°C
QUALITY	RoHS compliant **

Note: ** for detailed RoHS declaration, please contact your I'M representative.

2 Order Information

Table 1 – Part Number

Product Part Number	Density	Operation Temperature
IMC1B1A3C6A9A8**X**3A3A0000	4GB	-25°C ~ 85°C/ -40°C ~ 85°C
IMC1B1A4C6A9A8**X**3A4A0000	8GB	
IMC1B1A5C6A9A8**X**3A5A0000	16GB	
IMC1B1A6C6A9A8**X**3A6A0000	32GB	
IMC1B1A3C8A9A8**Y**3A3A0000	4GB	Auto.3 (-40°C ~ 85°C)/ Auto.2(-40°C ~ 105°C)
IMC1B1A4C8A9A8**Y**3A4A0000	8GB	
IMC1B1A5C8A9A8**Y**3A5A0000	16GB	
IMC1B1A6C8A9A8**Y**3A6A0000	32GB	

X: Temperature
E – Extended (-25°C ~ 85°C)
I – Industrial (-40°C ~ 85°C)
Y: Temperature
V – Auto. Grade3 (-40°C ~ 85°C)
A – Auto. Grade2 (-40°C ~ 105°C)

3 Product Introduction

I'M eMMC product family provides the ideal embedded storage solution for the Industrial and Medical applications, which require high performance, endurance across a wide range of operating temperatures, and good technical support. I'M eMMC integrates NAND Flash memory and a sophisticated eMMC controller inside a standard package, providing a standard interface to the host. The controller directly manages the NAND flash, implementing functions like bad block management, error handling (ECC), static and dynamic wear-leveling, IOPS optimization and read sensing. I'M eMMC supports Enhanced User Data Area feature which allows the User Data Area of eMMC to be configured for higher read/write performance, endurance and reliability.

3.1 Device Performance

Table 2 – Read/Write Performance

Device Capacity	Typical value	
	Read Sequential (MB/s)	Write Sequential (MB/s)
4GB	220	60
8GB	280	100
16GB	280	60
32GB	280	60
Notes: 1. Values given for an 8-bit bus width, running HS400 mode from I'M proprietary tool, V_{CC} =3.3V, V_{CCQ} =1.8V. 2. Performance numbers might be subject to changes without notice.		

3.2 User Density and Partition

Table 3 – User Density and Partition

Device Capacity	Partition			
	User Density	Boot 1	Boot 2	RPMB
4GB	3,909,091,328 Bytes	4096 KB	4096 KB	4096 KB
8GB	7,755,268,096 Bytes	4096 KB	4096 KB	4096 KB
16GB	15,634,268,160 Bytes	4096 KB	4096 KB	4096 KB
32GB	31,268,536,320 Bytes	4096 KB	4096 KB	4096 KB
Notes: 1. Total user density depends on device type.				

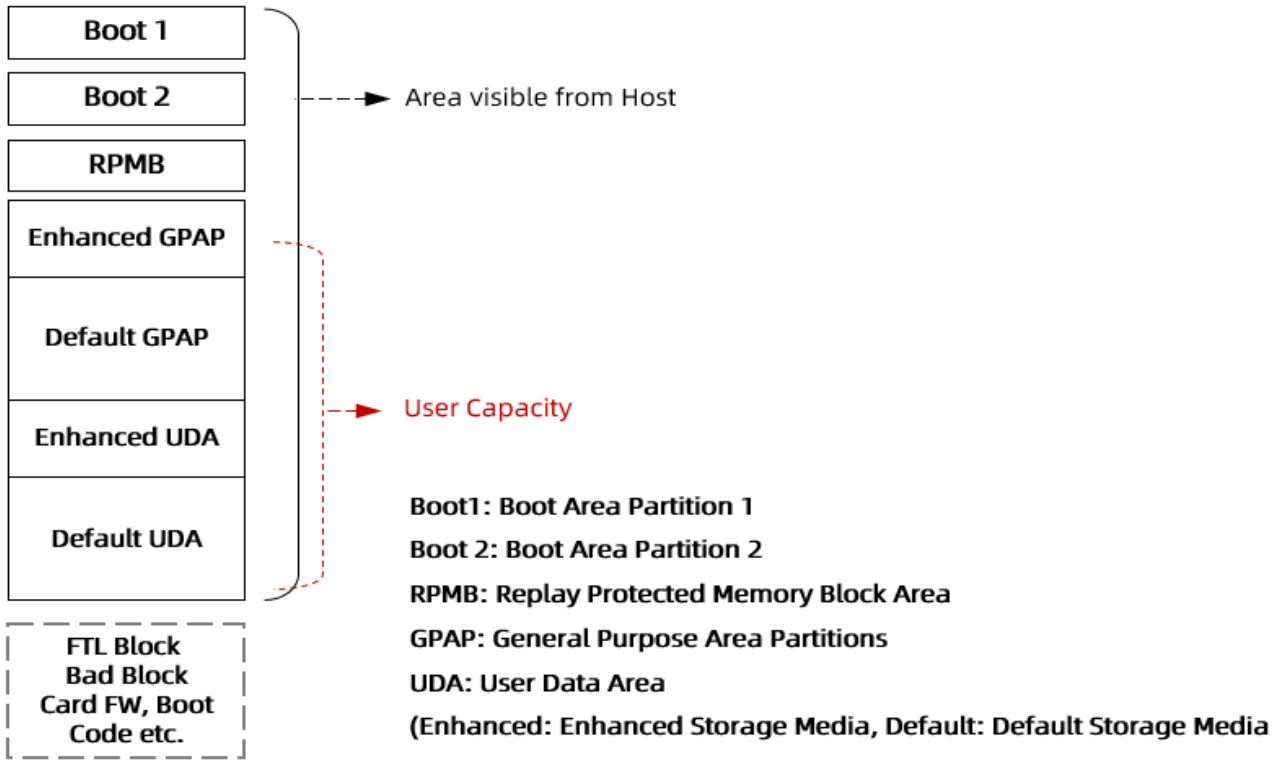


Figure 1 – User density configuration

3.3 Endurance

Table 4 – Endurance

Device Capacity	TBW (Tera Bytes)
4GB	7.8
8GB	15.5
16GB	31.3
32GB	62

3.4 Temperature

Table 5 – Temperature Range

Parameter	Grade	Range
Operating Temperature	Extended	-25~+85 °C
	Industrial	-40~+85 °C
	Auto. 2	-40~+105 °C
	Auto. 3	-40~+85 °C
Storage Temperature	All	-40~+85 °C

3.5 Power consumption

Table 6 – Power Consumption

Products	Read (mA)		Write (mA)	
Device Capacity	VCCQ (1.8V)	VCC (3.3V)	VCCQ (1.8V)	VCC (3.3V)
4GB	90	60	55	35
8GB	105	80	70	60
16GB	110	65	70	75
32GB	110	65	70	80

Note 1: Values given for an 8-bit bus width, a clock frequency of 200MHz DDR mode, V_{CC} = 3.3V±5%, V_{CCQ} =1.8V±5%
Note 2: Current numbers might be subject to changes without notice.
Note 3: The measurement for max RMS current is done as average RMS current consumption over a period of 100ms.

4 eMMC Device and System

4.1 eMMC System Overview

The eMMC specification covers the behavior of the interface and the Device controller. As part of this specification the existence of a host controller and a memory storage array are implied but the operation of these pieces is not fully specified. **I'M** eMMC Device consists of a single chip MMC controller and NAND flash memory module. The micro-controller interfaces with a host system allowing data to be written to and read from the NAND flash memory module. The controller allows the host to be independent from details of erasing and programming the flash memory.

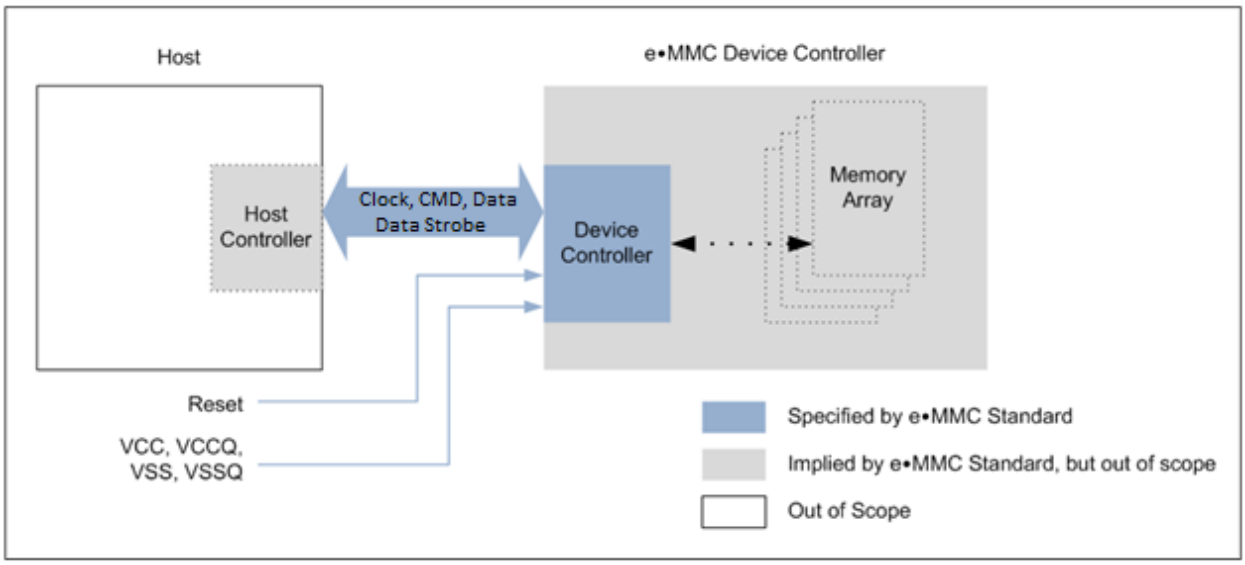


Figure 2 – eMMC System Overview

4.2 Memory Addressing

Previous implementations of the eMMC specification are following byte addressing with 32 bit field. This addressing mechanism permitted for eMMC densities up to and including 2 GB. To support larger densities the addressing mechanism was update to support sector addresses (512 Bytes sectors). The sector addresses shall be used for all devices with capacity larger than 2 GB. To determine the addressing mode use the host should read bit [30:29] in the OCR register.

4.3 eMMC Device Overview

The eMMC device transfers data via a configurable number of data bus signals. The communication signals are:

4.3.1 Clock (CLK)

Each cycle of this signal directs a one bit transfer on the command and either a one bit (1x) or a two bits transfer (2x) on all the data lines. The frequency may vary between zero and the maximum clock frequency.

4.3.2 Data Strobe(DS)

This signal is generated by the device and used for output in HS400 mode. The frequency of this signal follows the frequency of CLK. For data output each cycle of this signal directs two bits transfer(2x) on the data – one bit for positive edge and the other bit for negative edge. For CRC status response output and CMD response output (enabled only HS400 enhanced strobe mode), the CRC status is latched on the positive edge only, and don't care on the negative edge.

4.3.3 Command (CMD)

This signal is a bidirectional command channel used for Device initialization and transfer of commands. The CMD signal has two operation modes: open-drain for initialization mode, and push-pull for fast command transfer. Commands are sent from the eMMC host controller to the eMMC Device and responses are sent from the Device to the host.

4.3.4 Input/Outputs (DAT0-DAT7)

These are bidirectional data channels. The DAT signals operate in push-pull mode. Only the Device or the host is driving these signals at a time. By default, after power up or reset, only DAT0 is used for data transfer. A wider data bus can be configured for data transfer, using either DAT0-DAT3 or DAT0-DAT7, by the eMMC host controller. The eMMC Device includes internal pull-ups for data lines DAT1-DAT7. Immediately after entering the 4-bit mode, the Device disconnects the internal pull ups of lines DAT1, DAT2, and DAT3. Correspondingly, immediately after entering to the 8-bit mode the Device disconnects the internal pull-ups of lines DAT1–DAT7.

Table 7 – Communication Interface

Name	Type1	Description
CLK	I	Clock
DAT0	I/O/PP	Data
DAT1	I/O/PP	Data
DAT2	I/O/PP	Data
DAT3	I/O/PP	Data
DAT4	I/O/PP	Data
DAT5	I/O/PP	Data
DAT6	I/O/PP	Data
DAT7	I/O/PP	Data
CMD	I/O/PP/OD	Command/Response
RST_n	I	Hardware reset
VCC	S	Supply voltage for Core
VCCQ	S	Supply voltage for I/O

VSS	S	Supply voltage ground for Core
VSSQ	S	Supply voltage ground for I/O
DS	O/PP	Data strobe
Notes: 1.I: input; O: output; PP: push-pull; OD: open-drain; NC: Not connected (or logical high); S: power supply.		

Table 8 – eMMC Registers

Name	Width (Bytes)	Description	Implementation
CID	16	Device Identification number, an individual number for identification.	Mandatory
RCA	2	Relative Device Address is the Device system address, dynamically assigned by the host during initialization.	Mandatory
DSR	2	Driver Stage Register, to configure the Device's output drivers.	Optional
CSD	16	Device Specific Data, information about the Device operation conditions.	Mandatory
OCR	4	Operation Conditions Register. Used by a special broadcast command to identify the voltage type of the Device.	Mandatory
EXT_CSD	512	Extended Device Specific Data. Contains information about the Device capabilities and selected modes. Introduced in stan	Mandatory

The host may reset the device by:

- Switching the power supply off and back on. The device shall have its own power-on detection circuitry which puts the device into a defined state after the power-on Device.
- A reset signal
- By sending a special command

4.4 Bus Protocol

After a power-on reset, the host must initialize the device by a special message based on eMMC bus protocol. For more details, refer to section 5.3.1 of the JEDEC Standard Specification No.JESD84-B51.

4.5 Bus Speed Modes

eMMC defines several bus speed modes as shown in Table 8.

Table 9 – Bus Speed Mode

Mode Name	Data Rate	IO Voltage	Bus Width	Frequency	Max Data Transfer (implies x8 bus width)
Backwards Compatibility with legacy MMC card	Single	3.3/1.8V*	1, 4, 8	0-26MHz	26MB/s
High speed SDR	Single	3.3/1.8V*	4, 8	0-52MHz	52MB/s

High speed DDR	Dual	3.3/1.8V*	4, 8	0-52MHz	104MB/s
HS200	Single	1.8V	4, 8	0-200MHz	200MB/s
HS400	Dual	1.8V	8	0-200MHz	400MB/s
Note: I/O voltage 3.3V is only available for Industrial grade.					

4.5.1. HS200 Bus Speed Mode

Figure 2 shows a typical HS200 Host and Device system. The host has a clock generator, which supplies CLK to the Device. For write operations, clock and data direction are the same, write data can be transferred synchronous with CLK, regardless of transmission line delay. For read operations, clock and data direction are opposite; the read data received by Host is delayed by round-trip delay, output delay and latency of Host and Device. For reads, the Host needs to have an adjustable sampling point to reliably receive the incoming data.

The HS200 mode offers the following features:

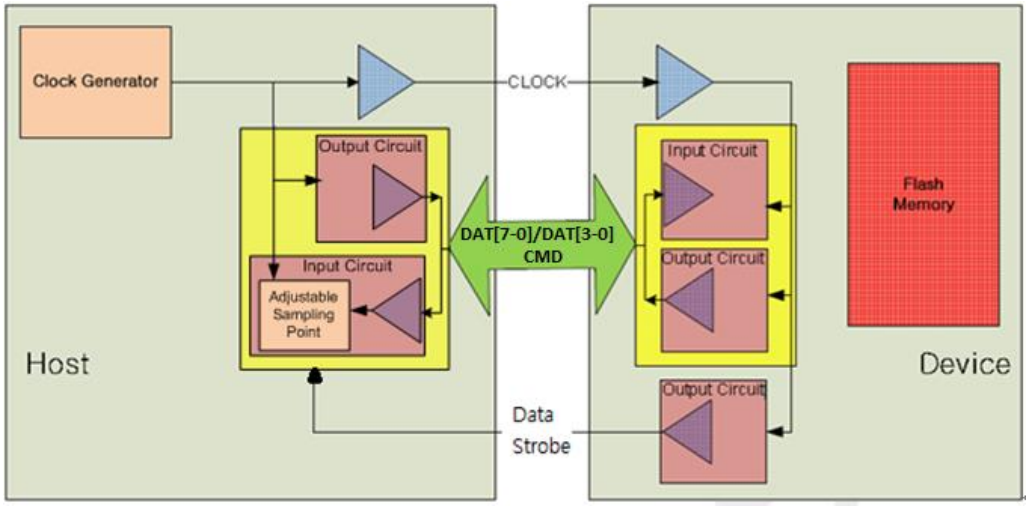
- SDR Data sampling method
- CLK frequency up to 200MHz Data rate – up to 200MB/s
- 8-bits bus width supported
- Single ended signaling with 4 selectable Drive Strength
- Signaling levels of 1.8V
- Tuning concept for Read Operations
- 

Figure 3 – HS200 Block Diagram

4.5.2. HS400 Bus Speed Mode

Figure 3 shows a typical HS400 Host and Device system. The host has a clock generator, which supplies CLK to the Device. For read operations, Data Strobe is generated by device output circuit. Host receives the data which is aligned to the edge of Data Strobe.

The HS400 mode offers the following features:

- DDR Data sampling method
- CLK frequency up to 200MHz, Data rate is – up to 400MB/s

- Only 8-bit bus width supported
- Signaling levels of 1.8V
- Support up to 5 selective Drive Strength
- Data strobe signal is toggled only for Data out and CRC response

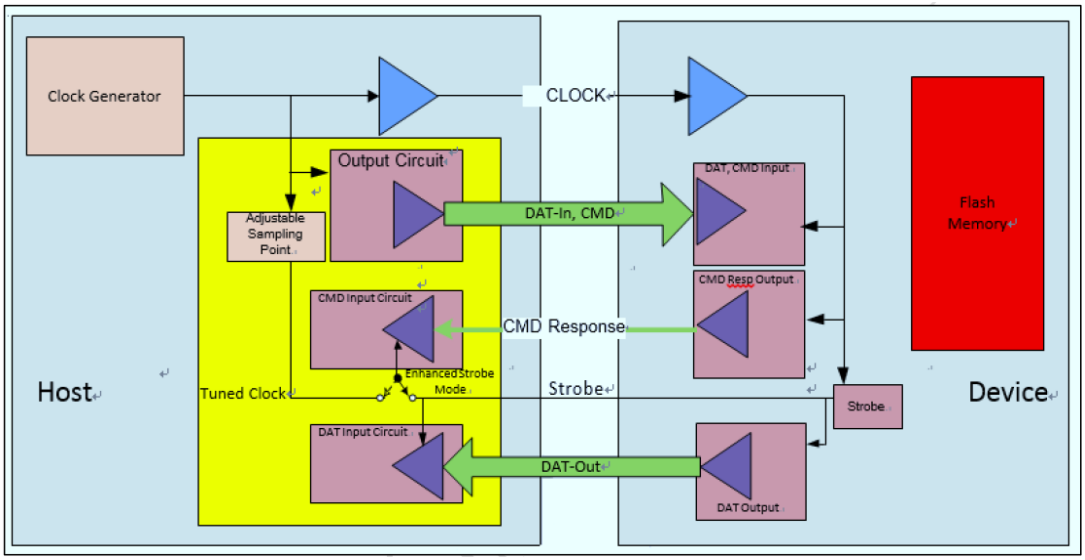


Figure 4 – HS400 Block Diagram

5 eMMC Function Description

5.1 Overview

Table 10 – Feature list

New Feature	JEDEC	Support
Cache Flushing Report	Mandatory	Yes
Background operation control	Mandatory	Yes
Command Queuing	Optional	Yes
Enhanced Strobe	Optional	Yes
RPMB Throughput improve	Optional	Yes

5.2 Command Queuing

To facilitate command queuing in eMMC, the device manages an internal task queue that the host can queue during data transfer tasks.

Every task is issued by the host and initially queued as pending. The device works to prepare pending tasks for execution. When a task is ready for execution, its state changes to “ready for execution”.

The host tracks the state of all queued tasks and may order the execution of any task, marked as “ready for execution”, by sending a command indicating its task ID. The device executes the data transfer transaction after receiving the execute command (CMD46/CMD47)

5.2.1 CMD Set description

Table 11 – CMD Set Description and Deatils

CMD	Type	Argument	Abbreviation	Purpose
CMD44	ac/R1	[31] Reliable Write Request [30] DAT_DIR - "0" write / "1" read [29] tag request [28:25] context ID [24] forced programming	QUEUED_TASK _PARAMS	Define direction of operation (Read or Write) and Set high priority CMD Queue with task ID

		[23] Priority: “0” simple / “1” high [20:16] TASK ID [15:0] number of blocks		
CMD45	ac/R1	[31:0] Start block address	QUEUED_TASK_ADDRESS	Indicate data address for Queued CMD
CMD46	adtc/R1	[20:16] TASK ID	EXECUTE_READ_TASK	(Read) Transmit the requested number of data blocks
CMD47	adtc/R1	[20:16] TASK ID	EXECUTE_WRITE_TASK	(Write) Transmit the requested number of data blocks
CMD48	ac/R1b	[20:16] Task ID [3:0] TM op-code	CMDQ_TASK _MGMT	Reset a specific task or entire queue. [20:16] when TM op-code = 2h these bits represent TaskID. When TM op-code = 1h these bits are reserved.

5.2.2 New response: QSR (Queue Status Register)

The 32-bit Queue Status Register (QSR) carries the state of tasks in the queue at a specific point in time. The host has read access to this register through device response to SEND_STATUS command (CMD13 with bit [15] = “1”), R1’s argument will be the 32-bit Queue Status Register (QSR). Every bit in the QSR represents the task who’s ID corresponds to the bit index. If bit QSR [i] = “0”, then the queued task with a Task ID i is not ready for execution. The task may be queued and pending, or the Task ID is unused. If bit QSR [i] = “1”, then the queued task with Task ID i is ready for execution.

5.2.3 Send Status: CMD 13

CMD13 for reading the Queue Status Register (QSR) by the host. If bit [15] in CMD13’s argument is set to 1, then the device shall send an R1 Response with the QSR instead of the Device Status. * There is still legacy CMD13 with R` response

5.2.4 Mechanism of CMD Queue Operation

Host issues CMD44 with Task ID number, Sector, Count, Direction, Priority to the device followed by CMD45 and host checks the Queue Status check with CMD13 [15] bits to 1 After that host issues CMD46 for Read or CMD47 for write During CMD queue operation, CMD44/CMD45 is able to be issued at any time when the CMD line is not in use.

5.2.5 CMD Queue Register description

Configuration and capability structures shall be added to the EXT_CSD register, as described as below:

Table 12 – CMD Queuing Support (EXT_CSD register: CMDQ_SUPPORT [308])

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved							CMD Queue supportability

This field indicates whether the device supports command queuing or not.
0x0: CMD Queue function is not supported
0x1: CMD Queue function is supported

Table 13 – CMD Queuing Mode Enable (EXT_CSD register: CMDQ_MODE_EN [15])

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved							

This field is used by the host enable command queuing.
0x0: Queue function is not enabled
0x1: Queue function is enable

Table 14 – CMD Queuing Depth (EXT_CSD register: CMDQ_DEPTH [307])

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved			N				

This field is used to calculate the depth of the queue supported by the device.
Bit encoding:
[7:5]: Reserved
[4:0]: N,a parameter used to calculate the Queue Depth of task queue in the device.
Queue Depth = N+1

5.3 Enhanced Strobe Mode

This product supports Enhanced Strobe in HS400 mode and refer to details as described in eMMC5.1 JEDEC standard.

Table 15 – Strobe Support (EXT_CSD register: STROBE_SUPPORT [184])

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved							STROBE_SUPPORT supportability

This register indicates whether a device supports Enhanced Strobe mode for operation modes that STROBE is used in HS400.

0x0: indicates No support of Enhanced Strobe mode
0x1: indicates the device supports Enhanced Strobe mode

5.4 PRMB Throughput improve

Table 16 – Strobe Support (EXT_CSD register: STROBE_SUPPORT [184])

Name	Field	Bit	Type
Enhanced RPMB Reliable Write	EN_RPMB_REL_WR	4	R

Bit [4]: EN_RPMB_REL_WR(R)
0x0: RPMB transfer size is either 256B (single 512B frame) or 512B (Two 512B frame).
0x1: RPMB transfer size is either 256B (single 512B frame), 512B (Two 512B frame), or 8KB (Thirty two 512B frames).

5.5 Partition Management

The memory configuration initially consists of (before any partitioning operation) of the User Data Area, RPMB Area Partitions and two Boot Area Partitions.

The embedded device also offers the host the possibility to configure additional local memory partitions with independent address spaces, starting from logical address 0x 00000000, for different usage models.

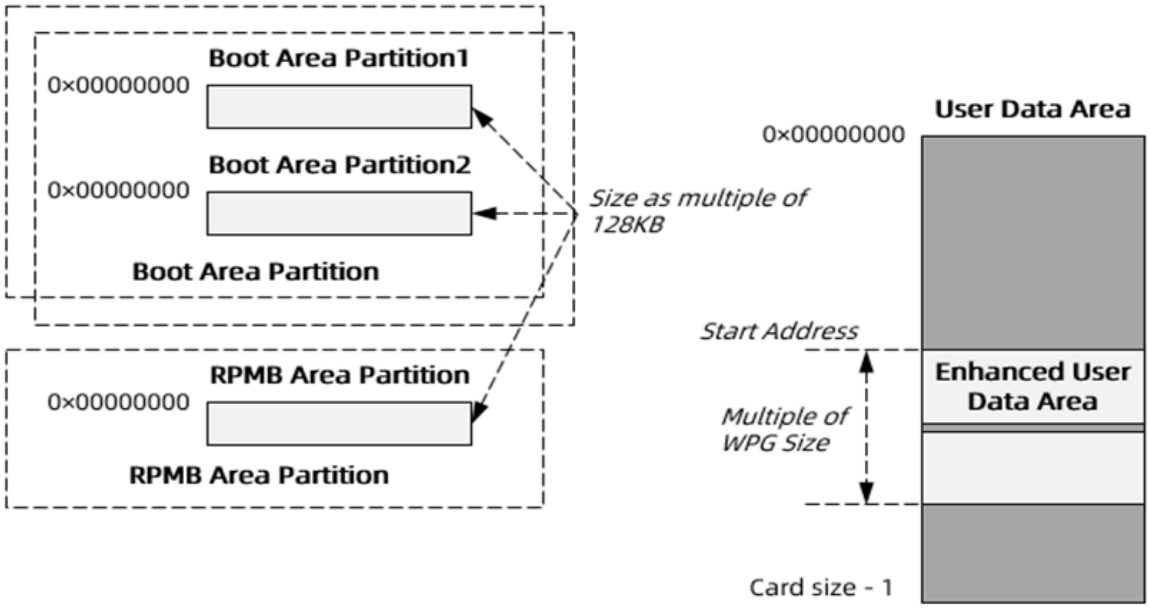
Therefore, the memory block areas can be classified as follows:

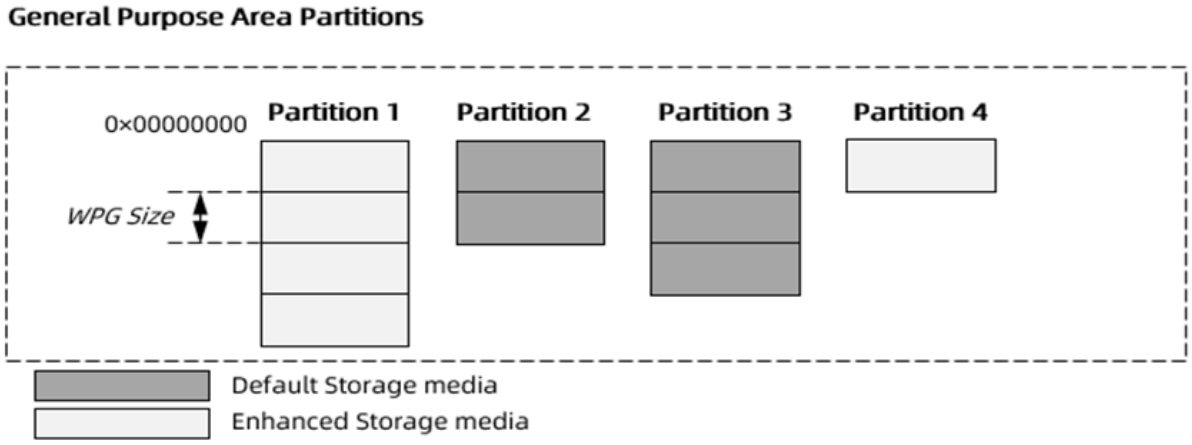
- Two Boot Area Partitions, whose size is multiple of 128 KB and where booting from e-MMC can be performed.
- One RPMB Partition accessed through a trusted mechanism, whose size is defined as multiple of 128 KB.
- Four General Purpose Area Partitions is used to store sensitive data or for other host usage models, whose sizes are a multiple of a Write Protect Group.

Sizes and attributes of Boot and RPMB Area Partitions are defined by the memory manufacturer (read-only), while sizes and attributes of General Purpose Area Partitions can be programmed by the host only once in the device life-cycle (one-time programmable).

Moreover, the host is free to configure one segment in the User Data Area implemented as enhanced storage media, and specify its starting location and size in terms of Write Protect Groups. Attributes of this Enhanced User Data Area can be programmed only once during the device life-cycle (one-time programmable).

A possible final configuration can be the following:





6 Register Settings

Within the Device interface six registers are defined: OCR, CID, CSD, EXT_CSD, RCA and DSR. These can be accessed only by corresponding commands (see Section 6.10 of JESD84-B51).

6.1 OCR Register

The 32-bit operation conditions register (OCR) stores the VDD voltage profile of the Device and the access mode indication. In addition, this register includes a status information bit. This status bit is set if the Device power up procedure has been finished. The OCR register shall be implemented by all Devices. For more details, refer to section 7.1 of the JEDEC Standard Specification No.JESD84-B51.

Table 17 – OCR Register

OCR bit	VCCQ voltage window	e•MMC
[6:0]	Reserved	000 0000b
[7]	1.7–1.95	1b
[14:8]	2.0–2.6	000 0000b
[23:15]	2.7–3.6	1 1111 1111b
[28:24]	Reserved	000 0000b
[30:29]	Access Mode	00b (byte mode) 10b (sector mode)
[31]	Card power up status bit (busy)*	

6.2 CID Register

The Card Identification (CID) register is 128 bits wide. It contains the Device identification information used during the Device identification phase (eMMC protocol). For details, refer to section 7.2 of JEDEC Standard Specification No.JESD84-B51.

Table 18 – CID Register

Name	Field	Width	CID-slice	CID Value
Manufacturer ID	MID	8	[127:120]	0xEA
Reserved	-	6	[119:114]	0x0
Card/BGA	CBX	2	[113:112]	0x1
OEM/Application ID	OID	8	[111:104]	0x0E
Product name	PNM	48	[103:56]	0x53 50 65 4D 4D 43 (SPeMMC)
Product revision	PRV	8	[55:48]	0x10
Product serial number	PSN	32	[47:16]	Serial number
Manufacturing date	MDT	8	[15:8]	Manufacturing date
CRC7 checksum	CRC	7	[7:1]	CRC7
Reserved, always '1'	-	1	[0:0]	0x1

6.3 CSD Register

The Card-Specific Data (CSD) register provides information on how to access the contents stored in eMMC. The CSD registers are used to define the error correction type, maximum data access time, data transfer speed, data format...etc. For details, refer to section 7.3 of the JEDEC Standard Specification No. JESD84-B51.

Table 19 – CSD Register

Name	Field	Width	Cell Type	CSD-slice	Value
CSD structure	CSD_STRUCTURE	2	R	[127:126]	0x3
System specification version	SPEC_VERS	4	R	[125:122]	0x4
Reserved	-	2	R	[121:120]	0x0
Data read access-time 1	TAAC	8	R	[119:112]	0x4F
Data read access-time 2 in CLK cycles (NSAC*100)	NSAC	8	R	[111:104]	0x1
Max. bus clock frequency	TRAN_SPEED	8	R	[103:96]	0x32
Card command classes	CCC	12	R	[95:84]	0xF5
Max. read data block length	READ_BL_LEN	4	R	[83:80]	0x9
Partial blocks for read allowed	READ_BL_PARTIAL	1	R	[79:79]	0x0
Write block misalignment	WRITE_BLK_MISALIGN	1	R	[78:78]	0x0
Read block misalignment	READ_BLK_MISALIGN	1	R	[77:77]	0x0
DSR implemented	DSR_IMP	1	R	[76:76]	0x0
Reserved	-	2	R	[75:74]	0x0
Device size	C_SIZE	12	R	[73:62]	0xFFF
Max. read current @ VDD min	VDD_R_CURR_MIN	3	R	[61:59]	0x6
Max. read current @ VDD max	VDD_R_CURR_MAX	3	R	[58:56]	0x6
Max. write current @ VDD min	VDD_W_CURR_MIN	3	R	[55:53]	0x6
Max. write current @ VDD max	VDD_W_CURR_MAX	3	R	[52:50]	0x6
Device size multiplier	C_SIZE_MULT	3	R	[49:47]	0x7
Erase group size	ERASE_GRP_SIZE	5	R	[46:42]	0x1F
Erase group size multiplier	ERASE_GRP_MULT	5	R	[41:37]	0x1F
Write protect group size	WP_GRP_SIZE	5	R	[36:32]	0xF
Write protect group enable	WP_GRP_MULT	1	R	[31:31]	0x1
Manufacturer default	ECC DEFAULT_ECC	2	R	[30:29]	0x0
Write speed factor	R2W_FACTOR	3	R	[28:26]	0x5
Max. write data block length	WRITE_BL_LEN	4	R	[25:22]	0x9
Partial blocks for write allowed	WRITE_BL_PARTIAL	1	R	[21:21]	0x0
Reserved	-	4	R	[20:17]	0x0
Content protection application	CONTENT_PROT_APP	1	R	[16:16]	0x0
File format group	FILE_FORMAT_GRP	1	R/W	[15:15]	0x0
Copy flag(OTP)	COPY	1	R/W	[14:14]	0x0
Permanent write protection	PERM_WRITE_PROTECT	1	R/W	[13:13]	0x0
Temporary write protection	TMP_WRITE_PROTECT	1	R/W/E	[12:12]	0x0
File format	FILE_FORMAT	2	R/W	[11:10]	0x0
ECC code	ECC	2	R/W/E	[9:8]	0x0
CRC	CRC	7	R/W/E	[7:1]	0x0

Reserved, always '1'	-	1	-	[0:0]	0x1

6.4 Extended CSD Register

The Extended CSD register defines the Device properties and selected modes. It is 512 bytes long. The most significant 320 bytes are the Properties segment, which defines the Device capabilities and cannot be modified by the host. The lower 192 bytes are the Modes segment, which defines the configuration the Device is working in. These modes can be changed by the host by means of the SWITCH command. For details, refer to section 7.4 of the JEDEC Standard Specification No.JESD84-B51.

Table 20 – Extended CSD Register

Name	**Field**	**Size** (Bytes)	**Cell** Type	**CSD-slice**	**Value**
Properties Segment					
Reserved	**-**	**6**	**TBD**	**[511:506]**	**All "0"**
Extended Security Commands Error	EXT_SECURITY_ERR	1	R	[505]	0x0
Supported Command Sets	S_CMD_SET	1	R	[504]	0x1
HPI features	HPI_FEATURES	1	R	[503]	0x1
Background operations support	BKOPS_SUPPORT	1	R	[502]	0x1
Max packed read commands	MAX_PACKED_READS	1	R	[501]	0x38
Max packed write commands	MAX_PACKED_WRITES	1	R	[500]	0x38
Data Tag Support	DATA_TAG_SUPPORT	1	R	[499]	0x1
Tag Unit Size	TAG_UNIT_SIZE	1	R	[498]	0x5
Tag Resources Size	TAG_RES_SIZE	1	R	[497]	0x1
Context management capabilities	CONTEXT_CAPABILITIES	1	R	[496]	0x5
Large Unit size	LARGE_UNIT_SIZE_M1	1	R	[495]	0x1
Extended partitions attribute support	EXT_SUPPORT	1	R	[494]	0x3
Supported modes	SUPPORTED_MODES	1	R	[493]	0x1
FFU features	FFU_FEATURES	1	R	[492]	0x1
Operation codes timeout	OPERATION_CODE_TIMEOUT	1	R	[491]	0xD
FFU Argument	FFU_ARG	4	R	[490:487]	0x0
Barrier support	BARRIER_SUPPORT	1	R	[486]	0x1
Reserved	-	177	TBD	[485:309]	All "0"
CMD Queuing Support	CMDQ_SUPPORT	1	R	[308]	0x1
CMD Queuing Depth	CMDQ_DEPTH	1	R	[307]	0x1F
Reserved	-	1	TBD	[306]	0x0
Number of FW sectors correctly programmed	NUMBER_OF_FW_SECTORS_CO R RECTLY_PROGRAMMED	4	R	[305:302]	0x0

Vendor proprietary health report	VENDOR_PROPRIETARY_HEALTH_ REPORT	32	R	[301:270]	All “0”
Device life time estimation type B	DEVICE_LIFE_TIME_EST_TYP_B	1	R	[269]	0x1
Device life time estimation type A	DEVICE_LIFE_TIME_EST_TYP_A	1	R	[268]	0x1
Pre EOL information	PRE_EOL_INFO	1	R	[267]	0x1
Optimal read size	OPTIMAL_READ_SIZE	1	R	[266]	0x40
Optimal write size	OPTIMAL_WRITE_SIZE	1	R	[265]	0x40
Optimal trim unit size	OPTIMAL_TRIM_UNIT_SIZE	1	R	[264]	0x7
Device version	DEVICE_VERSION	2	R	[263:262]	0x0
Firmware version	FIRMWARE_VERSION	8	R	[261:254]	FW version
Power class for 200MHz, DDR at VCC= 3.6V	PWR_CL_DDR_200_360	1	R	[253]	0x0
Cache size	CACHE_SIZE	4	R	[252:249]	0x300
Generic CMD6 timeout	GENERIC_CMD6_TIME	1	R	[248]	0x40
Power off notification(long) timeout	POWER_OFF_LONG_TIME	1	R	[247]	0x64
Background operations status	BKOPS_STATUS	1	R	[246]	0x0
Number of correctly programmed sectors	CORRECTLY_PRG_SECTORS_NUM	4	R	[245:242]	0x0
1st initialization time after partitioning	INI_TIMEOUT_AP	1	R	[241]	0xA
Cache Flushing Policy	CACHE_FLUSH_POLICY	1	R	[240]	0x1
Power class for 52MHz, DDR at VCC = 3.6V	PWR_CL_DDR_52_360	1	R	[239]	0x0
Power class for 52MHz, DDR at VCC = 1.95V	PWR_CL_DDR_52_195	1	R	[238]	0x0
Power class for 200MHz at VCCQ =1.95V, VCC = 3.6V	PWR_CL_200_195	1	R	[237]	0x0
Power class for 200MHz, at VCCQ=1.3V, VCC = 3.6V	PWR_CL_200_130	1	R	[236]	0x0
Minimum Write Performance for 8bit at 52MHz in DDR mode	MIN_PERF_DDR_W_8_52	1	R	[235]	0x0
Minimum Read Performance for 8bit at 52MHz in DDR mode	MIN_PERF_DDR_R_8_52	1	R	[234]	0x0
Reserved		**1**	**TBD**	**[233]**	**0x0**
TRIM Multiplier	TRIM_MULT	1	R	[232]	0x2
Secure Feature support	SEC_FEATURE_SUPPORT	1	R	[231]	0x55
Secure Erase Multiplier	SEC_ERASE_MULT	1	R	[230]	0x1Bh
Secure TRIM Multiplier	SEC_TRIM_MULT	1	R	[229]	0x11
Boot information	BOOT_INFO	1	R	[228]	0x7
Reserved		1	TBD	[227]	0x0
Boot partition size	BOOT_SIZE_MULT	1	R	[226]	0x20
Access size	ACC_SIZE	1	R	[225]	4GB:

					0x06 0x08: (4GB) 0x09: (8GB)
High-capacity erase unit size	HC_ERASE_GRP_SIZE	1	R	[224]	0x1
High-capacity erase timeout	ERASE_TIMEOUT_MULT	1	R	[223]	0x1
Reliable write sector count	REL_WR_SEC_C	1	R	[222]	0x1
High-capacity write protect group	HC_WP_GRP_SIZE	1	R	[221]	0x10
size					
Sleep current [VCC]	S_C_VCC	1	R	[220]	0xD
Sleep current [VCCQ]	S_C_VCCQ	1	R	[219]	0xD
Production state awareness timeout	PRODUCTION_STATE_AWARENES S_TIMEOUT	1	R	[218]	0x6
Sleep/awake timeout	S_A_TIMEOUT	1	R	[217]	0x17
Sleep Notification Timout1	SLEEP_NOTIFICATION_TIME	1	R	[216]	0xA
Sector Count	SEC_COUNT	4	R	[215:212]	4GB: 0×748000 8GB: 0×E72000 16GB: 0x1D1F000 32GB: 0x3A3E000
Secure Write Protect Information	SECURE_WP_INFO	1	R	[211]	0x0
Minimum Write Performance for 8bit at 52MHz	MIN_PERF_W_8_52	1	R	[210]	0x0
Minimum Read Performance for 8bit at 52MHz	MIN_PERF_R_8_52	1	R	[209]	0x0
Minimum Write Performance for 8bit at 26MHz, for 4bit at 52MHz	MIN_PERF_W_8_26_4_52	1	R	[208]	0x0
Minimum Read Performance for 8bit at 26MHz, for 4bit at 52MHz	MIN_PERF_R_8_26_4_52	1	R	[207]	0x0
Minimum Write Performance for 4bit at 26MHz	MIN_PERF_W_4_26	1	R	[206]	0x0
Minimum Read Performance for 4bit at 26MHz	MIN_PERF_R_4_26	1	R	[205]	0x0
Reserved		1	TBD	[204]	0x0
Power class for 26MHz at 3.6 V 1 R	PWR_CL_26_360	1	R	[203]	0x0
Power class for 52MHz at 3.6 V 1 R	PWR_CL_52_360	1	R	[202]	0x0
Power class for 26MHz at 1.95 V 1 R	PWR_CL_26_195	1	R	[201]	0x0

Power class for 52MHz at 1.95 V 1 R	PWR_CL_52_195	1	R	[200]	0x0
Partition switching timing	PARTITION_SWITCH_TIME	1	R	[199]	0x6
Out-of-interrupt busy timing	OUT_OF_INTERRUPT_TIME	1	R	[198]	0xA
I/O Driver Strength	DRIVER_STRENGTH	1	R	[197]	0x1
Device type	DEVICE_TYPE	1	R	[196]	0x57
Reserved		**1**	**TBD**	**[195]**	**0x0**
CSD Structure Version	CSD_STRUCTURE	1	R	[194]	0x2
Reserved		**1**	**TBD**	**[193]**	**0x0**
Extended CSD Revision	EXT_CSD_REV	1	R	[192]	0x8
Modes Segment					
Command Set	CMD_SET	1	R/W/E_P	[191]	0x0
Reserved		**1**	**TBD**	**[190]**	**0x0**
Command set revision	CMD_SET_REV		R	[189]	0x0
Reserved		1	TBD	[188]	0x0
Power class	POWER_CLASS		R/W/E_P	[187]	0x0
Reserved		**1**	**TBD**	**[186]**	**0x0**
High Speed Interface Timing	HS_TIMING	1	R/W/E_P	[185]	0x0
Strobe Support	STROBE_SUPPORT	1	R	[184]	0x1
Bus Width Mode	BUS_WIDTH	1	W/E_P	[183]	0x0
Reserved		**1**	**TBD**	**[182]**	**0x0**
Erased memory range	ERASE_MEM_CONT	1	R	[181]	0x0
Reserved		**1**	**TBD**	**[180]**	**0x0**
Partition Configuration	PARTITION_CONFIG	1	R/W/E & R/W/E_P	[179]	0x0
Boot Config protection	BOOT_CONFIG_PROT	1	R/W &R/W/C_P	[178]	0x0
Boot bus Conditions	BOOT_BUS_CONDITIONS	1	R/W/E	[177]	0x0
Reserved		1	TBD	[176]	0x0
High-density erase group definition	ERASE_GROUP_DEF	1	R/W/E	[175]	0x0
Boot write protection status registers	BOOT_WP_STATUS	1	R	[174]	0x0
Boot area write protect register	BOOT_WP	1	R/W &R/W/C_P	[173]	0x0
Reserved		**1**	**TBD**	**[172]**	**0x0**
User area write protect register	USER_WP	1	R/W,R/ W/C_P &R/W/E_P	[171]	0x0
Reserved		**1**	**TBD**	**[170]**	**0x0**
FW configuration	FW_CONFIG	1	R/W	[169]	0x0
RPMB Size	RPMB_SIZE_MULT	1	R	[168]	0x20
Write reliability setting register	WR_REL_SET	1	R/W	[167]	0x1F
Write reliability parameter register	WR_REL_PARAM	1	R	[166]	0x14
Start Sanitize operation	SANITIZE_START	1	W/E_P	[165]	0x0

Manually start background operations	BKOPS_START	1	W/E_P	[164]	0x0
Enable background operations handshake	BKOPS_EN	1	R/W & R/W/E	[163]	0x0
H/W reset function	RST_n_FUNCTION	1	R/W	[162]	0x0
HPI management	HPI_MGMT	1	R/W/E_P	[161]	0x0
Partitioning Support	PARTITIONING_SUPPORT	1	R	[160]	0x7
Max Enhanced Area Size	MAX_ENH_SIZE_MULT	3	R	[159:157]	4GB: 0xE9 8GB: 0x1CE 16GB:0x747 32GB:0xE8F
Partitions attribute	PARTITIONS_ATTRIBUTE	1	R/W	[156]	0x0
Partitioning Setting	PARTITION_SETTING_COMPLETED	1	R/W	[155]	0x0
General Purpose Partition Size	GP_SIZE_MULT	12	R/W	[154:143]	0x0
Enhanced User Data Area Size	ENH_SIZE_MULT	3	R/W	[142:140]	0x0
Enhanced User Data Start Address	ENH_START_ADDR	4	R/W	[139:136]	0x0
Reserved		1	TBD	[135]	0x0
Bad Block Management mode	SEC_BAD_BLK_MGMNT	1	R/W	[134]	0x0
Production state awareness	PRODUCTION_STATE_AWARENESS	1	R/W/E	[133]	0x0
Package Case Temperature is controlled	TCASE_SUPPORT	1	W/E_P	[132]	0x0
Periodic Wake-up	PERIODIC_WAKEUP	1	R/W/E	[131]	0x0
Program CID/CSD in DDR mode support	PROGRAM_CID_CSD_DDR_SUPPORT	1	R	[130]	0x0
Reserved		**2**	**TBD**	**[129:128]**	**0x0**
Vendor Specific Fields	NATIVE_SECTOR_SIZE	1	<vendor	[127:64]	0x0
Native sector size	NATIVE_SECTOR_SIZE	1	R	[63]	0x0
Sector size emulation	USE_NATIVE_SECTOR	1	R/W	[62]	0x0
Sector size	DATA_SECTOR_SIZE	1	R	[61]	0x0
1st initialization after disabling sector size emulation	INI_TIMEOUT_EMU	1	R	[60]	0x0
Class 6 commands control	CLASS_6_CTRL	1	R/W/E_P	[59]	0x0
Number of addressed group to be Released	DYNCAP_NEEDED	1	R	[58]	0x0
Exception events control	EXCEPTION_EVENTS_CTRL	2	R/W/E_P	[57:56]	0x0
Exception events status	EXCEPTION_EVENTS_STATUS	2	R	[55:54]	0x0
Extended Partitions Attribute	EXT_PARTITIONS_ATTRIBUTE	2	R/W	[53:52]	0x0
Context configuration	CONTEXT_CONF	15	R/W/E_P	[51:37]	0x0
Packed command status	PACKED_COMMAND_STATUS	1	R	[36]	0x0
Packed command failure index	PACKED_FAILURE_INDEX	1	R	[35]	0x0

Power Off Notification	POWER_OFF_NOTIFICATION	1	R/W/E_P	[34]	0x0
Control to turn the Cache ON/OFF	CACHE_CTRL	1	R/W/E_P	[33]	0x0
Flushing of the cache	FLUSH_CACHE	1	W/E_P	[32]	0x0
Control to turn the Barrier ON/OFF	BARRIER_CTRL	1	R/W	[31]	0x0
Mode config	MODE_CONFIG	1	R/W/E_ P	[30]	0x0
Mode operation codes	MODE_OPERATION_CODES	1	W/E_P	[29]	0x0
Reserved		**2**	**TBD**	**[28:27]**	**0x0**
FFU status	FFU_STATUS	1	R	[26]	0x0
Pre loading data size	PRE_LOADING_DATA_SIZE	4	R/W/E_P	[25:22]	0x0
Max pre loading data size	MAX_PRE_LOADING_DATA_SIZE	4	R	[21:18]	4GB: 0x1D2000 8GB: 0x39C800 16GB: 0x747C00 32GB: 0xE8F800
Product state awareness enablement	PRODUCT_STATE_AWARENESS_E NABLEMENT	1	R/W/E & R	[17]	0x3
Secure Removal Type	SECURE_REMOVAL_TYPE	1	R/W & R	[16]	0x1
Command Queue Mode Enable	CMDQ_MODE_EN	1	R/W/E_P	[15]	0x0
Reserved		**15**	**TBD**	**[14:0]**	**0x0**

6.5 RCA Register

The writable 16-bit Relative Device Address (RCA) register carries the Device address assigned by the host during the Device identification. This address is used for the addressed host-Device communication after the Device identification procedure. The default value of the RCA register is 0x0001. The value 0x0000 is reserved to set all Devices into the Stand-by State with CMD7.

6.6 DSR Register

The 16-bit driver stage register (DSR) is described in detail in Section 10.2 of the JEDEC Standard Specification No.JESD84-B51. It can be optionally used to improve the bus performance for extended operating conditions (depending on parameters like bus length, transfer rate or number of Devices). The CSD register carries the information about the DSR register usage.

7 The eMMC bus

The eMMC bus has ten communication lines and three supply lines:

- CMD： Command is a bidirectional signal. The host and Device drivers are operating in two
  modes, open drain and push/pull.
- DAT0-7： Data lines are bidirectional signals. Host and Device drivers are operating in push-pull mode
- CLK： Clock is a host to Device signal. CLK operates in push-pull mode
- Data Strobe: Data Strobe is a Device to host signal. Data Strobe operates in push-pull mode.

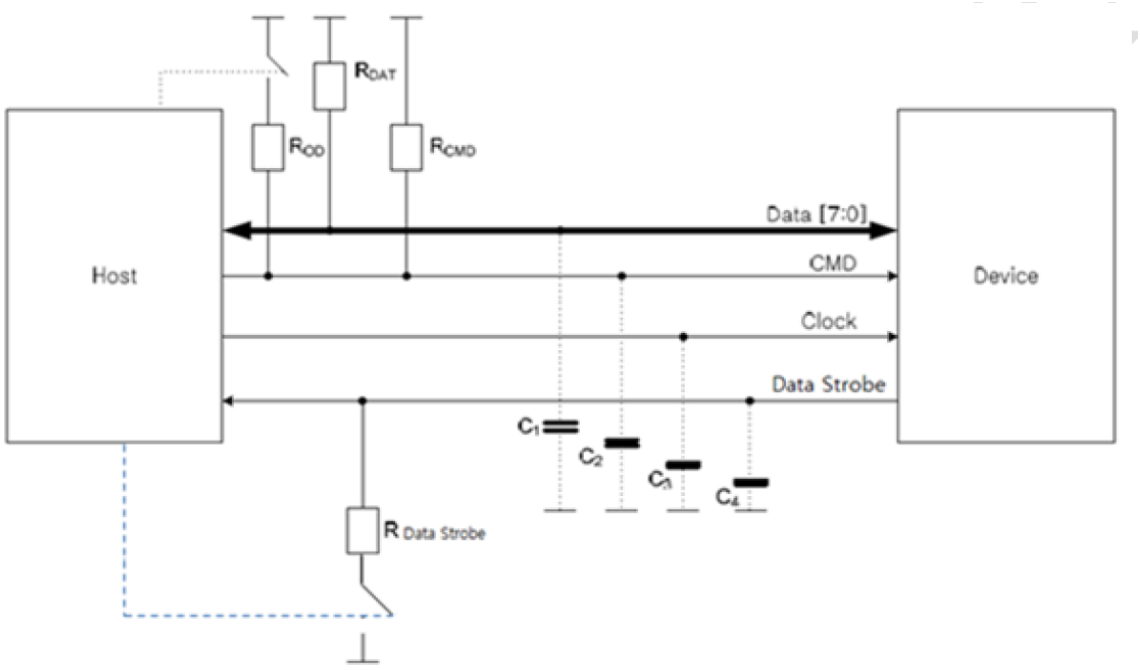


Figure 5 – Bus Circuitry Diagram

The ROD is switched on and off by the host synchronously to the open-drain and push-pull mode transitions. The host does not have to have open drain drivers, but must recognize this mode to switch on the ROD. RDAT and RCMD are pull-up resistors protecting the CMD and the DAT lines against bus floating device when all device drivers are in a high-impedance mode.

A constant current source can replace the ROD by achieving a better performance (constant slopes for the signal rising and falling edges). If the host does not allow the switchable ROD implementation, a fixed RCMD can be used).Consequently the maximum operating frequency in the open drain mode has to be reduced if the used RCMD value is higher than the minimal one given in.

$R_{data\ strobe}$ is pull-down resistor used in HS400 device.

7.1 Power-up

7.1.1 eMMC power-up

An eMMC bus power-up is handled locally in each device and in the bus master. Figure7 shows the power-up sequence and is followed by specific instructions regarding the power-up sequence. Refer to section 10.1 of the JEDEC Standard Specification No.JESD84-B51 for specific instructions regarding the power-up sequence.

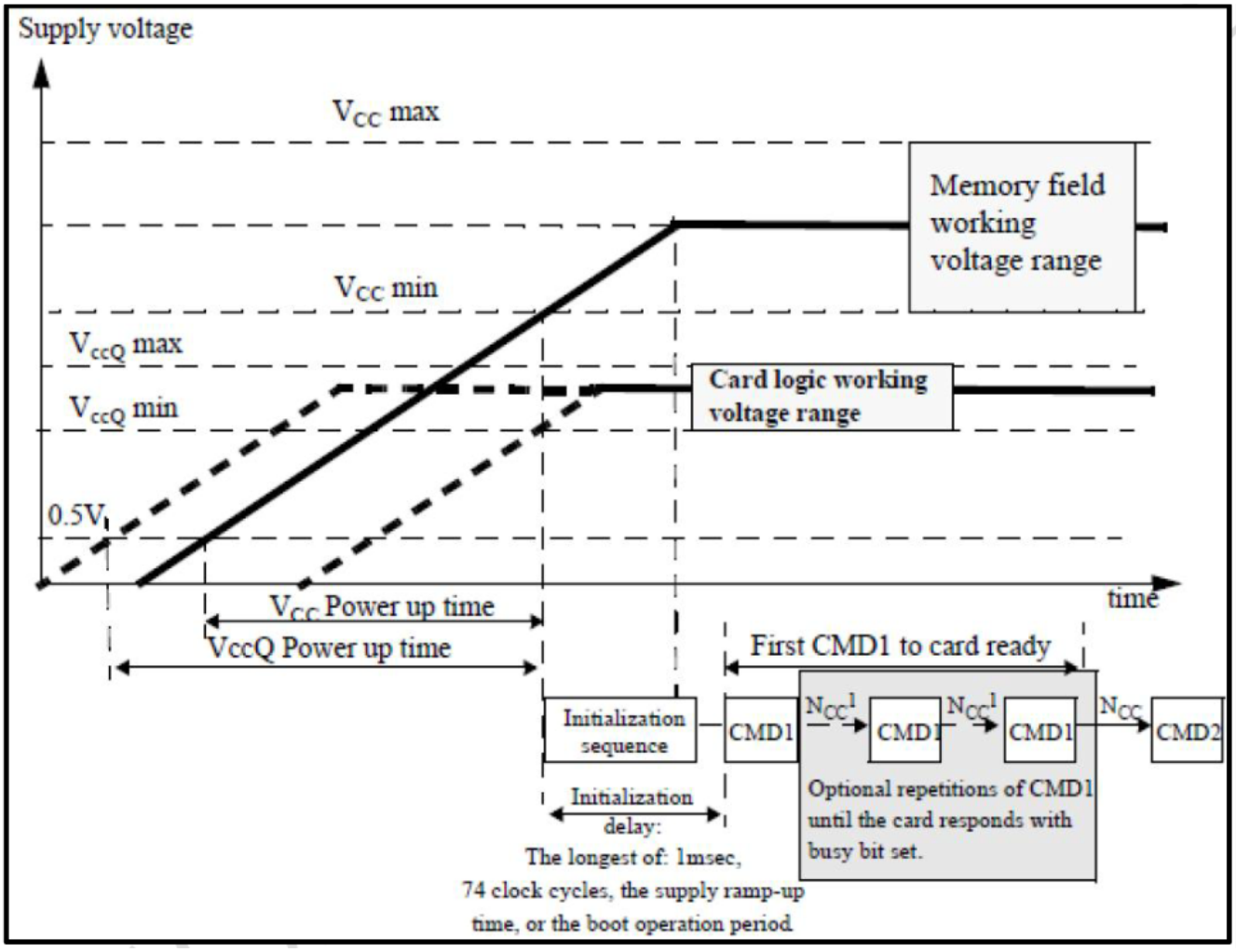


Figure 6 – eMMC Power-up Diagram

7.1.2 eMMC Power Cycling

The master can execute any sequence of VCC and VCCQ power-up/power-down. However, the master must not issue any commands until VCC and VCCQ are stable within each operating voltage range. After the slave enters sleep mode, the master can power-down VCC to reduce power consumption. It is necessary for the slave to be ramped up to VCC before the host issues CMD5 (SLEEP_AWAKE) to wake the slave unit. For more information about power cycling see Section 10.1.3 of the JEDEC Standard Specification No.JESD84-B51.

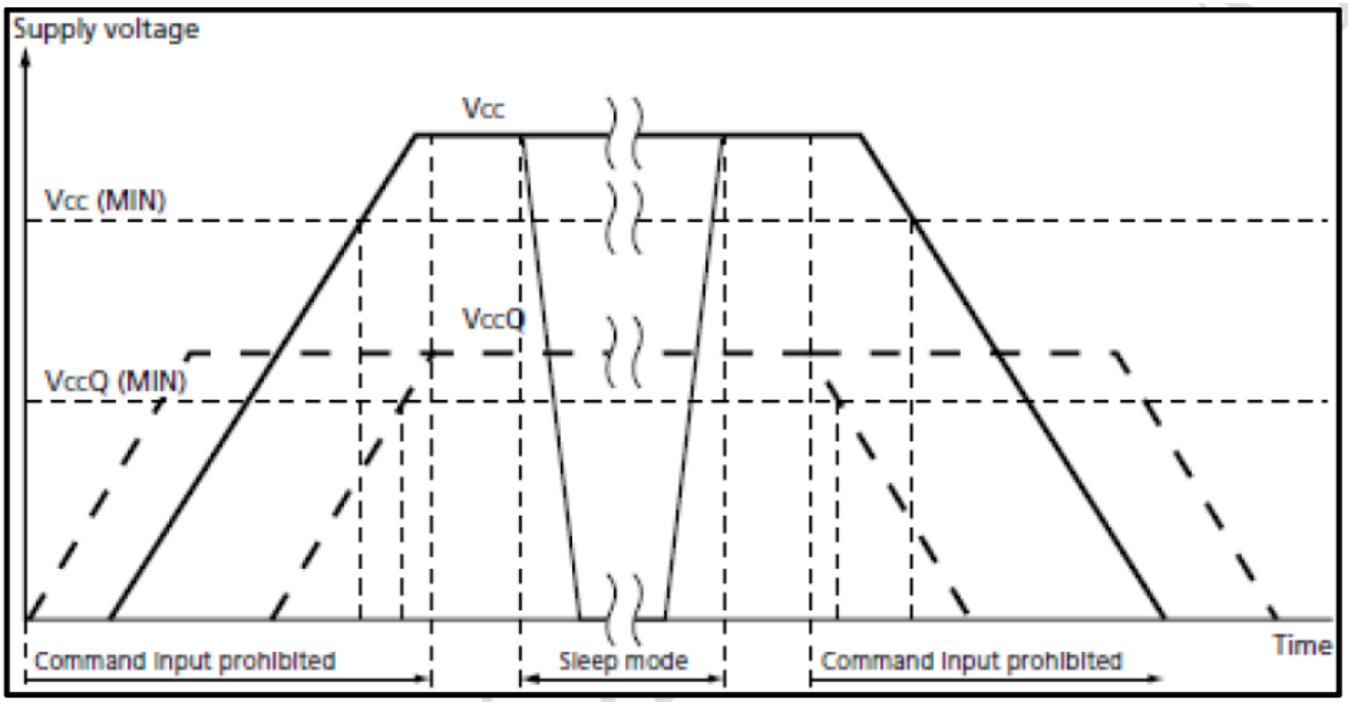


Figure 7 – The eMMC Power Cycle

7.2 Bus Operating Conditions

Table 21 – General Operating Conditions

Parameter	Symbol	Min	Max.	Unit
Peak voltage on all lines		-0.5	VCCQ +0.5	V
All Inputs				
Input Leakage Current (before initialization sequence [1] and/or the internal pull up resistors connected)		tbd	tbd	µA
Input Leakage Current (after initialization sequence and the internal pull up resistors disconnected)		tbd	tbd	µA
All Outputs				
Output Leakage Current (before initialization sequence)		tbd	tbd	µA

Output Leakage Current (after initialization sequence) [2]		tbd	tbd	µA
Notes: 1. Initialization sequence is defined in section 10.1 2. DS (Data strobe) pin is excluded.				

7.2.1 Power supply: eMMC

In the eMMC, VCC is used for the NAND flash device and its interface voltage; VCCQ is for the controller and the MMC interface voltage as shown in Figure 8. The core regulator is optional and only required when internal core logic voltage is regulated from VCCQ. A Creg capacitor must be connected to the VDDi terminal to stabilize regulator output on the system.

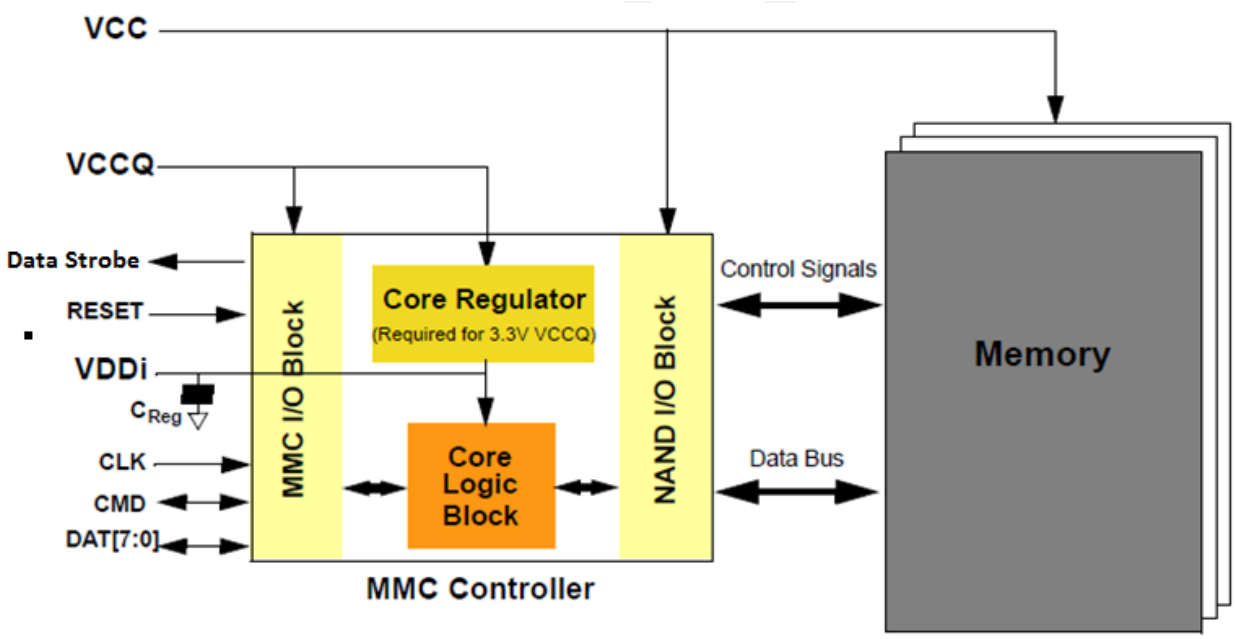


Figure 8 – eMMC Internal Power Diagram

7.2.2 eMMC Power Supply Voltages

The eMMC supports one or more combinations of V_{CC} and V_{CCQ} as shown in Table 8. The V_{CCQ} must be defined at equal to or less than V_{CC}.

Table 22 – eMMC Operating Voltage

Parameter	Symbol	MIN	MAX	Unit
Supply voltage (NAND)	V_{CC}	2.7	3.6	V
Supply voltage (I/O)	V_{CCQ}	2.7	3.6	V
		1.7	1.95	V
Supply power-up for 3.3V	t_{PRUH}		tbd	ms
Supply power-up for 1.8V	t_{PRUL}		tbd	ms

The eMMC must support at least one of the valid voltage configurations, and can optionally support all valid voltage configurations (see Table15).

Table 23 – eMMC Voltage Combinations

		V_{CCQ}	
		1.7V–1.95V	2.7V–3.6V[1]
Vcc	2.7V-3.6V	Valid	Valid
Notes: 1. CCQ (I/O) 3.3 volt range is not supported in HS200 /HS400 devices			

7.2.3 Bus Signal Line Load

The total capacitance C_L of each line of the eMMC bus is the sum of the bus master capacitance C_{HOST}, the bus capacitance C_{BUS} itself and the capacitance C_{DEVICE} of eMMC connected to this line:

- $C_L = C_{HOST} + C_{BUS} + C_{DEVICE}$

The sum of the host and bus capacitances must be under 20pF.

Table 24 – Signal Line Load

Parameter	Symbol	Min	Max	Typ	Unit	Remark
Pull-up resistance for CMD	R_{CMD}	4.7	50	10	Kohm	to prevent bus floating
Pull-up resistance for DAT0–7	R_{DAT}	10	50	10	Kohm	to prevent bus floating
Pull-up resistance for RST_n	R_{RST_n}	4.7	50	10	Kohm	It is not necessary to put pull-up resistance on RST_n (H/W rest) line if host does not use H/W reset. (Extended CSD register [162] = 0 b)
Bus signal line capacitance	C_L		30	30	pF	Single Device
Single Device capacitance	C_{DEVICE}		6	6	pF	
Maximum signal line inductance			16	16	nH	
Impedance on CLK / CMD / DAT0~7		45	55	50	ohm	Impedance match
Serial's resistance on CLK line	SR_{CLK}	0	47	0	ohm	
Serial's resistance on CMD / DAT0~7 line	SR_{CMD} $SR_{DAT0\sim7}$	0	47	0	ohm	

V_{CCQ} decoupling capacitor		2.2+0.1	10+0.22	2.2+0.1	μF	It should be located as close as possible to the balls defined in order to minimize connection parasitic
	CH1	1	2.2	1	μF	CH1 is only for HS200. It should be placed adjacent to VCCQ-VSSQ balls (#K6 and #K4 accordingly, next to DAT [7..0] balls). It should be located as close as possible to the balls defined in order to minimize connection parasitic.
V_{CC} capacitor value		2.2+0.1	10+0.22	4.7+0.1	μF	It should be located as close as possible to the balls defined in order to minimize connection parasitic
V_{Ddi} capacitor value		1+0.1	2.2+0.1	1+0.1	μF	To stabilize regulator output to controller core logics. It should be located as close as possible to the balls defined in order to minimize connection parasitic

7.2.4 Bus Signal Line Load

The circuit in Figure 10 shows the reference load used to define the HS400 Device Output Timings and overshoot / undershoot parameters. The reference load is made up by the transmission line and the CREFERENCE capacitance.

The reference load is not intended to be a precise representation of the typical system environment nor a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the reference load to system environment. Manufacturers should correlate to their production test conditions. Delay time (td) of the transmission line has been introduced to make the reference load independent from the PCB technology and trace length.

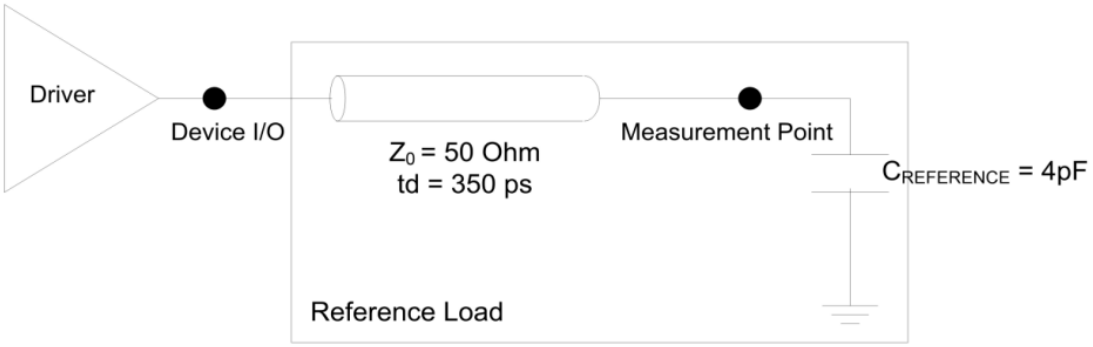


Figure 9 – HS400 reference load

7.3 Bus Signal Levels

As the bus can be supplied with a variable supply voltage, all signal levels are related to the supply voltage.

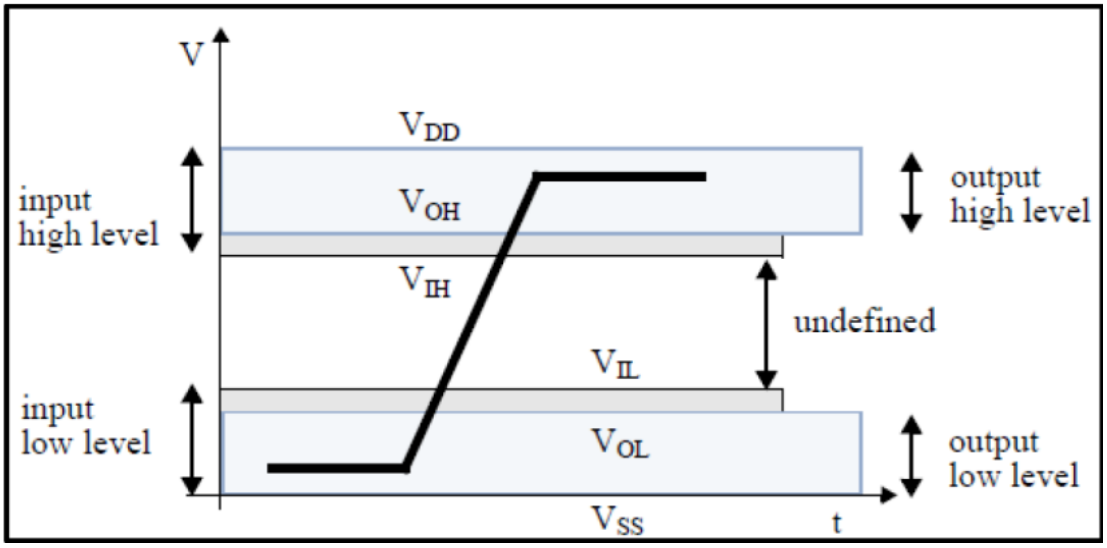


Figure 10 – Bus Signal Levels

7.3.1 Open-drain Mode Bus Signal Level

Table 25 – Open-drain Bus Signal Level

Parameter	Symbol	Min	Max.	Unit	Conditions
Output HIGH voltage	V_{OH}	V_{DD} – 0.2		V	I_{OH} = -100µA
Output LOW voltage	V_{OL}		0.3	V	I_{OL} = 2 mA

The input levels are identical with the push-pull mode bus signal levels.

7.3.2 Push-pull mode bus signal level— eMMC

The device input and output voltages shall be within the following specified ranges for any VDD of the allowed voltage range

For 2.7V-3.6V VCCQ range (compatible with JESD8C.01)

Table 26 – Push-pull Signal Level—High-voltage eMMC

Parameter	Symbol	Min	Max.	Conditions
		Unit: V		
Output HIGH voltage	V_{OH}	0.75 * V_{CCQ}		I_{OH} = -100 µA @ V_{CCQ} min
Output LOW voltage	V_{OL}		0.125 * V_{CCQ}	I_{OL} = 100 µA @ V_{CCQ} min
Input HIGH voltage	V_{IH}	0.625 * V_{CCQ}	V_{CCQ} + 0.3	
Input LOW voltage	V_{IL}	V_{SS} – 0.	0.25 * V_{CCQ}	

For 1.70V – 1.95V V_{CCQ} range (: Compatible with EIA/JEDEC Standard "EIA/JESD8-7 Normal Range" as defined in the following table.

Table 27 – Push-pull Signal Level—1.70 -1.95 V_{CCQ} Voltage Range

Parameter	Symbol	Min	Max.	Conditions
		Unit: V		
Output HIGH voltage	V_{OH}	V_{CCQ} – 0.45V		I_{OH} = -2mA
Output LOW voltage	V_{OL}		0.45V	I_{OL} = 2mA
Input HIGH voltage	V_{IH}	0.65 * V_{CCQ}[1]	V_{CCQ} + 0.3	
Input LOW voltage	V_{IL}	V_{SS} – 0.3.	0.35 * V_{DD}[2]	
Notes: 1. 0.7 * V_{DD} for MMC™4.3 and older revisions. 2. 0.3 * V_{DD} for MMC™4.3 and older revisions.				

7.3.3 Bus Operating Conditions for HS200 & HS400

The bus operating conditions for HS200 devices is the same as specified in sections 10.5.1 of JESD84-B51 through 10.5.2 of JESD84-B51. The only exception is that V_{CCQ}=3.3v is not supported.

7.3.4 Device Output Driver Requirements for HS200 & HS400

Refer to section 10.5.4 of the JEDEC Standard Specification No.JESD84-B51

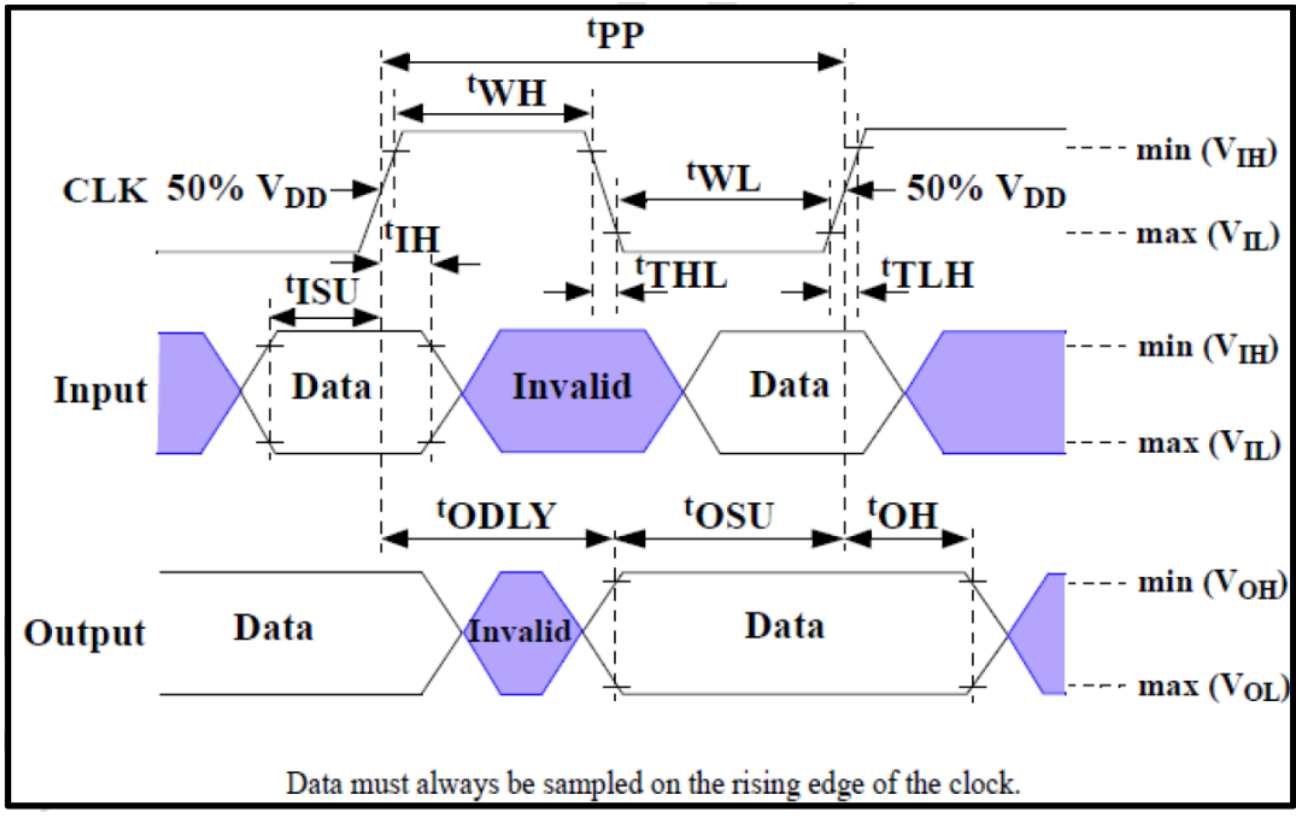


Figure 11 – Timing Diagram

7.4 Bus Timing

7.4.1 Device Interface Timings

Table 28 – High-speed Device Interface Timing

Parameter	Symbol	Min	Max.	Unit	Remark
Clock CLK[1]					
Clock frequency Data Transfer Mode (PP)[2]	fPP	0	52[3]	MHz	CL≤30 pF Tolerance:+100KHz
Clock frequency Identification Mode (OD)	fOD	0	400	kHz	Tolerance: +20KHz
Clock high time	tWH	6.5		ns	CL≤ 30 pF
Clock low time	tWL	6.5		ns	CL≤ 30 pF
Clock rise time[4]	tTLH		3	ns	CL≤ 30 pF
Clock fall time	tTHL		3	ns	CL≤ 30 pF
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	tISU	3		ns	CL≤ 30 pF
Input hold time	tIH	3		ns	CL≤ 30 pF
Outputs CMD, DAT (referenced to CLK)					
Output delay time during data transfer	tODLY		13.7	ns	CL≤ 30 pF
Output hold time	tOH	2.5		ns	CL≤ 30 pF
Signal rise time[5]	tRISE		3	ns	CL≤ 30 pF

Notes: 1. CLK timing is measured at 50% of VDD.
2. eMMC shall support the full frequency range from 0-26Mhz or 0-52MHz
3. Device can operate as high-speed Device interface timing at 26 MHz clock frequency.
4. CLK rise and fall times are measured by min (VIH) and max (VIL).
5. Inputs CMD DAT rise and fall times are measured by min (VIH) and max (VIL) and outputs CMD DAT rise and fall times are measured by min (VOH) and max (VOL). “

Table 29 – Backward-compatible Device Interface Timing

Parameter	Symbol	Min	Max.	Unit	Remark
Clock CLK[1]					
Clock frequency Data Transfer Mode (PP)[2]	fPP	0	52[3]	MHz	CL≤30 pF Tolerance:+100KHz
Clock frequency Identification Mode (OD)	fOD	0	400	kHz	Tolerance: +20KHz
Clock high time	tWH	6.5		ns	CL≤ 30 pF
Clock low time	tWL	6.5		ns	CL≤ 30 pF
Clock rise time[4]	tTLH		3	ns	CL≤ 30 pF
Clock fall time	tTHL		3	ns	CL≤ 30 pF
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	tISU	3		ns	CL≤ 30 pF
Input hold time	tIH	3		ns	CL≤ 30 pF
Outputs CMD, DAT (referenced to CLK)					
Output delay time during data transfer	tODLY		13.7	ns	CL≤ 30 pF
Output hold time	tOH	2.5		ns	CL≤ 30 pF
Signal rise time[5]	tRISE		3	ns	CL≤ 30 pF

Notes: 1. The Device must always start with the backward-compatible interface timing. The timing mode can be switched to high-speed interface timing by the host sending the SWITCH command (CMD6) with the argument for high-speed interface select.
2.CLK timing is measured at 50% of VDD.
3. For compatibility with Devices that support the v4.2 standard or earlier, host should not use > 26 MHz before switching to high-speed interface timing.
4. CLK rise and fall times are measured by min (VIH) and max (VIL).
5. tOSU and tOH are defined as values from clock rising edge. However, there may be Devices or devices which utilize clock falling edge to output data in backward compatibility mode. Therefore, it is recommended for hosts either to settWL value as long as possible within the range which will not go over tCK-tOH(min) in the system or to use slow clock frequency, so that host could have data set up margin for those devices. In this case, each device which utilizes clock falling edge might show the correlation either between tWL and tOSU or between tCK and tOSU for the device in its own datasheet as a note or its application notes.

7.4.2 Bus Timing for DAT Signals During Dual Data Rate Operation

These timings apply to the DAT[7:0] signals only when the device is configured for dual data mode operation. In this dual data mode, the DAT signals operate synchronously of both the rising and the falling edges of CLK. The CMD signal still operates synchronously of the rising edge of CLK and therefore complies with the bus timing specified in section 10.7 of JESD84-B51, therefore there is no timing change for the CMD signal.

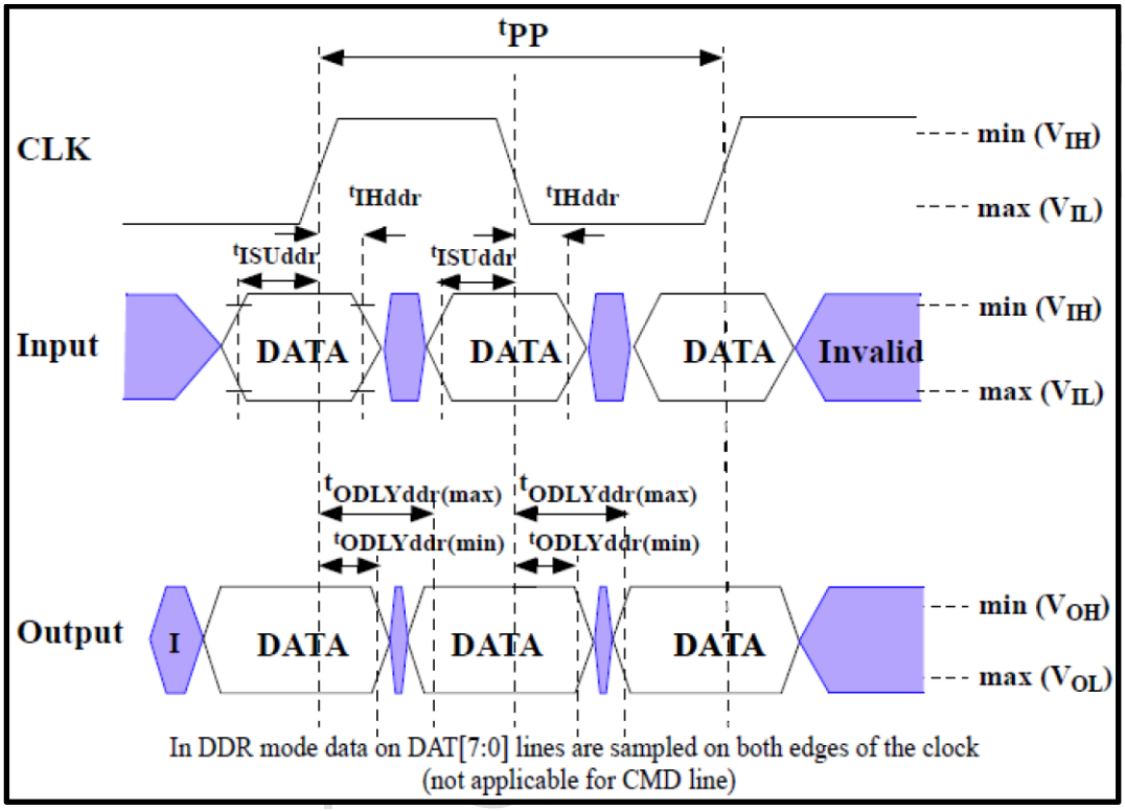


Figure 12 – Timing Diagram: Data Input/Output in Dual Data Rate Mode

7.4.3 Dual Data Rate Interface Timings

Table 30 – High-speed Dual Data Rate Interface Timing

Parameter	Symbol	Min	Max.	Unit	Remark
Input CLK[1]					
Clock duty cycle		45	55	%	Includes jitter, phase noise
Input DAT (referenced to CLK-DDR mode)					
Input set-up time	tISUddr	2.5		ns	CL≤ 20 pF
Input hold time	tIHddr	2.5		ns	CL≤ 20 pF
Output DAT (referenced to CLK-DDR mode)					
Output delay time during data transfer	tODLYddr	1.5	7	ns	CL≤ 30 pF
Signal rise time (all signals)[2]	tRISE		2	ns	CL≤ 30 pF
Signal fall time (all signals)	tFALL		2	ns	CL≤ 30 pF

Notes: 1. CLK timing is measured at 50% of VDD.
2. Inputs CMD, DAT rise and fall times are measured by min (V_{IH}) and max (V_{IL}), and outputs CMD, DAT rise and fall times are measured by min (V_{OH}) and max (V_{OL})

7.5 Bus Timing Specification in HS200 Mode

7.5.1 HS200 Clock Timing

Host CLK Timing in HS200 mode shall conform to the timing specified in Figure 14 and Table23. CLK input shall satisfy the clock timing over all possible operation and environment conditions. CLK input parameters should be measured while CMD and DAT lines are stable high or low, as close as possible to the Device.

The maximum frequency of HS200 is 200MHz. Hosts can use any frequency up to the maximum that HS200 mode allows.

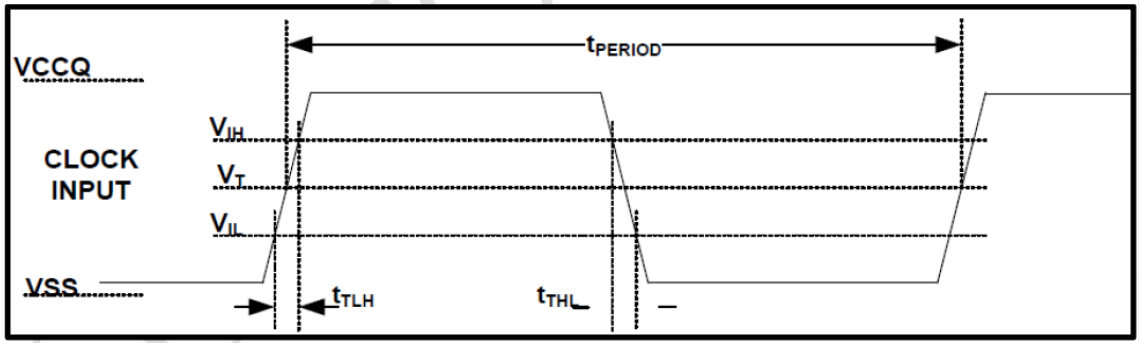


Figure 13 – HS200 Clock Signal Timing

Notes: 1. V_{IH} denote V_{IH}(min.) and V_{IL} denotes V_{IL}(max.).

0. V_T=0.975V – Clock Threshold, indicates clock reference point for timing measurements.

Table 31 – HS200 Clock Signal Timing

Symbol	Min.	Max.	Unit	Remark
t_{PERIOD}	5	-	ns	200MHz (Max.), between rising edges
t_{TLH}, t_{THL}	-	0.2* t_{PERIOD}	ns	t_{TLH}, t_{THL} < 1ns (max.) at 200MHz, C_{device} =12pF, The absolute maximum value of t_{TLH}, t_{THL} is 10ns regardless of clock frequency.
Duty Cycle	30	70	%	

7.5.2 HS200 Device Input Timing

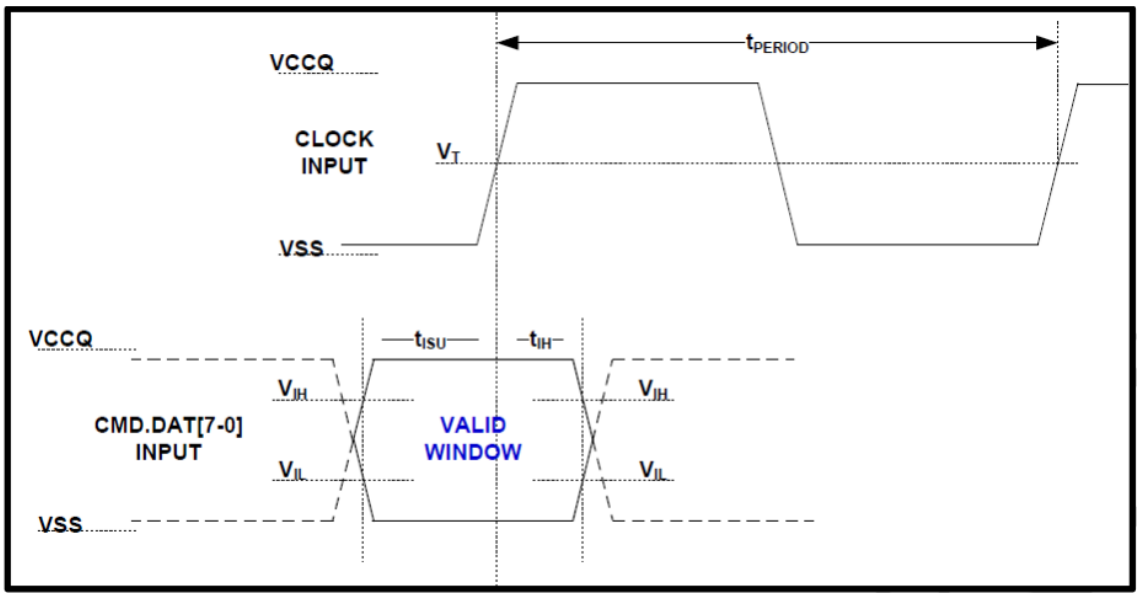


Figure 14 – HS200 Device Input Timing

Notes: 1. T_{ISU} and t_{IH} are measured at VIL (max.) and VIH (min.).

0. VIH denote VIH (min.) and VIL denotes VIL(max.).

Table 32 – HS200 Device Input Timing

Symbol	Min.	Max.	Unit	Remark
t_{ISU}	1.4	-	ns	C_{device} ≤ 6pF
t_{IH}	0.8	-	ns	C_{device} ≤ 6pF

7.5.3 HS200 Device Output Timing

tPH parameter is defined to allow device output delay to be longer than tPERIOD. After initialization, the tPH may have random phase relation to the clock. The Host is responsible to find the optimal sampling point for the Device outputs, while switching to the HS200 mode. Figure 16 and Table 20 define Device output timing. While setting the sampling point of data, a long term drift, which mainly depends on temperature drift, should be considered. The temperature drift is expressed by ΔTPH. Output valid data window (tVW) is available regardless of the drift (ΔTPH) but position of data window varies by the drift, as described in Figure 17.

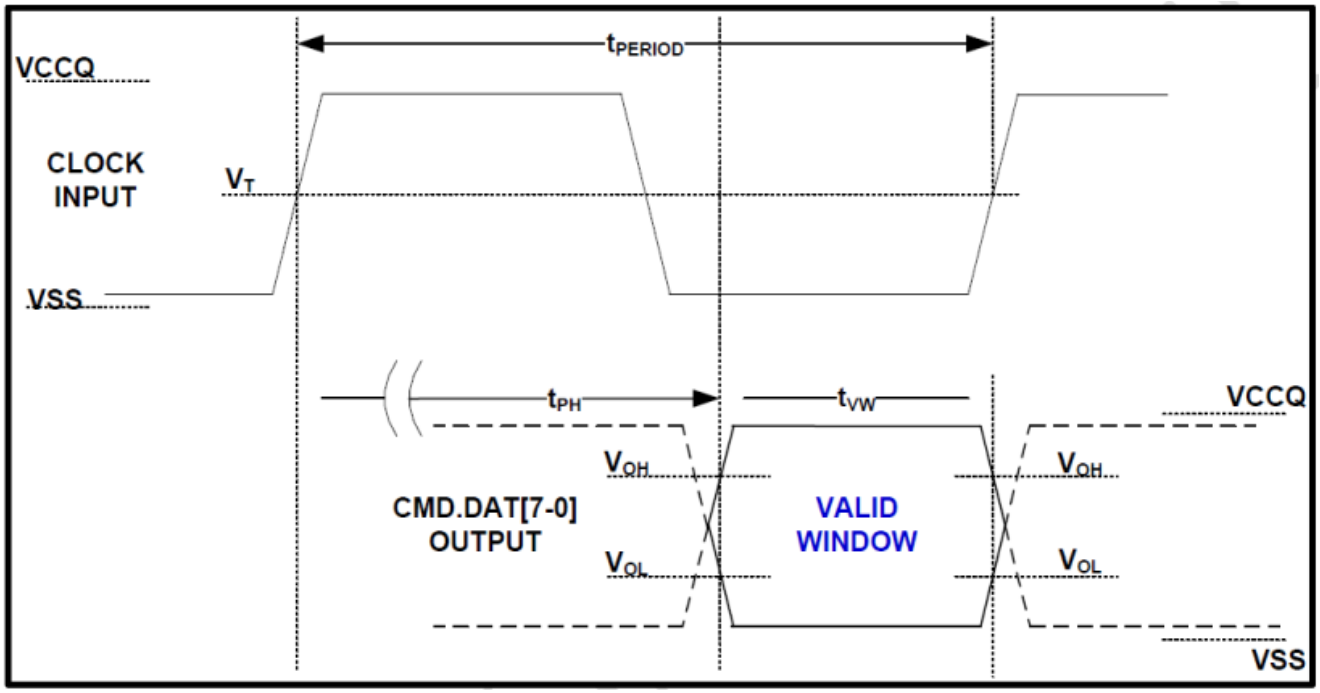


Figure 15 – HS200 Device Output Timing

Notes: 1. VOH denotes VOH(min.) and VOL denotes VOL(max.).

Table 33 – Output Timing

Symbol	Min.	Max.	Unit	Remark
t_{PH}	0	2	UI	Device output momentary phase from CLK input to CMD or DAT lines output. Does not include a long term temperature drift.
ΔT_{PH}	-350 (ΔT=-20°C)	+1550 (ΔT=90°C)	ps	Delay variation due to temperature change after tuning. Total allowable shift of output valid window (T_{VW}) from last system Tuning procedure ΔT_{PH} is 2600ps for ΔT from -25°C to 125°C during operation.
T_{VW}	0.575		UI	t_{VW}=2.88ns at 200MHz Using test circuit in Figure 18 including skew among CMD and DAT lines created by the Device. Host path may add Signal Integrity induced noise, skews, etc. Expected T_{VW} at Host input is larger than 0.475UI.

Notes: 1. Unit Interval (UI) is one bit nominal time. For example, UI=5ns at 200MHz.

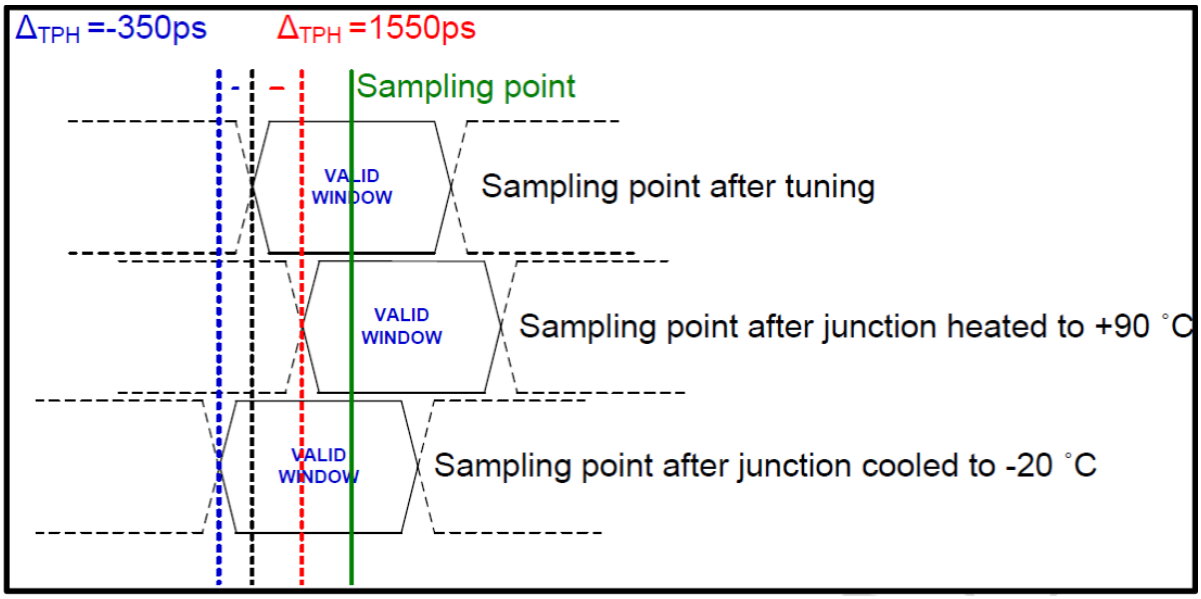


Figure 16 – ΔT_{PH} consideration

Implementation Guide: Host should design to avoid sampling errors that may be caused by the ΔT_{PH} drift. It is recommended to perform tuning procedure while Device wakes up, after sleep. One simple way to overcome the ΔT_{PH} drift is by reduction of operating frequency.

7.6 Bus Timing Specification in HS400 mode

7.6.1 HS400 Device Input Timing

The CMD input timing for HS400 mode is the same as CMD input timing for HS200 mode. Figure 17 show Device input timing

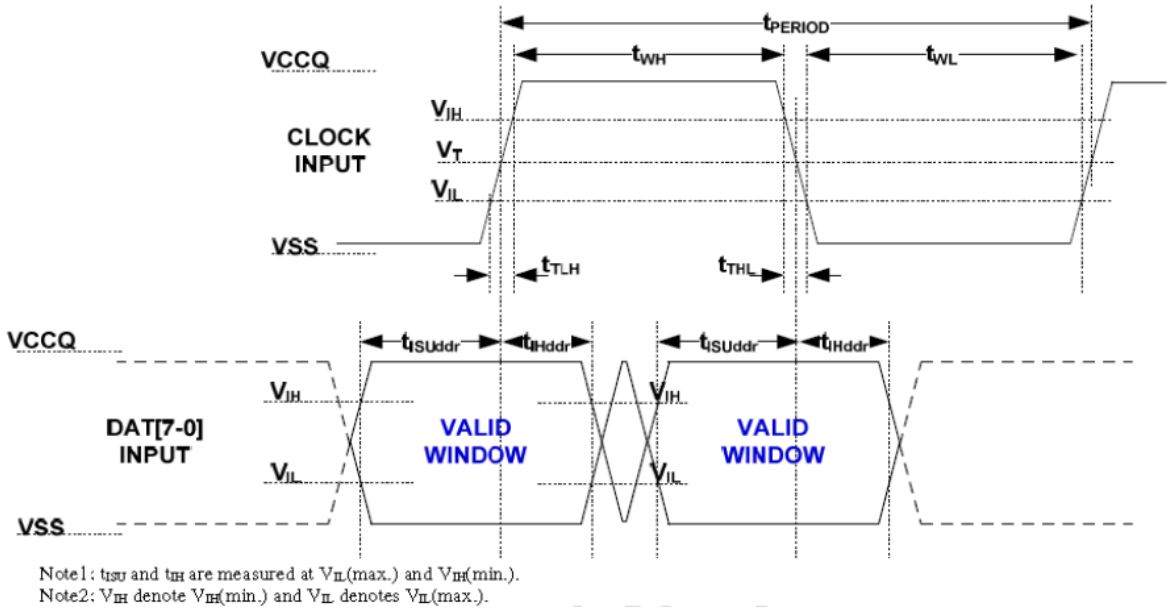


Figure 17 – HS400 Device Data input timing

Table 34 – HS400 Device input timing

	Symbol	Min	Max.	Unit	Remark
Input CLK					
Cycle time data transfer mode	tPERIOD	5			200MHz(Max), between rising edges With respect to VT.
Slew rate	SR	1.125		V/ns	With respect to VIH/VIL
Duty cycle distortion	tCKDCD	0.0	0.3	ns	Allowable deviation from an ideal 50% duty cycle. With respect to VT. Includes jitter
Minimum pulse width	tCKMPW	2.2		ns	With respect to VT.
Inputs DAT (referenced to CLK)					
Input set-up time	tISUddr	0.4		ns	Cdevice ≤ 6pF With respect to VIH/VIL.
Input hold time	tIHddr	0.4		ns	Cdevice ≤ 6pF With respect to VIH/VIL.
Slew rate	SR	1.125		V/ns	With respect to VIH/VIL.

7.6.2 HS400 Device Output Timing

The Data Strobe is used to read data in HS400 mode. The Data Strobe is toggled only during data read or CRC status response.

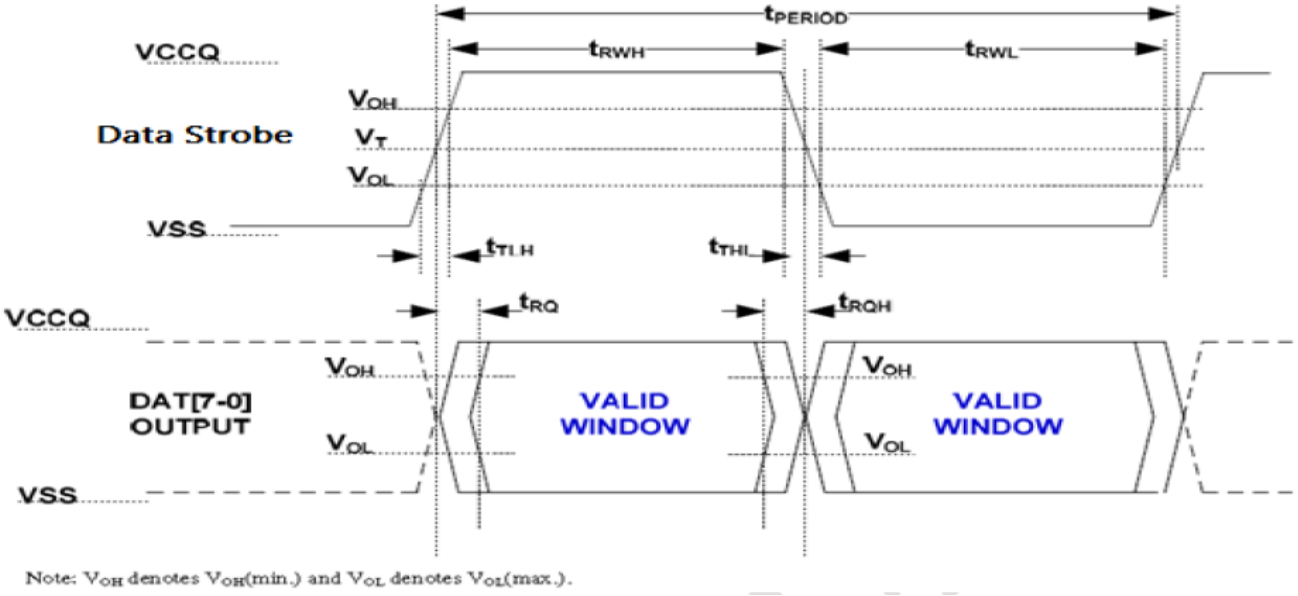


Figure 18 – HS400 Device output timing

Table 35 – HS400 Device Output timing

Parameter	Symbol	Min	Max.	Unit	Remark
Data Strobe					
Cycle time data transfer mode	tPERIOD	5			200MHz(Max), between rising edges With respect to VT.
Slew rate	SR	1.125		V/ns	With respect to VOH/VOL and HS400 reference load
Duty cycle distortion	tDSDCD	0.0	0.2	ns	Allowable deviation from the input CLK duty cycle distortion (tCKDCD) With respect to VT Includes jitter, phase noise
Minimum pulse width	tDSMPW	2.2		ns	With respect to VT.
Read pre-amble	tRPRE	0.4		ns	Max value is specified by anufacturer. Value up to infinite is valid
Read post-amble	tRPS	0.4		ns	Max value is specified by anufacturer. Value up to infinite is valid
Onputs DAT (referenced to Data Strobe)					
Slew rate	SR	1.125		V/ns	With respect to VOH/VOL and HS400 reference load

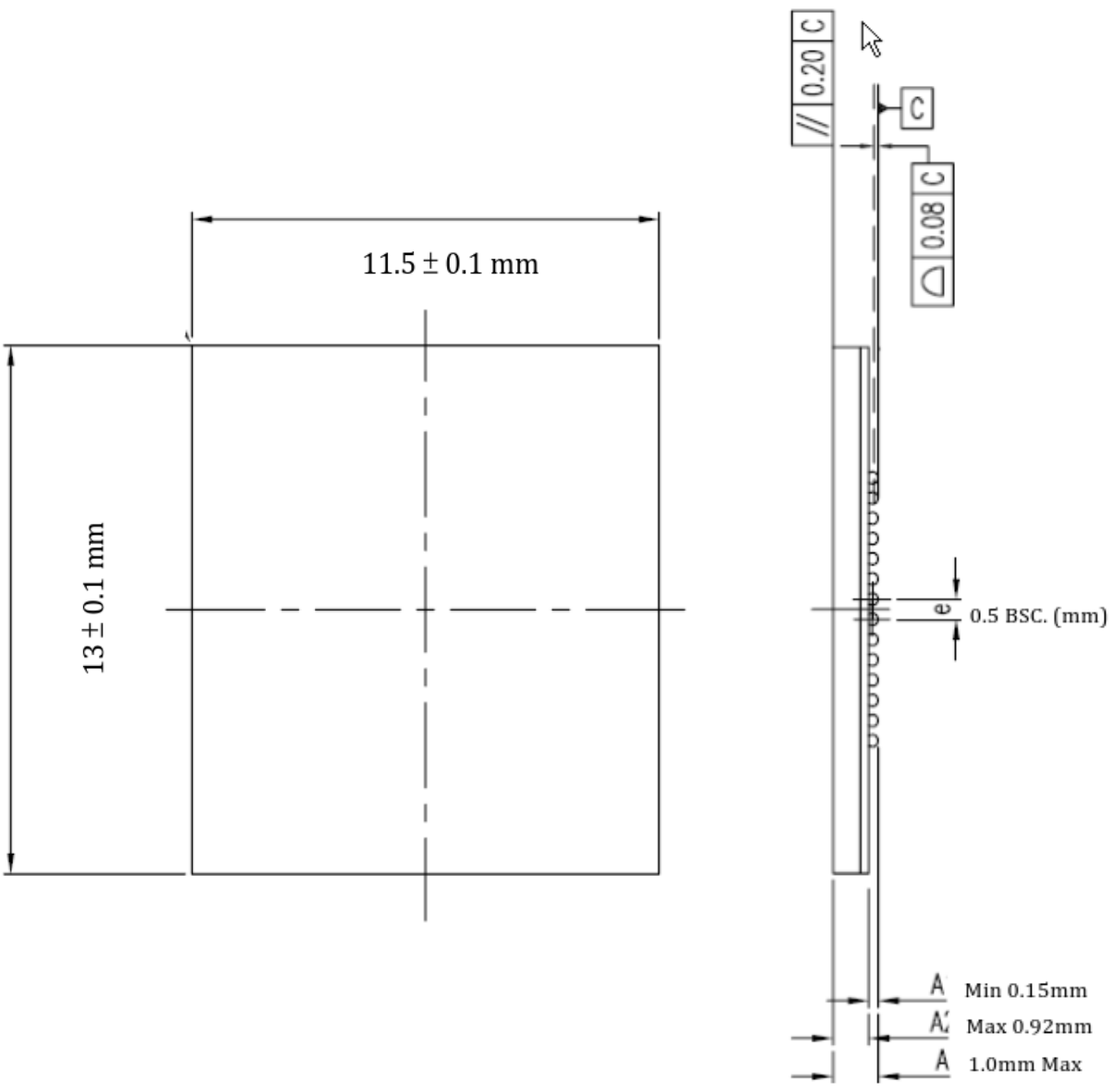
Table 36 – HS400 Capacitance

Parameter	Symbol	Min	Max.	Unit	Remark
Pull-up resistance for CMD	RCMD	4.7	50	Kohm	
Pull-up resistance for DAT0-7	RDAT	10	50	Kohm	
Pull-down resistance for Data Strobe	RDS	10	50	Kohm	
Internal pull up resistance DAT1-DAT7	Rint	10	150	Kohm	
Single Device capacitance	Cdevic		6	pF	

8 Package Dimensions

8.1 Package Dimensions

11.5 mm x 13.0 mm x 1.0 mm



8.2 Ball Pattern Dimensions (Bottom View)

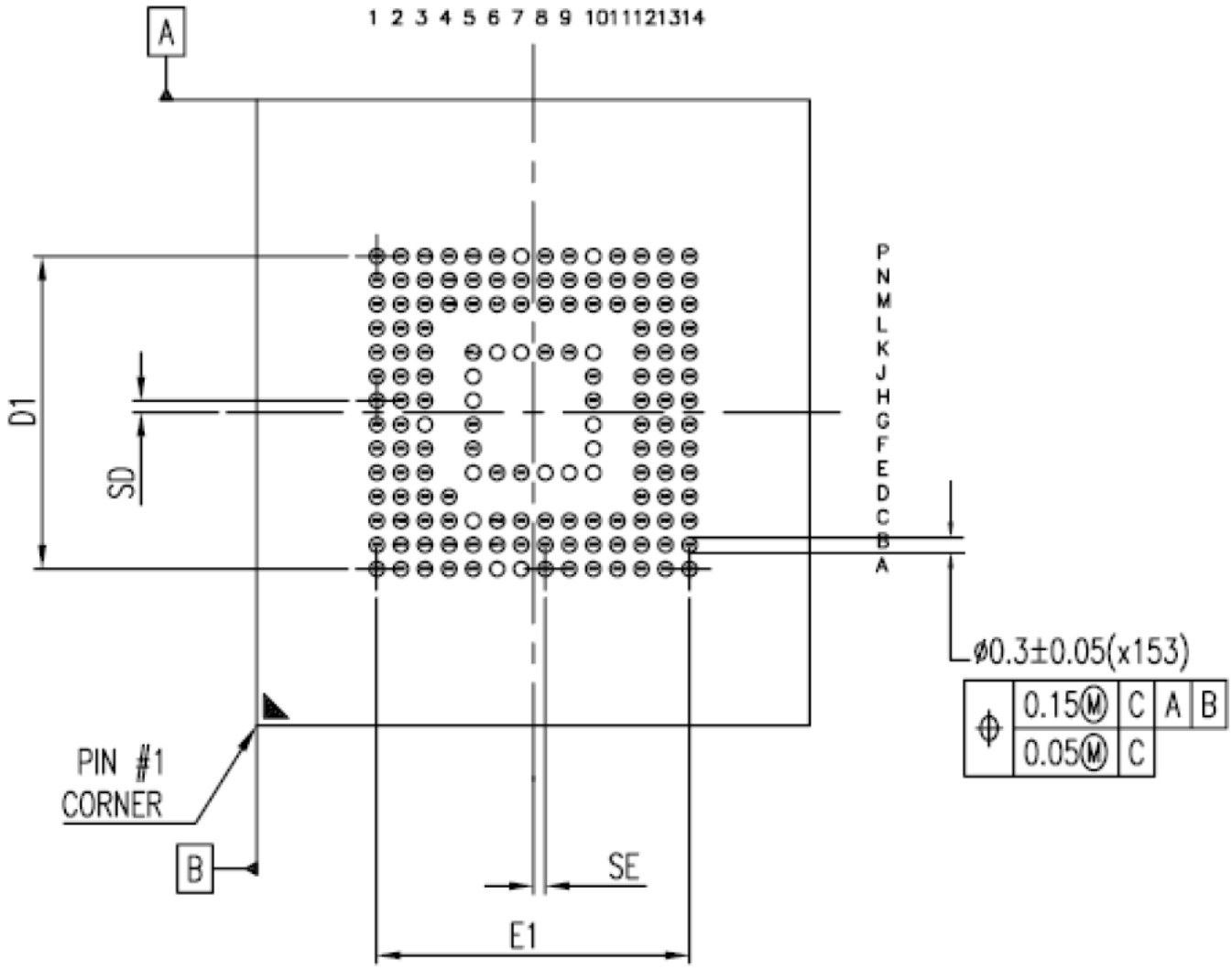


Figure 19 – Ball Pattern Dimensions

N	SE(MM)	SD(MM)	E1(MM)	D1(MM)	JEDEC(REF)
153	0.25 BSC.	0.25 BSC.	6.50 BSC.	6.50 BSC.	MO-276 BA

8.3 Ball Assignment (153 balls)

Ball Assignment, Top view

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	
14	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	14
13	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	13
12	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	12
11	NC	NC	NC									NC	NC	NC	11
10	NC	NC	NC		VSF	VSF	VSF	VSS	VCC	VSF		NC	NC	VSF	10
9	NC	NC	NC		VSF					VCC		NC	NC	NC	9
8	NC	NC	NC		VSF					VSS		NC	NC	NC	8
7	RFU	NC	NC		VSS					RFU		NC	NC	RFU	7
6	VSS	DAT7	VCCQ		VCC					RFU		CLK	NC	VSSQ	6
5	DAT2	DAT6	NC		RFU	VCC	VSS	DS	VSS	RST_n		CMD	VSSQ	VCCQ	5
4	DAT1	DAT5	VSSQ	NC								VCCQ	VCCQ	VSSQ	4
3	DAT0	DAT4	NC	NC	NC	NC	RFU	NC	NC	NC	NC	NC	NC	VCCQ	3
2	NC	DAT3	VDDi	NC	NC	NC	NC	NC	NC	NC	NC	NC	VSSQ	NC	2
1	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	1
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	

Figure 20 – Ball Assignment (Top View)

9 eMMC Device Signal

The eMMC device transfers data via a configurable number of data bus signals. The communication signals as below Table.

Table 37 – Device Signal

Name	Type	Ball No.	Description
CLK	Input	M6	Clock: each cycle directs a 1-bit transfer on the command and DAT lines.
CMD	Input	M5	Command: A bidirectional channel used for device initialization and command transfers. Command has two operating modes: 1. Open-drain for initialization. Push-pull for fast command transfer.
DAT	I/O	A3 ~ A5 B2 ~ B6	Bidirectional data channels, which are used for data transfer.
RST_n	Input	K5	H/W reset signal pin
DS	Output	H5	Newly assigned pin for HS400 mode. Data Strobe is generated from eMMC to host. In HS400 mode, read data and CRC response are synchronized with Data Strobe.
VCC	Supply	E6, F5, J10, K9	Supply voltage for NAND flash memory, its voltage range is from 2.7V to 3.6V
VCCQ	Supply	C6, M4, N4, P3, P5	Supply voltage for MMC interface and Controller. VCCQ have two power mode: 1. High power mode: 2.7V to 3.6V Lower power mode: 1.7V to 1.95V
VSS, VSSQ	Supply	VSS: A6, E7, G5, H10, J5, K8 VSSQ: C4, N2, N5, P4, P6	Ground connections
VDDi	--	C2	Internal power node to stabilize regulator output to controller core logic. Connect 0.1uF or 2.2uF capacitor from VDDi to ground

Revision History

Revision	Descriptions	Release Date
0.85	Preliminary Release	October, 2024
0.86	Revised Part number table	November, 2024
1.0	Release version of datasheet	November, 2024
1.1	Revised Part number table (Corrected Temperature Grade)	November, 2024