Features

NGC1081 is an IC, suitable and optimized for NFC communication controlled actuation and sensing. It contains a NFC transceiver, an actuation interface, a sensing unit, a microcontroller and wired communication interfaces. NGC1081 is available in a 32-pin package.

The chip can operate in two different power supply modes:

- active supply mode:
  - The chip is supplied by an external 3V power supply source (e.g. battery).
- passive supply mode:
  - The chip is harvesting energy from the external NFC RF field. No additional external supply source is required. Of course, operation of the chip requires the presence of the NFC field in this use case. The chip can charge external capacitors, in order to store harvested energy. External storing capacitors can be used to store the required amount of energy to initiate an actuation action (e.g. to drive a motor).

Main product features are:

- contact-less communication interface NFC
  - PICC according to ISO/ IEC 14443 Type A
  - data rate 106 kBit/s
  - initialization and anti-collision protocol processed in firmware
  - proprietary and customizable application protocol optimized for end custom applications
- Integrated microcontroller
  - 32-bit ARM Cortex-M0 CPU operating at clock frequency of 28 MHz
  - nested vector interrupt controller with 18 interrupts
  - integrated system tick timer (SysTick)
  - MicroDMA with 8 DMA channels
  - 16 kByte integrated ROM containing start-up code and system development kit software library
  - 16 kByte integrated SRAM
  - 60 kByte integrated non volatile flash memory
  - Serial Wire Debug interface
  - multilayer AHB-Lite on chip interconnect
- Digital Peripherals
  - Up to 16 programmable and configurable General Purpose Input/ Outputs (GPIO)
  - System Timer Unit containing six independent timer channels and PWM generator
  - watchdog timer
  - arithmetic divide operation hardware accelerator
  - full duplex capable UART transceiver with Rx/ Tx FIFOs
  - SPI master/ slave transceiver with Rx/ Tx FIFOs
  - AES accelerator
  - I^2C master/ slave transceiver
  - Real Time Clock
- Actuation interface
  - integrated H-Bridge driver capable to direct drive a motor up to peak current of 250 mA
  - ability to control an external H-bridge driver IC by applying gate drive control signals to GPIO
- Sensing Interface
  - Analog to Digital Converter (12-Bit SAR) with four different Input channels
  - Digital to Analog Converter (10-Bit)
  - Comparator
  - Current to Voltage Converter

  - integrated high precision temperature sensor
  -
- embedded Security
  - embedded AES hardware accelerator
  - True Random Number Generator (TRNG)
- Power Management
  - Ultra Low Power power saving Mode available
    - chip supply for almost all parts of the chip is switched off, except a small always-on power domain
    - entering power saving mode and configuring wake up sources is controlled by embedded software
    - chip can wake up by either detecting an external NFC RF field, expiration of an internal wake Up Timer or an external trigger event on a dedicated pin
  - software controlled CPU idle mode
  - CPU clock control by software
  - dedicated and software controlled switchable LDOs for sensing unit and flash memory
- Clock Generation
  - integrated 28 MHz oscillator for internal system clock generation
  - integrated ultra low power 32 kHz oscillator for "always on" standby clock generation
  - integrated oscillator pads to support external 32 kHz crystal
- Power Supply modes
  - passive supply Mode
    - energy is harvested from the external NFC RF field and the power supply of the chip is derived from the harvested energy
    - no external supply source apart from the NFC RF field required
  - active supply mode
    - the chip is supplied by an external supply source and operational, if no NFC field is applied
- Product qualified according to JEDEC Standard

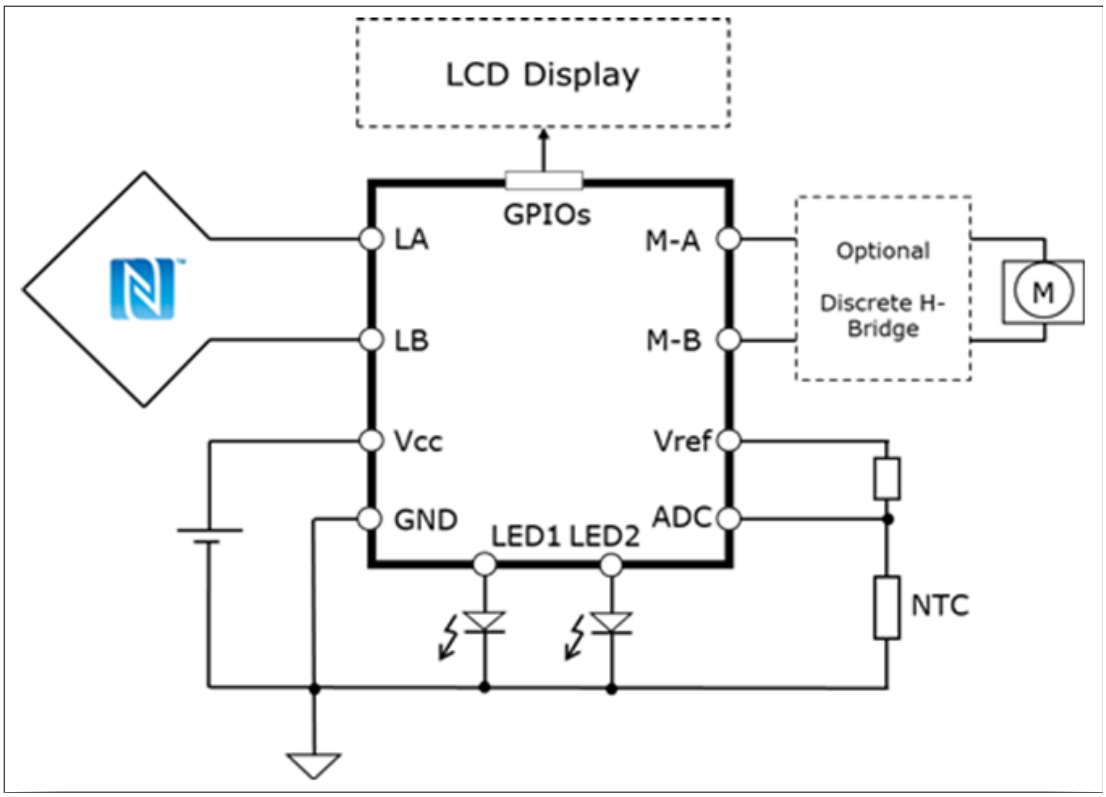
Potential applications

Potential applications and application use cases of NGC1081 are applications, which require embedded control together with a contact less communication interface, an actuation interface/ driver, a sensing and measurement interface and optional passive supply mode operation based on RF field energy harvesting.

That might be:

- NFC configured and controlled environmental sensing and data logging
- NFC configured thermostats
- NFC activated smart lock
- Health Care Passive Sensor

An example application diagram for lock application in passive supply mode is given:



Thermostat Example

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1 NGC1081 Pin Description

This section provides the pin description of NGC1081.

Table 1 NGC1081 Pin Description

Name	Pin at QFN-32	Characteristic	Direction	Comment
LA	18	analog	Input (internally load modulated)	NFC Antenna Pin LA
LB	19	analog	Input (internally load modulated)	NFC Antenna Pin LB
M_A	4	analog	In/Output	Motor A (driven by H-Bridge)
M_B	5	analog	In/Output	Motor B (driven by H-Bridge)
VCC	21	Supply	Input	external Supply (3.0V … 3.3V)
GND	3	Ground	Input	Ground Net
VCC_HB	6	Supply	Input/Output	Supply of H-Bridge output drivers - in passive supply mode to be connected to external energy storage element (capacitor); the energy is to be stored is harvested from the RF field - in active supply mode to be connected to the external supply (3.0 … 3.3V) *-if H-Bridge output driver is **not used** in application then:* • *in passive supply mode it should kept open or connect to an external capacitor (recommendation 1nF)* • *in active supply mode connect it to the external supply or GND*
VCC_CB	20	Supply	Input	in active mode connect to external supply (3.0V … 3.3V) - in passive mode connect to external capacitor (recommendation 2.2 uF)
Wake_UP	22	analog	input/Output	external Wake-Up - if not used in target application, then connect to GND
GPIO0	17	2.5V LVCMOS	Input/Output	General Purpose Input/Outputs with: • programmable direction and output value
GPIO1	14			
GPIO2	10			
GPIO3	8			

(table continues...)

Table 1 (continued) NGC1081 Pin Description

Name	Pin at QFN-32	Characteristic	Direction	Comment
GPIO4	1			• configurable internal Pull Up/ Pull Down Resistors • programmable alternate functions
GPIO5	31			
GPIO6	28			
OSC-A	11	2.5V LVCMOS	Input/Output	32-kHz Oscillator pins, to be connected to external crystal or single ended clock signal at OSC-A
OSC-B	12			
AN_OUT	23	analog	Output	Digital to Analog Converter output voltage of Sensing Unit
AN_IN0	27	analog	Input	Analog to Digital Converter input voltages of sensing unit
AN_IN1	26			
AN_IN2	25			
AN_IN3	24			
GPIO7	16	2.5V LVCMOS	Input/Output	• programmable direction and output value • configurable internal Pull Up/ Pull Down Resistors • programmable alternate functions
GPIO8	15			
GPIO9	13			
GPIO10	9			
GPIO11	7			
GPIO12	2			
GPIO13	32			
GPIO14	30			
GPIO15	29			

2 NGC1081 General Architecture

The general architecture is illustrated by the following block diagram:

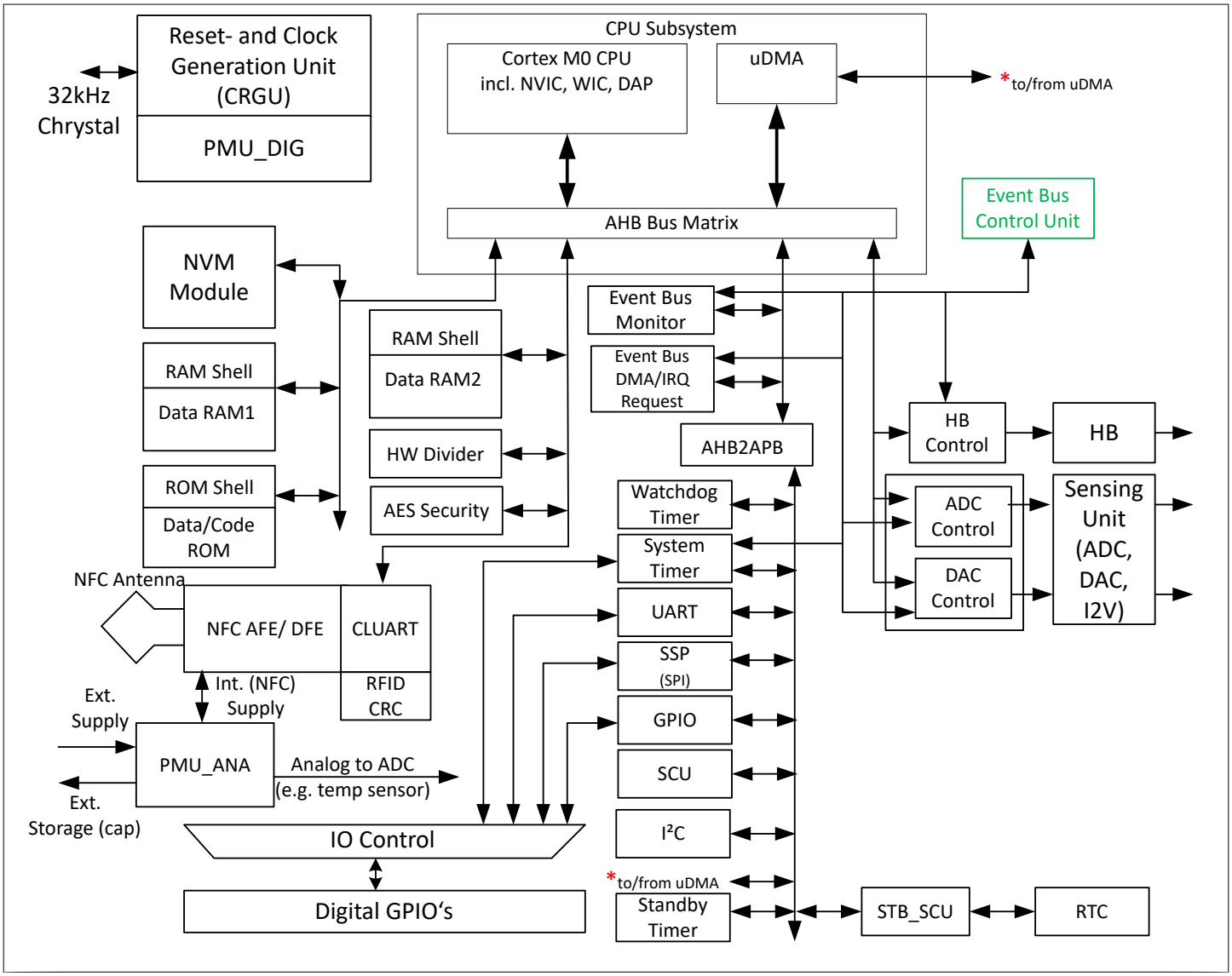

Figure 2 NGC1081 Block Diagram

3 NGC1081 Functional Description

Topics:

- NGC1081 Clock Generation
- NGC1081 Power Management
- NGC1081 Real Time Clock
- NGC1081 Sensing Unit
- NGC1081 Near Field Communication
- NGC1081 H-Bridge
- NGC1081 System Timer Unit
- NGC1081 Security Support
- NGC1081 General Purpose Inputs/Outputs
- NGC1081 SPI Controller Peripheral
- NGC1081 UART
- NGC1081 I^2C Peripheral

Topics

- NGC1081 Clock Generation
- NGC1081 Real Time Clock
- NGC1081 Sensing Unit
- NGC1081 Near Field Communication
- NGC1081 H-Bridge
- NGC1081 System Timer Unit
- NGC1081 Security Support
- NGC1081 General Purpose Inputs/Outputs
- NGC1081 SPI Controller Peripheral
- NGC1081 UART
- NGC1081 I^2C Peripheral

ARM Cortex M0 CPU

Details of the ARM Cortex-M0 CPU can be derived from the ARM Cortex-M0 technical reference manual.
The Cortex-M0 is configured with the following parameters:

- Nested Interrupt Controller NVIC with 18 IRQ lines plus NMI
- System Timer Option (*Systick*) enabled
- Fast (Single Cycle) Multiplier
- Support of Wake Up Controller with 20 Wake-Up Sources (18 IRQ's + NMI + RX Event)
- Reset of all registers enabled
- Debugging Option Enabled
  - Serial Wire Debug Interface (*SWD*)
  - Support of one hardware break point comparator

Furthermore NGC1081 integrates a direct memory access controller (*DMA*). Details of the DMA controller can be derived from the technical reference manual of the *"ARM PrimeCell DMA Controller (PL230)"*. In NGC1081 product the DMA controller is configured to serve ten independent DMA channels.

CPU Address Map

The CPU address space is used in NGC1081 as follows:

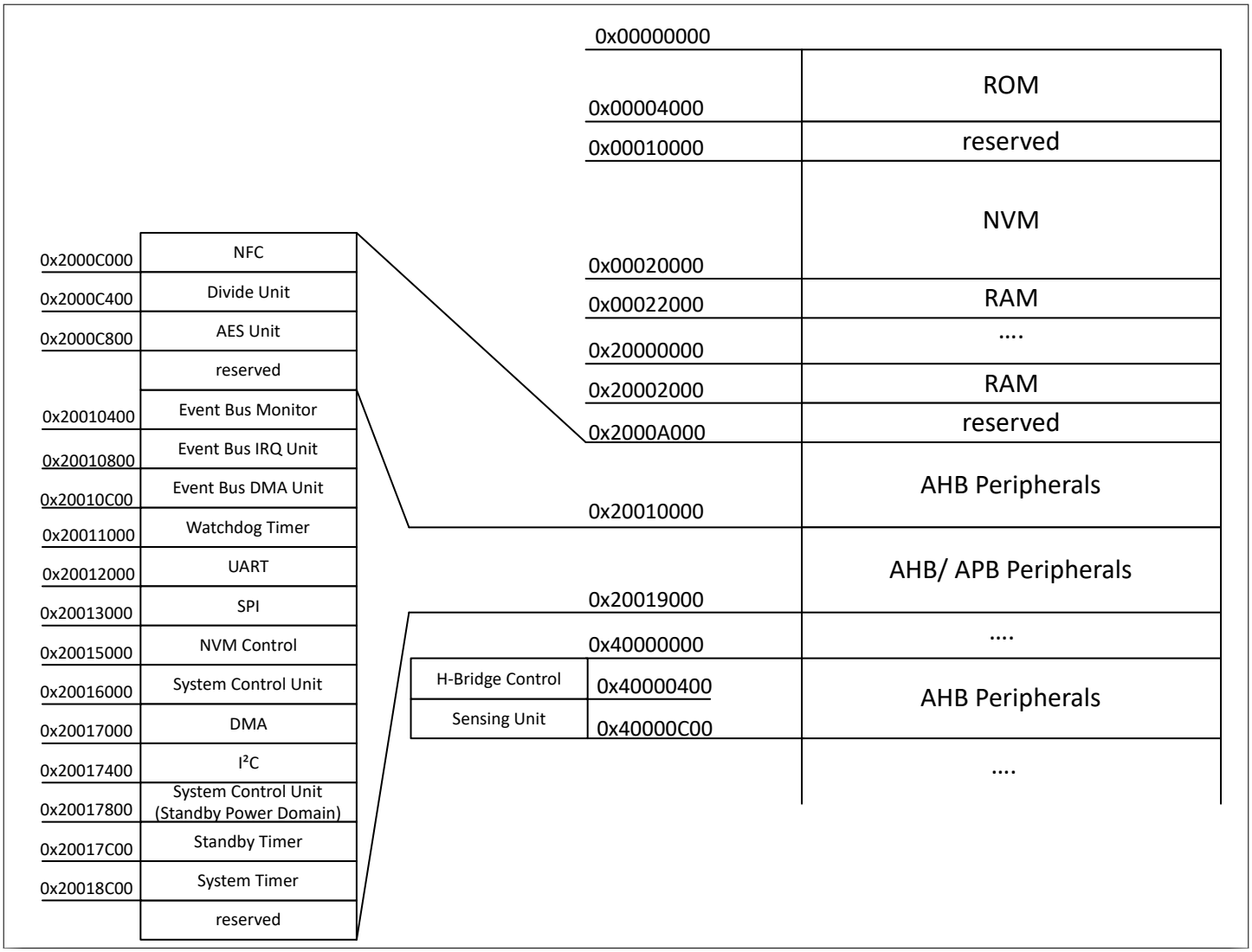

Figure 3 NGC1081 Address Map

Interrupts

In NGC1081 eighteen IRQs plus non mask-able interrupt are available. Following IRQ sources are assigned to the interrupts:

Interrupt	IRQ Source
NMI	Event Bus Interrupt Request/NMI
IRQ0	NFC frame data available
IRQ1	Event Bus Interrupt Request
IRQ2	Event Bus Interrupt Request
IRQ3	Event Bus Interrupt Request
IRQ4	Event Bus Interrupt Request
IRQ5	Event Bus Interrupt Request
IRQ6	Event Bus Interrupt Request
IRQ7	Event Bus Interrupt Request
IRQ8	Event Bus Interrupt Request

Interrupt	IRQ Source
IRQ9	Event Switch Matrix
IRQ10	Event Switch Matrix
IRQ11	Event Switch Matrix
IRQ12	Event Switch Matrix
IRQ13	Event Switch Matrix
IRQ14	Event Switch Matrix
IRQ15	Watchdog Timer Unit
IRQ16	Loss of NFC field
IRQ17	NVM busy

The event bus related interrupts have flexible IRQ sources, which are defined by the application run time software.

3.1 NGC1081 Clock Generation

Basically NGC1081 includes two major clock domains:

- A fast clock domain of 28 MHz: This clock is applied to the core supply domain. It is the CPU and peripheral clock. The fast clock is switched off during power save mode. In operating mode the fast clock is gated in CPU sleep mode.
- The standby clock domain of 32 kHz: This clock is applied to the standby "always on" power domain

Furthermore a clock is extracted from the NFC carrier, in case an NFC RF field is present. This clock of 13.56 MHz is used in the physical layer of the NFC transceiver and the related PHY layer digital logic.

The fast clock is generated on chip by an integrated clock oscillator. This clock oscillator is switched off in power save mode.

The standby clock can be sourced either by from an integrated oscillator or from an external crystal (connected to oscillator pins OSC_A and OSC_B). The nominal frequency of the crystal shall be 32.768 kHz. The integrated oscillator fits to a standard quartz with a load capacitive of 12.5 pF. The internal integrated 32 kHz oscillator does not reach the accuracy of a external quartz. The internal is measured during production test and trimmed to reach as close as possible the frequency of 32.768 kHz. The measured frequency of the trimmed integrated oscillator is finally stored in the non Volatile memory as a chip specific device parameter. The real time clock hardware is using this device parameter into account, when counting seconds. Hence a reasonable accuracy of real time clock sourced by internal oscillator can be achieved, which is sufficient for most application cases.

The fast clock oscillator is also measured and trimmed during manufacturing test. It will be trimmed as close as possible to a frequency of 28 MHz. The measured value of trimming is finally as well stored into the non volatile memory as a device parameter and can be used by hardware and firmware to for example to adjust baud rate generators of integrated UART or SPI.

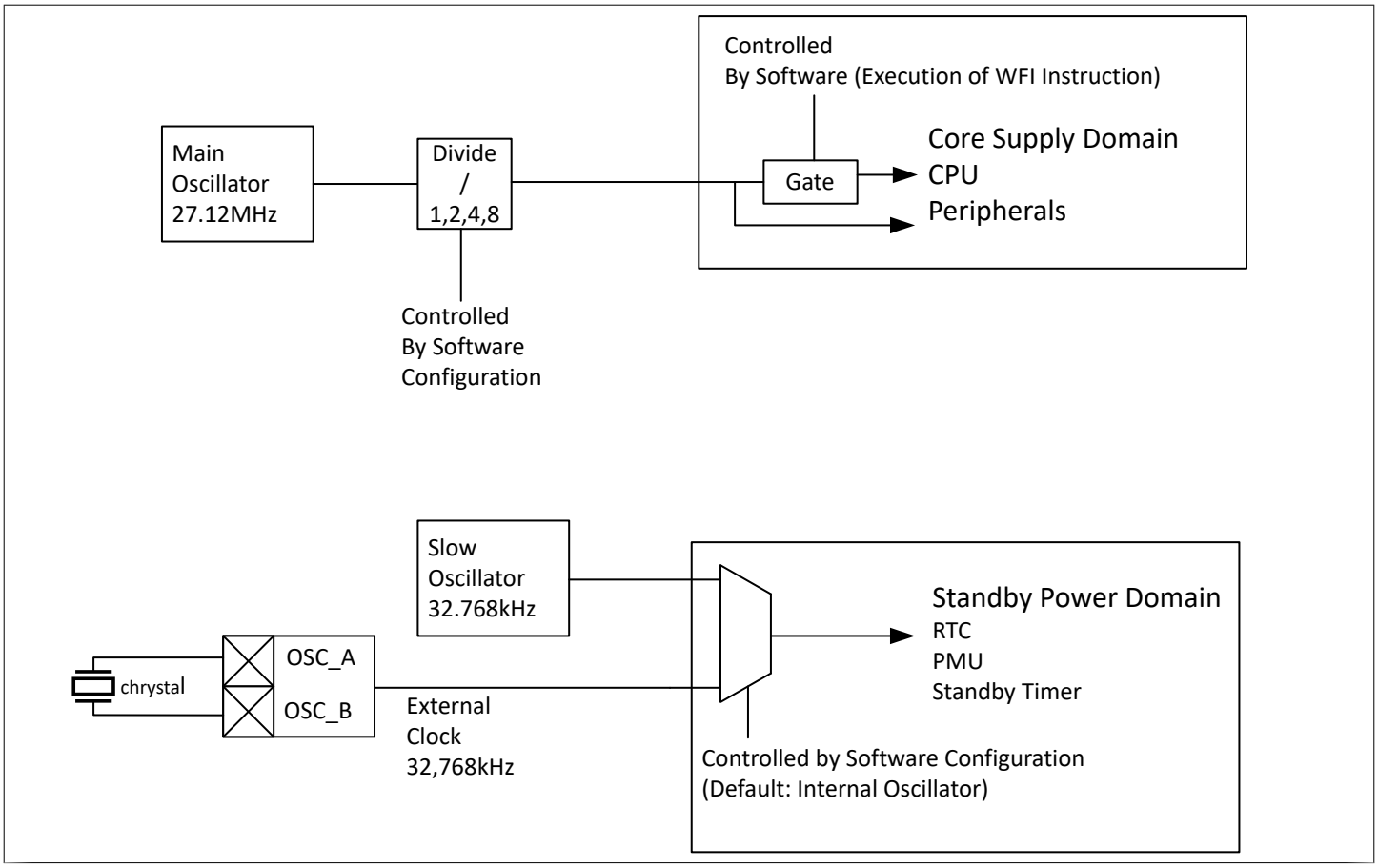

Figure 4 NGC1081 clock generation overview

I

3.2 NGC1081 Power Management

NGC1081 power management controls the power supply mode selection, the power on start-up and the power modes control.

NGC1081 can be supplied in two different supply modes:

- active supply mode:
  - in active supply mode an external supply voltage of has to be provided at pin VCC. The internal power management detects the presence of a supply voltage at pin VCC at power on and controls the proper start-up and operation.
- passive supply mode:
  - In passive supply mode no external supply source is required. The device is supplied by the energy of the RF field of NFC. The NFC receiver is harvesting the required energy from the field and the power management is controlling a proper start-up and operation

The device has different internal supply domains. Supply domains are internally separated from each other and are controlled by the power management. The purpose of separation of power supply domains are application dependent power saving and supply noise protection.

- core supply domain
  - This is a digital supply domain, which supplies the major part of digital logic and memories, including the CPU

- standby supply domain
  - This is a supply domain, which supplies a small part of the chip. It is an "always on" power domain, which includes the power management unit . Since it is responsible for power mode and status control and wake up , it needs to be permanently "on". Beside the power management it contains a wake up timer and a real time clock counter.
- NVM supply domain
  - This is a separate supply domain, which supplies the non volatile memory
- I/O supply domain
  - This supply domain supplies the digital I/Os.
- H-Bridge Driver Supply domain
  - This is a separate supply domain, which supplies the switching transistors of the H-Bridge. It is sourced by the external pin VCC_HB. In active supply mode an external supply source has to be connected to pin VCC_HB. In passive supply mode, an external storage capacitor has to be connected to pin VCC_HB. In passive supply mode this external storage capacitor will be charged by the power management in a controlled way with harvested energy from the external RF-field
- NFC Transceiver Power Domain
  - There is a small part of the NFC transceiver, which is sourced by the external RF field
- Sensing Unit Supply domain
  - This is a supply domain, which supplies the analog parts of the sensing unit. A separate voltage regulator generates a precise reference voltage for the analog to digital and digital to analog converter

The device integrates internal voltage regulators, which produce a stable output voltage in order to supply the domain specific circuitry. The internal voltage regulators are controlled by the power management and sourced by external supply at pin VCC in active supply mode or by supply harvested from RF field in passive mode. The pin VCC_CB is buffering the regulator input voltage by for example external capacitor. This is especially required in passive mode , when the RF field is low caused by NFC carrier modulation.

All chip internal supply domains, except the H-Bridge driver supply domain, are sourced by a dedicated internal voltage regulators.

The following figure gives an overview about the assignment of functions to power supply domains:

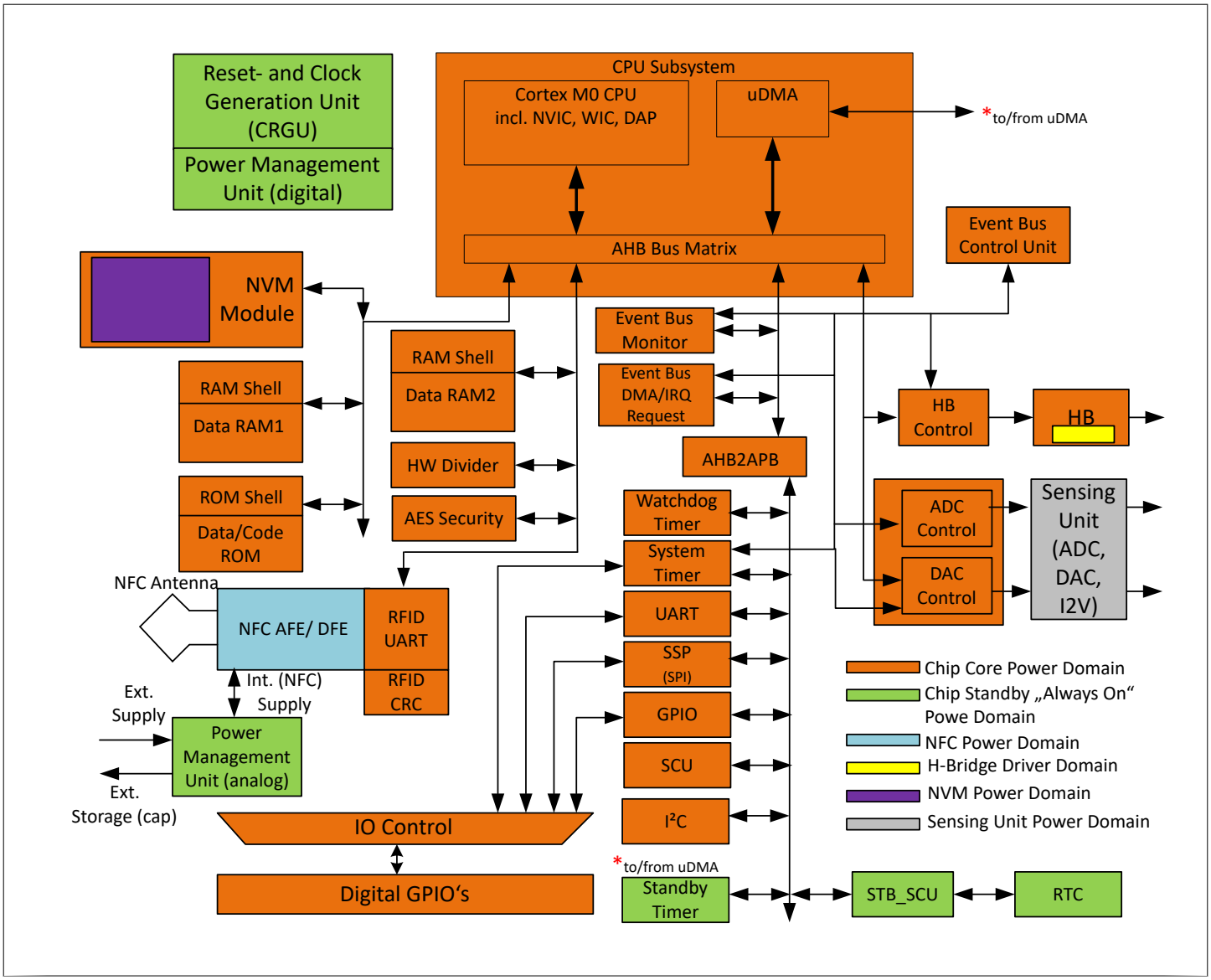

Figure 5 NGC1081 Power Domains

The device is operating in two supply modes:

- operating mode
- power save mode

In power saving modes major parts of the device is switched off.

Table 2 Power Mode

	Power Save Mode	Operation Mode
Standby Power Domain	ON	ON
Core Power Domain	OFF	ON
NFC Power Domain	ON, if NFC field is present. Otherwise OFF	ON, if NFC field is present. Otherwise OFF
I/O Power Domain	OFF	ON

(table continues...)

Table 2 (continued) Power Mode

	Power Save Mode	Operation Mode
NVM Power Domain	OFF	Power State controlled by CPU. (Default: ON)
H-Bridge Power Domain	OFF	ON
Main Clock Oscillator	OFF	ON
Standby Clock Oscillator	ON	ON
Sensing Unit Domain	OFF	Power State controlled by CPU (Default: OFF)

After applying external supply (or RF field in passive mode) the device will enter the operation mode. The CPU software can request a transition into power save mode to the power management. The power management will serve this request and perform the transition into power save mode. The CPU software will configure and enable the desired wake up condition(s) to leave the power save mode and to re-enter operating mode. Possible wake up conditions are:

- presence detection of a NFC field
- Valid logical level on the pin WAKE_UP present. The polarity of the desired wake up level can be configured by CPU.
- Standby Timer Expired. The standby timer unit can be enabled, to trigger a wake up event after a configured number of slow oscillator clock ticks are counted. The counting of slow clock ticks will start after power save mode is entered

In operating mode the system can enter a sleep mode state. The sleep mode will be entered, if the CPU is executing a *WFI (Wait For Interrupt)* or *WFE (Wait for Event)* instruction. The sleep mode is left, if an interrupt occurs. In sleep mode the clock of the CPU and memories is gated. Functional peripheral clocks are available. The clock gating of the CPU and memories provides a significant power save measure in operating mode. The fast clock of the system can be scaled as well by CPU software.

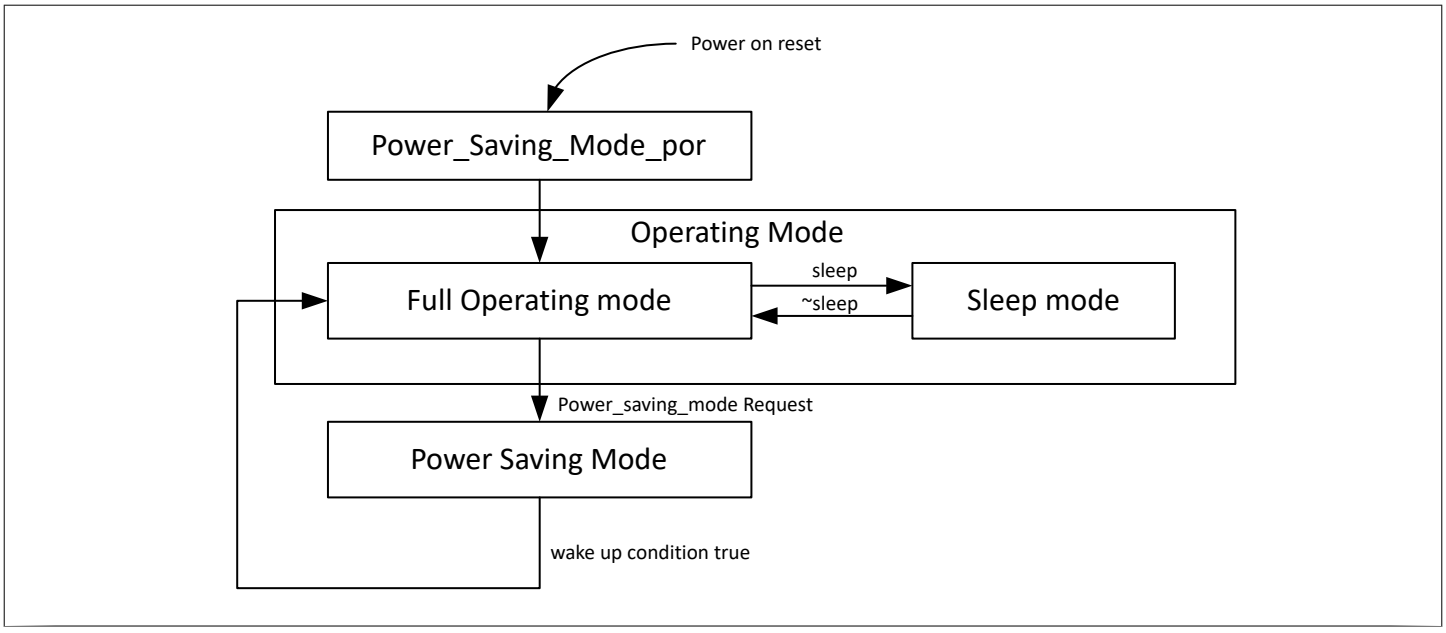

Figure 6 Power Management States

3.3 NGC1081 Real Time Clock

The Real Time Clock (RTC) of NGC1081 is located within the standby supply domain. After the real time clock is started (or enabled), it starts to count seconds, which are accumulated within a 32-bit register. This register can be read by software and the software can easily calculate the number of minutes, hours, days, weeks, months and years, which have passed after enabling the real time clock.

The clock reference for the second tick is either derived from the external 32-kHz crystal or from the internal standby clock oscillator. The non volatile flash memory contains a parameter, which contains the number of clock ticks of the internal standby clock oscillator within one second. This parameter is chip specific and measured within production test of NGC1081 and will be used by software during real time clock configuration.

In general the use of an external 32-kHz crystal (grade 50 ppm or less) as clock reference will provide a higher accuracy of the real time clock, compared to the internal standby clock oscillator. Nevertheless the use of the internal clock oscillator as clock reference is a reasonable and "bill of material" optimized alternative for application cases, which do not require 50 ppm or less accuracy.

3.4 NGC1081 Sensing Unit

The sensing unit is a flexible measurement interface.

It provides following functions:

- Analog to Digital conversion (ADC):
  - An 12-bit SAR ADC is integrated. The SAR ADC is connected to three Sample and Hold stages. Two of these sample and hold stages are sampling the four external analog voltages at pins AN_IN0, AN_IN1,AN_IN2, AN_IN3. The third sample and hold stage is sampling the temperature depending measurement voltage of the integrated temperature sensor
  - The sample and hold stages are active sample and hold stages. This means, after sampling is done, the sampled voltage keeps constant over time
  - An analog multiplexing scheme connects the sampling input of the sample and hold stages to the desired analog voltage
  - The ADC and the three sample and hold stages can individually be configured into an ultra low power consumption mode, if not used
- Digital to analog Conversion (DAC):
  - A 10 bit Digital to Analog converter is integrated
  - The digital to analog converter can be configured to an ultra low power consumption mode, if not used
  - The output of the DAC is measurable on pin AN_OUT
  - The output of the DAC is also the reference voltage of the comparator
- Comparator:
  - The comparator compares the voltage level of a selectable analog input pin to the output voltage of the digital to analog converter
  - The input of comparator can be selected between AN_IN0, AN_IN1, AN_IN2, AN_IN3
  - The comparator can be configured to an ultra low power consumption mode, if not used
  -
- Current to Voltage Converter:
  - The current to voltage converter converts the current, which is flowing through the pin AN_IN0 into a corresponding voltage. This voltage can be converted by the analog to digital converter and represents the measurement result of the current
  - The output of the current to voltage converter can be multiplexed to the sample and hold stages
  - The current to voltage converter can be configured to an ultra low power mode, if it is not used
- Temperature Sensor:
  - The sensing unit contains a temperature sensor
  - The temperature sensor is connected to a dedicated sample and hold stage
  - The temperature sensor can be configured to an ultra low power consumption mode, if it is not used

The overview schematic of the sensing unit is given hereby:

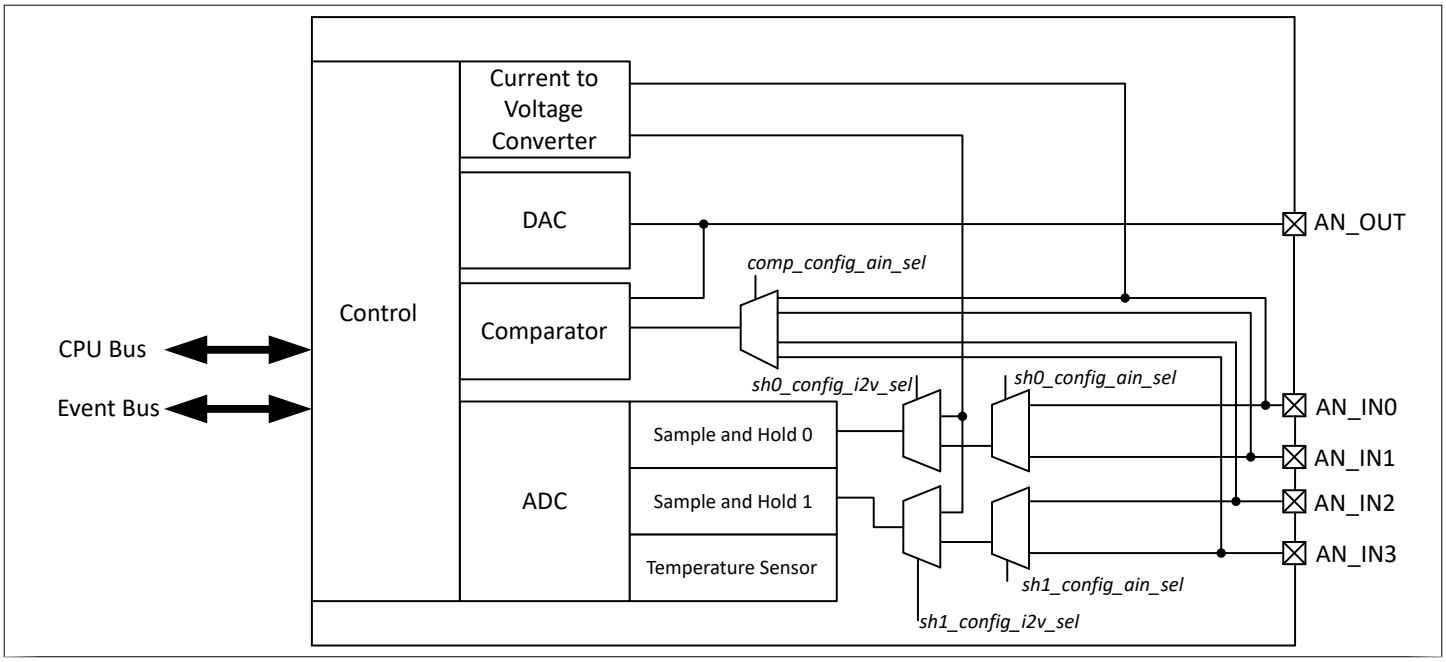

Figure 7 Sensing Unit Overview

The System ROM Library contains the required driver functions to configure the sensing unit, to trigger a measurement and to return the result and status of measurement.

3.5 NGC1081 Near Field Communication

NGC1081 supports Near Field Communication according to standard ISO/IEC 14443 Type A (PICC).

A data Rate of 106 kBit/s is supported.

The device includes a transceiver, which processes the physical layer and parts of link layer function of near field communication. The upper layers of communication are processed in software. The NFC protocol stack is part of the ROM system library.

The NFC communication link initialization and anti collision is fully compliant to the PICC initialization Type A procedure as defined in standard ISO-14443-3. NGC1081 is using a fixed unique RFID UID with length of 7 bytes. NGC-1081 is using proprietary protocol state with proprietary protocol commands.

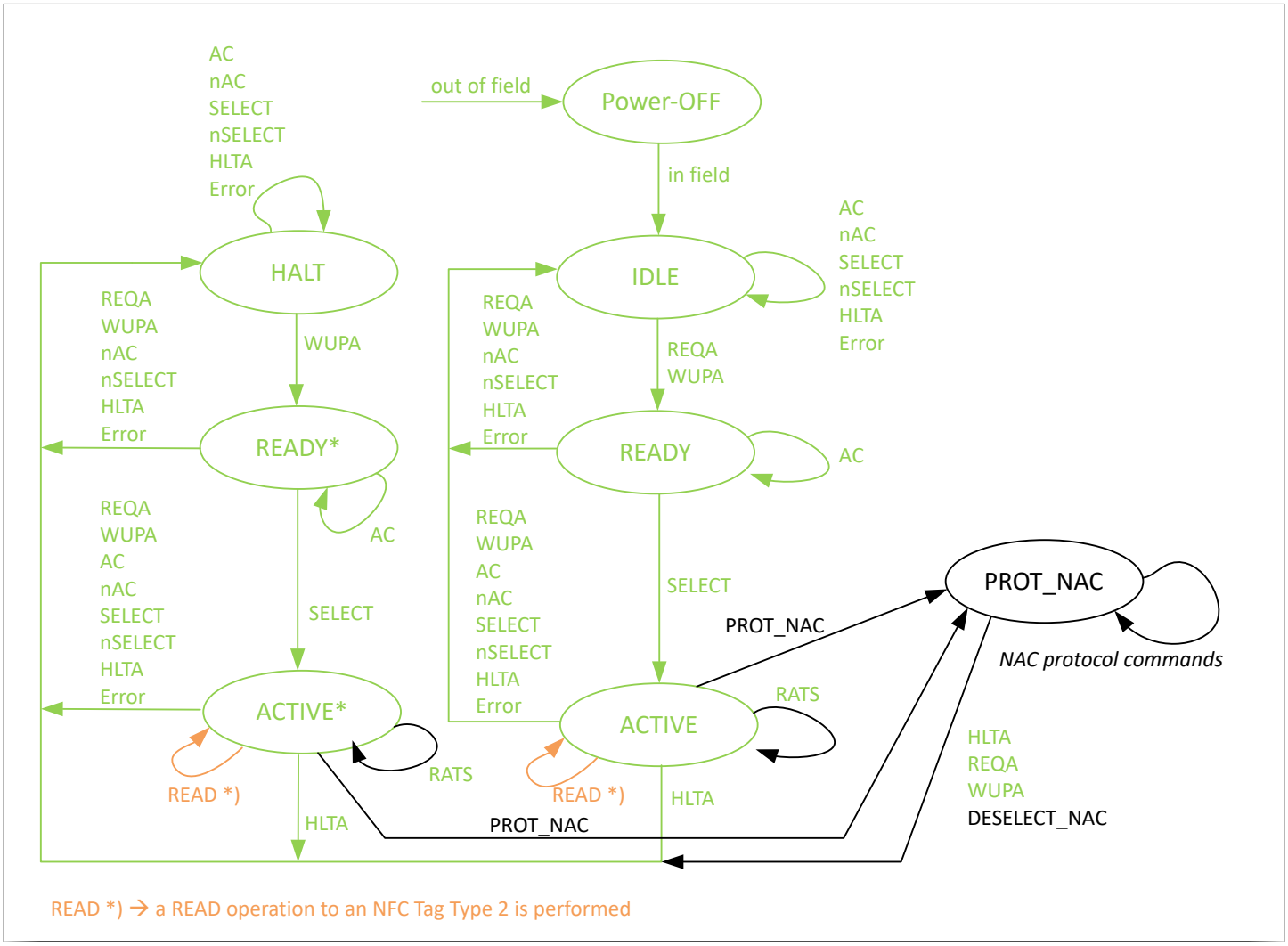

Figure 8 NGC1081 PICC states

The states and transition drawn in *green* are according to ISO14443-3. The transitions and states are drawn in *black* are proprietary. The transition into the proprietary protocol state is triggered in *ACTIVE/ACTIVE** state as the standard requires.

In protocol state *PROT_NAC* the NGC1081 is able to react on external requests. Following types of requests are possible:

- Read/Write Access to CPU address space
  - A read/write request to CPU address space is only granted, if the access to the specific address is authorized.

- Message Request
  - A message request will call a defined function of the ROM
- Call a CPU subprogram
  - A call of subprogram request will call an application specific subprogram located in the NVM
- Far End Loop back Test
  - NGC1081 will loop back received payload data of a loop back request frame

In *ACTIVE/ ACTIVE** state the NGC1081 accepts a NFC tag *READ* command. Using that command, a reserved area within the NVM can be read, which is considered to be compliant to an NFC tag type 2.

3.6 NGC1081 H-Bridge

The H-Bridge provides an on chip interface to control an external actuation element, like an electrical motor. The H-Bridge driver is suitable to switch voltages up to 3.6V at a peak current of up to 250 mA.

A simplified functional diagram describes the H-bridge driver function.

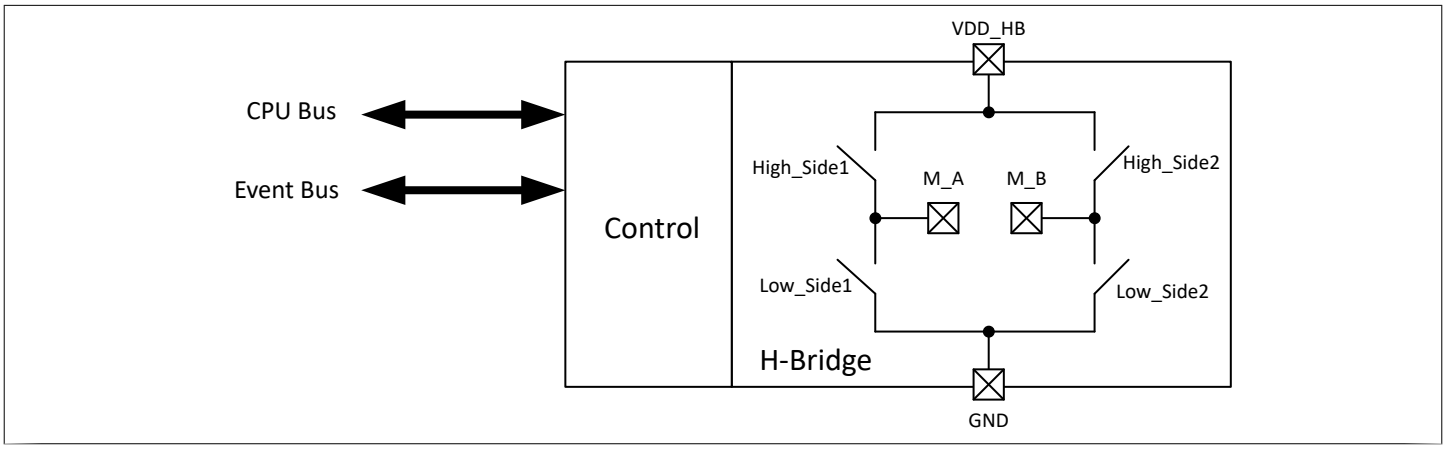

Figure 9 H-Bridge simplified functional view

Basically the H-bridge consists of 4 switching transistors, which are individually controlled by the CPU via the CPU bus or the event bus. An external load (e.g. a motor) will be connected to the pins M_A and M_B. In case the switches *High_Side1* and *Low_Side2* are closed and the other two switches are open, then a current will flow from *VDD_HB* via pin *M_A* to pin*M_B* to *GND*. In case *High_side2* and *Low_side1* are closed and the other two switches are open, the current will flow from pin *M_B* to pin *M_A*.

The system ROM library contains driver functions to configure and control the H-bridge.

3.7 NGC1081 System Timer Unit

The system timer unit consists of 6 independent programmable timer channels (16-bit).

A timer can operate in :

- continuous mode
- single shot mode

The timer per

If a timer expires, an IRQ request could be generated or an event could be sent to the event bus.

A timer can be started by CPU software access or by receiving an timer start event on the event bus.

System timer channels can be chained, in order to increase the timer length up to maximum 96 bit.

The system ROM library contains the necessary functions to configure and control the system timer unit.

3.8 NGC1081 Security Support

NGC1081 supports two security features by hardware:

- AES encryption and decryption
- True Random Number Generation

The AES accelerator hardware supports encryption and decryption operations with key length of 128-bit. The accelerator hardware encrypts or decrypts a 128-bit data gram within 16 clock cycles.

The True Random Number Generator generates a sequence of 128 random bits within 5 microseconds.

The system ROM library contains security driver functions to calculate the result of a data encryption or decryption operations and to generate a random number.

3.9 NGC1081 General Purpose Inputs/Outputs

General Purpose Input and Outputs are bidirectional input/output structures.

The output state of a GPIO can be set by the Cortex-M0 CPU. The input state of a GPIO can be read by the Cortex-M0 CPU.

Beside to the CPU read/write access to the GPIO, alternate port functions can be enabled . An alternate port function connects the GPIO port to the input or output of an internal hardware peripheral (for example to connect a selected GPIO to the TxD of UART).

A GPIO port consists of:

- input stage
- output driver
- internal Pull Up resistor
- internal Pull Down resistor

The input stage can be enabled or disabled by CPU software. In case of disabled input stage, the CPU will always read a logic *HIGH* level. The output driver can be enabled or disabled by CPU software or controlled by an alternate function control signal, if an alternate function is selected. The internal pull up resistor can be enabled or disabled by CPU software. The internal pull down resistor can be enabled or disabled by CPU software. The output characteristic can be set by CPU software to CMOS Push-Pull output or Open Drain output.

The system ROM library contains the required functions to configure and control the GPIOs and to select alternate port functions.

Table 3 Alternate GPIO Functions GPIO0-7

	GPIO0	**GPIO1**	**GPIO2**	**GPIO3**	**GPIO4**	**GPIO5**	**GPIO6**	**GPIO7**
Primary Output	OUT0	OUT1	OUT2	OUT3	OUT4	OUT5	OUT6	OUT7
Alternate Output 1	SPI TxD	SPI Clock Out		SPI Frame Sync Out			Debugger Data	
Alternate Output 2	UART TxD		UART TxD	reserved	reserved	reserved	reserved	
Alternate Output 3	PWM Out	PWM Out	PWM Out	reserved	reserved	reserved	reserved	
Primary Input	IN0	IN1	IN2	IN3	IN4	IN5	IN6	IN7
Alternate Input 1			SPI RxD		SPI CLKIN	SPI Frame Sync In	Debugger Data	
Alternate Input 2	UART RxD		UART RxD			Debugger Clock		
Alternate Input 3	reserved	reserved	reserved	reserved	reserved	reserved	reserved	

Table 4 Alternate GPIO Functions GPIO8-15

	GPIO8	**GPIO9**	**GPIO10**	**GPIO11**	**GPIO12**	**GPIO13**	**GPIO14**	**GPIO15**
Primary Output	OUT8	OUT9	OUT10	OUT11	OUT12	OUT13	OUT14	GPIO15

(table continues...)

Table 4 (continued) Alternate GPIO Functions GPIO8-15

	GPIO8	GPIO9	GPIO10	GPIO11	GPIO12	GPIO13	GPIO14	GPIO15
Alternate Output 1	Trigger Timer 0	Trigger Timer 1	Trigger Timer 2	Trigger Timer 3	I^2C Data Out	I^2C Clock Out	Trigger Timer 4	Trigger Timer 5
Alternate Output 2	reserved	reserved	reserved					
Alternate Output 3	reserved	reserved	reserved	reserved			PWM Out	PWM Out
Primary Input	IN8	IN9	IN10	IN11	IN12	IN13	IN14	IN15
Alternate Input 1					I^2C Data In	I^2C Clock In		
Alternate Input 2								
Alternate Input 3	reserved						reserved	reserved

3.10 NGC1081 SPI Controller Peripheral

The SPI controller peripheral provides compatibility to following interface types :

- Motorola SPI
- Texas instruments serial synchronous interface (SSI)
- National Semiconductor micro-wire interface

It can operate in master or in slave mode.

It contains a receive FIFO buffer and a transmit FIFO buffer, of eight entries of 16 bit width.

When operating in SPI mode, frame sizes of 4 to 16 bit are supported. It provides a full duplex synchronous data transfer utilizing 4 wires. Clock polarity and clock phase are programmable.

The SPI signals can be mapped to general purpose IOs using alternate input and output functions.

3.11 NGC1081 UART

The product contains an UART transceiver peripheral.

Following features are included:

- full duplex capable UART
- Separate 32x8 transmit and 32x12 receive First-In, First-Out memory buffers (FIFOs) to reduce CPU interrupts.
- Programmable baud rate generator
- Programmable line characteristics:
  - one or two STOP bits
  - support of 5, 6, 7 or 8 data bits
  - even, odd, stick, or no-parity bit generation and detection

Start-bit, stop-bit and parity-bit are added prior to transmission within the transceiver in transmit direction and processed and removed in receive direction.

The UART ports can be mapped to general purpose IOs using alternate input and output functions.

The product does not support the modem control functions like CTS, RTS et .

3.12 NGC1081 I²C Peripheral

The device includes an I²C peripheral, which is offloading the processor from processing the I²C protocol.
Major product features are:

- master or slave operation
- Support of multi master systems
- Support of 10-bit addressing
- Support of speeds up to 400 Kbit/s
- Own address and General Call address detection
- Arbitration and clock synchronization

4 NGC1081 Electrical Characteristics

Table 5 Absolute Maximum Ratings

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Input peak voltage between LA-LB	V_{Inpeak}			3.6	V_{Peak}	
Absolute Maximum Field Strength for indefinite exposure without damage. The chip functionality can be affected.	H_{absmax}			10	A/m	
Absolute Maximum Field Strength for exposure for up to 10 seconds without damage. The chip is not guaranteed to function	$H_{absmax12}$			12	A/m	Conditions: $T_{joperating}$ = 110°C
Input peak voltage at VCC, VCC_HB, VCC_CB	V_{CC}, V_{CC_HB}, V_{CC_CB}	0		3.6	V	
electrostatic discharge voltage Human Body model	V_{ESD_HB}			2	kV	ANSI/ESDA/JEDEC JS-001
electrostatic discharge voltage charged device model	V_{ESD_CDM}			500	V	ANSI/ESDA/JEDEC JS-002
Storage Temperature	$T_{Storage}$	-40		125	°C	
Operating Temperature	$T_{Ambient}$	-40		85	°C	Ambient temperature range, where device is operating. The operation in NFC system requires a NFC reader, which is operational within the $T_{Ambient}$ temperature range. All external system components need to support the full $T_{Ambient}$ range, if the full $T_{Ambient}$ range is used.

Table 6 static characteristics

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
The static parameters are valid for the Ambient Temperature range T_A of -25°C to 85°C.						

(table continues...)

Table 6 (continued) static characteristics

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Supply Pins						
Supply Voltage	V_{CC}, V_{CC_HB}, V_{CC_CB}	2.8	3.0	3.3	V	
Supply Current	I_{CC}			5	mA	average value and operating mode dependent, CPU running at 27 MHz, NVM access enabled
Power Down Mode Supply Current	I_{CC_PD}		30		uA	Chip is in Power Down Mode and wait for Wake Up Event, RTC and Standby Timer active
GPIO Pins						
HIGH Level input Voltage	V_{IH}	1.75		3.6	V	
LOW Level input Voltage	V_{IL}	0		0.7	V	
HIGH Level Output Voltage	V_{OH}	2.2			V	load 1mA
Low Level Output Voltage	V_{OL}			0.2	V	load 1mA
Pull-Up Resistance	R_{PU}		200		kOhm	
Pull-Down Resistance	R_{PD}		200		kOhm	
Wake-Up Pin						
Wake Up Threshold HIGH Level	V_{WU_HIGH}	2			V	
Wake Up Threshold Low Level	V_{WU_LOW}			0.4	V	
Antenna Pins						
Resonance Capacitance between terminals LA and LB	C_{Chip}		23.5		pF	

Table 7 NVM characteristics

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
The NVM are valid for the Ambient Temperature range T_A of -25°C to 85°C.						
Program/ Erase Cycles	NC	500k				Every Page, T =27°C
Data Retention after 100 cycles	DR	15			a	

Table 8 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
The Dynamic characteristics are valid for the Ambient Temperature range T_A of -25°C to 85°C.						
GPIO Pins						
Rise Time (output)	t_R	2		7	ns	capacitive load of 50pF
Fall Time (output)	t_F	2		7	ns	capacitive load of 50pF
Wake Up Pin						
Input Slope Low to High	t_{LH}	2		50	ns	
Input Slope High to Low	t_{HL}	2		50	ns	

Table 9 H-Bridge characteristics

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
The H_bridge characteristics are valid for the Ambient Temperature range T_A of -25°C to 85°C.						
Current between M_A and M_B	I_{HB}			250	mA	
Voltage at VCC_HB	VDDHB		3	3.6	V	VDDHB shall be smaller or equal to the voltage at pin VCC_CB. In passive supply mode this is guaranteed by chip internal control. In active supply mode pins VCC, VCC_HB, VCC_CB might be connected to the same supply source.

Table 10 Analog to Digital Converter characteristics

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
The ADC parameters are valid for the Ambient Temperature range T_A of -25°C to 85°C.						
Input Voltage Range	V_{AIN}	0		1.8	V	Pins AN_IN0, AN_IN1, AN_IN2, AN_IN3

(table continues...)

Table 10 (continued) Analog to Digital Converter characteristics

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Effective Number of Bits	ENOB		10			
Conversion Time	t_{conv}			15	us	
Sample Rate	F_{sample}			70k	Samples/s	
Active Current	I_{ADC_ACTIVE}		100		uA	average current consumption of analog supply domain of ADC during conversion
Powerdown Current	I_{ADC_PD}		100		nA	ADC in powerdown mode

Table 11 Digital to Analog Converter characteristics

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
The DAC parameters are valid for the Ambient Temperature range T_A of -25°C to 85°C.						
Analog Output Voltage Range	V_{AOUT}	0		1.7	V	Pin AN_OUT
ENOB	Effective Number of Bits	10			Bits	
Conversion Time	t_{CONV_DAC}			100	us	
Load Capacitance	C_{LOAD_DAC}			200	pF	
Load Resistance	R_{LOAD_DAC}	1			kOhm	
Integrated Non Linearity	INL		5	25	lsb	
Differential Non Linearity	DNL		6		lsb	
Source Current	I_{DAC}			1.7	mA	
Power Down Current	I_{DAC_PD}			250	nA	
Active Mode Current	I_{DAC_ACTIVE}			100	uA	Excluding external output AN_OUT drive

Table 12 Comparator characteristics

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
The comparator parameters are valid for the Ambient Temperature range T_A of -25°C to 85°C.						
Active Mode Current	I_{COMP_ACTIVE}			100	uA	
Power Down Current	I_{COMP_PD}			0.5	uA	
Reference Voltage range	V_{REF_COMP}	0		1.7	V	

(table continues...)

Table 12 (continued) Comparator characteristics

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Input Voltage Range	V_{RANGE_COMP}	0		1.8	V	
Settling Time	t_{SETTLE}			200	us	Voltage at AN_IN* stable and reference of DAC is settled

Table 13 Current to Voltage converter characteristics

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
The I2V parameters are valid for the Ambient Temperature range T_A of -25°C to 85°C.						
Active Mode Current	I_{I2V_ACTIVE}		50		uA	
Power Down Current	I_{I2V_PD}			0.5	uA	
Current Measurement Resolution	RES_{I2V}		1		uA	
Maximum Input Current	I_{MAX_I2V}	-0.5		0.5	mA	Pin AN_IN0

Table 14 Temperature Sensor characteristics

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
The temperature sensor parameters are valid for the Ambient Temperature range T_A of -20°C to 80°C.						
Active Mode Current	I_{TEMP_ACTIVE}			5	uA	
Power Down Current	I_{TEMP_PD}			50	nA	
Temperature Resolution	T_{TEMP_RES}		0.1		°C	
Temperature Accuracy	T_{TEMP_ACC1}	-0.3		+0.3	°C	Temperature Range from 0°C to 45°C
Temperature Accuracy	T_{TEMP_ACC2}	-0.4		+0.4	°C	Temperature Range from -20°C to 0°C and from 45°C to 85°C
Measurement Time	t_{MEAS_TEMP}			50	us	

5 NGC1081 Package Outline

NGC1081 is offered in PG-VQFN-32 package. The geometry is provided in the subsequent figure.

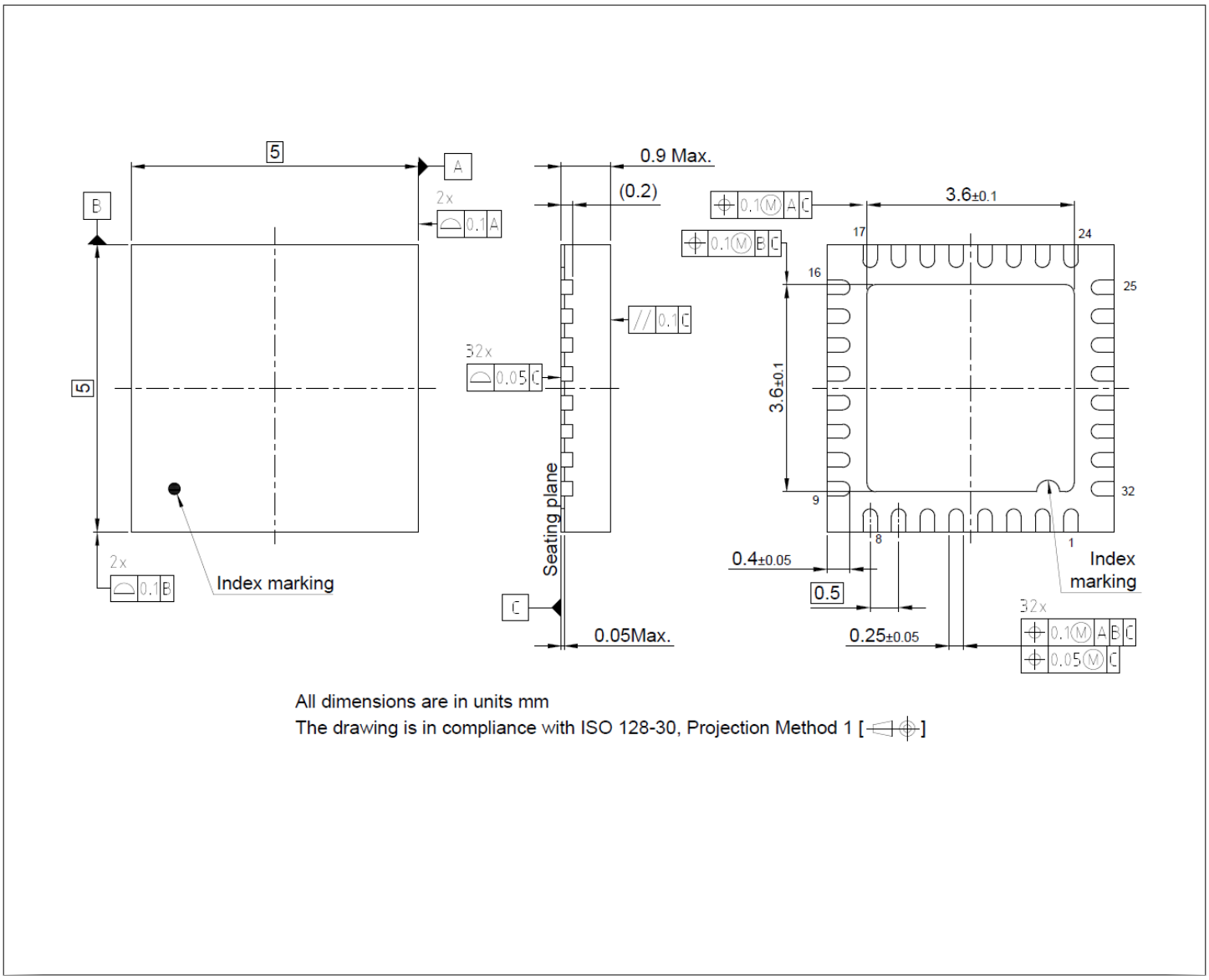

Figure 10 NGC1081 package drawing

Revision history

Document version	Date of release	Description of changes
1.0	2023-02-16	• initial release
1.1	2023-07-19	• added operating temperature to Electrical Characteristics

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