

ISL8282M

15A High Efficiency Hybrid Digital Step-Down Power Module

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The [ISL8282M](#) is a PMBus enabled DC/DC single channel step-down power supply featuring the proprietary Renesas R4™ Technology. The module supports a wide 4.5V to 16.5V input voltage range and a wide 0.5V to 5V output range capable of delivering up to 15A of continuous current. The ISL8282M achieves up to 95% conversion efficiency and is optimized for high power density. Integrated LDOs provide module bias voltage allowing for single supply operation. The ISL8282M includes a SMBus/PMBus/I²C interface for device configuration, telemetry (V_{IN} , V_{OUT} , I_{OUT} , and temperature), and fault reporting.

The proprietary Renesas R4 control scheme has extremely fast transient performance, accurately regulated frequency control, and all internal compensation. An efficiency enhancing PFM mode greatly improves light-load efficiency. The ISL8282M's serial bus allows for easy R4 loop optimization that results in fast transient performance across a wide range of applications including all ceramic output filters.

The ISL8282M has four 8-bit configuration pins that provide very flexible configuration options (such as frequency, V_{OUT} , and AV gain) without the need for built-in NVM memory. As a result, the design flow closely matches traditional analog modules while still offering the design flexibility and feature set of a digital SMBus/PMBus/I²C interface. The ISL8282M features remote voltage sensing, completely eliminates any potential difference between remote and local ground, and improves regulation and protection accuracy. A precision enable input coordinates the startup of the ISL8282M with other voltage rails and is especially useful for power sequencing.

The ISL8282M integrates all power and most passive components to minimize the external components and significantly reduce design complexity and board space. The ISL8282M is available in a low-profile, thermally enhanced, compact 12mmx11mmx5.3mm fully encapsulated HDA package.

Applications

- Servers, telecom, storage, and datacom
- Industrial/ATE and networking equipment
- Graphics cards
- General purpose power for ASIC, FPGA, DSP, and memory

Features

- Proprietary Renesas [R4 Technology](#)
 - Linear control loop for optimal transient response
 - Variable frequency and duty cycle control during load transient for fastest possible response
 - Inherent voltage feed-forward for wide range input
- Input voltage range: 4.5V to 16.5V
- Output voltage range: 0.5V to 5V
- $\pm 1.5\%$ load/line/temperature regulation with remote sense
- Supports all ceramic solutions
- Integrated LDOs for single input rail solution
- SMBus/PMBus/I²C compatible up to 1.25MHz
- 256 boot-up voltage levels with a configuration pin
- Seven switching frequency options from 300kHz to 1MHz
- PFM operation option for improved light-load efficiency
- Startup into precharged load
- Power-good monitor for soft-start and fault detection
- Comprehensive fault protection for high system reliability
 - Over-temperature protection
 - Output overcurrent and short-circuit protection
 - Output overvoltage and undervoltage protection
 - Open remote sense protection
 - Input UVLO and power sequence, fault reset
- Compatible with Renesas [PowerNavigator™](#) software
- Thermally enhanced 12mmx11mmx5.3mm HDA package

Related Literature

For a full list of related documents, visit our website:

- [ISL8282M](#) device page

Contents

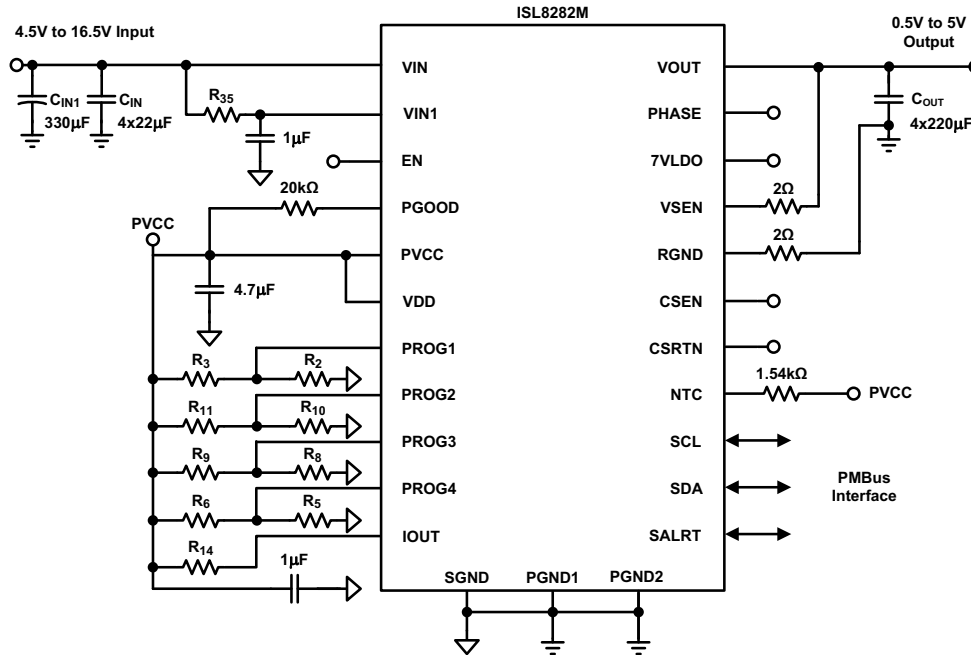
1. Overview	4
1.1 Typical Application Circuit	4
1.2 Block Diagram	5
1.3 Ordering Information	5
1.4 Pin Configuration	7
1.5 Functional Pin Descriptions	8
2. Specifications	11
2.1 Absolute Maximum Ratings	11
2.2 Thermal Information	11
2.3 Recommended Operating Conditions	12
2.4 Electrical Specifications	12
3. Typical Performance Curves	16
3.1 Efficiency Performance	16
3.2 Output Voltage Ripple	17
3.3 Load Transient Response Performance	19
3.4 Startup and Shutdown	20
3.5 Derating Curves	21
4. Functional Description	23
4.1 Configuring Internal Bias and LDO	23
4.2 Enabling and Disabling the ISL8282M	23
4.3 Programming the Resistor Reader	24
4.4 Soft-Starting	27
4.5 Boot-Up Voltage Programming	28
4.6 Thermal Monitoring and Compensation	35
4.7 Fault Protection	36
4.8 PGOOD Monitor	38
4.9 PFM Mode Operation	38
4.10 SMBus, PMBus, and I ² C Operation	38
5. Layout Guidelines	45
6. Thermal Considerations	46
7. Package Description	47
7.1 PCB Layout Pattern Design	47
7.2 Thermal Vias	47
7.3 Stencil Pattern Design	47
7.4 Reflow Parameters	48

8. **Revision History** 49

9. **Package Outline Drawing** 50

1. Overview

1.1 Typical Application Circuit



- For $V_{OUT} = 3.3V$, minimum V_{IN} is 5.5V; for $V_{OUT} = 5V$, minimum V_{IN} is 8V.
- R_{35} : see [Table 2 on page 9](#).
- R_2 and R_3 : to program output voltage, see [Table 4 on page 25](#) for typical V_{OUT} .
- R_{10} and R_{11} : to program PFM/PWM mode, temperature compensation, and PMBus address, see [Table 5 on page 25](#) for typical applications.
- R_8 and R_9 : to program f_{SW} , AV gain, OCP retry/latch off, and ultrasonic PFM enable, see [Table 6 on page 26](#) for typical applications.
- R_5 and R_6 : to program soft-start ramp rate, RR impedance, and AV gain multiplier (1x or 2x), see [Table 7 on page 27](#) for typical applications.
- R_{14} : I_{OUT} pull-up resistor. See [Table 2 on page 9](#).

Figure 1. Wide Range Input and Output Application

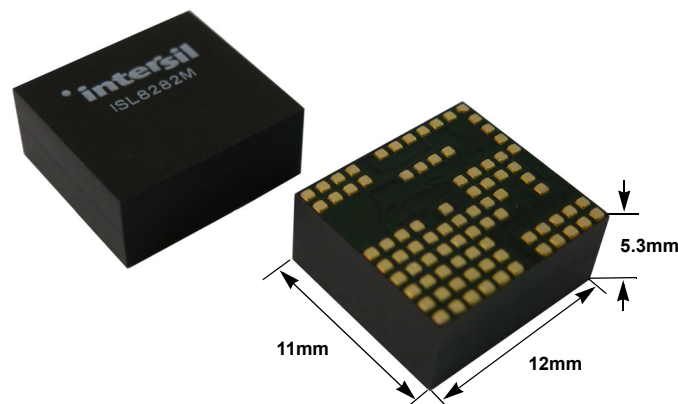
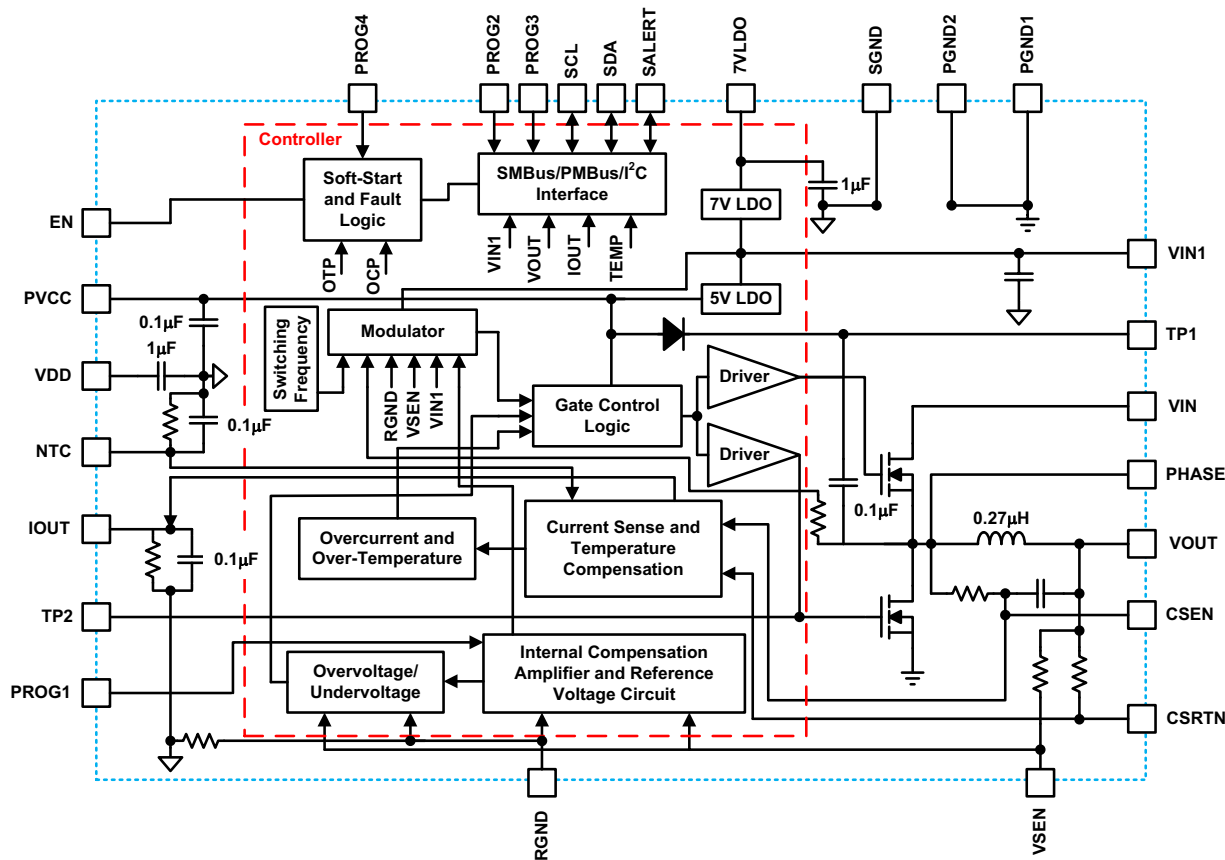


Figure 2. Small Package for High Power Density

1.2 Block Diagram



1.3 Ordering Information

Part Number (Notes 2, 3)	Part Marking	Temp Range (°C)	Tape and Reel (Units) (Note 1)	Package (RoHS Compliant)	Pkg. Dwg. #
ISL8282MFRZ	ISL8282M	-40 to +125	-	83 Ld 12x11 HDA Module	Y83.12x11
ISL8282MFRZ-T	ISL8282M	-40 to +125	720	83 Ld 12x11 HDA Module	Y83.12x11
ISL8282MFRZ-T1	ISL8282M	-40 to +125	100	83 Ld 12x11 HDA Module	Y83.12x11
ISL8282MEVAL1Z	Evaluation Board				

- Notes:
1. See [TB347](#) for details about reel specifications.
 2. These plastic packaged products are RoHS compliant by EU exemption 7C-I and employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu plate - e4 termination finish which is compatible with both SnPb and Pbfree soldering operations. RoHS compliant products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
 3. For Moisture Sensitivity Level (MSL), see the [ISL8282M](#) device page. For more information about MSL, see [TB363](#).

Table 1. Key Differences Between Family of Parts

Parameters	ISL8282M	ISL8280M	ISL8212M	ISL8210M
Load Current (A)	15	10	15	10
Minimum V_{IN} (V)	4.5	4.5	4.5	4.5
Maximum V_{IN} (V)	16.5	16.5	16.5	16.5
Minimum V_{OUT} (min) (V)	0.5	0.5	0.5	0.5
Maximum V_{OUT} (V)	5	5	5	5
Peak Efficiency (%)	95.2	95.2	95.2	95.2
POR	Yes	Yes	Yes	Yes
Minimum Switching Frequency (kHz)	255	255	255	255
Maximum Switching Frequency (kHz)	1130	1130	1130	1130
Control Type	R4	R4	R4	R4
Sync Capability	No	No	No	No
Load Sharing	No	No	No	No
PMBus	Yes	Yes	No	No

1.4 Pin Configuration

83 Ld 12x11 HDA
Top View

	1	2	3	4	5	6	7	8	9	10	11	12
A	SCLK	VDD	EN	EN	NC	NC	NC		PGND2	PGND2	PGND2	PGND2
B	SALERT								PGND2	PGND2	PGND2	PGND2
C	SDA			7VLDO	VIN1	PVCC	TP1					
D	RGND											
E	VSEN	PGOOD	SGND	SGND	SGND							
F		CSRTN	SGND	SGND	SGND		VIN		VIN	PHASE	TP2	PGND1
G		CSEN		IOUT	PROG3	PROG1	VIN	VIN	VIN	PHASE	PGND1	PGND1
H		NTC			PROG4	PROG2	VIN	VIN	VIN	PHASE	PGND1	PGND1
J							VIN	VIN	VIN	PHASE	PGND1	PGND1
K	VOUT	VOUT	VOUT	VOUT	VOUT		PHASE	PHASE	PHASE	PHASE	PHASE	PGND1
L	VOUT	VOUT	VOUT	VOUT	VOUT		PHASE	PHASE	PHASE	PHASE	PHASE	PGND1

1.5 Functional Pin Descriptions

Pin Number	Symbol	Description
A5, A6, A7	NC	No connection pads. The pads dissipate the inductor heat and provide good thermal performance. Do not connect to any other circuits.
A9, A10, A11, A12, B9, B10, B11, B12	PGND2	Power ground. The pads are connected to the source of the low-side MOSFET inside the module.
F7, F9, G7, G8, G9, H7, H8, H9, J7, J8, J9	VIN	Power input. Connect the pads directly to an input rail in the range of 4.5V to 16.5V. Connect the input ceramic capacitors between VIN and PGND1 as close as possible to the module.
F10, G10, H10, J10, K7, K8, K9, K10, K11, L7, L8, L9, L10, L11	PHASE	Phase node connection. The pads are connected to the junction of the high-side MOSFET's source, output filter inductor, low-side MOSFET's drain, and return path for the UGATE high-side MOSFET driver.
F12, G11, G12, H11, H12, J11, J12, K12, L12	PGND1	Power ground. The pads are the sources of the lower MOSFET inside the module and should be connected to the (-) terminals of the external input capacitors and output capacitors.
K1, K2, K3, K4, K5, L1, L2, L3, L4, L5	VOOUT	Regulated power module output. Apply the output load between VOOUT and PGND1.
A1	SCLK	SMBus/PMBus/I ² C synchronous clock signal input. A pull-up resistor is required for this application.
A2	VDD	Logic bias supply. Connect the pin externally to the PVCC rail.
A3, A4	EN	Precision enable input. Pulling EN above the rising threshold voltage initiates the soft-start sequence. Pulling EN below the falling threshold voltage suspends module operation.
B1	SALERT	Output pin for transferring the active low signal driven asynchronously from the module to SMBus/PMBus. A pull-up resistor is required for this application.
C1	SDA	I/O pin for transferring data signals between the SMBus/PMBus/I ² C host and the module. A pull-up resistor is required for this application.
C4	7VLDO	7V LDO used to bias the current sensing amplifier.
C5	VIN1	Input voltage pin for the R4 loop (5V) and LDO (7V). Place a high quality low ESR ceramic capacitor (1.0μF, X7R) in close proximity to the pin.
C6	PVCC	Output of the 5V LDO to bias internal control circuits and MOSFETs drivers of ISL8282M. Place a high quality low ESR ceramic capacitor (4.7μF, X7R) in close proximity to the pin.
C7	TP1	Test pad. Leave this pin open.
D1	RGND	Monitors the negative rail of the module output. Connect to ground at the point of regulation.
E1	VSEN	Monitors the positive rail of the module output. Connect to the point of regulation.
E2	PGOOD	Open-drain indicator output. The PGOOD signal is asserted when the output voltage is within ±12.5% of the nominal set output voltage and is deasserted when the output voltage is outside of the stated range or the EN pin is pulled low.
E3, E4, E5, F3, F4, F5	SGND	Signal ground pads. The small-signal ground is common to all control circuitry and all voltage levels are measured with respect to this pin. Tie SGND to a solid low noise GND plane.
F2	CSRTN	Monitors the negative flow of output current for overcurrent protection and telemetry.
F11	TP2	Test pad. Leave this pin open.
G2	CSEN	Monitors the positive flow of output current for overcurrent protection and telemetry.
G4	IOOUT	Output current monitor pin. An internal resistor sets the gain and an internal capacitor provides the averaging function; an external pull-up resistor to VDD is recommended to calibrate the no load offset.
G5	PROG3	Programming pin for ultrasonic PFM operation, fault behavior, switching frequency, and R4 (AV) control loop gain.

Pin Number	Symbol	Description
G6	PROG1	Programming pin for boot-up voltage.
H2	NTC	Input pin for temperature measurement. An NTC thermistor and a decoupling capacitor inside the module are connected between this pin and SGND. Connect this pin through a resistor (1.54k Ω) to a VDD pad externally. The voltage at this pin is inversely proportional to the module temperature.
H5	PROG4	Programming pin for modulator (R4) RR impedance and output slew rate during soft-start (SS). This pin also sets the AV gain multiplier to 1x or 2x and determines the AV gain on PROG3.
H6	PROG2	Programming pin for PWM/PFM mode, temperature compensation, and serial bus (SMBus/PMBus/I ² C) address.

Table 2. ISL8282M Design Guide Matrix of Typical Applications

V _{OUT} (V)	V _{IN} (V)	Frequency (kHz)	AV Gain	RR (Ω)	TCOMP ($^{\circ}$ C)	R ₁₄ (M Ω)	R ₃₅ (Ω)
0.5	5	400	49	200k	5	1.2	0
	10					2	
	12					2	
	15					3	
0.6	5	400	49	200k	5	1.2	0
	10					2	
	12					2	
	15					3	
0.75	5	400	49	200k	5	1.2	0
	10					3	
	12					3	
	15					open	
0.9	5	400	49	200k	5	1.2	0
	10					3	
	12					open	
	15					open	
1	5	400	49	200k	5	1.2	0
	10					3	
	12					open	
	15					open	
1.2	5	400	26	200k	5	1.2	0
	10					3	
	12					open	
	15					open	
1.5	5	500	26	200k	5	1.2	0
	10					3	
	12					open	
	15					open	
1.8	5	500	26	200k	5	1.2	0
	10					3	
	12					open	
	15					open	

Table 2. ISL8282M Design Guide Matrix of Typical Applications (Continued)

V_{OUT} (V)	V_{IN} (V)	Frequency (kHz)	AV Gain	RR (Ω)	TCOMP ($^{\circ}\text{C}$)	R_{14} (M Ω)	R_{35} (Ω)
2.5	5	600	26	200k	5	1.2	0
	10					3	
	12					open	
	15					open	
3.3	5.5	700	26	200k	5	1.2	0
	10					3	
	12					open	
	15					open	121 (Note 4)
5	8	850	26	200k	5	0.909	0
	10					1.2	
	12					4.02	121 (Note 4)
	15					open	

Note:

4. A 121 Ω resistor is needed only when OCP behavior is set to Retry. When a 121 Ω resistor is connected between VIN and VIN1, the READ_VIN command in PowerNavigator reads back the V_{IN1} voltage.

2. Specifications

2.1 Absolute Maximum Ratings

Parameter	Minimum	Maximum	Unit
V_{DD} , PVCC, V_{SEN}	-0.3	+7	V
Module Input Voltage, V_{IN}	-0.3	+20	V
Module Input Voltage, V_{IN1}	-0.3	+20	V
7VLDO	-0.3	+7.75	V
Output Voltage, V_{OUT}	-0.3	+5.5	V
BOOT Voltage ($V_{BOOT-GND}$)	-0.3	+30	V
BOOT to PHASE Voltage ($V_{BOOT-PHASE}$) (DC)	-0.3	+7	V
BOOT to PHASE Voltage ($V_{BOOT-PHASE}$) (<10ns)	-0.3	+9	V
PHASE Voltage	-0.3	+25	V
PHASE Voltage (<20ns Pulse Width, 10μJ)	-9	+25	V
All Other Pins	-0.3 to GND	$V_{DD} + 0.3$	V
ESD Rating	Value		Unit
Machine Model (Tested per JESD22-A115C)	200		V
Charged Device Model (Tested per JS-002-2014)	750		V
Human Body Model (Tested per JS-001-2017)	2		kV
Latch-Up (Tested per JESD78E; Class 2, Level A)	100 at +125°C		mA

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

2.2 Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
83 Ld HDA Module (Notes 5, 6)	16.8	5.6

Notes:

- θ_{JA} is measured in free air with the module mounted on a 6-layer thermal test board 3 x 3.4 inches in size with significant coverage of 2oz Cu on all layers, with numerous vias.
- For θ_{JC} , the "case temp" location is the center of the package underside.

Parameter	Minimum	Maximum	Unit
Junction Temperature Range	-55	+150	°C
Storage Temperature Range	-65	+150	°C
Pb-Free Reflow Profile	See Figure 52 on page 48		

2.3 Recommended Operating Conditions

Parameter	Minimum	Maximum	Unit
Junction Temperature Range	-40	+125	°C
Wide Range Input Voltage, V_{IN} , Figure 1	4.5	16.5	V
Output Voltage, V_{OUT} , Figure 1	0.5	5	V
Output Current, I_{OUT} , Figure 1	0	15	A

2.4 Electrical Specifications

All typical specifications $T_A = +25^\circ\text{C}$, $V_{IN} = 12\text{V}$, $V_{IN1} = 12\text{V}$, $V_{OUT} = 1\text{V}$. **Boldface limits apply across the junction temperature range, -40°C to $+125^\circ\text{C}$ ([Note 7](#)), unless otherwise stated.**

Parameter	Symbol	Test Conditions	Min (Note 8)	Typ	Max (Note 8)	Unit
V_{IN} and V_{IN1} Supply						
Input Voltage Range	V_{IN}		4.5		16.5	V
	V_{IN1}		4.5		16.5	V
Input Voltage Read Back Resolution	$V_{IN_READ_RES}$	(Note 4)		62.5		mV
V_{IN} Supply Current						
Input Supply Current in PFM mode Operation	$I_{S(PFM)}$	PFM mode, $V_{IN} = 12\text{V}$, $V_{OUT} = 1\text{V}$, $I_{OUT} = 0\text{A}$		0.2		mA
Input Supply Current in PWM mode Operation	$I_{S(PWM)}$	PWM mode, $V_{IN} = 12\text{V}$, $V_{OUT} = 1\text{V}$, $I_{OUT} = 0\text{A}$		35		mA
Input Supply Current in PWM mode Operation	$I_{S(PWM)}$	PWM mode, $V_{IN} = 12\text{V}$, $V_{OUT} = 1\text{V}$, $I_{OUT} = 15\text{A}$		1.49		A
Input Supply Current in Shutdown	$I_{S(SHUTDOWN)}$	Shutdown		0.05		μA
V_{IN1} Supply Current						
Shutdown Current	I_{VIN1Q}	EN = 0, PGOOD is floating, $V_{IN1} = 12\text{V}$		14.5	17	mA
Operating Current	I_{VIN1OP}	PGOOD is floating, $V_{IN1} = 12\text{V}$		19	25	mA
V_{DD} and V_{IN} POR Threshold						
V_{DD} , PVCC Rising POR Threshold Voltage				4.2	4.35	V
V_{DD} , PVCC Falling POR Threshold Voltage			3.8	3.95	4.15	V
V_{IN} , 7VLDO Rising POR Threshold Voltage				4.2	4.35	V
V_{IN} , 7VLDO Falling POR Threshold Voltage			3.8	3.95	4.15	V
Output Regulation						
Output Continuous Current Range	I_{OUT}	(Note 9)	0		15	A
Output Current Read Back Resolution	$I_{OUT_READ_RES}$			0.125		A
Output Current Read Back Total Error	$I_{OUT_READ_ERR}$	READ_IOUT, V_{IN} from 4.5V to 16.5V, V_{OUT} from 0.5V to 5V (Note 10)		±0.875		A
Output Voltage Range	V_{OUT_RANGE}		0.5		5	V
Output Voltage Read Back Resolution	$V_{OUT_READ_RES}$	(Note 11)		7.8125		mV

All typical specifications $T_A = +25^\circ\text{C}$, $V_{IN} = 12\text{V}$, $V_{IN1} = 12\text{V}$, $V_{OUT} = 1\text{V}$. **Boldface limits apply across the junction temperature range, -40°C to $+125^\circ\text{C}$ (Note 7), unless otherwise stated. (Continued)**

Parameter	Symbol	Test Conditions	Min (Note 8)	Typ	Max (Note 8)	Unit
Output Voltage Set-Point Accuracy		$0.5\text{V} \leq V_{OUT} \leq 0.75\text{V}$, total variation with line, load, and temperature ($-40^\circ\text{C} \leq T_J \leq +125^\circ\text{C}$)	-12.5		+12.5	mV
		$0.75\text{V} \leq V_{OUT} \leq 0.9\text{V}$, total variation with line, load, and temperature ($-40^\circ\text{C} \leq T_J \leq +125^\circ\text{C}$)	-15		+15	mV
		$0.9\text{V} \leq V_{OUT} \leq 5\text{V}$, total variation with line, load, and temperature ($-40^\circ\text{C} \leq T_J \leq +125^\circ\text{C}$)	-1.5		+1.5	%
Line Regulation	$\Delta V_{OUT}/V_{OUT_SET}$	$V_{OUT} = 1\text{V}$, V_{IN} from 4.5V to 16.5V, $I_L = 0\text{A}$	-1.2		+1.2	%
		$V_{OUT} = 1.8\text{V}$, V_{IN} from 4.5V to 16.5V, $I_L = 0\text{A}$	-1.2		+1.2	%
Load Regulation	$\Delta V_{OUT}/V_{OUT_SET}$	From 0A to 15A, $V_{IN} = 5\text{V}/12\text{V}$, $V_{OUT} = 1\text{V}$	-1.2		+1.2	%
		From 0A to 15A, $V_{IN} = 5\text{V}/12\text{V}$, $V_{OUT} = 1.8\text{V}$	-1.2		+1.2	%
Output Ripple Voltage	$V_{OUT(AC)}$	$V_{IN} = 12\text{V}$, $V_{OUT} = 1\text{V}$, $I_{OUT} = 15\text{A}$, 4x220 μF ceramic capacitor		8		mV _{P-P}
Dynamic Characteristics						
Voltage Change of Positive Load Step	V_{OUT_DP}	Current slew rate = 2.5A/ μs , $V_{IN} = 12\text{V}$, 4x220 μF ceramic capacitor $V_{OUT} = 1\text{V}$, I_{OUT} from 0A to 7.5A		10		mV
Voltage Change of Negative Load Step	V_{OUT_DN}	Current slew rate = 2.5A/ μs , $V_{IN} = 12\text{V}$, 4x220 μF ceramic capacitor $V_{OUT} = 1\text{V}$, I_{OUT} from 7.5A to 0A		10		mV
Enable Input						
EN High Threshold Voltage	V_{ENTHR}		0.81	0.84	0.87	V
EN Low Threshold Voltage	V_{ENTHF}		0.71	0.76	0.81	V
Channel Frequency						
300kHz Configuration		PWM mode	255	300	340	kHz
400kHz Configuration			340	400	455	kHz
500kHz Configuration			425	500	565	kHz
600kHz Configuration			510	600	680	kHz
700kHz Configuration			600	700	790	kHz
850kHz Configuration			720	850	960	kHz
1000kHz Configuration			855	1000	1130	kHz

All typical specifications $T_A = +25^\circ\text{C}$, $V_{IN} = 12\text{V}$, $V_{IN1} = 12\text{V}$, $V_{OUT} = 1\text{V}$. **Boldface limits apply across the junction temperature range, -40°C to $+125^\circ\text{C}$ (Note 7), unless otherwise stated. (Continued)**

Parameter	Symbol	Test Conditions	Min (Note 8)	Typ	Max (Note 8)	Unit
Soft-Start						
Soft-Start Slew Rate			0.125	0.157	0.18	mV/ μs
			0.25	0.315	0.37	mV/ μs
			0.52	0.625	0.7	mV/ μs
			1	1.25	1.4	mV/ μs
			2	2.5	2.8	mV/ μs
			4.1	5	5.6	mV/ μs
			8.4	10	10.9	mV/ μs
Soft-Start Delay from Enable High		Excluding 5.5ms POR timeout. See Figures 47 and 48 on page 39	140	200	260	μs
Remote Sense						
Bias Current of VSEN and RGND Pins					250	μA
Maximum Differential Input Voltage			5.8			V
Power-Good						
PGOOD Pull-Down Impedance	R_{PG}	PGOOD = 5mA sink		10	50	Ω
PGOOD Leakage Current	I_{PG}	PGOOD = 5V			1	μA
LDOs						
5V LDO Regulation		$V_{IN} = 12\text{V}$, load = 50mA	4.8	5	5.15	V
5V LDO Regulation		$V_{IN} = 4.75\text{V}$, load = 50mA	4.15			V
5V LDO Maximum Current Capability			100			mA
7V LDO Regulation		250 μA load	7.15	7.4	7.5	
7V Dropout		$V_{IN} = 4.75\text{V}$, 250 μA load	4.3			V
7V LDO Current Capability		Not recommended for external use	2			mA
Current Sense						
OCP	I_{OCP}	$V_{IN} = 12\text{V}$, $V_{OUT} = 1\text{V}$	15	18.8		A
Maximum Common-Mode Input Voltage		7VLDO = 7.4V	5.7			V
		$V_{DD} = PVCC = 7VLDO = 4.5\text{V}$	2.8			V
Fault Protection						
UVP Threshold Voltage		$0.5\text{V} \leq V_{OUT} \leq 0.7\text{V}$	67	74	88	% V_{OUT}
		$0.7\text{V} \leq V_{OUT} < 1\text{V}$	68	74	85	% V_{OUT}
		$1\text{V} \leq V_{OUT} < 1.5\text{V}$	68	74	82	% V_{OUT}
		$1.5\text{V} \leq V_{OUT} \leq 5\text{V}$	68	74	80	% V_{OUT}
Startup OVP Threshold Voltage		$0\text{V} \leq V_{OUT} \leq 1.08\text{V}$	1.1	1.15	1.25	V
		$1.08\text{V} < V_{OUT} \leq 1.55\text{V}$	1.58	1.65	1.75	V
		$1.55\text{V} < V_{OUT} \leq 1.85\text{V}$	1.88	1.95	2.05	V
		$1.85\text{V} < V_{OUT} \leq 2.08\text{V}$	2.09	2.15	2.25	V
		$2.08\text{V} < V_{OUT} \leq 2.53\text{V}$	2.56	2.65	2.75	V
		$2.53\text{V} < V_{OUT} \leq 3.33\text{V}$	3.36	3.45	3.6	V
		$3.33\text{V} < V_{OUT} \leq 5\text{V}$	5.52	5.65	5.85	V

All typical specifications $T_A = +25^{\circ}\text{C}$, $V_{IN} = 12\text{V}$, $V_{IN1} = 12\text{V}$, $V_{OUT} = 1\text{V}$. **Boldface limits apply across the junction temperature range, -40°C to $+125^{\circ}\text{C}$ (Note 7), unless otherwise stated. (Continued)**

Parameter	Symbol	Test Conditions	Min (Note 8)	Typ	Max (Note 8)	Unit
Startup OVP Hysteresis				100		mV
OVP Rising Threshold Voltage	V_{OVRTH}	$0.5\text{V} \leq V_{OUT} \leq 0.7\text{V}$	111	120	136	% V_{OUT}
		$0.7\text{V} \leq V_{OUT} < 1\text{V}$	113	120	132	% V_{OUT}
		$1\text{V} \leq V_{OUT} < 1.5\text{V}$	114	120	128	% V_{OUT}
		$1.5\text{V} \leq V_{OUT} \leq 5\text{V}$	114	120	127	% V_{OUT}
OVP Falling Threshold Voltage	V_{OVFTH}	$0.5\text{V} \leq V_{OUT} \leq 0.7\text{V}$	93	100	115	% V_{OUT}
		$0.7\text{V} \leq V_{OUT} < 1\text{V}$	95	100	111	% V_{OUT}
		$1\text{V} \leq V_{OUT} < 1.5\text{V}$	96	100	109	% V_{OUT}
		$1.5\text{V} \leq V_{OUT} \leq 5\text{V}$	96	100	108	% V_{OUT}
Over-Temperature Shutdown Threshold		$22.31\%V_{DD}$ ($\sim +136^{\circ}\text{C}$)	20	22.31	26	% V_{DD}
Over-Temperature Shutdown Reset Threshold		$27.79\%V_{DD}$ ($\sim +122^{\circ}\text{C}$)	25	27.79	30	% V_{DD}
SMBus/PMBus/I²C (Note 12)						
Signal Input Low Voltage					1	V
Signal Input High Voltage			1.6			V
Signal Output Low Voltage		4mA pull-up current			0.4	V
DATE, ALERT # Pull-Down Impedance				11	50	Ω
CLOCK Maximum Speed			1.25			MHz
CLOCK Minimum Speed					0.05	MHz
Telemetry Update Rate				108		μs
Timeout			25	30	35	ms
PMBus Accessible Timeout from All Rails' POR		See Figure 47 on page 39		5.5	6.5	ms

Notes:

- The ISL8282M is tested under pulsed-load conditions such that $T_J \approx T_A$.
- Compliance to datasheet limits is assured by one or more methods: production test, characterization, and/or design.
- See output current derating curves for different V_{OUT} and T_A located ["Derating Curves" on page 21](#).
- See [Table 2 on page 9](#).
- When $0.5\text{V} \leq V_{OUT} \leq 1.8\text{V}$, the output voltage read back resolution is 7.8125mV. When $V_{OUT} > 1.8\text{V}$, the resolution can be higher than that from adjacent codes. However, the resolution is always 7.8125mV around typical V_{OUT} , as in [Table 8 on page 28](#).
- Limits apply across the junction temperature range of -40°C to $+85^{\circ}\text{C}$.

3. Typical Performance Curves

3.1 Efficiency Performance

Operating conditions: $T_A = 25^\circ\text{C}$, no air flow, PWM mode. Typical values are used unless otherwise noted. The efficiency curves were measured on the evaluation board. For the test conditions, see [Table 2 on page 9](#).

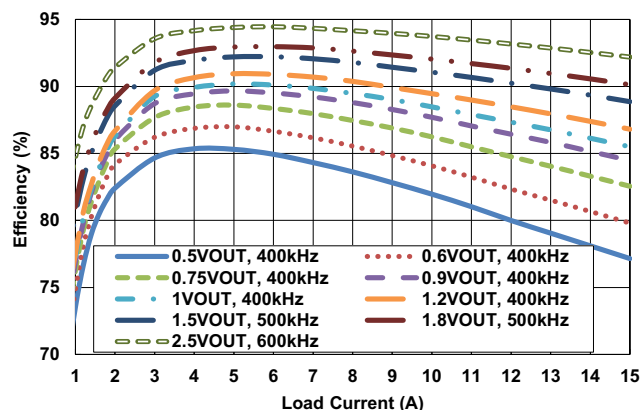


Figure 3. Efficiency vs Load Current at 5V_{IN} (PWM)

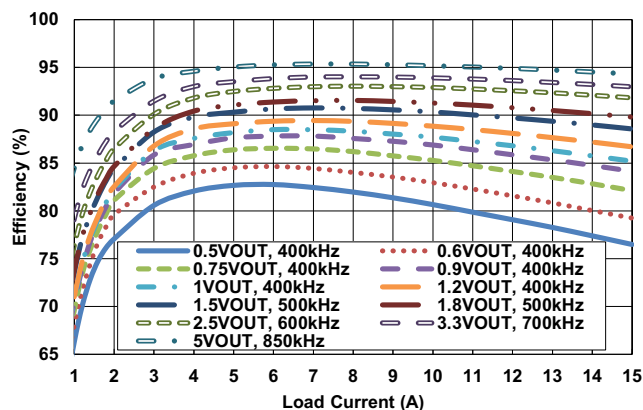


Figure 4. Efficiency vs Load Current at 8V_{IN} (PWM)

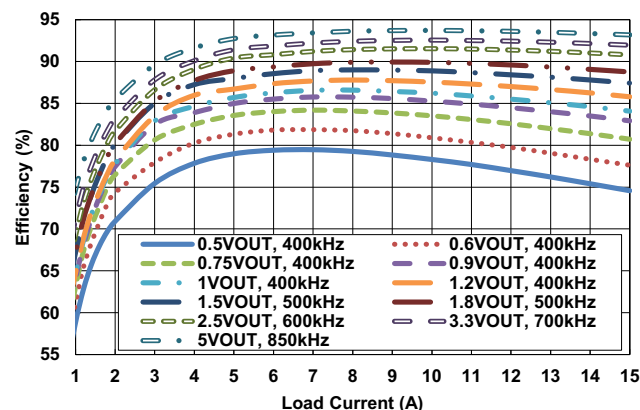


Figure 5. Efficiency vs Load Current at 12V_{IN} (PWM)

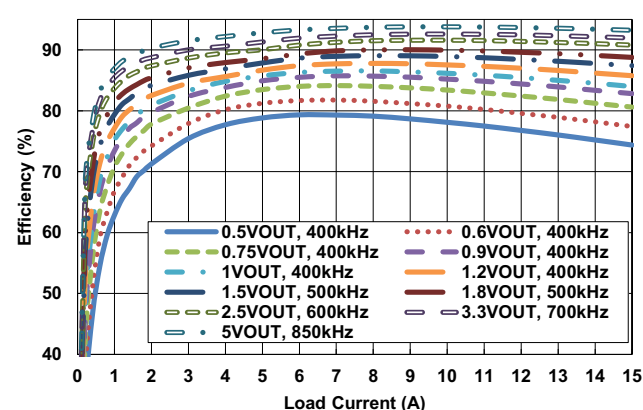


Figure 6. Efficiency vs Load Current at 12V_{IN} (PFM)

3.2 Output Voltage Ripple

Operating conditions: $T_A = +25^\circ\text{C}$, no air flow, PWM mode, $C_{OUT} = 4 \times 220\mu\text{F}$ Ceramic, $RR = 200\text{k}\Omega$. Typical values are used unless otherwise noted. For the test conditions, see [Table 2 on page 9](#).

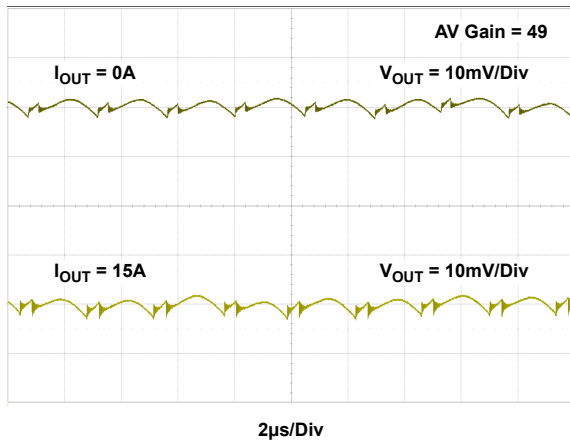


Figure 7. Output Ripple at $5V_{IN}$ and $0.75V_{OUT}$

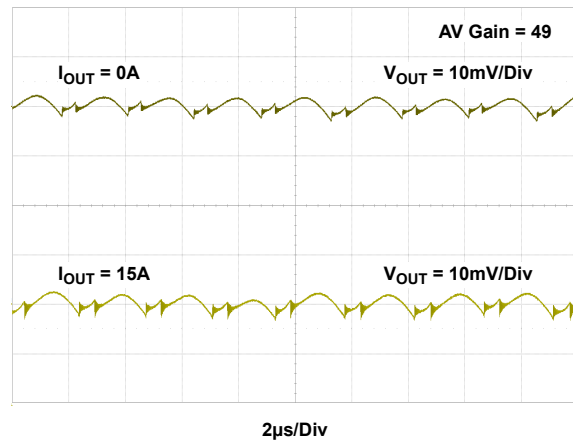


Figure 8. Output Ripple at $5V_{IN}$ and $1V_{OUT}$

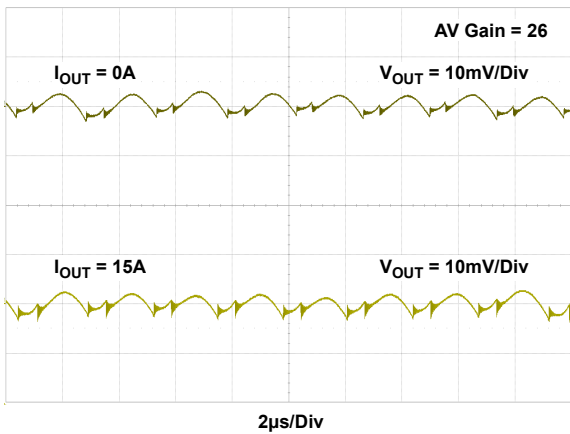


Figure 9. Output Ripple at $5V_{IN}$ and $1.2V_{OUT}$

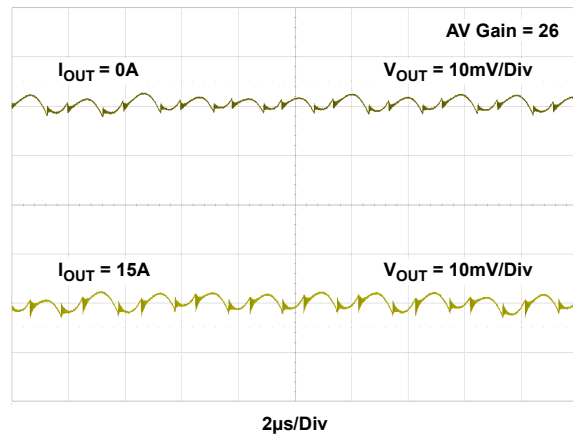


Figure 10. Output Ripple at $5V_{IN}$ and $1.8V_{OUT}$

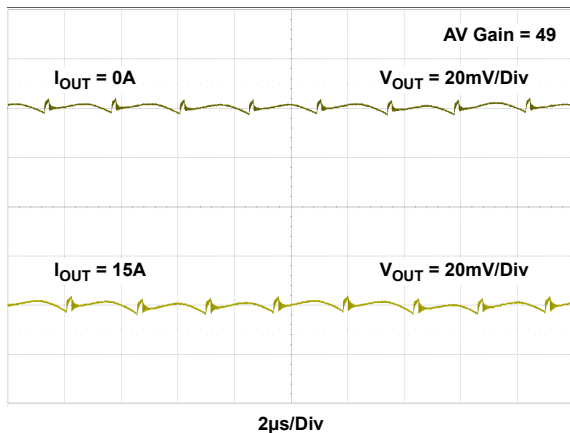


Figure 11. Output Ripple at $12V_{IN}$ and $0.75V_{OUT}$

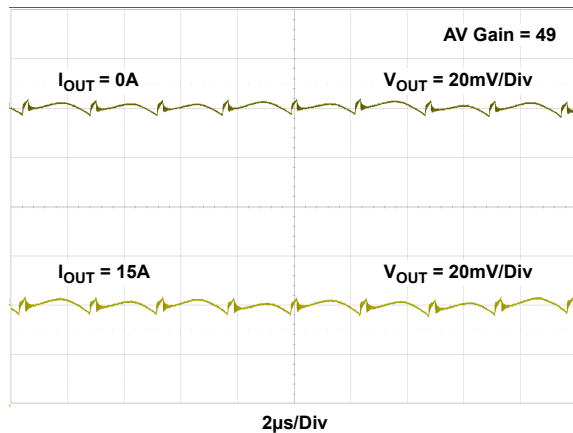


Figure 12. Output Ripple at $12V_{IN}$ and $1V_{OUT}$

Operating conditions: $T_A = +25^\circ\text{C}$, no air flow, PWM mode, $C_{OUT} = 4 \times 220\mu\text{F}$ Ceramic, $RR = 200\text{k}\Omega$. Typical values are used unless otherwise noted. For the test conditions, see [Table 2 on page 9](#). (Continued)

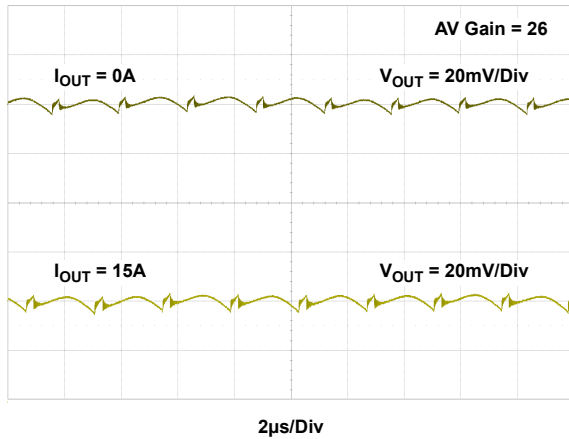


Figure 13. Output Ripple at $12V_{IN}$ and $1.2V_{OUT}$

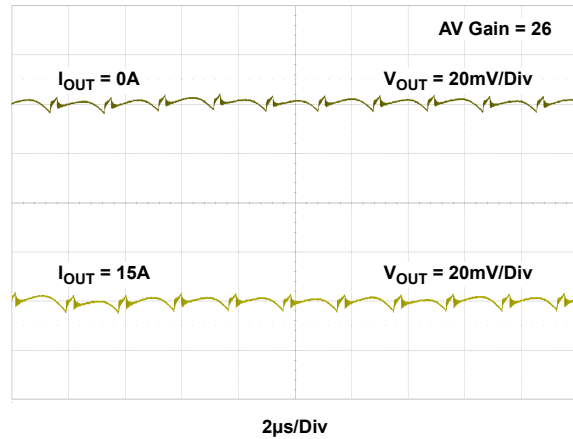


Figure 14. Output Ripple at $12V_{IN}$ and $1.5V_{OUT}$

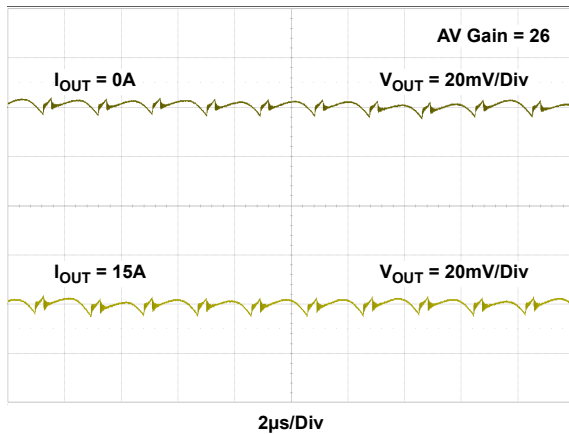


Figure 15. Output Ripple at $12V_{IN}$ and $1.8V_{OUT}$

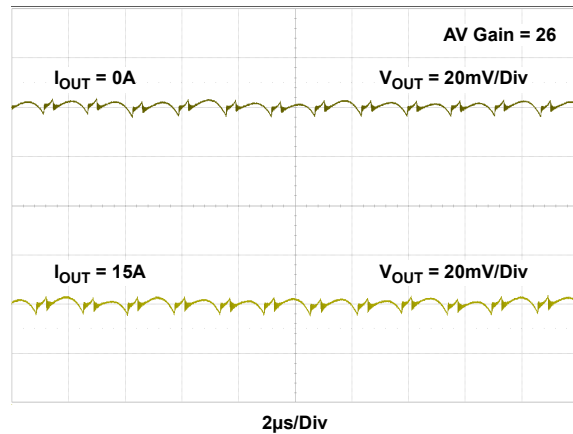


Figure 16. Output Ripple at $12V_{IN}$ and $2.5V_{OUT}$

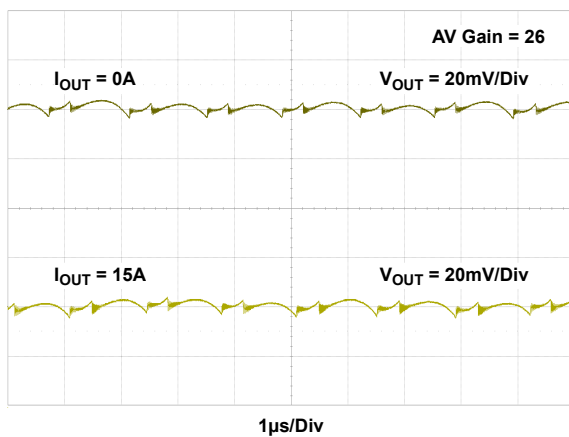


Figure 17. Output Ripple at $12V_{IN}$ and $3.3V_{OUT}$

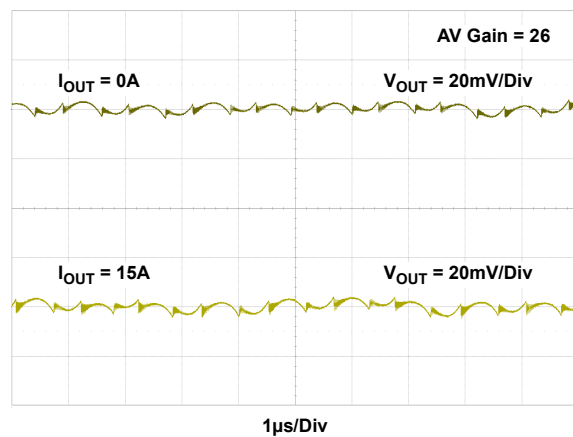


Figure 18. Output Ripple at $12V_{IN}$ and $5V_{OUT}$

3.3 Load Transient Response Performance

Operating conditions: $T_A = +25^\circ\text{C}$, no air flow, $V_{IN} = 12\text{V}$, PWM mode, $C_{OUT} = 4 \times 220\mu\text{F}$ Ceramic, 0A to 7.5A step load at 7.5A/ μs slew rate, $RR = 200\text{k}\Omega$. Typical values are used unless otherwise noted. For the test conditions, see [Table 2 on page 9](#).

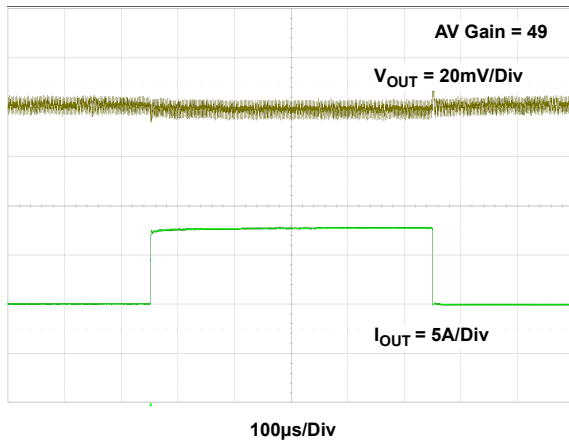


Figure 19. Load Transient Response at $0.75V_{OUT}$

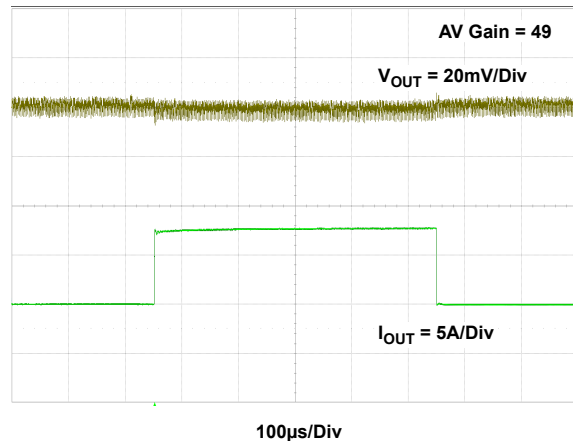


Figure 20. Load Transient Response at $1V_{OUT}$

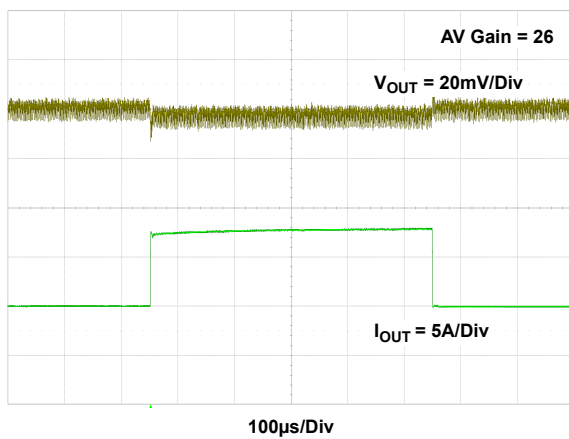


Figure 21. Load Transient Response at $1.8V_{OUT}$

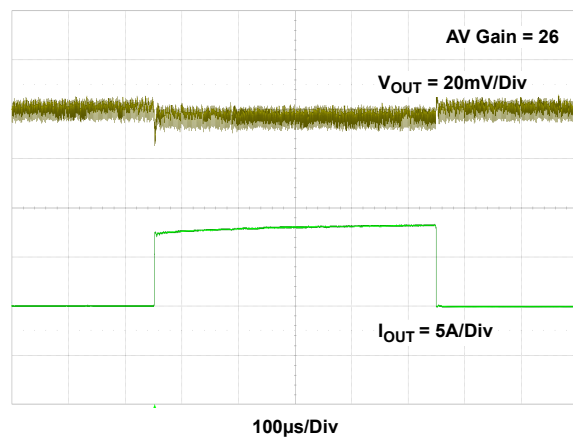


Figure 22. Load Transient Response at $2.5V_{OUT}$

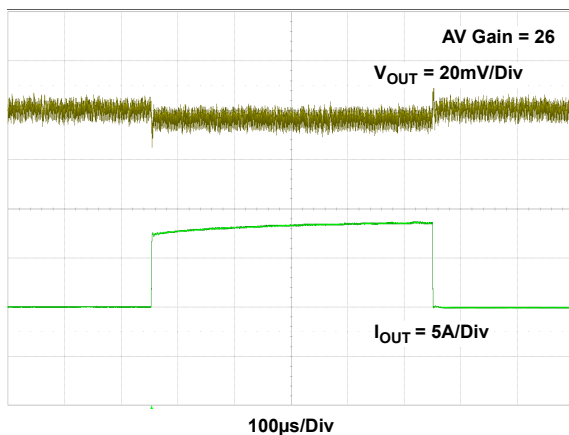


Figure 23. Load Transient Response at $3.3V_{OUT}$

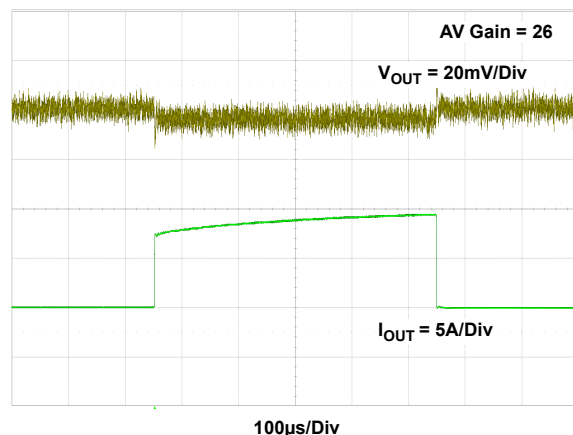


Figure 24. Load Transient Response at $5V_{OUT}$

3.4 Startup and Shutdown

Operating conditions: $T_A = +25^\circ\text{C}$, no air flow, $V_{IN} = 12\text{V}$, $V_{OUT} = 1\text{V}$, PWM mode. Typical values are used unless otherwise noted. For the test conditions, see [Table 2 on page 9](#).

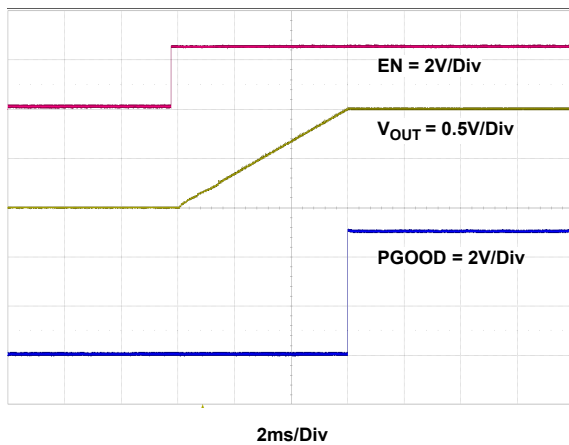


Figure 25. Startup Waveform at $I_{OUT} = 0\text{A}$

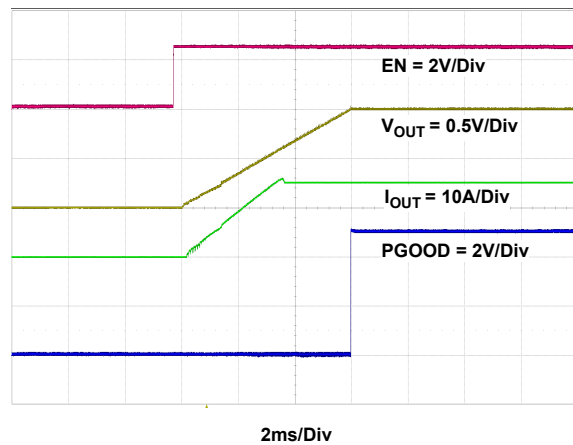


Figure 26. Startup Waveform at $I_{OUT} = 15\text{A}$

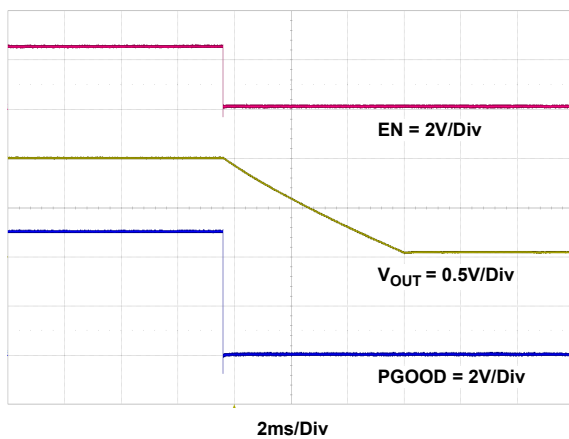


Figure 27. Shutdown Waveform at $I_{OUT} = 0\text{A}$

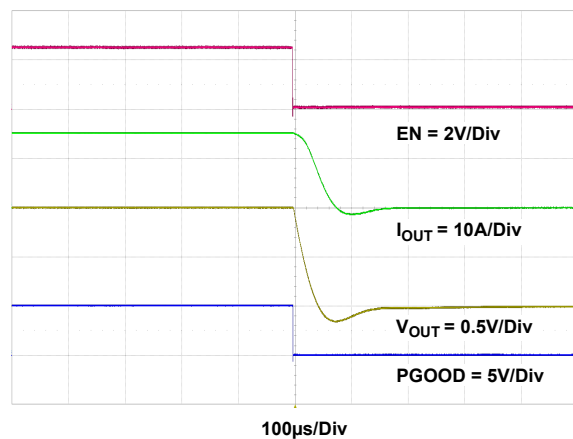


Figure 28. Shutdown Waveform at $I_{OUT} = 15\text{A}$

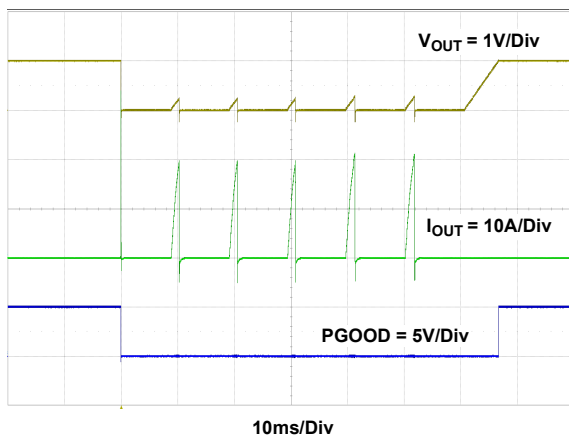


Figure 29. OCP Response; Output Short-Circuited from No Load to Ground and Released at $I_{OUT} = 0\text{A}$

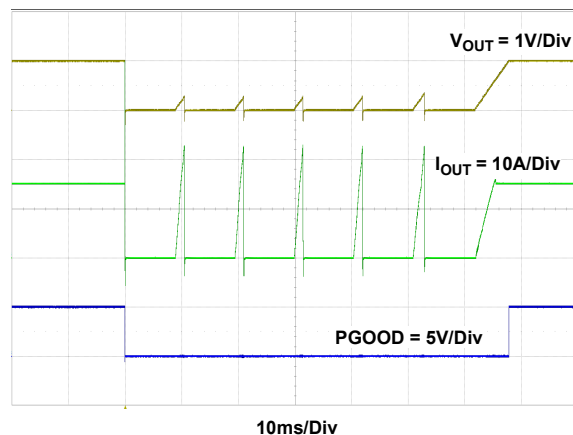
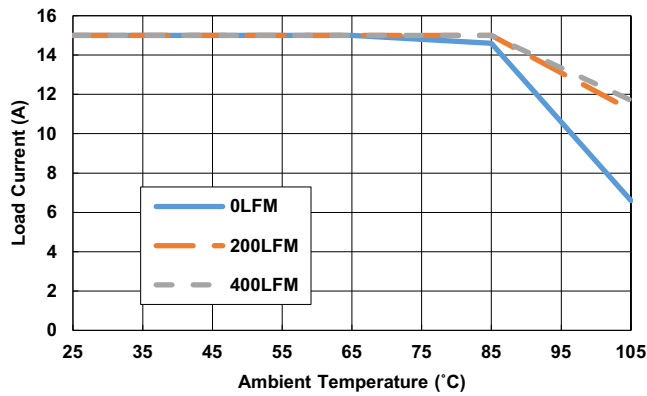
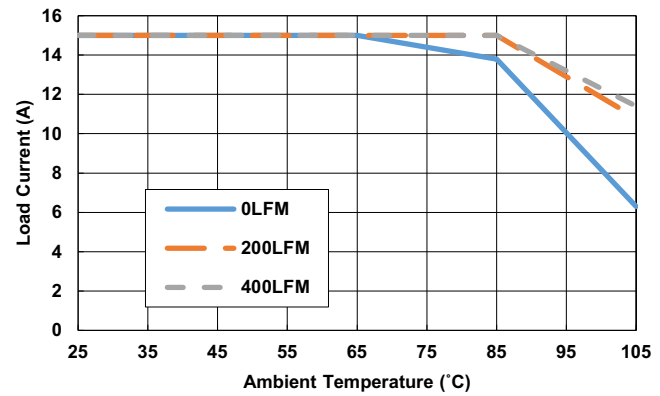
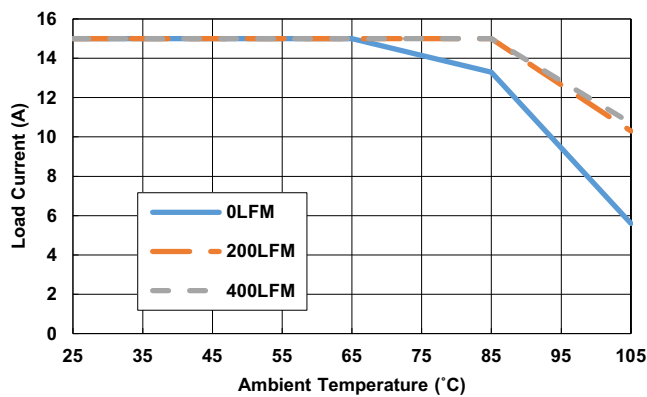
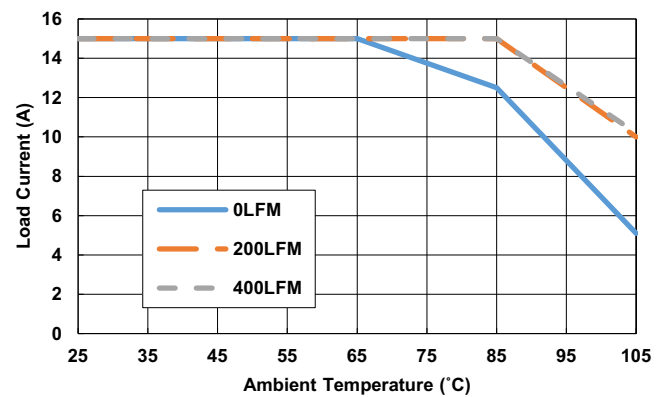
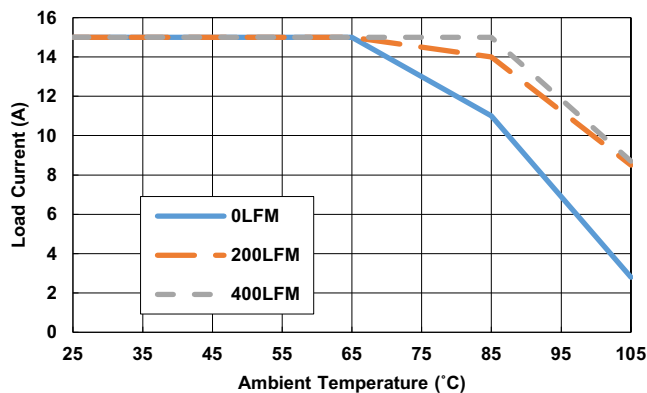
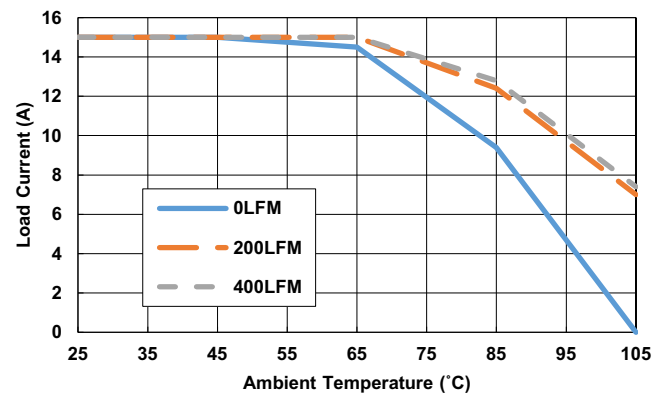


Figure 30. OCP Response; Output Short-Circuited from No Load to Ground and Released at $I_{OUT} = 15\text{A}$

3.5 Derating Curves

Operating conditions: $V_{IN} = 12V$, PWM mode. All of the following curves were plotted at $T_J = +125^{\circ}C$. The derating curves were measured on the evaluation board. For the test conditions, see [Table 2 on page 9](#).

Figure 31. $0.6V_{OUT}$ Figure 32. $0.8V_{OUT}$ Figure 33. $1V_{OUT}$ Figure 34. $1.2V_{OUT}$ Figure 35. $1.8V_{OUT}$ Figure 36. $2.5V_{OUT}$

Operating conditions: $V_{IN} = 12V$, PWM mode. All of the following curves were plotted at $T_J = +125^{\circ}C$. The derating curves were measured on the evaluation board. For the test conditions, see [Table 2 on page 9](#). (Continued)

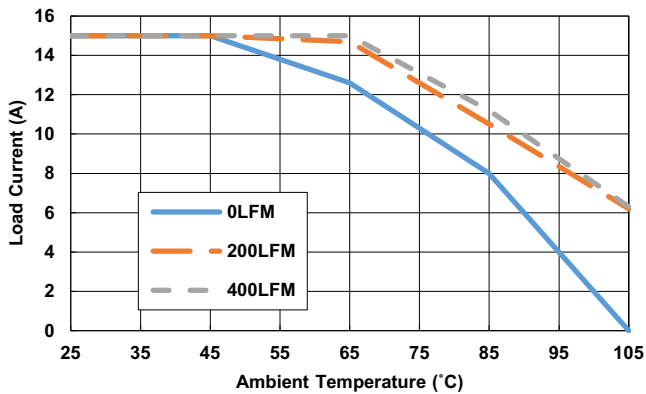


Figure 37. 3.3V_{OUT}

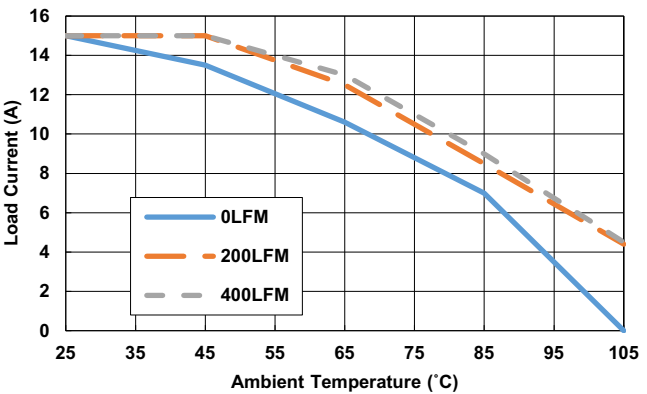


Figure 38. 5V_{OUT}

4. Functional Description

The following sections describe the operation of the ISL8282M.

4.1 Configuring Internal Bias and LDO

The ISL8282M has four bias pins: VIN1, 7VLDO, PVCC, and VDD. The PVCC voltage rail is 5V LDO and supplied by VIN1. The 7VLDO voltage rail is 7V LDO supplied by VIN1. The VDD pin must connect to the PVCC rail externally to be biased.

4.2 Enabling and Disabling the ISL8282M

The module is enabled until the 7VLDO, PVCC, VDD, VIN1, and EN pins increase above their respective rising threshold voltages and the typical 5.5ms timeout (worst case = 6.5ms) expires, as shown in [Figures 47](#) and [48](#) on [page 39](#). The module is disabled when the 7VLDO, PVCC, VDD, VIN1, or EN pins drop below their respective falling POR threshold voltages.

The precision threshold EN pin allows you to set a precision input UVLO level with an external resistor divider as shown in [Figure 39](#).

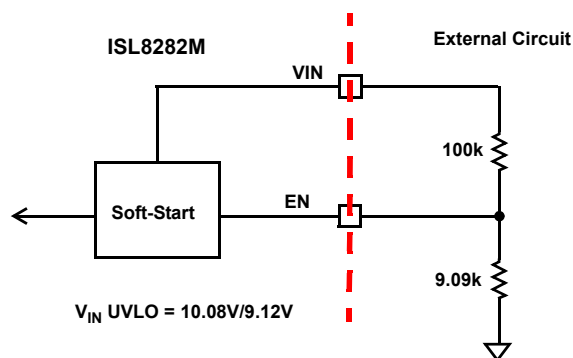


Figure 39. Input UVP Configuration

For 5V input applications or wide range input applications, the EN pin can directly connect to V_{DD} as shown in [Figure 40](#). If an external enable control signal is available and is an open-drain signal, use a 100k or higher pull-up impedance to connect the pull-up resistor to V_{DD}.

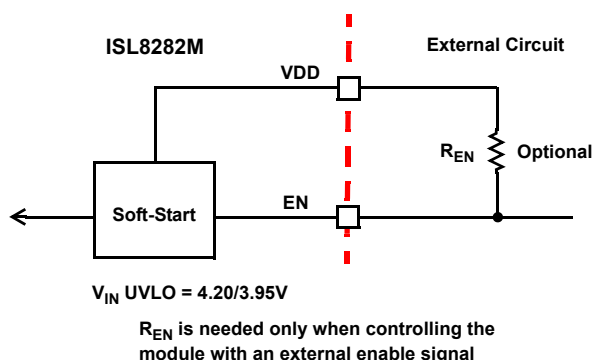


Figure 40. 5V Input or Wide Range Input Configuration

The module can be enabled or disabled by the serial bus command “OPERATION [01h]” based on the ON_OFF_CONFIG [02h] setting and/or the EN pin. See [Table 12 on page 42](#) for more details.

4.3 Programming the Resistor Reader

This section contains information about operating the resistors reader with the ISL8282M's four programming pins (PROG1, PROG2, PROG3, and PROG4) to customize module specifications. [Table 3](#) contains information about the pins and resistor reader operation.

Table 3. Programming Pin Descriptions

Pin	Bit	Name	Description
PROG1	[7:0]	BOOT-UP VOLTAGE	Sets the 256 output boot-up voltage options: 0V, 0.5V to 5V (see Table 8)
PROG2	[7:7]	PWM/PFM	Enables PFM mode or forced PWM
	[6:5]	Temperature Compensation	Adjusts NTC temperature compensation: OFF, +5°C, +15°C, +30°C
	[4:0]	ADDR	Sets the 32 serial bus addresses (see Table 11)
PROG3	[7:7]	uSPFM	Ultrasonic (25kHz clamp) PFM enable
	[6:6]	Fault Behavior	OCF fault behavior: Latch, infinite 9ms retry
	[5:3]	FSW	Sets the switching frequency (f_{SW})
	[2:0]	AV Gain	Sets the error amplifier gain (AV)
PROG4	[7:5]	RAMP_RATE	Sets the soft-start ramp rate
	[4:3]	R4 RR	Selects the RR impedance for R4 loop
	[2:2]	AVMLTI	Selects the AV gain multiplier (1x or 2x)
	[1:0]	Not Used	Not used

Renesas has developed a high resolution ADC using a patented technique with a simple 1%, 100ppm/K or better temperature coefficient resistor divider. Renesas recommends using the same type of resistor in the design so the ADC has similar change over temperature. The divider is compared to the internal divider off the VDD and SGND nodes; therefore, the divider must refer to the VDD and SGND pins and not through any RC decoupling network as shown in [Figure 41](#).

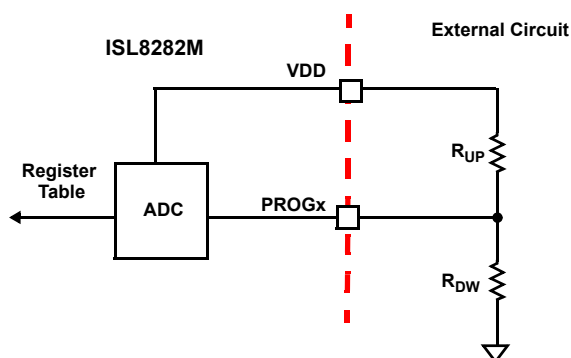


Figure 41. Simplified Resistor Divider ADC

[Tables 4](#) through [7](#) show the R_{UP} and R_{DW} values of each pin for a specific system design with some tie-high and tie-low options that enable easy programming with reduced resistors. You can use the tie-high and tie-low options to validate the module operation during In-Circuit Test (ICT) for 0V boot-up voltage. Additional options are described in the [ISL8282MEVAL1Z User's Manual](#) and [PowerNavigator](#). Data for corresponding registers can be read out through the serial bus commands ([DC\[7:0\]](#) to [DF\[7:0\]](#)). The AV gain multiplier (AVMLTI) in PROG4 of [Table 3](#) can be set by external R_{UP} and R_{DW} only. Note: the 10k Ω tie-high or tie-low is equivalent to the 0 Ω tie-high or tie-low.

Table 4. PROG 1 Resistor Reader Example

PROG1 (DC)	R _{UP} (kΩ)	R _{DW} (kΩ)	V _{OUT} (V)
01h	49.9	12.4	0.500
0Dh	23.2	17.8	0.594
0Eh	22.1	18.2	0.602
22h	97.6	27.4	0.742
23h	90.9	28.7	0.750
24h	82.5	28.7	0.758
40h	Open	34.8	0.898
37h	34	57.6	0.906
44h	133	46.4	0.992
80h	Open	75	1.000
46h	118	49.9	1.008
5Eh	45.3	150	1.195
E0h	Open	499	1.203
88h	221	113	1.492
3Fh	21.5	Open	1.500
8Ah	200	121	1.508
5Fh	34.8	Open	1.797
B2h	196	226	1.805
C4h	576	200	2.492
7Fh	52.3	Open	2.500
C6h	499	210	2.508
BFh	105	Open	3.297
D5h	249	357	3.305
F2h	374	422	4.992
DFh	147	Open	5.000
F4h	348	464	5.008
FFh	499	Open	0.000

Table 5. PROG 2 Resistor Reader Example

PROG2 (DD)	R _{UP} (kΩ)	R _{DW} (kΩ)	PFM	Temp Comp (°C)	PM_ADDR(7-Bit)
00h	Open	10	Enabled	+30	60
20h	Open	21.5	Enabled	+15	60
40h	Open	34.8	Enabled	+5	60
60h	Open	52.3	Enabled	OFF	60
80h	Open	75	Disabled	+30	60
A0h	Open	105	Disabled	+15	60
C0h	Open	147	Disabled	+5	60
E0h	Open	499	Disabled	OFF	60
1Fh	10	Open	Enabled	+30	7F
3Fh	21.5	Open	Enabled	+15	7F

Table 5. PROG 2 Resistor Reader Example (Continued)

PROG2 (DD)	R _{UP} (kΩ)	R _{DW} (kΩ)	PFM	Temp Comp (°C)	PM_ADDR(7-Bit)
5Fh	34.8	Open	Enabled	+5	7F
7Fh	52.3	Open	Enabled	OFF	7F
9Fh	75	Open	Disabled	+30	7F
BFh	105	Open	Disabled	+15	7F
DFh	147	Open	Disabled	+5	7F
FFh	499	Open	Disabled	OFF	7F

Table 6. PROG 3 Resistor Reader Example

PROG3 (DE)	R _{UP} (kΩ)	R _{DW} (kΩ)	Ultrasonic PFM	Fault Behavior	f _{sw} (kHz)	AV Gain	
						1x	2x
0Bh	25.5	16.5	Disabled	Retry	400	24.5	49
4Bh	88.7	57.6	Disabled	Latch	400	24.5	49
8Bh	191	124	Enabled	Retry	400	24.5	49
CBh	374	243	Enabled	Latch	400	24.5	49
0Dh	23.2	17.8	Disabled	Retry	400	13	26
4Dh	80.6	61.9	Disabled	Latch	400	13	26
8Dh	174	133	Enabled	Retry	400	13	26
CDh	340	261	Enabled	Latch	400	13	26
15h	16.9	24.3	Disabled	Retry	500	13	26
1Dh	13.3	39.2	Disabled	Retry	600	13	26
55h	59	84.5	Disabled	Latch	500	13	26
5Dh	46.4	137	Disabled	Latch	600	13	26
95h	127	182	Enabled	Retry	500	13	26
9Dh	100	294	Enabled	Retry	600	13	26
D5h	249	357	Enabled	Latch	500	13	26
DDh	196	576	Enabled	Latch	600	13	26
25h	76.8	29.4	Disabled	Retry	700	13	26
2Dh	49.9	38.3	Disabled	Retry	850	13	26
65h	187	71.5	Disabled	Latch	700	13	26
6Dh	121	93.1	Disabled	Latch	850	13	26
A5h	374	143	Enabled	Retry	700	13	26
ADh	243	187	Enabled	Retry	850	13	26
E5h	715	274	Enabled	Latch	700	13	26
EDh	464	357	Enabled	Latch	850	13	26

Table 7. PROG 4 Resistor Reader Example

PROG4 (DF)	R _{UP} (kΩ)	R _{DW} (kΩ)	SS Rate (mV/μs)	RR (Ω)	AVMLTI
07h	31.6	14.7	1.25	200k	2
27h	68.1	31.6	2.5	200k	2
47h	110	51.1	5	200k	2
67h	165	76.8	10	200k	2
A7h	332	154	0.157	200k	2
C7h	464	215	0.315	200k	2
E7h	634	294	0.625	200k	2
18h	15.4	28.7	1.25	800k	1
38h	33.2	61.9	2.5	800k	1
58h	53.6	100	5	800k	1
78h	80.6	150	10	800k	1
B8h	162	301	0.157	800k	1
D8h	226	422	0.315	800k	1
F8h	309	576	0.625	800k	1

4.4 Soft-Starting

The ISL8282M has four periods during soft-start as shown in [Figure 42](#).

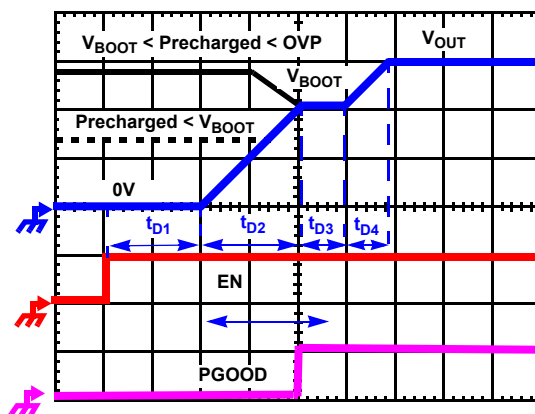


Figure 42. Soft-Start Waveforms

The ISL8282M begins the first soft-start ramp after a fixed soft-start delay period of t_{D1} and a 5.5ms timeout (worst case = 6.5ms) of bias supplies when the EN pin reaches above its enable threshold as shown in [Figures 47](#) and [48](#) on [page 39](#). The output voltage reaches the boot-up voltage (V_{BOOT}) at a fixed slew rate in period t_{D2} . The ISL8282M regulates the output voltage at V_{BOOT} for another period t_{D3} until the SMBus/PMBus/ I²C sends a new V_{OUT} command. If the V_{OUT} command is valid, the ISL8282M initiates the ramp until the voltage reaches the new V_{OUT} command voltage in period t_{D4} . The soft-start time is the sum of the four periods as shown in [Equation 1](#).

$$(EQ. 1) \quad t_{SS} = t_{D1} + t_{D2} + t_{D3} + t_{D4}$$

t_{D1} is a fixed delay with a typical value of 200μs. t_{D3} is determined by the time to obtain a new valid V_{OUT} command voltage from the SMBus/PMBus/I²C bus. If the V_{OUT} command is valid before the output reaches the boot-up voltage, the output turns around to respond to the new V_{OUT} command code.

The ISL8282M digitally controls the DAC voltage change during t_{D2} and t_{D4} . The ramp time t_{D2} and t_{D4} can be calculated based on [Equations 2](#) and [3](#) when the slew rate is set by the PROG4 pin.

$$(EQ. 2) \quad t_{D2} = \frac{V_{BOOT}}{RAMP_RATE} (\mu s)$$

$$(EQ. 3) \quad t_{D4} = \frac{V_{OUT} - V_{BOOT}}{RAMP_RATE} (\mu s)$$

The ISL8282M supports precharged startup by initiating the first PWM pulse until the internal reference (DAC) reaches the pre-charged level at the RAMP_RATE programmed by PROG4 or D5[2:0]. When the precharged level is below V_{BOOT} , the output walks up to the V_{BOOT} at RAMP_RATE and releases PGOOD at $t_{D1} + t_{D2}$. When the precharged output is above V_{BOOT} but below OVP it walks down to V_{BOOT} at RAMP_RATE, then releases PGOOD at $t_{D1} + t_{D2}$. The value t_{D2} is defined in [Equation 4](#) and is longer than a normal startup.

$$(EQ. 4) \quad t_{D2} = \frac{V_{PRECHARGED}}{RAMP_RATE} + \frac{V_{PRECHARGED} - V_{BOOT}}{RAMP_RATE} (\mu s)$$

If the boot capacitor voltage is high enough, the ISL8282M can handle up to 5.5V precharged load. However, high boot voltage cannot be guaranteed for all precharged loads. If the precharged load is above 2.5V and the precharged start-up time is long, the boot capacitor is discharged to $PV_{CC} - V_{OUT} - V_D$ by the high-side drive circuits' standby current. For a 4V precharged load, the boot capacitor can be discharged to less than 1V, which is insufficient to turn on the high-side MOSFET. Renesas recommends allowing the output voltage to drop below 2.5V before soft-start with an external bleed resistor, or by using a high RAMP_RATE to reduce the startup time.

4.5 Boot-Up Voltage Programming

The 8-bit PROG1 pin is dedicated for boot-up voltage programmability, which offers 256 options: 0V and 0.5V to 5.5V as shown in [Table 8](#). A 0V boot-up voltage is considered OFF. The driver is in tri-state and the internal DAC sets to 0V. If the [VOUT_COMMAND](#) (21h) is executed successfully before enable and 5.5ms after V_{DD} POR (typically, at worst 6.5ms), it overrides the boot-up voltage set by the PROG1 pin.

Table 8. PROG1 8-Bit (Boot-Up Voltage)

Binary Code	Hex Code	V_{BOOT} (V)	VOUT Command Code (Hex)	Delta from Previous Code (mV)
00000000	0	0.7969	66	7.8125
00000001	1	0.5000	40	
00000010	2	0.5078	41	7.8125
00000011	3	0.5156	42	7.8125
00000100	4	0.5234	43	7.8125
00000101	5	0.5313	44	7.8125
00000110	6	0.5391	45	7.8125
00000111	7	0.5469	46	7.8125
00001000	8	0.5547	47	7.8125
00001001	9	0.5625	48	7.8125
00001010	A	0.5703	49	7.8125
00001011	B	0.5781	4A	7.8125
00001100	C	0.5859	4B	7.8125
00001101	D	0.5938	4C	7.8125
00001110	E	0.6016	4D	7.8125
00001111	F	0.6094	4E	7.8125
00010000	10	0.6172	4F	7.8125

Table 8. PROG1 8-Bit (Boot-Up Voltage) (Continued)

Binary Code	Hex Code	V _{BOOT} (V)	VOUT Command Code (Hex)	Delta from Previous Code (mV)
00010001	11	0.6250	50	7.8125
00010010	12	0.6328	51	7.8125
00010011	13	0.6406	52	7.8125
00010100	14	0.6484	53	7.8125
00010101	15	0.6563	54	7.8125
00010110	16	0.6641	55	7.8125
00010111	17	0.6719	56	7.8125
00011000	18	0.6797	57	7.8125
00011001	19	0.6875	58	7.8125
00011010	1A	0.6953	59	7.8125
00011011	1B	0.7031	5A	7.8125
00011100	1C	0.7109	5B	7.8125
00011101	1D	0.7188	5C	7.8125
00011110	1E	0.7266	5D	7.8125
00011111	1F	1.3516	AD	7.8125
00100000	20	0.8516	6D	7.8125
00100001	21	0.7344	5E	7.8125
00100010	22	0.7422	5F	7.8125
00100011	23	0.7500	60	7.8125
00100100	24	0.7578	61	7.8125
00100101	25	0.7656	62	7.8125
00100110	26	0.7734	63	7.8125
00100111	27	0.7813	64	7.8125
00101000	28	0.7891	65	7.8125
00101001	29	0.7969	66	7.8125
00101010	2A	0.8047	67	7.8125
00101011	2B	0.8125	68	7.8125
00101100	2C	0.8203	69	7.8125
00101101	2D	0.8281	6A	7.8125
00101110	2E	0.8359	6B	7.8125
00101111	2F	0.8438	6C	7.8125
00110001	31	0.8594	6E	7.8125
00110010	32	0.8672	6F	7.8125
00110011	33	0.8750	70	7.8125
00110100	34	0.8828	71	7.8125
00110101	35	0.8906	72	7.8125
00110111	37	0.9063	74	7.8125
00111000	38	0.9141	75	7.8125
00111001	39	0.9219	76	7.8125
00111010	3A	0.9297	77	7.8125

Table 8. PROG1 8-Bit (Boot-Up Voltage) (Continued)

Binary Code	Hex Code	V _{BOOT} (V)	VOUT Command Code (Hex)	Delta from Previous Code (mV)
00111011	3B	0.9375	78	7.8125
00111100	3C	0.9453	79	7.8125
00111110	3E	0.9609	7B	7.8125
00111111	3F	1.5000	C0	7.8125
01000000	40	0.8984	73	7.8125
01000001	41	0.9688	7C	7.8125
01000010	42	0.9766	7D	7.8125
01000011	43	0.9844	7E	7.8125
01000100	44	0.9922	7F	7.8125
01000110	46	1.0078	81	7.8125
01000111	47	1.0156	82	7.8125
01001000	48	1.0234	83	7.8125
01001001	49	1.0313	84	7.8125
01001010	4A	1.0391	85	7.8125
01001100	4C	1.0547	87	7.8125
01001101	4D	1.0625	88	7.8125
01001110	4E	1.0703	89	7.8125
01001111	4F	1.0781	8A	7.8125
01010000	50	1.0859	8B	7.8125
01010001	51	1.0938	8C	7.8125
01010011	53	1.1094	8E	7.8125
01010100	54	1.1172	8F	7.8125
01010101	55	1.1250	90	7.8125
01010110	56	1.1328	91	7.8125
01010111	57	1.1406	92	7.8125
01011000	58	1.1484	93	7.8125
01011001	59	1.1563	94	7.8125
01011010	5A	1.1641	95	7.8125
01011011	5B	1.1719	96	7.8125
01011100	5C	1.1797	97	7.8125
01011101	5D	1.1875	98	7.8125
01011110	5E	1.1953	99	7.8125
01011111	5F	1.7969	E6	7.8125
01100000	60	0.9531	7A	7.8125
01100010	62	1.2109	9B	7.8125
01100011	63	1.2188	9C	7.8125
01100100	64	1.2266	9D	7.8125
01100101	65	1.2344	9E	7.8125
01100110	66	1.2422	9F	7.8125
01100111	67	1.2500	A0	7.8125

Table 8. PROG1 8-Bit (Boot-Up Voltage) (Continued)

Binary Code	Hex Code	V _{BOOT} (V)	VOUT Command Code (Hex)	Delta from Previous Code (mV)
01101000	68	1.2578	A1	7.8125
01101001	69	1.2656	A2	7.8125
01101010	6A	1.2734	A3	7.8125
01101011	6B	1.2813	A4	7.8125
01101100	6C	1.2891	A5	7.8125
01101101	6D	1.2969	A6	7.8125
01101110	6E	1.3047	A7	7.8125
01101111	6F	1.3125	A8	7.8125
01110000	70	1.3203	A9	7.8125
01110001	71	1.3281	AA	7.8125
01110010	72	1.3359	AB	7.8125
01110011	73	1.3438	AC	7.8125
01110101	75	1.3594	AE	7.8125
01110110	76	1.3672	AF	7.8125
01110111	77	1.3750	B0	7.8125
01111000	78	1.3828	B1	7.8125
01111001	79	1.3906	B2	7.8125
01111010	7A	1.3984	B3	7.8125
01111011	7B	1.4063	B4	7.8125
01111100	7C	1.4141	B5	7.8125
01111101	7D	1.4219	B6	7.8125
01111110	7E	1.4297	B7	7.8125
01111111	7F	2.5000	140	7.8125
10000000	80	1.0000	80	7.8125
10000001	81	1.4375	B8	7.8125
10000010	82	1.4453	B9	7.8125
10000011	83	1.4531	BA	7.8125
10000100	84	1.4609	BB	7.8125
10000101	85	1.4688	BC	7.8125
10000110	86	1.4766	BD	7.8125
10000111	87	1.4844	BE	7.8125
10001000	88	1.4922	BF	7.8125
10001010	8A	1.5078	C1	7.8125
10001011	8B	1.5156	C2	7.8125
10001100	8C	1.5234	C3	7.8125
10001101	8D	1.5313	C4	7.8125
10001110	8E	1.5391	C5	7.8125
10001111	8F	1.5469	C6	7.8125
10010000	90	1.5547	C7	7.8125
10010001	91	1.5625	C8	7.8125

Table 8. PROG1 8-Bit (Boot-Up Voltage) (Continued)

Binary Code	Hex Code	V _{BOOT} (V)	VOUT Command Code (Hex)	Delta from Previous Code (mV)
10010010	92	1.5703	C9	7.8125
10010011	93	1.5781	CA	7.8125
10010100	94	1.5859	CB	7.8125
10010101	95	1.5938	CC	7.8125
10010110	96	1.6016	CD	7.8125
10010111	97	1.6094	CE	7.8125
10011000	98	1.6172	CF	7.8125
10011001	99	1.6250	D0	7.8125
10011010	9A	1.6328	D1	7.8125
10011011	9B	1.6406	D2	7.8125
10011100	9C	1.6484	D3	7.8125
10011101	9D	1.6563	D4	7.8125
10011110	9E	1.6641	D5	7.8125
10011111	9F	3.0000	180	7.8125
10100000	A0	1.0469	86	7.8125
10100001	A1	1.6719	D6	7.8125
10100010	A2	1.6797	D7	7.8125
10100011	A3	1.6875	D8	7.8125
10100100	A4	1.6953	D9	7.8125
10100101	A5	1.7031	DA	7.8125
10100110	A6	1.7109	DB	7.8125
10100111	A7	1.7188	DC	7.8125
10101000	A8	1.7266	DD	7.8125
10101001	A9	1.7344	DE	7.8125
10101010	AA	1.7422	DF	7.8125
10101011	AB	1.7500	E0	7.8125
10101100	AC	1.7578	E1	7.8125
10101101	AD	1.7656	E2	7.8125
10101110	AE	1.7734	E3	7.8125
10101111	AF	1.7813	E4	7.8125
10110000	B0	1.7891	E5	7.8125
10110010	B2	1.8047	E7	7.8125
10110011	B3	1.8125	E8	7.8125
10110100	B4	1.8203	E9	7.8125
10110101	B5	1.8281	EA	7.8125
10110110	B6	1.8359	EB	7.8125
10110111	B7	1.9141	F5	78.125
10111000	B8	1.9922	FF	78.125
10111001	B9	2.0703	109	78.125
10111010	BA	2.1484	113	78.125

Table 8. PROG1 8-Bit (Boot-Up Voltage) (Continued)

Binary Code	Hex Code	V _{BOOT} (V)	VOUT Command Code (Hex)	Delta from Previous Code (mV)
10111011	BB	2.2266	11D	78.125
10111100	BC	2.3047	127	78.125
10111101	BD	2.3828	131	78.125
10111110	BE	2.4609	13B	78.125
10111111	BF	3.2969	1A6	7.8125
11000000	C0	1.1016	8D	7.8125
11000001	C1	2.4688	13C	7.8125
11000010	C2	2.4766	13D	7.8125
11000011	C3	2.4844	13E	7.8125
11000100	C4	2.4922	13F	7.8125
11000110	C6	2.5078	141	7.8125
11000111	C7	2.5156	142	7.8125
11001000	C8	2.5234	143	7.8125
11001001	C9	2.6016	14D	78.125
11001010	CA	2.6797	157	78.125
11001011	CB	2.7578	161	78.125
11001100	CC	2.8359	16B	78.125
11001101	CD	2.9141	175	78.125
11001110	CE	2.9922	17F	78.125
11001111	CF	3.0703	189	78.125
11010000	D0	3.1484	193	78.125
11010001	D1	3.2266	19D	78.125
11010010	D2	3.2813	1A4	54.6875
11010011	D3	3.2891	1A5	7.8125
11010101	D5	3.3047	1A7	7.8125
11010110	D6	3.3125	1A8	7.8125
11010111	D7	3.3203	1A9	7.8125
11011000	D8	3.3281	1AA	7.8125
11011001	D9	3.4063	1B4	78.125
11011010	DA	3.4844	1BE	78.125
11011011	DB	3.5625	1C8	78.125
11011100	DC	3.6406	1D2	78.125
11011101	DD	3.7188	1DC	78.125
11011110	DE	3.7969	1E6	78.125
11011111	DF	5.0000	280	7.8125
11100000	E0	1.2031	9A	7.8125
11100001	E1	3.8750	1F0	78.125
11100010	E2	3.9531	1FA	78.125
11100011	E3	4.0313	204	78.125
11100100	E4	4.1094	20E	78.125

Table 8. PROG1 8-Bit (Boot-Up Voltage) (Continued)

Binary Code	Hex Code	V _{BOOT} (V)	V _{OUT} Command Code (Hex)	Delta from Previous Code (mV)
11100101	E5	4.1875	218	78.125
11100110	E6	4.2656	222	78.125
11100111	E7	4.3438	22C	78.125
11101000	E8	4.4219	236	78.125
11101001	E9	4.5000	240	78.125
11101010	EA	4.5781	24A	78.125
11101011	EB	4.6563	254	78.125
11101100	EC	4.7344	25E	78.125
11101101	ED	4.8125	268	78.125
11101110	EE	4.8906	272	78.125
11101111	EF	4.9688	27C	78.125
11110000	F0	4.9766	27D	7.8125
11110001	F1	4.9844	27E	7.8125
11110010	F2	4.9922	27F	7.8125
11110100	F4	5.0078	281	7.8125
11110101	F5	5.0156	282	7.8125
11110110	F6	5.0234	283	7.8125
11110111	F7	5.0313	284	7.8125
11111000	F8	5.1094	28E	78.125
11111001	F9	5.1875	298	78.125
11111010	FA	5.2656	2A2	78.125
11111011	FB	5.3438	2AC	78.125
11111100	FC	5.4219	2B6	78.125
11111101	FD	5.4922	2BF	70.3125
11111110	FE	5.5000	2C0	7.8125
11111111	FF	0	0	

As shown in [Table 8](#), one step is $2^{-7} = 7.8125\text{mV}$; some selections are higher than one step from adjacent codes. However, the resolution is $\pm 7.8125\text{mV}$ around the popular voltage regulation points, as shown in [Table 4 on page 25](#), for fine-tuning. For finer than 7.8125mV tuning, place a large ratio resistor divider on the VSEN pin between the output (V_{OUT}) and either RGND for positive offset or VDD for negative offset as shown in [Figure 43](#).

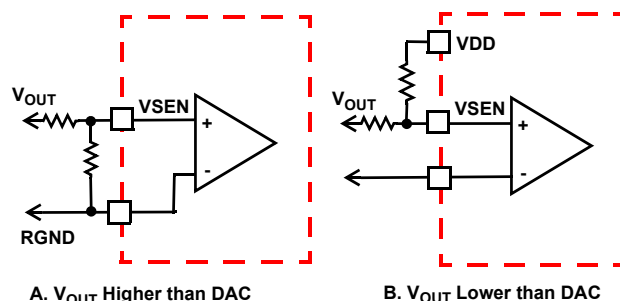


Figure 43. External Programmable Regulation

4.6 Thermal Monitoring and Compensation

The thermal monitoring function block diagram is shown in [Figure 44](#). A 10k Ω NTC resistor (P/N: NCP15XH103J03RC from Murata, $\beta = 3380$) inside the module is placed close to the output rail of the inductor to sense the operational temperature of the current sense component. An external 1.54k Ω pull-up resistor, R_{TM} , forms the voltage divider for the NTC pin. Because the NTC pin voltage can pick up noise from the phase node, an internal 0.1 μ F ceramic capacitor is placed in close proximity to the NTC pin. As the temperature of the inductor increases, the resistance of the NTC decreases resulting in reduced voltage at the NTC pin.

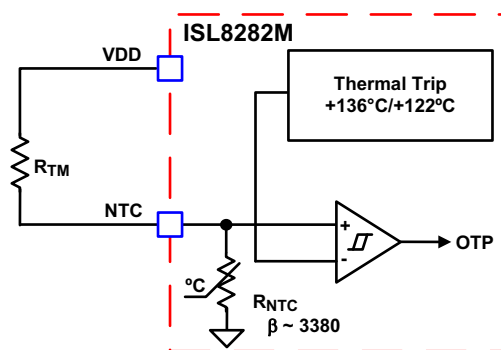


Figure 44. Thermal Monitoring and Protection Block Diagram

[Figure 45](#) shows the TM voltage over the temperature. Renesas recommends using a 1.54k Ω resistor for accurate temperature compensation because the internal thermal digital code is based on that component.

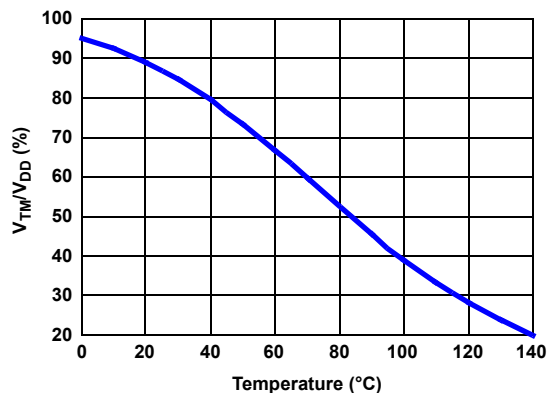


Figure 45. Ratio of TM Voltage to NTC Temperature with Recommended Parts

Because the voltage across the inductor is sensed for the output current information, the sensed current has the same positive temperature coefficient as the inductor DCR, which is about +0.385%/°C. To obtain the correct current information, the ISL8282M uses the voltage at the NTC pin and “TCOMP” register values to compensate the temperature impact on the sensed current. The block diagram of this function is shown in [Figure 46 on page 36](#).

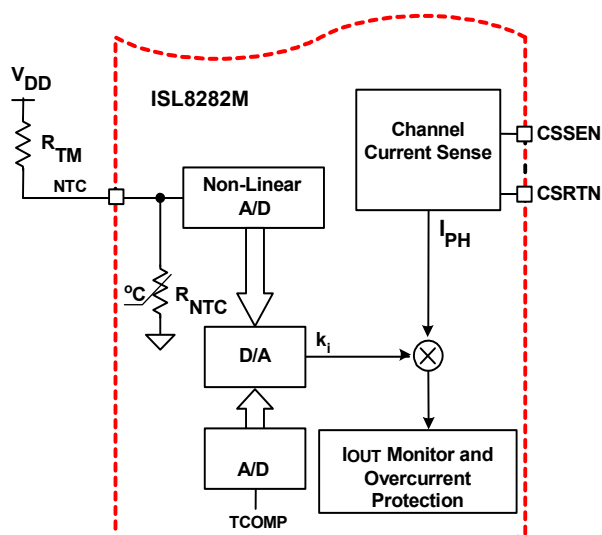


Figure 46. Integrated Temperature Compensation Block Diagram

Based on the V_{DD} voltage, the ISL8282M converts the NTC pin voltage to a digital signal for temperature compensation. With the ISL8282M nonlinear A/D converter, the NTC digital signal is linearly proportional to the NTC temperature. Because the NTC is not directly attached to the current sense component, it inherits high thermal impedance between the NTC and the current sense component. The temperature difference between them can be corrected by the TCOMP register values, which include four different TCOMP options that can be set by the PROG2 pin. The ISL8282M multiplexes the TCOMP register values with the NTC digital signal to obtain the adjustment gain to compensate the temperature impact on the sensed current. The compensated current signal is used for both I_{OUT} and OCP functions. Renesas recommends using $+5^{\circ}\text{C}$ as the TCOMP.

Table 9. TCOMP Values

D1h	TCOMP ($^{\circ}\text{C}$)	D1h	TCOMP ($^{\circ}\text{C}$)
0h	+30	2h	+5
1h	+15	3h	OFF

4.7 Fault Protection

The ISL8282M provides high system reliability with many fault protections, as summarized in [Table 10](#).

Table 10. Fault Protection Summary

Fault	Description	Fault Action
Input UVLO	VIN pin UVLO; or set by the EN pin with an external divider for higher level. See Figures 39 and 40 .	Shut down and recover when $V_{IN} > \text{UVLO}$
Bias UVLO	VDD, PVCC, 7VLDO UVLO	Shut down and recover when Bias $> \text{UVLO}$
Startup OVP	Higher than V_{BOOT} . See "Electrical Specifications" on page 12 .	Latch OFF, reset by VDD or toggling Enable (including the EN pin and/or OPERATION command based on the ON_OFF_CONFIG setting)
Output OVP	Rising = 116%; Falling = 100%	
Output UVP	74% of V_{OUT} , Latch OFF	
Short-Circuit and OCP Protection	Peak load current = 18.8A typical	Latch OFF, reset by VDD or toggling Enable (including the EN pin and/or OPERATION command based on the ON_OFF_CONFIG setting), or retry every 9ms; option is programmable by PROG3 or D3[0]
OTP	Rising = $22.31\%V_{DD}$ ($\sim +136^{\circ}\text{C}$) Falling = $27.79\%V_{DD}$ ($\sim +122^{\circ}\text{C}$)	Shut down above $+136^{\circ}\text{C}$ and recover when temperature drops below $+122^{\circ}\text{C}$

Input UVLO and OTP faults respond to the current state with hysteresis. Output OVP and output UVP faults are latch events. Output OCP and output short-circuit faults can be latch or retry events depending on the PROG3 or D3[0] setting. All fault latch events can be reset by VDD cycling, toggling the EN pin, or with the serial bus OPERATION command based on the ON_OFF_CONFIG setting. The OCP retry event has a hiccup time of 9ms and the module can be recovered when the fault is removed.

4.7.1 Overvoltage Protection

The Overvoltage Protection (OVP) fault detection circuit triggers when the voltage between V_{SEN+} and V_{SEN-} is above the rising overvoltage threshold. When an OVP fault is declared, the module latches off and the PGOOD pin is asserted low. The fault remains latched and can be reset by VDD cycling, toggling the EN pin, and/or the serial bus OPERATION command based on the ON_OFF_CONFIG setting.

Although the module latches off in response to an OVP fault, the Low-Side Gate Driver (LGATE) retains the ability to toggle the low-side MOSFET on and off in response to the output voltage transverse the OVP rising and falling thresholds. The LGATE turns on the low-side MOSFET to discharge the output voltage, protecting the load. The LGATE turns off the low-side MOSFET when the sensed output voltage is lower than the falling overvoltage threshold (typically 100%). If the output voltage rises again, the LGATE turns on the low-side MOSFET when the output voltage is above the rising overvoltage threshold (typically 120%). This process protects the load when there is a consistent overvoltage condition.

In addition to normal OVP operation, the startup OVP circuits are enabled to protect against OVP events 5.5ms (typical, worst 6.5ms) after all rails (VDD, PVCC, 7VLDO, VIN) POR and before the end of soft-start while the OVP level is set higher than V_{BOOT} . See [“Electrical Specifications” on page 12](#).

4.7.2 Undervoltage Protection

The Undervoltage Protection (UVP) fault detection circuit triggers if the output voltage is below the undervoltage threshold (typically 74% of DAC). When an UVP fault is declared, the module latches off, forcing the LGATE and High-Side Gate Driver (UGATE) outputs low, and the PGOOD pin is asserted low. The fault remains latched and can be reset by VDD cycling, toggling the EN pin, and/or with the serial bus OPERATION command based on the ON_OFF_CONFIG setting.

4.7.3 Overcurrent and Short-Circuit Protection

Inductor DCR sensing is used for current sense and senses current continuously for fast response. The current sense amplifier uses the CSEN and CSRTN inputs to reproduce a signal proportional to the inductor current, I_L . The reproduced signal is used for current reporting and overcurrent protection.

The Overcurrent Protection (OCP) is triggered when the load current is typically 18.8A. OCP protects inductor saturation from short-circuit events and provides a more robust power train and system protection. When an OCP or short-circuit fault is declared, the module latches off, forcing the both the high-side and low-side gate driver outputs low, or it retries with a hiccup time of 9ms. The fault response is programmable by PROG3 or D3[0]. However, the latched off event can be reset by VDD cycling, toggling the EN pin, and/or with the serial bus OPERATION command based on the ON_OFF_CONFIG setting.

4.7.4 Over-Temperature Protection

An NTC inside the module senses the inductor temperature for both over-temperature and current sense temperature compensation. The NTC is connected to the NTC pin and SGND pad and results in lower NTC pin voltage at higher temperatures. A comparator with hysteresis compares the NTC pin voltage to the threshold set. At +136°C (typical), Over-Temperature Protection (OTP) is triggered and the ISL8282M operation is disabled. When the sensed temperature is around +122.4°C, the ISL8282M resumes normal operation. When an OTP fault is declared, the module forces the LGATE and UGATE outputs low.

4.8 PGOOD Monitor

The PGOOD pin indicates when the converter is capable of supplying regulated voltage. PGOOD is asserted low if there is a fault condition of a rail's (VDD, PVCC, 7VLDO, or VIN) UVLO, output Overcurrent (OCP), output Overvoltage (OVP), output Undervoltage (UVP), or Over-Temperature (OTP). Note: the PGOOD pin is an undefined impedance with insufficient V_{DD} (typically <2.5V).

4.9 PFM Mode Operation

In PFM mode, programmable by the PROG2 pin, the switching frequency is dramatically reduced to minimize the switching loss and significantly improve light-load efficiency. The ISL8282M can achieve seamless transition between PFM mode and PWM mode as load changes. For high V_{OUT} applications, the LGATE might not turn on long enough to charge the boot capacitor in PFM mode with 0A load. Renesas recommends enabling the ISL8282M's ultrasonic PFM feature, programmable by the PROG3 pin, which maintains the LGATE switching frequency above 20kHz and keeps the boot capacitor charged for immediate load apply events. Alternatively, maintaining a minimum load can enhance the boot capacitor charge.

4.10 SMBus, PMBus, and I²C Operation

The ISL8282M features SMBus, PMBus, and I²C with 32 programmable addresses through the PROG2 pin. The SMBus/PMBus includes an Alert# line (SALERT) and Packet Error Check (PEC) to ensure data is properly transmitted. The telemetry update rate is typically 108μs. The supported SMBus/PMBus/I²C addresses are summarized in [Table 11 on page 38](#). The 7-bit format address does not include the last bit (write and read): 40-47h, 60-67h, and 70-7Fh.

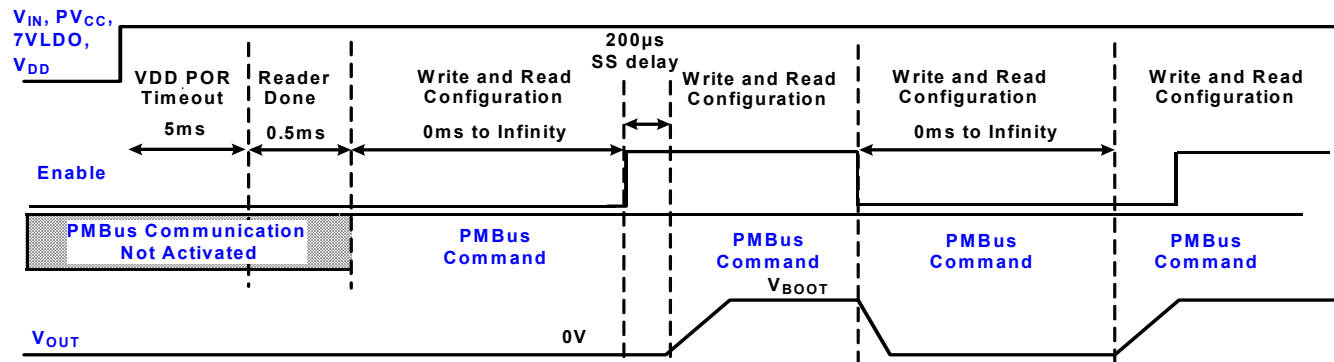
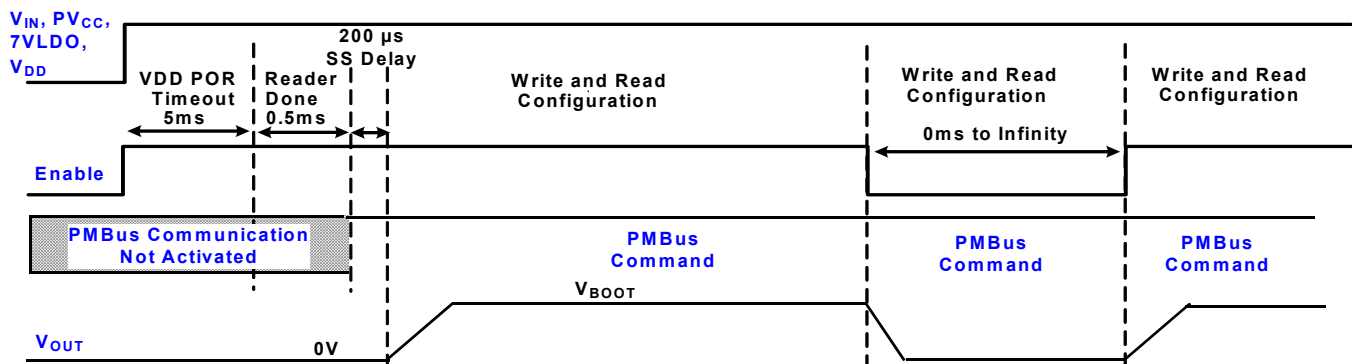
SMBus/PMBus/I²C allows the user to program the registers, as shown in [Table 12 on page 42](#), except for SMBus/PMBus/I²C addresses, 5.5ms (typical, worst 6.6ms) after all rails (VDD, PVCC, 7VLDO, and VIN) are above POR. [Figures 47 and 48 on page 39](#) show the initialization timing diagram for the serial bus with different EN (Enable) pin states.

For proper operation, follow the SMBus, PMBus, and I²C protocol shown in [Figure 49 on page 41](#). Note: the STOP (P) bit is NOT allowed before the repeated START condition when reading the contents of a register.

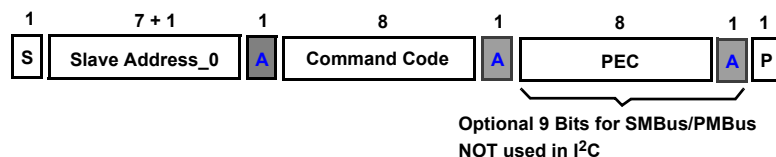
When the device's serial bus is not used, ground the device's SCL, SDA, and ALERT pins and do not connect them to the bus.

Table 11. SMBus/PMBus/I²C 7-Bit Format Address (Hex)

7-Bit Address	7-Bit Address	7-Bit Address
40	63	76
41	64	77
42	65	78
43	66	79
44	67	7A
45	70	7B
46	71	7C
47	72	7D
60	73	7E
61	74	7F
62	75	

Figure 47. Simplified SMBus/PMBus/I²C Initialization Timing Diagram with Enable LowFigure 48. Simplified SMBus/PMBus/I²C Initialization Timing Diagram with Enable High

1. Send Byte Protocol



Example command: 03h Clear Faults
(This clears all of the bits in Status Byte for the selected Rail)

S: Start Condition

A: Acknowledge ("0")

N: Not Acknowledge ("1")

W: Write ("0")

RS: Repeated Start Condition

R: Read ("1")

PEC: Packet Error Checking

P: Stop Condition

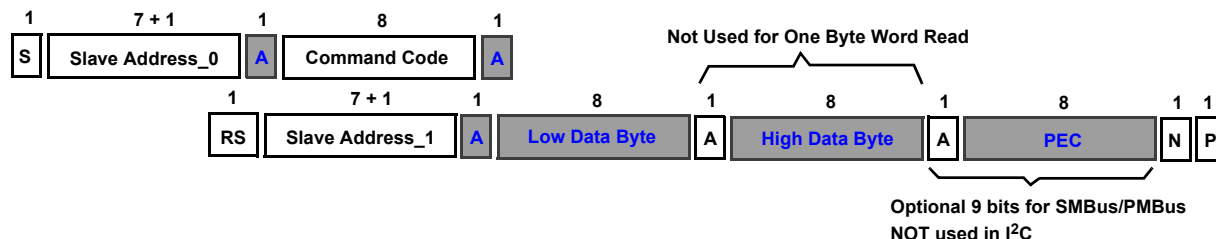
Acknowledge or DATA from Slave, ISL8282M

2. Write Byte/Word Protocol



Example command: D0h ENABLE_PFM (one word, High Data Byte, and ACK are not used)

3. Read Byte/Word Protocol

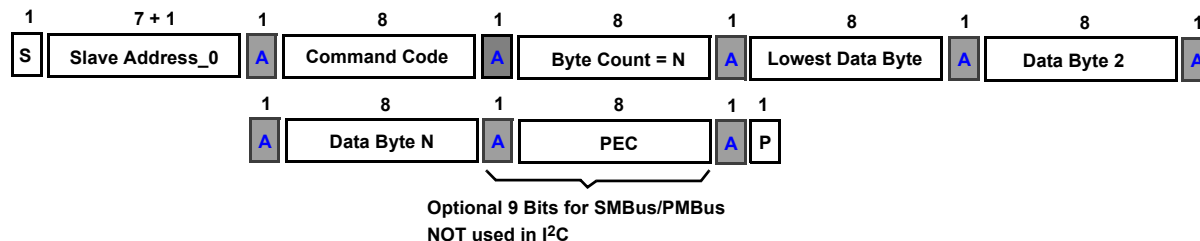


Example command: 8B READ_VOUT (two words, read voltage of the selected rail).

NOTE: All Writable commands are read with one byte word protocol.

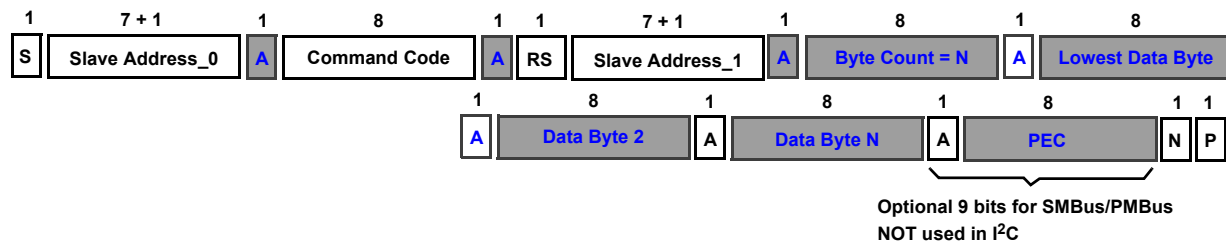
The STOP (P) bit is NOT allowed before the repeated START condition when "reading" contents of a register.

4. Block Write Protocol



Example command: ADh IC_DEVICE_ID (2 Data Byte)

5. Block Read Protocol



Example command: 8B READ_VOUT (two words, read voltage of the selected rail).

NOTE: All Writable commands are read with one byte word protocol.

The STOP (P) bit is NOT allowed before the repeated START condition when “reading” contents of a register.

6. Group Command Protocol - No more than one command can be sent to the same Address

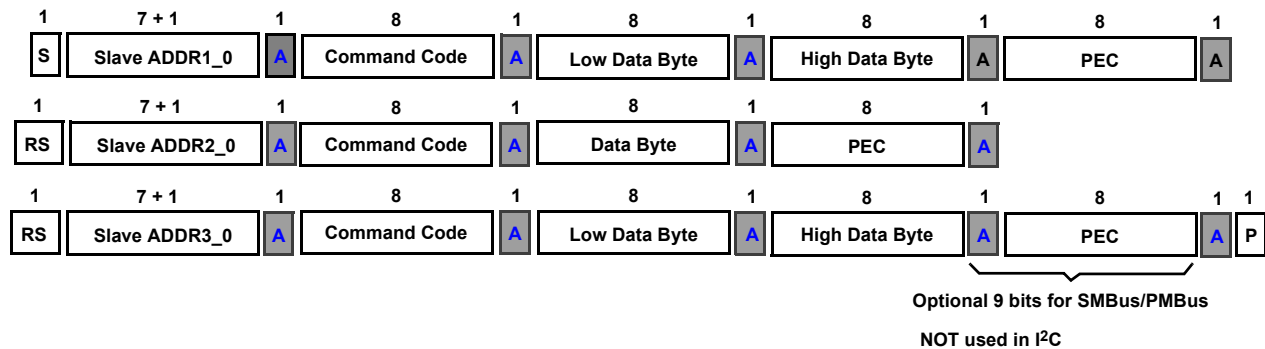


Figure 49. SMBus/PMBus/I²C Command Protocol

Table 12. SMBus, PMBus, and I²C Supported Commands

Command Code	Access	Word Length (Byte)	Default Value	Command Name	Description
01h[7:0]	R/W	One	80h	OPERATION	Module Enable (depending up the ON_OFF_CONFIG configuration): Bit[7]: 0 = OFF (0-F); 1 = ON (80-8Fh) Bit[6:4] = 0 Bit[3:0] = Don't care
02h[7:0]	R/W	One	1Fh	ON_OFF_CONFIG	Configures module enabled by OPERATION and/or EN pin: Bit[7:5] = 0 Bit[4] = 1 Bit[3] = OPERATION command Enable 0h = OPERATION command has no control on module 1h = OPERATION command can turn module ON/OFF Bit[2] = CONTROL pin Enable 0h = EN pin has no control on module 1h = EN pin can turn ON/OFF module Bit[1] = 1 Bit[0] = 1 Bit[3:2] = 00b = 13h (always on) Bit[3:2] = 01b = 17h (EN controls module) Bit[3:2] = 10b = 1Bh (OPERATION controls module) Bit[3:2] = 11b = 1Fh (EN and OPERATION control module)
03h	Send Byte	N/A		CLEAR_FAULTS	Clears faults in status registers
20h[7:0]	R	One	19h	VOUT_MODE	Sets host format of V _{OUT} command. Always linear format: N = -7
21h[2:0]	R/W	Two	PROG1[7:0]	VOUT_COMMAND	Sets output voltage Hex code = DEC2HEX [ROUND(V _{OUT} /2 ⁻⁷)]
24h[15:0]	R/W	Two	VBOOT + 500mV	VOUT_MAX	Sets maximum output voltage that module can command (DAC ≤ VOUT_MAX). Linear format. N = -7 Hex Code = DEC2HEX(ROUNDUP(VOUT_MAX/ 2 ⁻⁷))
33h[15:0]	R/W	Two	PROG3[5:3]	FREQUENCY_SWITCH	Sets module switching frequency (in linear format) Supports seven options (N = 0): 12Ch = 300kHz 190h = 400kHz 1F4h = 500kHz 258h = 600kHz 2BCh = 700kHz 352h = 850kHz 3E8h = 1MHz
78h[8:0]	R	One		STATUS_BYTE	Fault reporting; Bit7 = Busy Bit6 = OFF (Reflects current state of operation and ON_OFF_CONFIG registers as well as module operation) Bit5 = OVP Bit4 = OCP Bit3 = 0 Bit2 = OTP Bit1 = Bus communication error Bit0 = NONE OF ABOVE (OUTPUT UVP, VOUT_COMAND > VOUT_MAX, or V _{OUT} OPEN SENSE)

Table 12. SMBus, PMBus, and I²C Supported Commands (Continued)

Command Code	Access	Word Length (Byte)	Default Value	Command Name	Description
88h[15:0]	R	Two		READ_VIN	Input voltage (N = - 4, Max = 31.9375V) $V_{IN} (V) = \text{HEX2DEC}(88 \text{ hex data} - E000h) \times 0.0625V$
8Bh[15:0]	R	Two		READ_VOUT	Module output voltage, resolution = 7.8125mV = 2 ⁻⁷ $V_{OUT} (V) = \text{HEX2DEC}(8B \text{ hex data}) \times 2^{-7}$
8Ch[15:0]	R	Two		READ_IOUT	Module output current (N = -3, IMAX = 63.875A) $I_{OUT} (A) = \text{HEX2DEC}(8C \text{ hex data} - E800) \times 0.125A$ when I_{OUT} pin voltage = 2.5V at 63.875A load.
8Dh[15:0]	R	Two		READ_TEMP	Module temperature
98h[7:0]	R	One	02h	PMBUS_REVISION	Indicates PMBus revision 1.2
AD[15:0]	Block R	Two	0xD000	IC_DEVICE_ID	ISL8282M device ID
AE[15:0]	Block R	Two	0x000A	IC_DEVICE_REVISION	ISL8282M device revision
D0[0:0]	R/W	One	PROG2[7:7]	ENABLE_PFM	PFM OPERATION 0h = PFM Enabled 1h = PFM Disabled (always CCM mode)
D1[1:0]	R/W	One	PROG2[6:5]	TEMP_COMP	Thermal compensation: 0h = +30°C 01h = +15°C 02h = +5°C 03h = OFF
D2[0:0]	R/W	One	PROG3[7:7]	ENABLE_ULTRASONIC	Ultrasonic PFM enable 0h = 25kHz clamp disabled 1h = 25kHz clamp enabled
D3[0:0]	R/W	One	PROG3[6:6]	OCP_BEHAVIOR	Set latch or infinite retry for OCP fault: 0h = Retry every 9ms 01 = Latch-OFF
D4[2:0]	R/W	One	PROG3[2:0]	AV_GAIN	R4 AV GAIN (PROG4, AV Gain Multiplier = 2x) 0h = 84 1h = 73 2h = 61 3h = 49 4h = 38 5h = 26 6h = 14 7h = 2 R4 AV GAIN (PROG4, AV Gain Multiplier = 1x) 0h = 42 1h = 36.5 2h = 30.5 3h = 29.5 4h = 19 5h = 13 6h = 7 7h = 1
D5[2:0]	R/W	One	PROG4[7:5]	RAMP_RATE	Soft-start rate (mV/μs) 0h = 1.25 1h = 2.5 2h = 5 3h = 10 5h = 0.157 6h = 0.315 7h = 0.625;

Table 12. SMBus, PMBus, and I²C Supported Commands (Continued)

Command Code	Access	Word Length (Byte)	Default Value	Command Name	Description
D6[1:0]	R/W	One	PROG4[4:3]	SET_RR	Sets RR 0h = 200k 01h = 400k 02h = 600k 03h = 800k
DC[7:0]	R	One		READ_PROG1	Reads PROG1
DD[7:0]	R	One		READ_PROG2	Reads PROG2
DE[7:0]	R	One		READ_PROG3	Reads PROG3
DF[7:0]	R	One		READ_PROG4	Reads PROG4

Note: Serial bus communication is valid 5.5ms (typical, worst 6.5ms) after VDD, VIN, 7VLDO, and PVCC above POR. The telemetry update rate is 108μs.

5. Layout Guidelines

Careful attention to layout requirements is necessary for a successful implementation of the ISL8282M power module. The ISL8282M switches at a very high frequency. Therefore, the switching times are very short. At these switching frequencies, even the shortest trace has significant impedance. The peak gate drive current also rises significantly in an extremely short time. Current transition from one MOSFET to another causes voltage spikes across the interconnecting impedances and parasitic circuit elements. The voltage spikes can degrade efficiency, generate EMI, and increase MOSFET voltage stress and ringing. Careful component selection and proper PCB layout minimize the magnitude of these voltage spikes. Use the ISL8282MEVAL1Z as a example and reference for the PCB layout.

The following are layout considerations:

- Renesas recommends using a six-layer PCB board. Use the top and bottom layer to route VIN and VOUT. Use a full ground plane in the internal layers (underneath the module) with shared SGND and PGND to simplify the layout design. Use another full ground plane directly above the bottom layer. Use the other internal layers to route the remote sense, PGOOD, SCL, SDA, and SALERT signals.
- Place the input capacitors and high frequency decoupling ceramic capacitors between VIN and PGND as close to the module as possible. The loop formed by the input capacitors, VIN, and PGND must be as small as possible to minimize high frequency noise. Place the output ceramic capacitors close to VOUT. Use a copper plane to connect the output ceramic capacitors to the load to avoid any parasitic inductances and resistances. An example layout is illustrated in [Figures 50](#) and [51](#).
- Use large copper planes for power paths (VIN, VOUT, and PGND) to minimize conduction loss and thermal stress. Also, use multiple vias to connect the power planes in different layers.
- Do not oversize the copper planes for the PHASE planes. Because the PHASE planes are subjected to very high dv/dt, the parasitic capacitor formed between these planes and the surrounding circuitry tends to couple the switching noise. Ensure that none of the sensitive signal traces are routed close to the PHASE plane.
- Place the PVCC and VIN1 bypass capacitors underneath the PVCC and VIN1 pins and connect their grounds to the SGND. For the external pin-strap resistor dividers connected to PROG1, PROG2, PROG3, and PROG4, connect the low side dividers' ground to the SGND. If a local decoupling capacitor is used to bias these resistor dividers, place the decoupling capacitor close to the dividers, and connect the capacitor's ground to the SGND. An example layout is illustrated in [Figure 51](#).
- Connect remote sensing traces to the regulation point to achieve a tight output voltage regulation. Route the remote sensing traces in parallel underneath the PGND layer and avoid routing the sensing trace near noisy planes such as PHASE. Place 2Ω resistors close to VSEN and RGND, respectively, to dampen the noise on the traces.

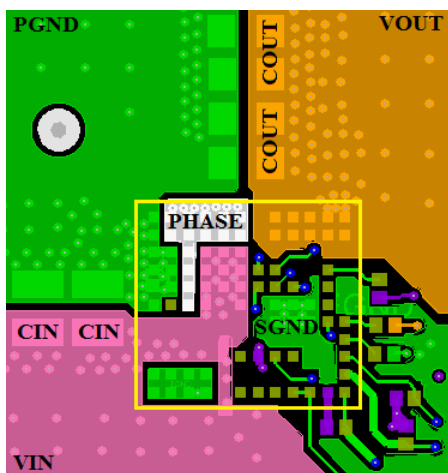


Figure 50. Layout Example - Top Layer

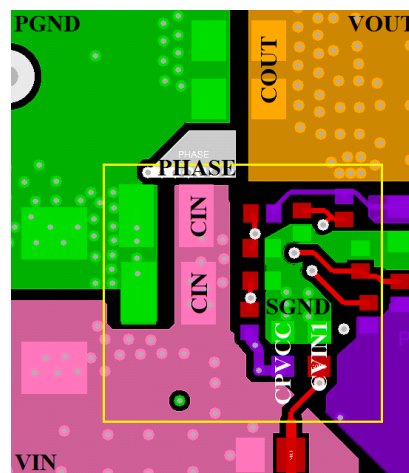


Figure 51. Layout Example - Bottom Layer

6. Thermal Considerations

Use the experimental power loss and θ_{JA} from thermal modeling analysis to evaluate the thermal consideration for the module. The derating curves are derived from the maximum power allowed while maintaining the temperature below the maximum junction temperature of +125°C. The derating curves are derived based on tests of the ISL8282M evaluation board, which is a 6-layer board 3 x 3.4 inches in size with 2oz Cu on all layers and multiple via interconnects. In the actual application, other heat sources and design margins should be considered.

7. Package Description

The structure of the ISL8282M belongs to the High Density Array no-lead package (HDA). The HDA package has good thermal and electrical conductivity, low weight, and small size and is applicable for surface mounting technology that is being more readily used in the industry. The ISL8282M contains several types of devices, including resistors, capacitors, inductors, MOSFETs, and control ICs. The ISL8282M is a copper leadframe-based package with exposed copper thermal pads that have good electrical and thermal conductivity. The copper leadframe and multicomponent assembly is overmolded with a polymer mold compound to protect these devices.

The package outline, typical Printed Circuit Board (PCB) layout pattern design, and typical stencil pattern design are shown in the [“Package Outline Drawing” on page 50](#). The module has a small size of 12mm x 11mm x 5.3mm.

7.1 PCB Layout Pattern Design

The bottom of the ISL8282M is a leadframe footprint attached to the PCB by a surface mounting process. The PCB layout pattern is shown in the [“Package Outline Drawing” on page 50](#). The PCB layout pattern is an array of solder mask defined PCB lands that align with the perimeters of the HDA exposed pads and I/O termination dimensions. The thermal lands on the PCB layout also feature an array of solder mask defined lands and should match 1:1 with the package exposed die pad perimeters. The exposed solder mask defined PCB land area should be 50-80% of the available module I/O area.

7.2 Thermal Vias

A grid of 1.0mm to 1.2mm pitch thermal vias drops down and connects to buried copper plane(s). Place the grid under the thermal land. The vias should be about 0.3mm to 0.33mm in diameter with the barrel plated to about 1.0 oz. of copper. Although adding more vias (by decreasing via pitch) improves the thermal performance, increasing the number of vias eventually yields diminishing returns. Use as many vias as practical for the thermal land size allowed by your board design rules.

7.3 Stencil Pattern Design

Reflowed solder joints on the perimeter I/O lands should have about a 50µm to 75µm (2mil to 3mil) standoff height. The solder paste stencil design is the first step in developing optimized, reliable solder joints. The stencil aperture size to solder mask defined PCB land size ratio should typically be 1:1. The aperture width can be reduced slightly to help prevent solder bridging between adjacent I/O lands. A typical solder stencil pattern is shown in the [“Package Outline Drawing” on page 50](#). Consider the symmetry of the whole stencil pattern when designing its pads. A laser cut, stainless steel stencil with electropolished trapezoidal walls is recommended. Electropolishing “smooths” the aperture walls resulting in reduced surface friction and better paste release, which reduces voids. Using a Trapezoidal Section Aperture (TSA) also promotes paste release and forms a brick-like paste deposit that assists in firm component placement. A 0.1mm to 0.15mm stencil thickness is recommended for this large pitch HDA.

7.4 Reflow Parameters

Due to the low mount height of the HDA, “No-Clean” Type 3 solder paste per ANSI/J-STD-005 is recommended. A nitrogen purge is also recommended during reflow. A system board reflow profile depends on the thermal mass of the entire populated board, so it is not practical to define a specific soldering profile just for the HDA. The profile given in [Figure 52](#) is a guideline that can be adapted for varying manufacturing practices and applications.

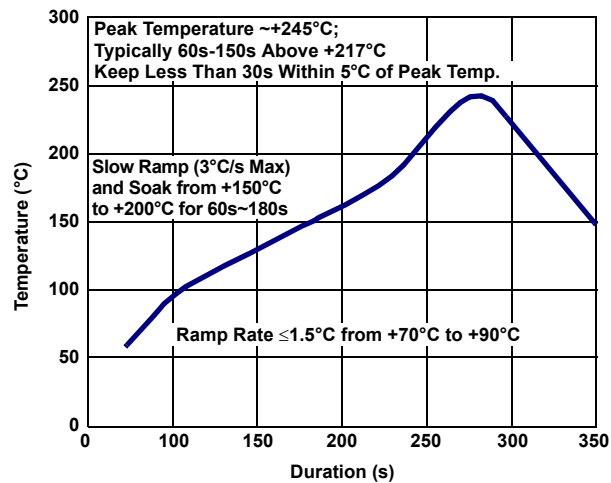


Figure 52. Typical Reflow Profile

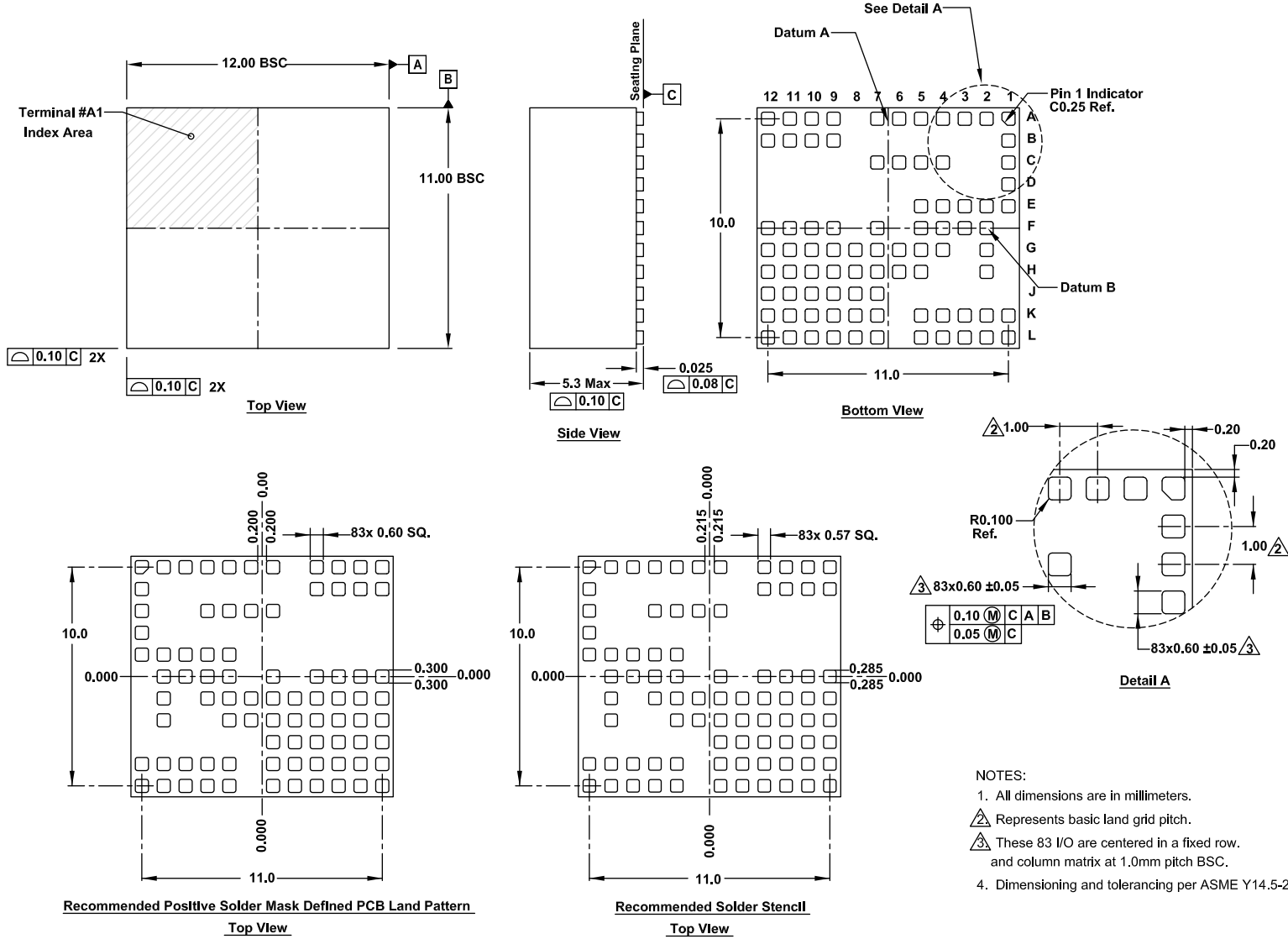
8. Revision History

Rev.	Date	Description
1.00	Feb 14, 2019	Updated Title on page 1. Updated VOUT, SALERT, and SDA pin descriptions on page 8. Updated Figure 28 label on page 20. Updated the ENABLE_PFM command description on page 43. Removed subheading on page 45. Updated Disclaimer.
0.00	Dec 14, 2018	Initial release.

9. Package Outline Drawing

Y83.12x11
83 I/O 12mmx11mmx5.3mm HDA Module
Rev 0, 3/18

For the most recent package outline drawing, see [Y83.12x11](#).



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