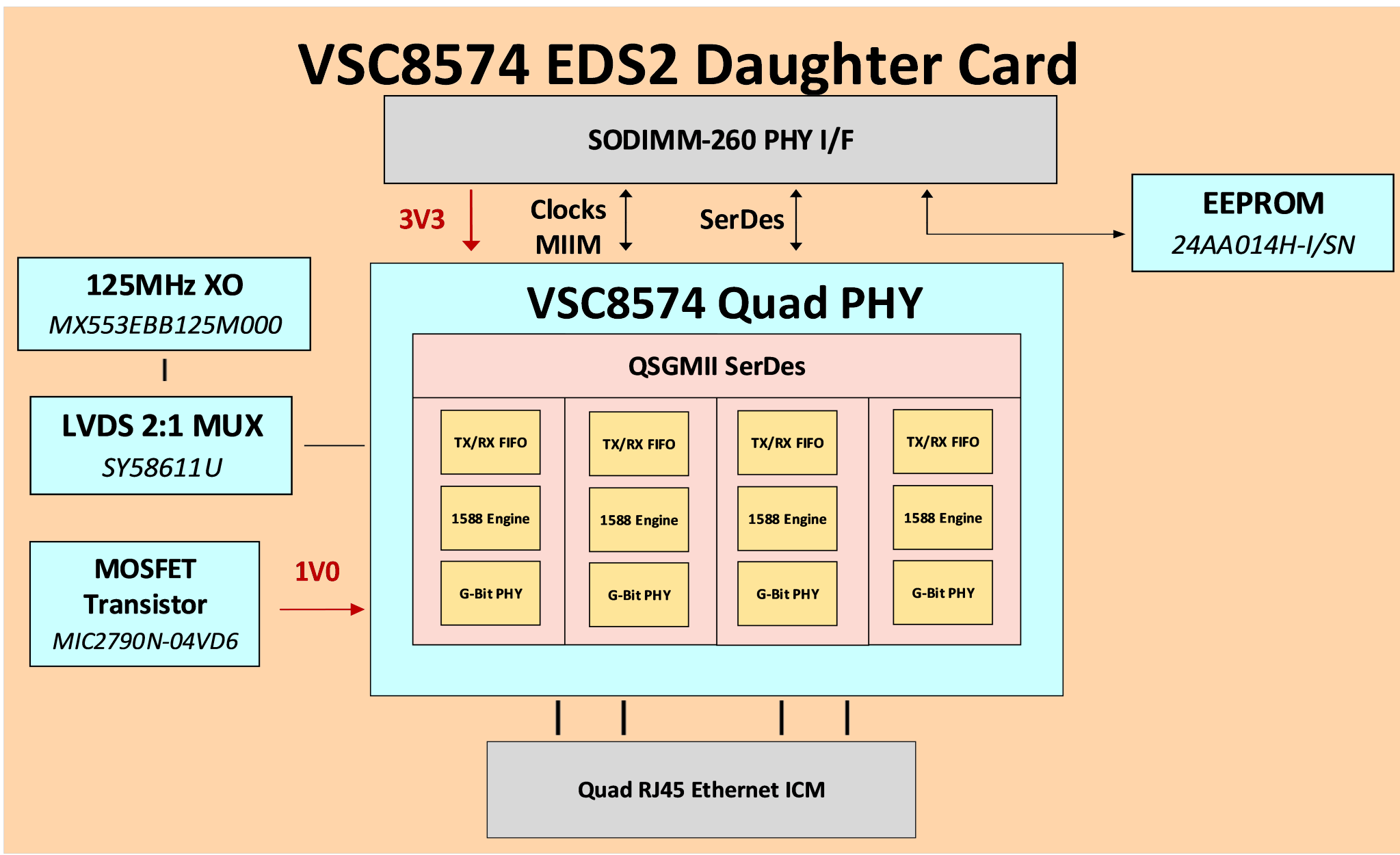


Title Page

| Revision History | | | |
|------------------|------------|-----------------------------------|---------------|
| Revision | Date | Revision Summary | Author |
| R2 | 03/28/2025 | Adjusted PTP connection. Released | Alexys Antell |

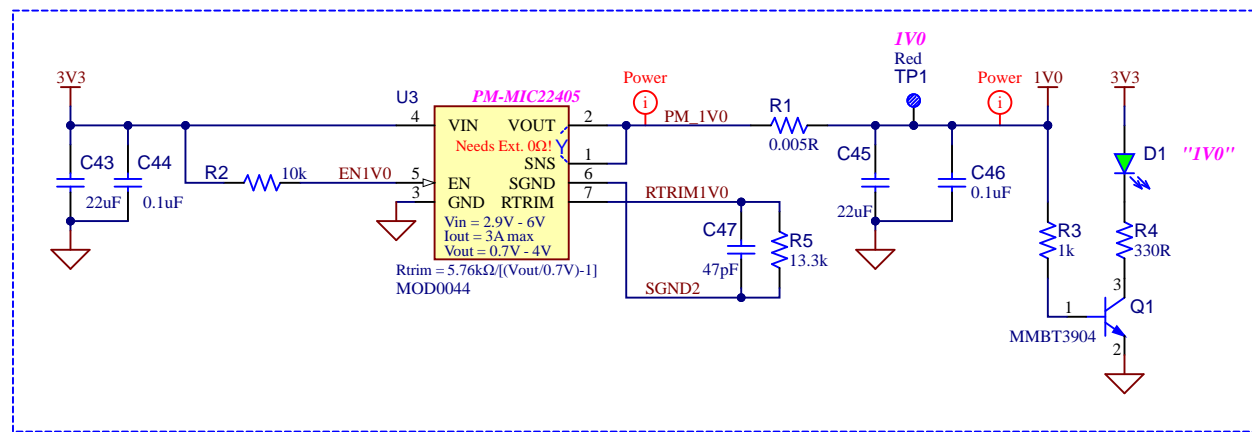
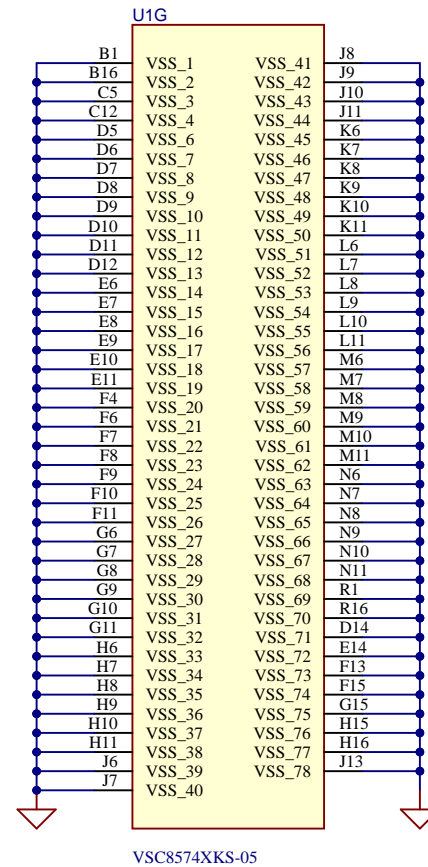
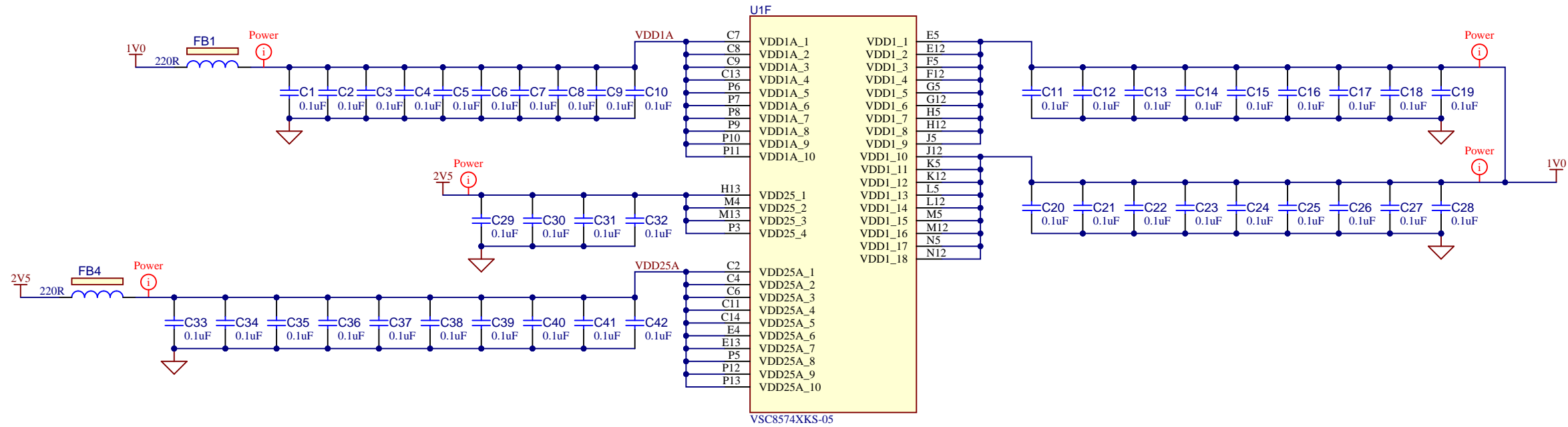
| Table of Contents | |
|-------------------|-----------------------|
| Sheet | Description |
| 1 | Title Page |
| 2 | Power |
| 3 | PHY, Reset, Clock |
| 4 | Ethernet Ports |
| 5 | SODIMM Edge Connector |

VSC8574 EDS2 Daughter Card



| | | | |
|---------------------------------------|---|-------------------|----------------|
| Project Owner: Alexys Antell | | | |
| PCB Layout Contact: Lori Cantrell | | | |
| PartNumber: EV16R73A | Project Title: VSC8574 EDS2 Daughter Card | Variant: Standard | |
| Sheet Title: Title Page | | | |
| Size: B | SCH #: 02-01031 | Rev: 2 | Date: 4/4/2025 |
| | PCB #: 04-12101 | Rev: 2 | Sheet 1 of 5 |
| File: 1 Title Page_UNG10045_B0.SchDoc | | | |

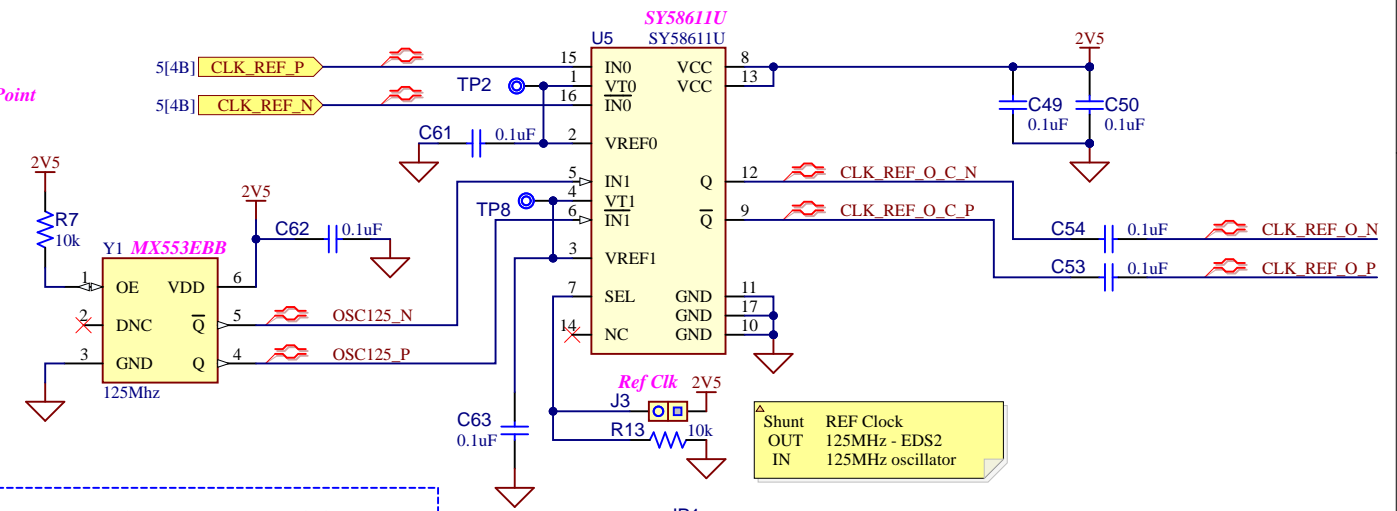
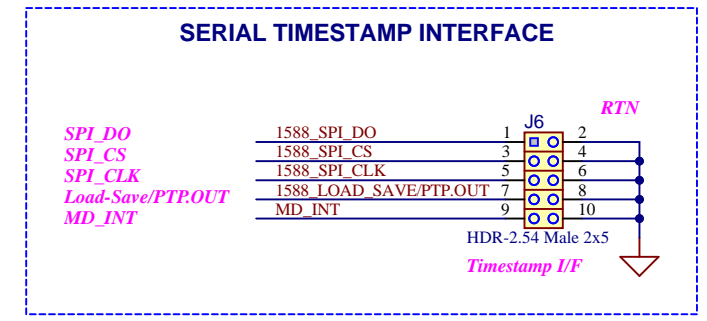
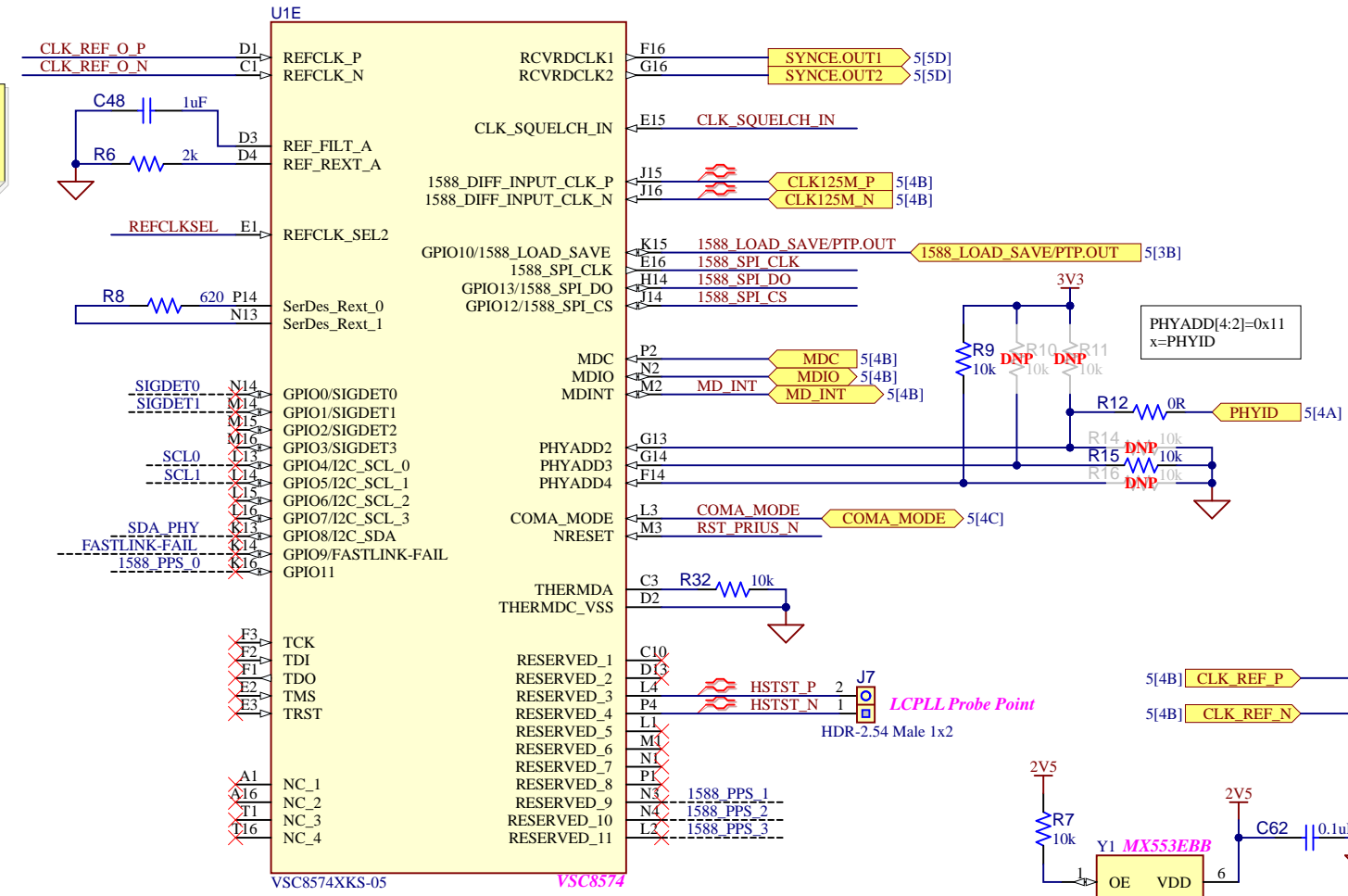
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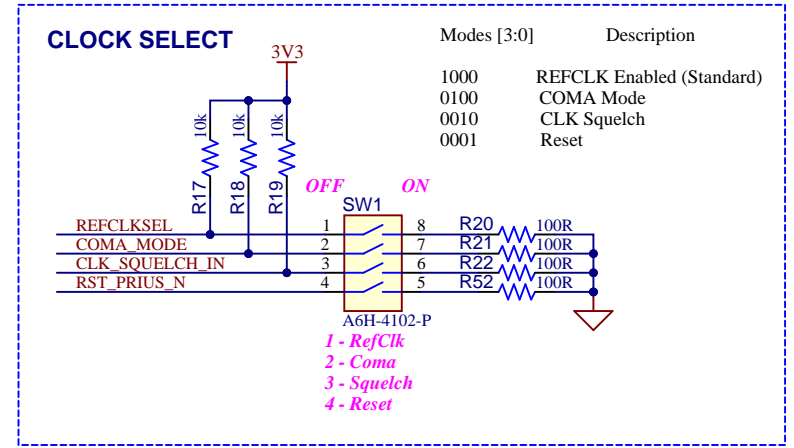
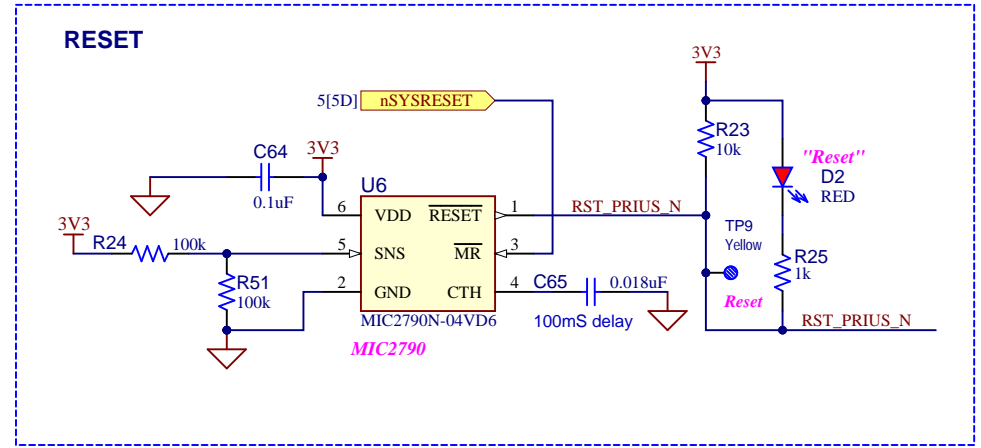
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| Project Owner: Alexys Antell | | | |
| PCB Layout Contact: Lori Cantrell | | | |
| PartNumber: EV16R73A | Project Title VSC8574 EDS2 Daughter Card | Variant: Standard | |
| Sheet Title Power | | | |
| Size B | SCH #: 02-01031 | Rev: 2 | Date: 4/4/2025 |
| | PCB #: 04-12101 | Rev: 2 | Sheet 2 of 5 |
| File: 2_Power_UNG10045_B0.SchDoc | | | |



Layout Note:
 REF_FILT_A (D3) and REF_REXT_A (D4) -
 The ground connections of the resistor and
 capacitor should each be connected to a shared
 PCB signal trace (rather than being connected
 individually to a common ground plane)



Shunt REF Clock
 OUT 125MHz - EDS2
 IN 125MHz oscillator

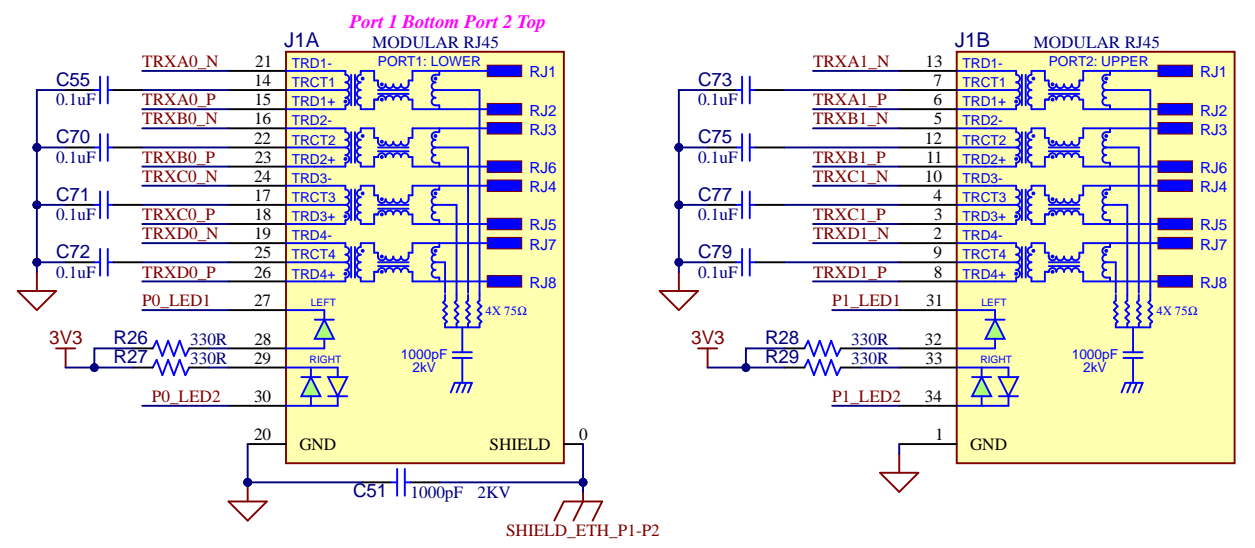
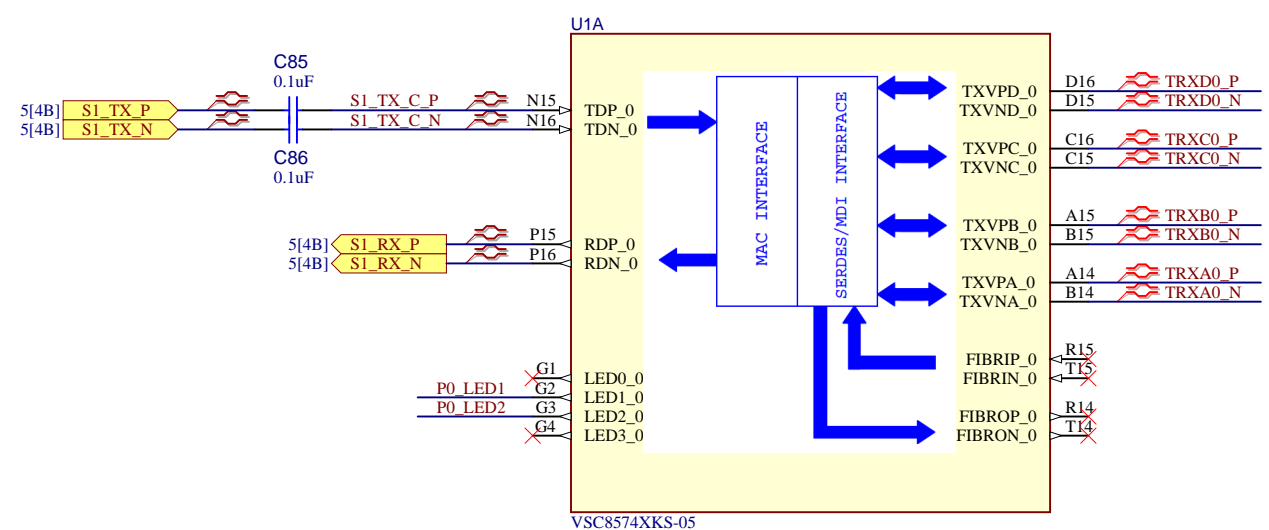


| Modes [3:0] | Description |
|-------------|---------------------------|
| 1000 | REFCLK Enabled (Standard) |
| 0100 | COMA Mode |
| 0010 | CLK Squelch |
| 0001 | Reset |

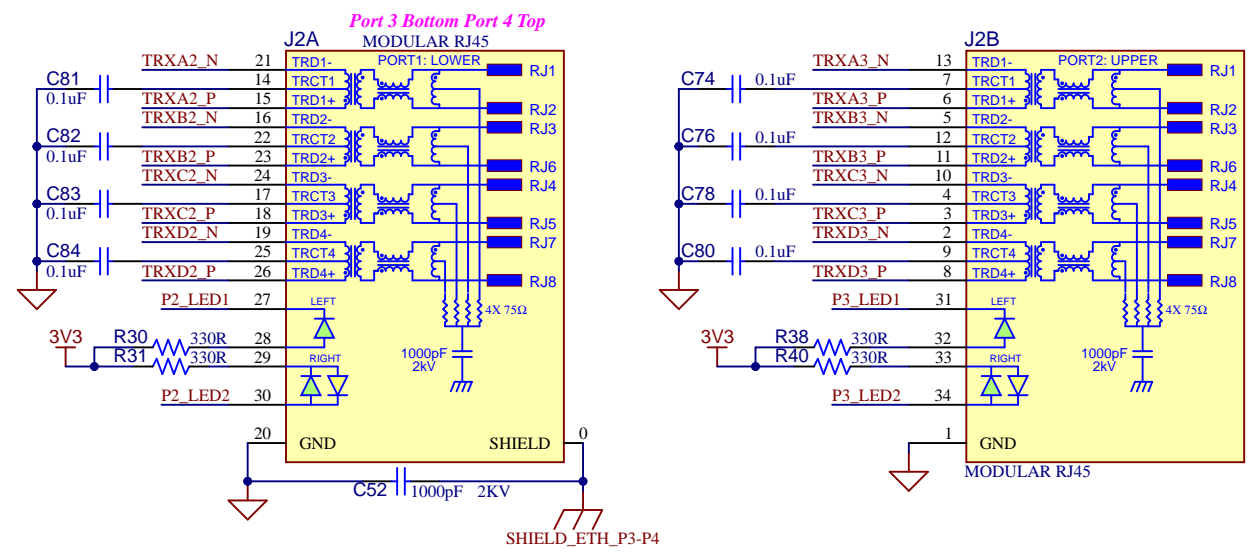
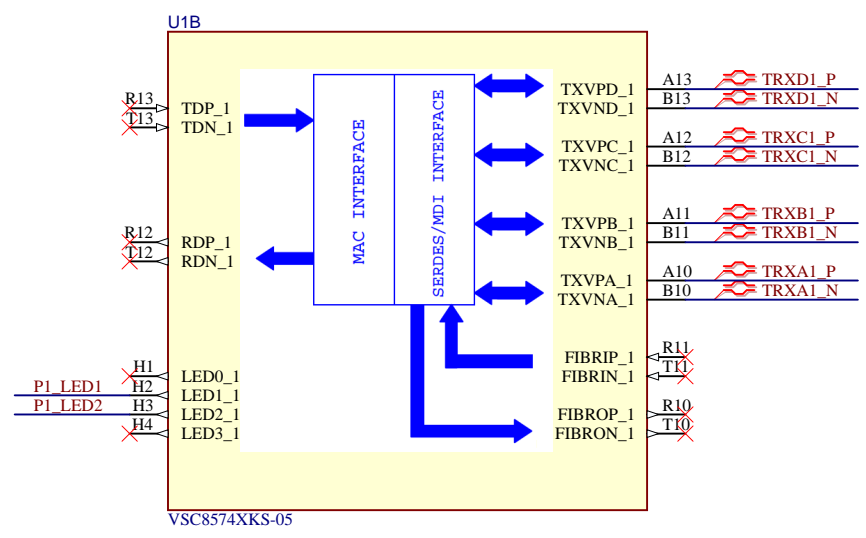
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|--|--|-------------------|
| Project Owner: Alexys Antell | | |
| PCB Layout Contact: Lori Cantrell | | |
| Part Number: EV16R73A | Project Title VSC8574 EDS2 Daughter Card | Variant: Standard |
| Sheet Title PHY, Reset, Clock | | |
| Size B | SCH #: 02-01031 | Rev: 2 |
| | PCB #: 04-12101 | Rev: 2 |
| | | Date: 4/4/2025 |
| | | Sheet 3 of 5 |
| File: 3_PHY_Reset_Clock_UNG10045_B0.SchDoc | | |



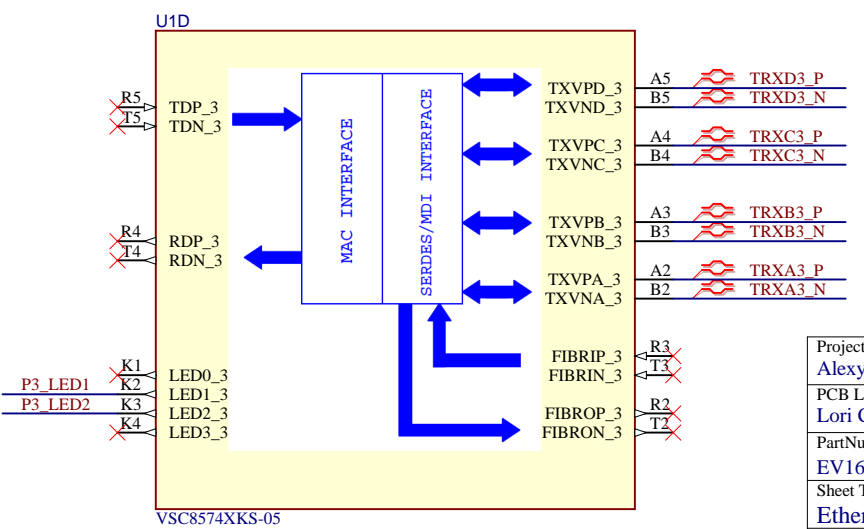
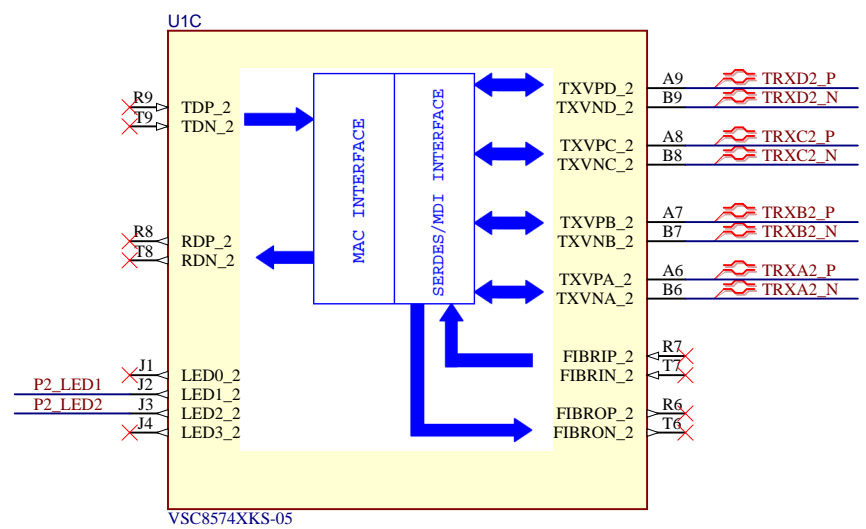
A



B



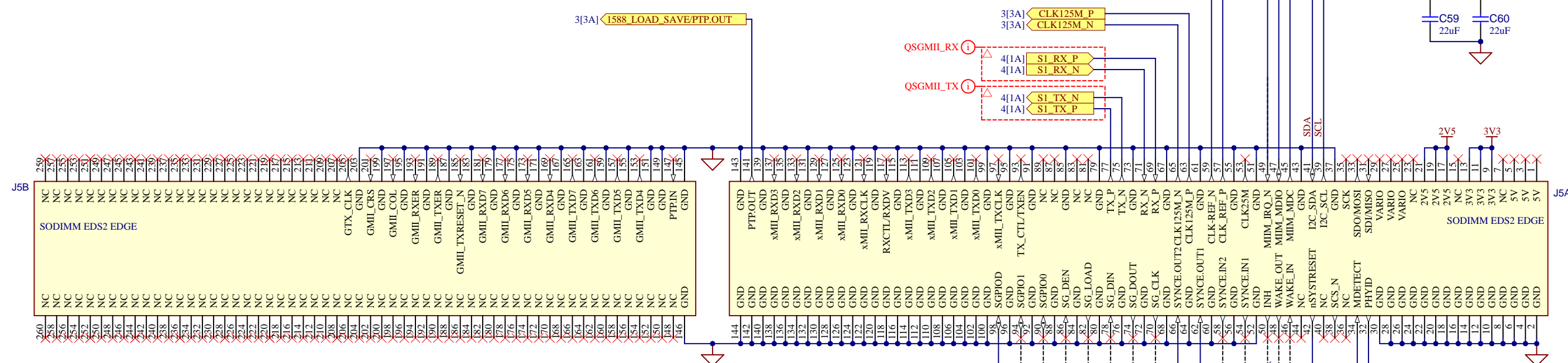
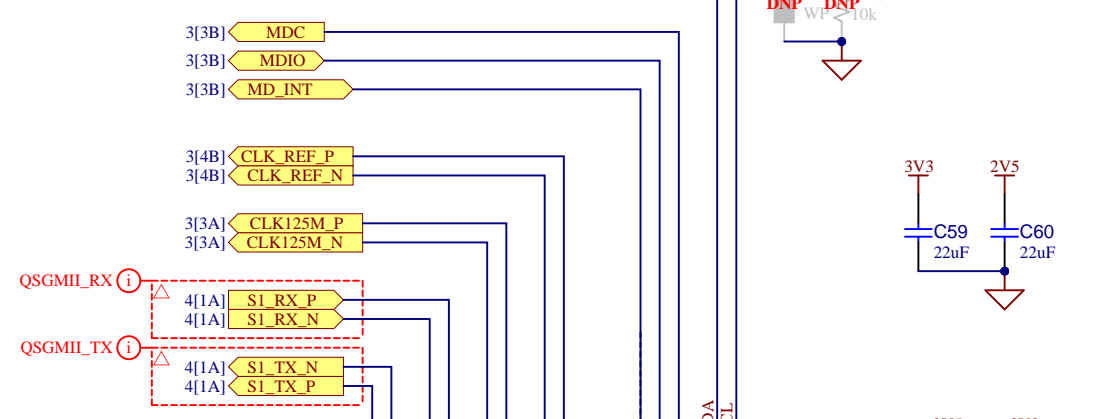
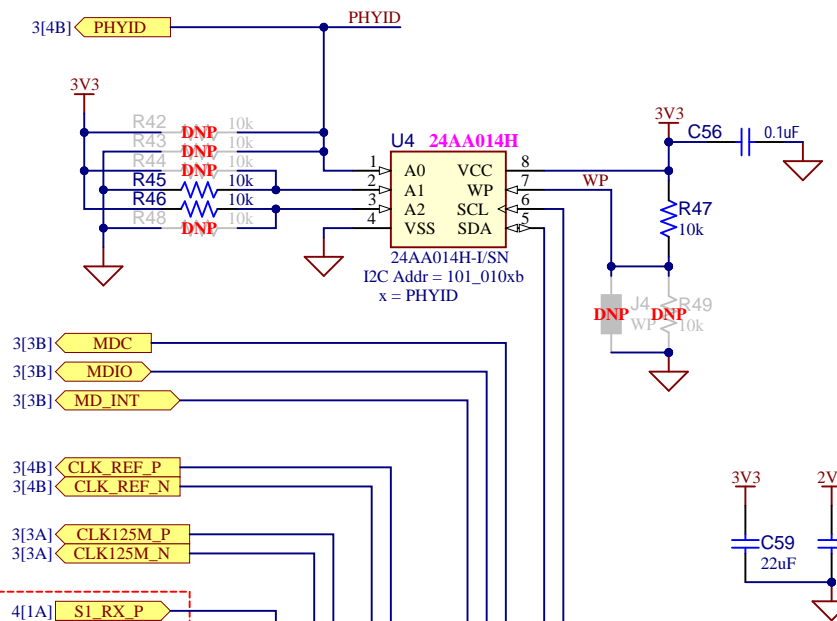
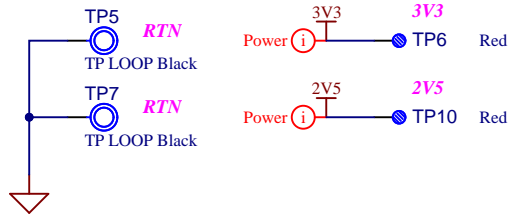
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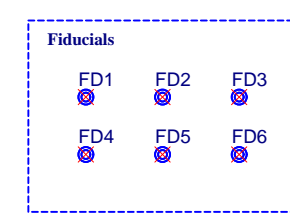
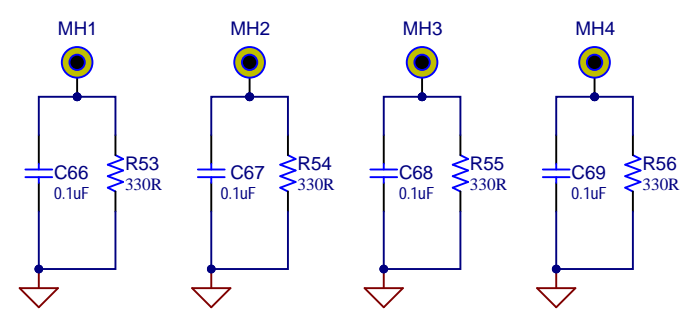
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| | | | |
|--|--|-------------------|----------------|
| Project Owner: Alexys Antell | | | |
| PCB Layout Contact: Lori Cantrell | | | |
| PartNumber: EV16R73A | Project Title VSC8574 EDS2 Daughter Card | Variant: Standard | |
| Sheet Title Ethernet Ports | | | |
| Size B | SCH #: 02-01031 | Rev: 2 | Date: 4/4/2025 |
| | PCB #: 04-12101 | Rev: 2 | Sheet 4 of 5 |
| File: 4_Ethernet Ports_ UNG10045_B0.SchDoc | | | |

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Mounting Holes in Corners



| | | | |
|--|---|-------------------|----------------|
| Project Owner: Alexys Antell | | | |
| PCB Layout Contact: Lori Cantrell | | | |
| PartNumber: EV16R73A | Project Title VSC8574 EDS2 Daughter Card | Variant: Standard | |
| Sheet Title SODIMM Edge Connector | | | |
| Size B | SCH #: 02-01031 | Rev: 2 | Date: 4/4/2025 |
| | PCB #: 04-12101 | Rev: 2 | Sheet 5 of 5 |
| File: 5_SODIMM Edge Connector_UNG10045_B0.SchDoc | | | |

