mXT112UD-MAUHA1 1.0

maXTouch 112-node Touchscreen Controller

Functional Safety

- UL/IEC 60730 Class B support
- Self diagnostics at power-on and as periodic tests during operation
- Heartbeat (alive) signal output to host
- Safety manual available

maXTouch® Adaptive Sensing Touchscreen Technology

- Up to 14 X (transmit) lines and 24 Y (receive) lines for use by a touchscreen (see Section 4.2.3 “Permitted Configurations”)
- A maximum of 112 nodes can be allocated to the touch sensor
- Touchscreen size of 4.47 inches (2:1 aspect ratio), assuming a sensor electrode pitch of 6.5 mm. Other sizes are possible with different electrode pitches and appropriate sensor material
- Multiple touch support with up to 10 concurrent touches tracked in real time

Touch Sensor Technology

- Discrete/out-cell support including glass and PET film-based sensors
- On-cell/touch-on display support including TFT, LCD (ITPS, IPS) and OLED
- Synchronization with display refresh timing capability
- Support for standard (for example, Diamond) and proprietary sensor patterns (review of designs by Microchip or a Microchip-qualified touch sensor module partner is recommended)

Front Panel Material and Design

- Works with PET or glass, including curved profiles (configuration and stack-up to be approved by Microchip or a Microchip-qualified touch sensor module partner)
- 10 mm glass (or 5 mm PMMA) with bare finger (dependent on screen size, touch size, configuration and stack-up)
- 6 mm glass (or 3 mm PMMA) with multi-finger 5 mm glove (2.7 mm PMMA equivalent) (dependent on screen size, touch size, configuration and stack-up)
- Support for non-rectangular sensor designs (for example, circular, rounded or with cutouts)

Touch Performance

- Moisture/Water Compensation
  - No false touch with condensation or water drop up to 22 mm diameter
  - One-finger tracking with condensation or water drop up to 22 mm diameter
- Mutual capacitance and self capacitance measurements supported for robust touch detection
- P2P mutual capacitance measurements supported for extra sensitive multi-touch sensing
- Noise suppression technology to combat ambient, charger, and power-line noise
  - Up to 240 V_{PP} between 1 Hz and 1 kHz sinusoidal waveform
  - Up to 20 V_{PP} between 1 kHz and 1 MHz sinusoidal waveform
- Burst Frequency
  - Controlled Tx burst frequency drift over process and temperature range
- Scan Speed
  - Typical report rate for 10 touches ≥70 Hz (subject to configuration)
  - Initial touch latency <18 ms for first touch from idle (subject to configuration)
  - Configurable to allow for power and speed optimization

Enhanced Algorithms

- Lens bending algorithms to remove display noise
- Touch suppression algorithms to remove unintentional large touches, such as palm
- Palm Recovery Algorithm for quick restoration to normal state

Power Saving

- Programmable timeout for automatic transition from Active to Idle state
- Pipelined analog sensing detection and digital processing to optimize system power efficiency

Application Interfaces

- I^2C interface with support for Standard mode (up to 100 kHz), Fast mode (up to 400 kHz), Fast-mode Plus (up to 1 MHz)
- Interrupt to indicate when a message is available
- Additional SPI Debug Interface to read the raw data for tuning and debugging purposes

Power Supply

- Digital (Vdd) 3.3V nominal
- Digital I/O (VddIO) 3.3V nominal
- Analog (AVdd) 3.3V nominal
- High voltage internal X line drive (XVdd) 6.6V with internal voltage pump (XVdd connected to AVdd if voltage pump not used)

Package

- 56-pin XQFN 6 × 6 × 0.4 mm, 0.35 mm pitch

Operating Temperature

- –40°C to +85°C

Design Services

- Review of device configuration, stack-up and sensor patterns
- Custom firmware versions can be considered
- Contact your Microchip representative for more information

PIN CONFIGURATION

Pin Configuration – 56-pin XQFN

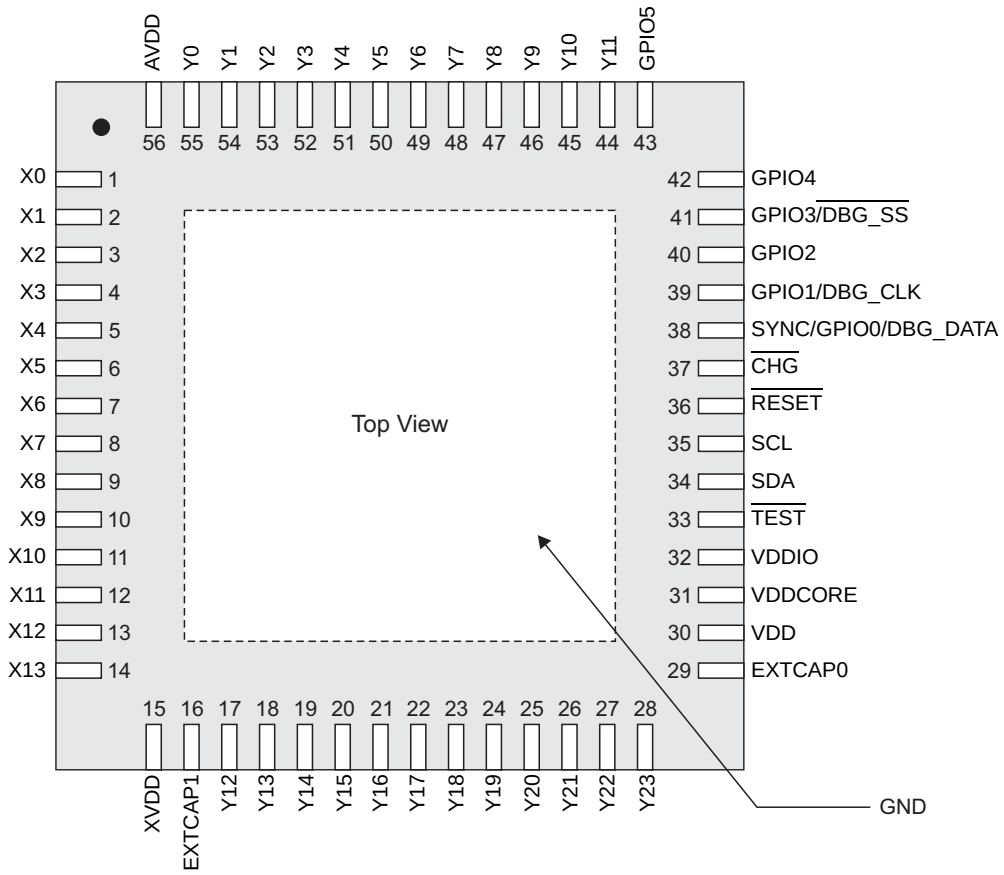

TABLE 1: PIN LISTING – 56-PIN XQFN

Pin	Name	Type	Supply	Description	If Unused...
1	X0	S	XVdd	X line connection	Leave open
2	X1	S	XVdd	X line connection	Leave open
3	X2	S	XVdd	X line connection	Leave open
4	X3	S	XVdd	X line connection	Leave open
5	X4	S	XVdd	X line connection	Leave open
6	X5	S	XVdd	X line connection	Leave open
7	X6	S	XVdd	X line connection	Leave open
8	X7	S	XVdd	X line connection	Leave open
9	X8	S	XVdd	X line connection	Leave open
10	X9	S	XVdd	X line connection	Leave open
11	X10	S	XVdd	X line connection	Leave open
12	X11	S	XVdd	X line connection	Leave open
13	X12	S	XVdd	X line connection	Leave open
14	X13	S	XVdd	X line connection	Leave open
15	XVDD	P	–	X line drive power	–
16	EXTCAP1	P	–	Voltage doubler – connect to EXTCAP0 via capacitor; see Section 2.2.6 “XVdd”	Leave open
17	Y12	S	AVdd	Y line connection	Leave open
18	Y13	S	AVdd	Y line connection	Leave open
19	Y14	S	AVdd	Y line connection	Leave open
20	Y15	S	AVdd	Y line connection	Leave open
21	Y16	S	AVdd	Y line connection	Leave open
22	Y17	S	AVdd	Y line connection	Leave open
23	Y18	S	AVdd	Y line connection	Leave open
24	Y19	S	AVdd	Y line connection	Leave open
25	Y20	S	AVdd	Y line connection	Leave open
26	Y21	S	AVdd	Y line connection	Leave open
27	Y22	S	AVdd	Y line connection	Leave open
28	Y23	S	AVdd	Y line connection	Leave open
29	EXTCAP0	P	–	Voltage doubler – connect to EXTCAP1 via capacitor; see Section 2.2.6 “XVdd”	Leave open
30	VDD	P	–	Digital power	–
31	VDDCORE	P	–	Digital core power	–
32	VDDIO	P	–	Digital IO interface power	–
33	$\overline{\text{TEST}}$	–	VddIO	Reserved for factory use; pull up to VddIO	–
34	SDA	OD	VddIO	I^2C Serial Data	–
35	SCL	OD	VddIO	I^2C Serial Clock	–
36	$\overline{\text{RESET}}$	I	VddIO	Reset low. Pull up to VddIO. Connection to host system is recommended	Pull up to VddIO
37	$\overline{\text{CHG}}$	OD	VddIO	State change interrupt. Pull up to VddIO Note: Briefly set (~100 ms) as an input after power-up/reset for diagnostic purposes	–

TABLE 1: PIN LISTING – 56-PIN XQFN (CONTINUED)

Pin	Name	Type	Supply	Description	If Unused...
38	SYNC	I	VddIO	External synchronization: frame synchronization (VSync) or pulse synchronization (HSync) (2) (3)	–
	GPIO0	I/O	VddIO	General purpose IO; see Section 2.2.10 “GPIO Pins” (1)	Connect to test point Input: Connect to GND Output: Leave open
	DBG_DATA	O		Debug Data	
39	GPIO1	I/O	VddIO	General purpose IO; see Section 2.2.10 “GPIO Pins” (1)	Connect to test point Input: Connect to GND Output: Leave open
	DBG_CLK	O		Debug Clock	
40	GPIO2	I/O	Vdd	General purpose IO; see Section 2.2.10 “GPIO Pins” (1)	Input: Connect to GND Output: Leave open
41	GPIO3	I/O	Vdd	General purpose IO; see Section 2.2.10 “GPIO Pins” (1)	Connect to test point Input: Connect to GND Output: Leave open
	$\overline{\text{DBG\_SS}}$	O		Debug SS line	
42	GPIO4	I/O	Vdd	General purpose IO; see Section 2.2.10 “GPIO Pins” (1)	Input: Connect to GND Output: Leave open
43	GPIO5	I/O	Vdd	General purpose IO; see Section 2.2.10 “GPIO Pins” (1)	Input: Connect to GND Output: Leave open
44	Y11	S	AVdd	Y line connection	Leave open
45	Y10	S	AVdd	Y line connection	Leave open
46	Y9	S	AVdd	Y line connection	Leave open
47	Y8	S	AVdd	Y line connection	Leave open
48	Y7	S	AVdd	Y line connection	Leave open
49	Y6	S	AVdd	Y line connection	Leave open
50	Y5	S	AVdd	Y line connection	Leave open
51	Y4	S	AVdd	Y line connection	Leave open
52	Y3	S	AVdd	Y line connection	Leave open
53	Y2	S	AVdd	Y line connection	Leave open
54	Y1	S	AVdd	Y line connection	Leave open
55	Y0	S	AVdd	Y line connection	Leave open
56	AVDD	P	–	Analog power	–
Pad	GND	P	–	Exposed pad must be connected to GND	–

Note 1: Use of the GPIO pins is not supported for functional safety purposes under UL/IEC 60730 Class B.
2: Use of the SYNC pin is not considered UL/IEC 60730 Class B compliant.
3: The SYNC line can be used for either pulse synchronization or frame synchronization, but not both.

Key:

I	Input only	O	Output only	I/O	Input or output
OD	Open drain output	P	Ground or power	S	Sense pin

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1.0 OVERVIEW OF MXT112UD-MAUHA1

The Microchip maXTouch family of touch controllers brings industry-leading capacitive touch performance to customer applications. The mXT112UD-MAUHA1 features the latest generation of Microchip adaptive sensing technology that utilizes a hybrid mutual and self capacitive sensing system in order to deliver unparalleled touch features and a robust user experience.

- **Functional Safety** – The device is designed with functional safety applications in mind (for example, for the home appliance market). Specifically, the device complies with the UL/IEC 60730 Class B safety specifications. See Section 6.7 “Functional Safety – UL/IEC 60730 Class B Compliance” for more information.
- **Patented capacitive sensing method** – The mXT112UD-MAUHA1 uses a unique charge-transfer acquisition engine to implement Microchip’s patented capacitive sensing method. Coupled with a state-of-the-art CPU, the entire touchscreen sensing solution can measure, classify and track a number of individual finger touches with a high degree of accuracy in the shortest response time.
- **Capacitive Touch Engine (CTE)** – The mXT112UD-MAUHA1 features an acquisition engine that uses an optimal measurement approach to ensure almost complete immunity from parasitic capacitance on the receiver input lines. The engine includes sufficient dynamic range to cope with anticipated touchscreen self and mutual capacitances, which allows great flexibility for use with the Microchip proprietary sensor pattern designs. One- and two-layer ITO sensors are possible using glass or PET substrates.
- **Touch detection** – The mXT112UD-MAUHA1 allows for both mutual and self capacitance measurements, with the self capacitance measurements being used to augment the mutual capacitance measurements to produce reliable touch information.

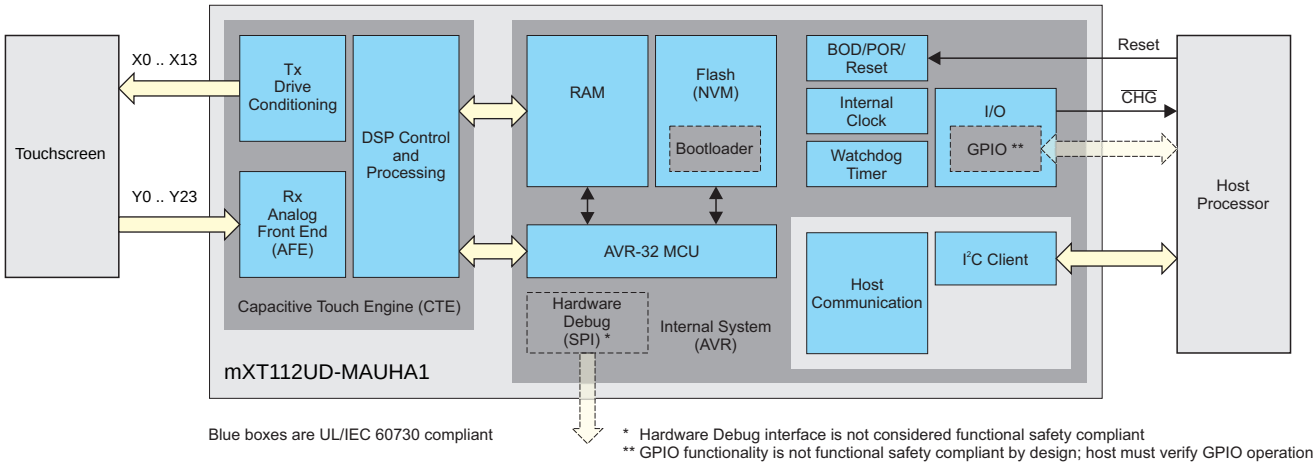
  When self capacitance measurements are enabled, touch classification is achieved using both mutual and self capacitance touch data. This has the advantage that both types of measurement systems can work together to detect touches under a wide variety of circumstances.

  The system may be configured for different types of default measurements in both idle and active modes. For example, the device may be configured for Mutual Capacitance Touch as the default in active mode and Self Capacitance Touch as the default in idle mode. Note that other types of scans (such as P2P mutual capacitance scans and other types of self capacitance scans) may also be made depending on configuration.

  Mutual capacitance touch data is used wherever possible to classify touches as this has a greater resolution than self capacitance measurements and provides positional information on touches. For this reason, multiple touches can only be determined by mutual capacitance touch data. In Self Capacitance Touch Default mode, if the self capacitance touch processing detects multiple touches, touchscreen processing is skipped until mutual capacitance touch data is available.

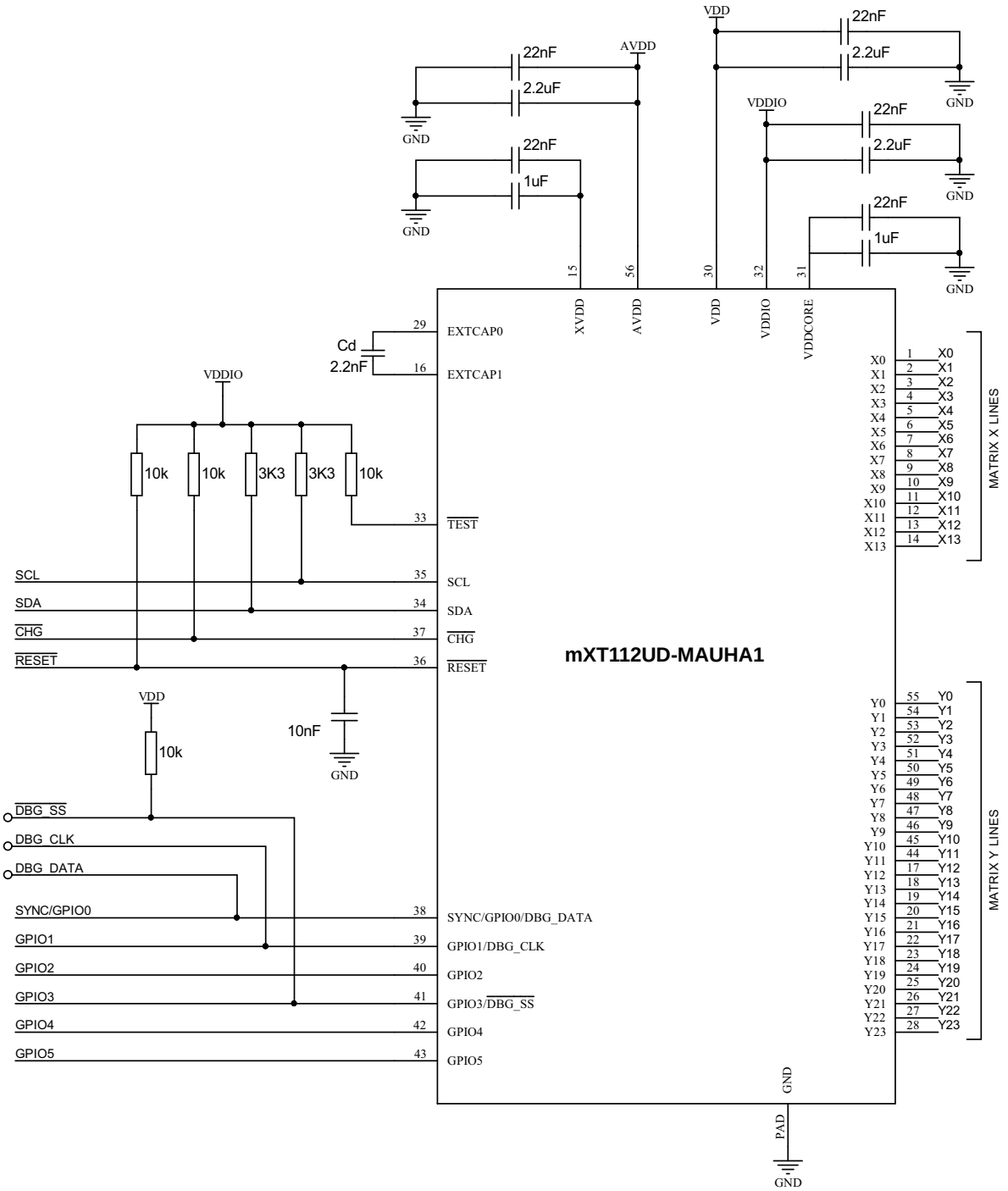
  Self capacitance and P2P mutual capacitance measurements allow for the detection of touches in extreme scenarios, such as thick glove touches, when mutual capacitance touch detection alone may miss touches.
- **Display Noise Cancellation** – A combination of analog circuitry, hardware noise processing, and firmware combats display noise without requiring additional listening channels or synchronization to display timing. This enables the use of shieldless touch sensor stacks, including touch-on-lens.
- **Noise filtering** – Hardware noise processing in the capacitive touch engine provides enhanced autonomous filtering and allows a broad range of noise profiles to be handled. The result is good performance in the presence of LCD noise.
- **Processing power** – The main CPU has two companion microsequencer coprocessors under its control consuming low power. This system allows the signal acquisition, preprocessing and postprocessing to be partitioned in an efficient and flexible way.
- **Interpreting user intention** – The Microchip hybrid mutual and self capacitance method provides unambiguous multitouch performance. Algorithms in the mXT112UD-MAUHA1 provide optimized touchscreen position filtering for the smooth tracking of touches, responding to a user's intended touches while preventing false touches triggered by ambient noise, conductive material on the sensor surface, such as moisture, or unintentional touches from the user’s resting palm or fingers.

FIGURE 1-1: SYSTEM ARCHITECTURE



2.0 SCHEMATIC

2.1 56-pin XQFN



Notes:

1. The schematic shown assumes that the voltage doubler is used. If low voltage operation is required, capacitor Cd must be omitted and XVDD connected directly to the AVdd supply (see Section 2.2.6 “XVdd”).
2. See “Pin configuration” for information on I/O pin supply
3. See Section 2.2 “Schematic Notes” for additional notes

2.2 Schematic Notes

2.2.1 NUMBER OF AVAILABLE NODES

Although 14 X lines and 24 Y lines are provided, only a maximum of 112 nodes on the matrix can be used for the touchscreen.

2.2.2 POWER SUPPLY

The sense and I/O pins are supplied by the power rails on the device as listed in Table 2-1. This information is also indicated in "Pin configuration".

TABLE 2-1: POWER SUPPLY FOR SENSE AND I/O PINS

Power Supply	Pins
XVdd	X sense pins
AVdd	Y sense pins
Vdd	GPIO2, GPIO3/$\overline{\text{DBG\_SS}}$, GPIO4, GPIO5
VddIO	$\overline{\text{RESET}}$, $\overline{\text{TEST}}$, $\overline{\text{CHG}}$ SCL, SDA, SYNC/GPIO0/DBG_DATA, GPIO1/DBG_CLK

2.2.3 DECOUPLING CAPACITORS

All decoupling capacitors must be X7R or X5R and placed less than 5 mm away from the pins for which they act as bypass capacitors. Pins of the same type can share a capacitor provided no pin is more than 10 mm from the capacitor.

The schematics on the previous pages show the capacitors required. The parallel combination of capacitors is recommended to give high and low frequency filtering, which is beneficial if the voltage regulators are likely to be some distance from the device (for example, If an active tail design is used). Note that this requires that the voltage regulator supplies for AVdd, Vdd and VddIO are clean and noise free. It also assumes that the track length between the capacitors and on-board power supplies is less than 50 mm.

The number of base capacitors can be reduced if the pinout configuration means that sharing a bypass capacitor is possible (subject to the distance between the pins satisfying the conditions above and there being no routing difficulties).

2.2.4 PULL-UP RESISTORS

The pull-up resistors shown in the schematic are suggested typical values and may be modified to meet the requirements of an individual customer design.

This applies, in particular, to the pull-up resistors on the I^2C SDA and SCL lines (shown on the schematic), as the values of these resistors depend on the speed of the I^2C interface. See Section 11.9 "I2C Specification" for details.

Note that if a VddIO supply at the low end of the allowable range is used, the I^2C pull-up resistor values may need to be reduced.

2.2.5 VDDCORE

VddCore is internally generated from the Vdd power supply. To guarantee stability of the internal voltage regulator, one or more external decoupling capacitors are required.

2.2.6 XVDD

XVdd power can be supplied either as high voltage (using an internal voltage pump) or as low voltage (connected directly to the AVdd supply). The operating mode should be chosen according to the final application.

The voltage pump requires one external capacitor:

- EXTCAP0 must be connected to EXTCAP1 via a capacitor (Cd).
- The capacitor on XVDD should be rated at least 10 V if the voltage doubler is used.

Capacitor Cd should provide a capacitance of 2.2 nF. The capacitor must be placed as close as possible to the EXTCAP*n* pins.

If low voltage XVdd is required (that is, the XVdd voltage doubler is not required):

- Capacitor Cd must be omitted and EXTCAP0 and EXTCAP1 left unconnected.
- XVDD must be connected directly to the AVdd supply.

CAUTION! The device may be permanently damaged if one of the XVDD supply pins is shorted to Ground or high current is drawn from it.

2.2.7 AVDD

A diode from AVDD to VDD is present in the device. If AVDD and VDD are driven from different supplies, the Vdd supply must be powered up earlier than AVdd.

2.2.8 MULTIPLE FUNCTION PINS

Some pins may have multiple functions. In this case, only one function can be chosen and the circuit should be designed accordingly.

2.2.9 SYNC PIN

The mXT112UD-MAUHA1 has a single SYNC pin that can be used for either frame synchronization (typically connected to VSYNC) or pulse synchronization (typically connected to HSYNC), but not both.

IMPORTANT! Use of the SYNC pin is not considered UL/IEC 60730 Class B compliant.

2.2.10 GPIO PINS

The mXT112UD-MAUHA1 has 6 GPIO pins. The pins can be set to be either an input or an output, as required, using the GPIO Configuration T19 object.

IMPORTANT! Use of the GPIO pins is not considered UL/IEC 60730 Class B compliant.

If a GPIO pin is unused, it can be left unconnected externally as long as it is given a defined state by the GPIO Configuration T19 object.

By default the GPIO pins are set to be inputs so if a pin is not used, and is left configured as an input, it should be connected to GND through a resistor. Alternatively, the internal pull-up resistor should be enabled (in the GPIO Configuration T19 object) to pull up the pin. Note that this does not apply if the GPIO pin is shared with a debug line; see Section 2.2.11 “SPI Debug Interface” for advice on how to treat an unused GPIO pin in this case.

Alternatively, the GPIO pin can be set as an output low using the GPIO Configuration T19 object and left open. This second option avoids any problems should the pin accidentally be configured as output high at a later date.

If the GPIO Configuration T19 object is not enabled for use, the GPIO pins cannot be used for GPIO purposes, although any alternative function can still be used.

Some GPIO pins have alternative functions. If an alternative function is used then this takes precedence over the GPIO function and the pin cannot be used as a GPIO pin. In particular:

- GPIO0 cannot be used if the SYNC function is in use.
- The SPI Debug Interface functionality is shared with some of the GPIO pins. See Section 2.2.11 “SPI Debug Interface” for more details on the SPI Debug Interface and how to handle these pins if they are totally unused.

2.2.11 SPI DEBUG INTERFACE

IMPORTANT! Use of the SPI Debug Interface is not considered UL/IEC 60730 Class B compliant.

The DBG_CLK, DBG_DATA and $\overline{\text{DBG\_SS}}$ lines form the SPI Debug Interface. These pins should be routed to test points on all designs, such that they can be connected to external hardware during system development and for debug purposes. See also Section 10.1 “SPI Debug Interface”.

The debug lines may share pins with other functionality. If the circuit is designed to use the SPI Debug Interface, then any alternative functionality cannot be used. Specifically:

- The DBG_CLK line shares functionality with GPIO1; therefore GPIO1 cannot be used if the SPI Debug Interface is in use.
- The DBG_DATA line shares functionality with GPIO0; therefore GPIO0 cannot be used if the SPI Debug Interface is in use.
- The $\overline{\text{DBG\_SS}}$ line shares functionality with GPIO3; therefore GPIO3 cannot be used if the $\overline{\text{DBG\_SS}}$ line is in use.
- The pull-up resistor for $\overline{\text{DBG\_SS}}$ in the schematics is optional and should be present only if the line is used as $\overline{\text{DBG\_SS}}$.

The DBG_CLK, DBG_DATA and $\overline{\text{DBG\_SS}}$ lines should not be connected to power or GND. For this reason, where these pins are shared with GPIO pins and they are totally unused (that is, they are not being used as debug or GPIO pins), they should be set as outputs using the GPIO Configuration T19 object.

3.0 TOUCHSCREEN BASICS

3.1 Sensor Construction

A touchscreen is usually constructed from a number of transparent electrodes. These are typically on a glass or plastic substrate. They can also be made using non-transparent electrodes, such as copper or carbon. Electrodes are constructed from Indium Tin Oxide (ITO) or metal mesh. Thicker electrodes yield lower levels of resistance (perhaps tens to hundreds of Ω/square) at the expense of reduced optical clarity. Lower levels of resistance are generally more compatible with capacitive sensing. Thinner electrodes lead to higher levels of resistance (perhaps hundreds of Ω/square) with some of the best optical characteristics.

Interconnecting tracks in ITO can cause problems. The excessive RC time constants formed between the resistance of the track and the capacitance of the electrode to ground can inhibit the capacitive sensing function. In such cases, the tracks should be replaced by screen printed conductive inks (non-transparent) outside the touchscreen viewing area.

3.2 Electrode Configuration

The specific electrode designs used in Microchip touchscreens are the subject of various patents and patent applications. Further information is available on request.

The device supports various configurations of electrodes as summarized in Section 4.0 “Sensor Layout”.

3.3 Scanning Sequence

All nodes are scanned in sequence by the device. Where possible, there is a parallelism in the scanning sequence to improve overall response time. The nodes are scanned by measuring capacitive changes at the intersections formed between the first drive (X) line and all the receive (Y) lines. Then the intersections between the next drive line and all the receive lines are scanned, and so on, until all X and Y combinations have been measured.

The device can be configured in various ways. It is possible to disable some nodes so that they are not scanned at all. This can be used to improve overall scanning time.

3.4 Touchscreen Sensitivity

3.4.1 ADJUSTMENT

Sensitivity of touchscreens can vary across the extents of the electrode pattern due to natural differences in the parasitic capacitance of the interconnections, control chip, and so on. An important factor in the uniformity of sensitivity is the electrode design itself. It is a natural consequence of a touchscreen pattern that the edges form a discontinuity and hence tend to have a different sensitivity. The electrodes at the edges do not have a neighboring electrode on one side and this affects the electric field distribution in that region.

A sensitivity adjustment is available for the whole touchscreen. This adjustment is a basic algorithmic threshold that defines when a node is considered to have enough signal change to qualify as being in detect.

3.4.2 MECHANICAL STACKUP

The mechanical stackup refers to the arrangement of material layers that exist above and below a touchscreen. The arrangement of the touchscreen in relation to other parts of the mechanical stackup has an effect on the overall sensitivity of the screen. The maXTouch technology has an excellent ability to operate in the presence of ground planes close to the sensor. The sensitivity of the maXTouch technology is attributed more to the interaction of the electric fields between the transmitting (X) and receiving (Y) electrodes than to the surface area of these electrodes. For this reason, stray capacitance on the X or Y electrodes does not strongly reduce sensitivity.

Front panel dielectric material has a direct bearing on sensitivity. Plastic front panels are usually suitable up to about 5 mm, and glass up to about 10 mm (dependent upon the screen size and layout). The thicker the front panel, the lower the signal-to-noise ratio of the measured capacitive changes and hence the lower the resolution of the touchscreen. In general, glass front panels are near optimal because they conduct electric fields almost twice as easily as plastic panels.

NOTE	Care should be taken using ultra-thin glass panels as retransmission effects can occur, which can significantly degrade performance.

4.0 SENSOR LAYOUT

NOTE	The specific electrode designs used in Microchip touchscreens may be the subject of various patents and patent applications. Further information is available on request.

4.1 Electrodes

The device supports various configurations of touch electrodes as summarized below:

- Touchscreen: 1 touchscreen panel occupies a rectangular matrix of up to 14 X × 24 Y lines (subject to other configurations).

NOTE	Although there is a total of 38 lines, arranged as a matrix of 14 X by 24 Y, only a maximum of 112 nodes can be used for all the touch objects on this device. The matrix can be made up of any combination of X and Y lines in the design (subject to the limitations described below), provided the X and Y lines are contiguous and subject to the maximum of 112 nodes. For example the matrix could be constructed as a matrix of 14 X by 8 Y lines (giving 112 nodes), as a matrix of 4 X by 24 Y (giving 96 nodes) or as a matrix of any other combination in between. The arrangement chosen depends on the application.

4.2 Sensor Matrix Layout

When designing the physical layout of the touch panel, the following rules must be obeyed:

4.2.1 GENERAL LAYOUT RULES

- The Multiple Touch Touchscreen T100 object should be a regular rectangular shape in terms of the lines it uses.

4.2.2 ADDITIONAL LAYOUT RULES FOR MULTIPLE TOUCH TOUCHSCREEN T100

- The Multiple Touch Touchscreen T100 object ***must*** start at (X0, Y0).
- For mutual capacitance measurements (see Table 4-1):
  - The touchscreen must contain a minimum of 3 X lines. If Dual X Drive is enabled for use in the Noise Suppression T72 object, the minimum is 4 X lines.
  - The touchscreen must contain a minimum of 3 Y lines.
  - If P2P mutual capacitance measurements are required, the number of Y lines must be one of 24, 23, 20, 19, 16, 15, 12, 11, 8 or 7.
- For self capacitance measurements (see Table 4-1):
  - The touchscreen must contain a minimum of 6 X lines.
  - The number of Y lines must be one of 24, 23, 20, 19, 16, 15, 12, 11, 8 or 7.

4.2.3 PERMITTED CONFIGURATIONS

The permitted X/Y configurations are shown in Table 4-1.

TABLE 4-1: PERMITTED TOUCHSCREEN CONFIGURATIONS

Number of X Lines \ Number of Y Lines	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
14																	Y	Y	M	M	M	M		
13																M	Y	Y	M	M	M	M		
12																M	Y	Y	M	M	M	M		
11															M	M	Y	Y	M	M	M	M		
10														Y	M	M	Y	Y	M	M	M	M		
9													Y	Y	M	M	Y	Y	M	M	M	M		
8											M*	M	Y	Y	M	M	Y	Y	M	M	M	M		
7									Y*	Y	M	M	Y	Y	M	M	Y	Y	M	M	M	M		
6							M	M	Y	Y	M	M	Y	Y	M	M	Y	Y	M	M	M	M		
5			M	M	P	P	M	M	P	P	M	M	P	P	M	M	P	P	M	M	M	M		
4	P	P	M	M	P	P	M	M	P	P	M	M	P	P	M	M	P	P	M	M	M	M		
3	X	X	Z	Z	X	X	Z	Z	X	X	Z	Z	X	X	Z	Z	X	X	Z	Z	Z	Z		
2																								
1																								

Key:

- Y — Configuration supported for self capacitance and all mutual capacitance measurements; configuration recommended (Y* = optimum 112 nodes)
- P — Configuration supported for all mutual capacitance measurement types; self capacitance measurements not supported
- M — Configuration supported for non P2P mutual capacitance measurements only; self capacitance measurements not supported (M* = optimum 112 nodes)
- X — Configuration supported for all mutual capacitance measurements types, but only if dual X is *not* used; self capacitance measurements not supported
- Z — Configuration supported for non P2P mutual capacitance measurements, but only if dual X is *not* used; self capacitance measurements not supported
- Configuration not supported

4.3 Screen Size

Table 4-2 lists some typical screen size and electrode pitch combinations to achieve various aspect ratios.

TABLE 4-2: TYPICAL SCREEN SIZES

Aspect Ratio	Matrix Size	Node Count	Screen Diagonal (Inches)		
			4.5 mm Pitch	5.5 mm Pitch	6.5 mm Pitch
3:2	X = 8, Y = 12	96	2.56	3.12	3.69
3:1	X = 6, Y = 18	108	3.36	4.11	4.86
2:1	X = 7, Y = 16	112	3.09	3.78	4.47

Note 1: The figures given in the table are for a Touchscreen and show the largest node count possible to achieve the desired aspect ratio.

5.0 POWER-UP / RESET REQUIREMENTS

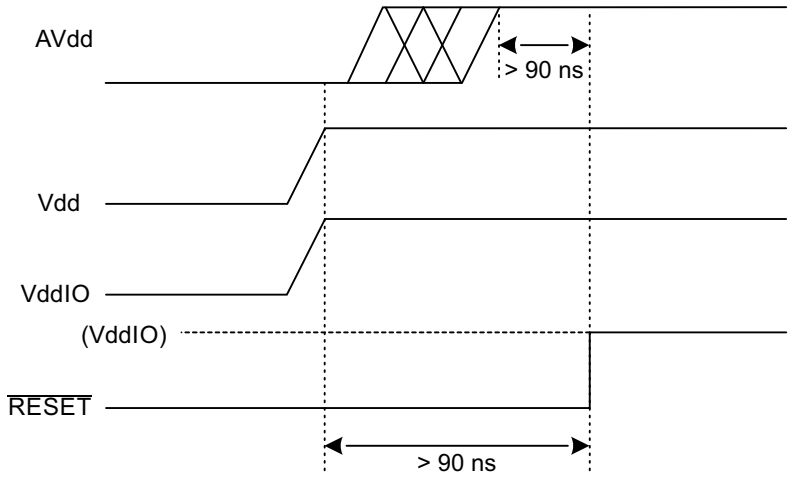
5.1 Power-on Reset

There is an internal Power-on Reset (POR) in the device.

If an external reset is to be used the device must be held in $\overline{\text{RESET}}$ (active low) while the digital (Vdd), analog (AVdd) and digital I/O (VddIO) power supplies are powering up. The supplies must have reached their nominal values before the $\overline{\text{RESET}}$ signal is deasserted (that is, goes high). This is shown in Figure 5-1. See Section 11.2 “Recommended Operating Conditions” for nominal values for the power supplies to the device.

A diode from AVDD to VDD is present in the device. If AVDD and VDD are driven from different supplies, the Vdd supply must be powered up earlier than AVdd.

FIGURE 5-1: POWER SEQUENCING ON THE MXT112UD-MAUHA1



Note: When using external $\overline{\text{RESET}}$ at power-up,
VddIO must not be enabled after Vdd

It is recommended that customer designs include the capability for the host to control all the maXTouch power supplies and pull the $\overline{\text{RESET}}$ line low.

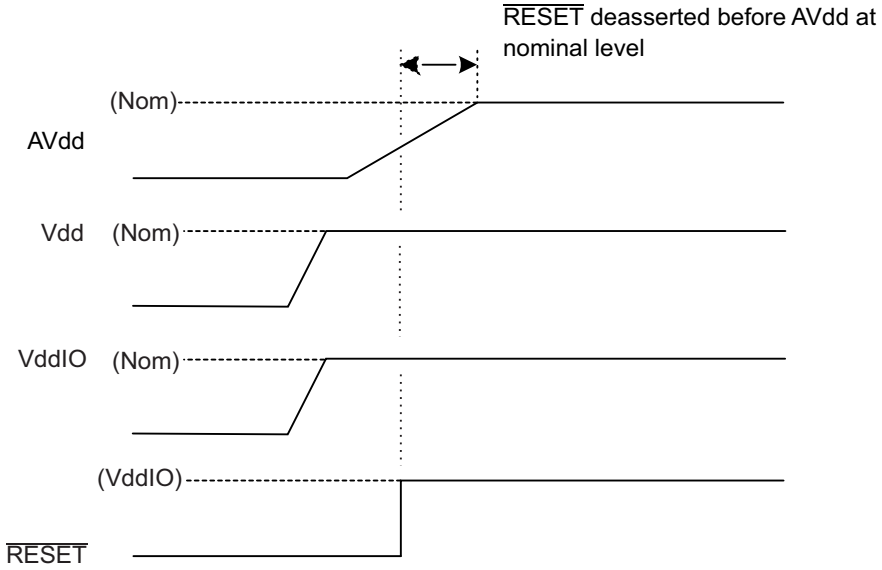
After power-up, the device typically takes 122 ms to 362 ms before it is ready to start communications, depending on the configuration.

NOTE	Device initialization will not complete until after all the power supplies are present. If any power supply is not present, internal initialization stalls and the device will not communicate with the host.

If the $\overline{\text{RESET}}$ line is released before the AVdd supply has reached its nominal voltage (see Figure 5-2), then some additional operations need to be carried out by the host. There are two options open to the host controller:

- Start the part in Deep Sleep mode and then send the command sequence to set the cycle time to wake the part and allow it to run normally. Note that in this case a calibration command is also needed.
- Send a RESET command.

FIGURE 5-2: POWER SEQUENCING ON THE MXT112UD-MAUHA1 – LATE RISE ON AVDD



The RESET pin can be used to reset the device whenever necessary. The RESET pin must be asserted low for at least 90 ns to cause a reset. After the host has released the RESET pin, the device typically takes 122 ms to 362 ms before it is ready to start communications, depending on the configuration. It is recommended to connect the RESET pin to a host controller to allow the host to initiate a full hardware reset without requiring the mXT112UD-MAUHA1 to be powered down.

WARNING	The device should be reset only by using the RESET line. If an attempt is made to reset by removing the power from the device without also sending the signal lines low, power will be drawn from the communication and I/O lines and the device will not reset correctly.

Make sure that any lines connected to the device are below or equal to Vdd during power-up and power-down. For example, if RESET is supplied from a different power domain to the VDDIO pin, make sure that it is held low when Vdd is off. If this is not done, the RESET signal could parasitically couple power via the RESET pin into the Vdd supply.

NOTE	The voltage level on the RESET pin of the device must never exceed VddIO (digital supply voltage).

A software RESET command (using the Command Processor T6 object) can be used to reset the chip. A software reset typically takes 362 ms before the device is ready to start communications. After the chip has finished it asserts the CHG line to signal to the host that a message is available. The reset flag is set in the Command Processor T6 object message data to indicate to the host that it has just completed a reset cycle. This bit can be used by the host to detect any unexpected brownout events. This allows the host to take any necessary corrective actions, such as reconfiguration.

NOTE	The CHG line is briefly set (~100 ms) as an input during power-up or reset. It is therefore particularly important that the line should be allowed to float high via the CHG line pull-up resistor during this period. It should never be driven by the host (see Section 11.5.4 “Reset Timings”).

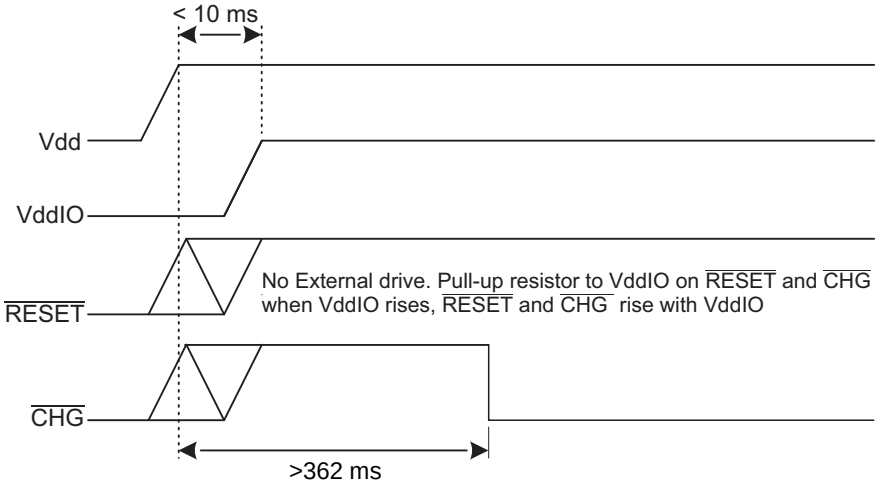
At power-on, the device can be configured to perform self tests (using the Self Test Control T10 object) to check for faults in the device.

5.2 Power-up and Reset Sequence – VddIO Enabled after Vdd

The power-up sequence that can be used in applications where VddIO must be powered up after Vdd, is shown in Figure 5-3.

In this case the communication interface to the maXTouch device is not driven by the host system. The RESET and CHG pins are connected to VddIO using suitable pull-up resistors. Vdd is powered up, followed by VddIO, no more than 10 ms after Vdd. Due to the pull-up resistors, RESET and CHG will rise with VddIO. The internal POR system ensures reliable boot up of the device and the CHG line will go low approximately 122 ms to 362 ms (depending on the configuration) after Vdd to notify the host that the device is ready to start communication.

FIGURE 5-3: POWER-UP SEQUENCE



6.0 DETAILED OPERATION

6.1 Touch Detection

The mXT112UD-MAUHA1 allows for both mutual and self capacitance measurements, with the self capacitance measurements being used to augment the mutual capacitance measurements to produce reliable touch information.

When self capacitance measurements are enabled, touch classification is achieved using both mutual and self capacitance touch data. This has the advantage that both types of measurement systems can work together to detect touches under a wide variety of circumstances.

Mutual capacitance touch data is used wherever possible to classify touches as this has greater granularity than self capacitance measurements and provides positional information on touches.

Self capacitance measurements, on the other hand, allow for the detection of single touches in extreme cases, such as single thick glove touches, when touches can only be detected by self capacitance data and may be missed by mutual capacitance touch detection.

6.2 Operational Modes

The device operates in two modes: **Active** (touch detected) and **Idle** (no touches detected). Both modes operate as a series of burst cycles. Each cycle consists of a short burst (during which measurements are taken) followed by an inactive sleep period. The difference between these modes is the length of the cycles. Those in idle mode typically have longer sleep periods. The cycle length is configured using the IDLEACQINT and ACTVACQINT settings in the Power Configuration T7. In addition, an *Active to Idle Timeout* setting is provided.

6.3 Detection Integrator

The device features a touch detection integration mechanism. This acts to confirm a detection in a robust fashion. A counter is incremented each time a touch has exceeded its threshold and has remained above the threshold for the current acquisition. When this counter reaches a preset limit the sensor is finally declared to be touched. If, on any acquisition, the signal is not seen to exceed the threshold level, the counter is cleared and the process has to start from the beginning.

The detection integrator is configured using the appropriate touch objects (Multiple Touch Touchscreen T100).

6.4 Sensor Acquisition

The charge time for mutual capacitance measurements is set using the Acquisition Configuration T8 object. The device combines a number of factors together to arrive at the total acquisition time for one drive line (that is, one X line for mutual capacitance acquisitions or one axis for self capacitance acquisitions).

The following constraints apply on the mXT112UD-MAUHA1:

- The per X line mutual capacitance touch measurement and the per axis self capacitance measurement must not exceed 2 ms. If either of these are exceeded, a SIGERR will be reported.
- The high and low pulse periods must not exceed 51.26 µs each. This means that the maximum possible burst period is 102.46 µs (that is, a minimum frequency of 9.76 kHz). In addition, the burst period must not be less than 4 µs (that is, a maximum frequency of 250 kHz).

Unpredictable system behavior might occur if any of the above constraints are not met.

Care should be taken to configure all the objects that can affect the measurement timing so that these limits are not exceeded.

6.5 Calibration

Calibration is the process by which a sensor chip assesses the background capacitance on each node. Calibration occurs in a variety of circumstances, for example:

- When determined by the mutual capacitance recalibration process, as controlled by the Acquisition Configuration T8 object
- When determined by the self capacitance recalibration process, as controlled by the Self Capacitance Configuration T111 object
- When the Retransmission Compensation T80 object detects calibrated-in moisture has been removed

- Following a Self Capacitance Global Configuration T109 Tune command
- When the host issues a recalibrate command
- When certain configuration settings are changed

6.6 Digital Filtering and Noise Suppression

The mXT112UD-MAUHA1 supports on-chip filtering of the acquisition data received from the sensor. Specifically, the Noise Suppression T72 object provides an algorithm to suppress the effects of noise (for example, from a noisy charger plugged into the user's product). This algorithm can automatically adjust some of the acquisition parameters on-the-fly to filter the Analog-to-Digital Conversions (ADCs) received from the sensor.

Additional noise suppression is provided by the Self Capacitance Noise Suppression T108 object. Similar in both design and configuration to the Noise Suppression T72 object, the Self Capacitance Noise Suppression T108 object is the noise suppression interface for self capacitance touch measurements.

Noise suppression is triggered when a noise source is detected.

- The host driver code can indicate when a noise source is present.
- The noise suppression is also triggered based on the noise levels detected using internal line measurements.The Noise Suppression T72 and Self Capacitance Noise Suppression T108 object selects the appropriate controls to suppress the noise present in the system.

6.7 Functional Safety – UL/IEC 60730 Class B Compliance

- The device is designed with functional safety applications in mind (for example, for the home appliance market). Specifically, the device complies with the UL/IEC 60730 Class B safety specification:
  - User-configurable self diagnostics to detect internal system errors (for example, CPU, memory and system clocks), power, pin fault errors and signal errors for immediate action by the host system (see Table 6-1). These tests can be configured to run at power-on/reset and/or as periodic testing during operation.
  - Other built-in automatic system-level tests (for example interrupts, CTE and peripheral I/O)
  - Heartbeat (alive) signal output to host
  - Enhanced communications that includes sequence numbers (timing) and CRC error checking

The following document gives detailed guidance on achieving UL/IEC 60730 Class B compliance:

- *mXT336UD-MAUHA1 1.0 Family UL/IEC 60730 Class B Compliance Guide*

TABLE 6-1: SELF TESTS

	Run as…			
Self Test Group	**Pre-Operation Self Test (POST)**	**Built-In Self Test (BIST)**	**On Demand Test**	
CPU	Automatically tested at start-up	Yes	–	Internal System
Internal Interrupts	Yes	Yes	–	
Clock	Yes	Yes	–	
Flash Memory	Yes	Yes	–	
RAM	Yes	Yes	–	
Power	Yes	Yes	Yes	
CTE (Capacitive Touch Engine)	Yes	Yes	–	CTE and Touch System
Pin Faults	Yes	Yes	Yes	
Signal Limits	Yes	Yes	Yes	

6.8 EMC Reduction

The mXT112UD-MAUHA1 has the following mechanisms to help reduce EMC emissions and ensure that the user's product operates within the desired EMC limits:

- **Configurable Voltage Reference Mode** – Allows for the selection of voltage swing of the self capacitance measurements.This feature is configured by the Self Capacitance Global Configuration T109 object.
- **Input Buffer Power Configuration** – Controls the positive/negative drive strength of the Input Buffer for self capacitance measurements. This feature is configured by the Self Capacitance Global Configuration T109 object.

- **Configurable Input Amplifier Bias** – Controls the Input Amplifier Bias. This feature is configured by the Self Capacitance Global Configuration T109 object.

6.9 Shieldless Support and Display Noise Suppression

The mXT112UD-MAUHA1 can support shieldless sensor design even with a noisy LCD.

The Optimal Integration feature is not filtering as such, but enables the user to use a shorter integration window. The integration window optimizes the amount of charge collected against the amount of noise collected, to ensure an optimal SNR. This feature also benefits the system in the presence of an external noise source. This feature is configured using the Shieldless T56 object.

Display noise suppression allows the device to overcome display noise simultaneously with external noise. This feature is based on filtering provided by the Lens Bending T65 object (see Section 6.11 “Lens Bending”).

6.10 Retransmission Compensation

The device can limit the undesirable effects on the mutual capacitance touch signals caused by poor device coupling to ground, such as poor sensitivity and touch break-up. This is achieved using the Retransmission Compensation T80 object. This object can be configured to allow the touchscreen to compensate for signal degradation due to these undesirable effects. If self capacitance measurements are also scheduled, the Retransmission Compensation T80 object will use the resultant data to enhance the compensation process.

The Retransmission Compensation T80 object is also capable of compensating for water presence on the sensor if self capacitance measurements are scheduled. In this case, both mutual capacitance and self capacitance measurements are used to detect moisture and then, once moisture is detected, self capacitance measurements are used to detect single touches in the presence of moisture.

6.11 Lens Bending

The device supports algorithms to eliminate disturbances from the measured signal.

When the sensor suffers from the screen deformation (lens bending) the signal values acquired by normal procedure are corrupted by the disturbance component (bend). The amount of bend depends on:

- The mechanical and electrical characteristics of the sensor
- The amount and location of the force applied by the user touch to the sensor

The Lens Bending T65 object measures the bend component and compensates for any distortion caused by the bend. As the bend component is primarily influenced by the user touch force, it can be used as a secondary source to identify the presence of a touch. The additional benefit of the Lens Bending T65 object is that it will eliminate LCD noise as well.

6.12 Glove Detection

The device has glove detection algorithms that process the measurement data received from the touchscreen classifying touches as potential gloved touches.

The Glove Detection T78 object is used to detect glove touches. In Normal Mode the Glove Detection T78 object applies vigorous glove classification to small signal touches to minimize the effect of unintentional hovering finger reporting. Once a gloved touch is found, the Glove Detection T78 object enters Glove Confidence Mode. In this mode the device expects the user to be wearing gloves so the classification process is much less stringent.

6.13 Unintentional Touch Suppression

The Touch Suppression T42 object provides a mechanism to suppress false detections from unintentional touches from a large body area, such as from a face, ear or palm. The Touch Suppression T42 object also provides Maximum Touch Suppression to suppress all touches if more than a specified number of touches has been detected.

7.0 I²C COMMUNICATIONS

Communication with the device is carried out over the I²C interface.

The I²C interface is used in conjunction with the $\overline{\text{CHG}}$ line. The $\overline{\text{CHG}}$ line going active signifies that a new data packet is available. This provides an interrupt-style interface and allows the device to present data packets when internal changes have occurred. See Section 7.4 “CHG line” for more information.

7.1 I²C Address

The device supports one I²C device address – 0x4A.

The I²C address is shifted left to form the SLA+W or SLA+R address when transmitted over the I²C interface, as shown in Table 7-1.

TABLE 7-1: FORMAT OF SLA+W/SLA+R

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address: 0x4A							Read/write

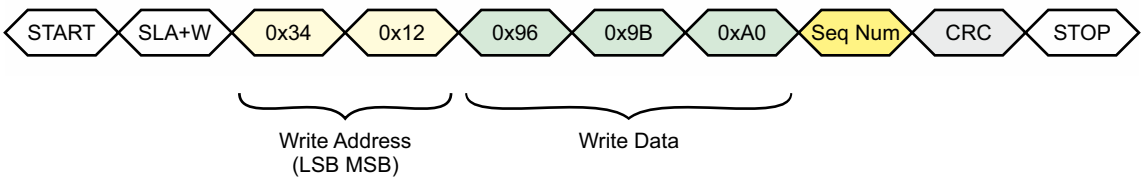
7.2 Writing To the Device

An I²C WRITE cycle consists of the following bytes:

START	1 bit	I²C START condition
SLA+W	1 byte	I²C address of the device (see Section 7.1 “I2C Address”)
Address (LSByte, MSByte)	2 bytes	Address of the location at which the data writing starts. This address is stored as the address pointer.
Data	0 .. 11 bytes	The actual data to be written. The data is written to the device, starting at the location of the address pointer. The address pointer returns to its starting value when the I²C STOP condition is detected. Note that a maximum of 11 bytes of data can be written in any one transaction.
Sequence number	1 byte	The sequence number for this write. The sequence number must start at 0 for the first write after power-up/reset and incremented by 1 for each subsequent write. When the sequence number reaches 255, it is reset to 0.
CRC	1 byte	An 8-bit CRC that includes all the bytes that have been sent, including the two address bytes, but not the SLA+W byte. If the device detects an error in the CRC during a write transfer, a COMSERR fault is reported by the Command Processor T6 object.
STOP	1 bit	I²C STOP condition

Figure 7-1 shows an example of writing three bytes of data to contiguous addresses starting at 0x1234.

FIGURE 7-1: EXAMPLE OF A THREE-BYTE WRITE STARTING AT ADDRESS 0x1234



7.3 Reading From the Device

Two I²C bus activities must take place to read from the device. The first activity is an I²C write to set the address pointer (LSByte then MSByte). The second activity is the actual I²C read to receive the data. The address pointer returns to its starting value when the read cycle NACK or STOP is detected.

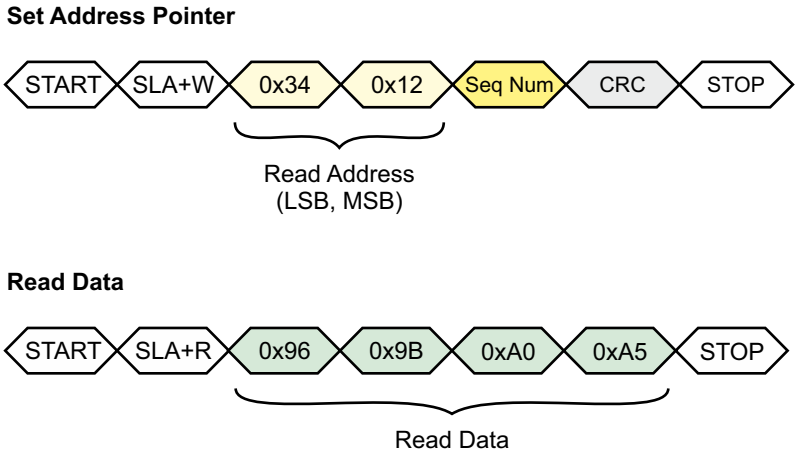
It is not necessary to set the address pointer before every read. The address pointer is updated automatically after every read operation. The address pointer will be correct if the reads occur in order. In particular, when reading multiple messages from the Message Processor T5 object, the address pointer is automatically reset to the address of the Message Processor T5 object, in order to allow continuous reads (see Section 7.3.3 “Reading Status Messages with DMA”).

The WRITE and READ cycles consist of a START condition followed by the I^2C address of the device (SLA+W or SLA+R respectively).

NOTE	Note that only certain read operations include a CRC of the data packets (see Section 7.3.1 “checksums for Read Transactions”).

Figure 7-2 shows the I^2C commands to read four bytes starting at address 0x1234.

FIGURE 7-2: EXAMPLE OF A FOUR-BYTE READ STARTING AT ADDRESS 0x1234



NOTE	At least one data byte must be read during an I^2C READ transaction; it is illegal to abort the transaction with an I^2C STOP condition without reading any data.

7.3.1 CHECKSUMS FOR READ TRANSACTIONS

The following memory locations include a CRC within their data when it is read, so read operations from these memory locations are UL/IEC 60730 Class B compliant:

- Reading status messages from the Message Processor T5 object – All messages include an 8-bit CRC (see Section 7.3.2 “Reading a Message from the Message Processor T5 Object”)
- Reading the Message Count T144 object during DMA access
- Reading the Information Block – The Information Block contains a 24-bit CRC

All other reads do not include a CRC as part of the packet, so it is the host’s responsibility to provide alternative means of validating any read data to make it UL/IEC 60730 Class B compliant. For example, any user data stored in the User Data T38 may need to include its own checksum.

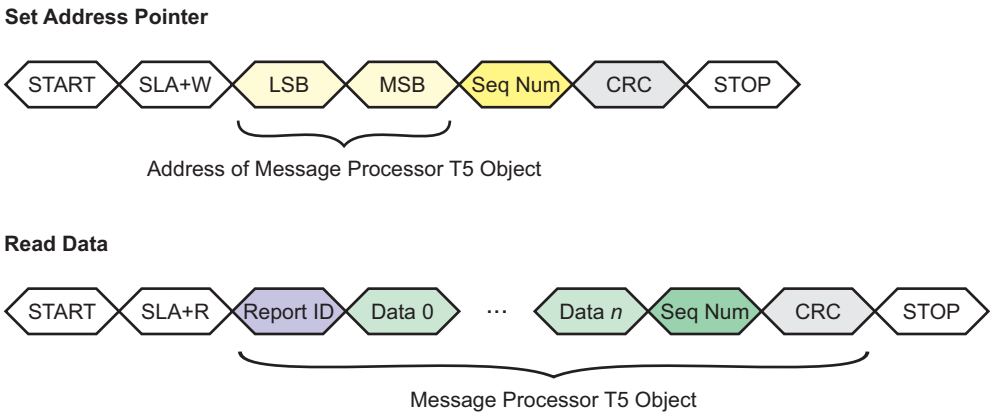
7.3.2 READING A MESSAGE FROM THE MESSAGE PROCESSOR T5 OBJECT

An I^2C read of the Message Processor T5 object contains the following bytes:

START	1 bit	I^2C START condition
SLA+R	1 byte	I^2C address of the device (see Section 7.1 “I2C Address”)
Report ID	1 byte	Message report ID
Data	1 or more bytes	The message data (size = size of Message Processor T5 MESSAGE field)
Sequence number	1 byte	The Message Processor T5 sequence number for this read. The sequence number starts at 0 for the first write after power-up/reset and is incremented by 1 for each subsequent read, wrapping round when it reaches 255.
CRC	1 byte	An 8-bit CRC for the Message Processor T5 report ID, message data and sequence number
STOP	1 bit	I^2C STOP condition

Figure 7-3 shows an example read from the Message Processor T5 object. To read multiple messages using Direct Memory Access, see Section 7.3.3 “Reading Status Messages with DMA”.

FIGURE 7-3: EXAMPLE READ FROM MESSAGE PROCESSOR T5



7.3.3 READING STATUS MESSAGES WITH DMA

The device facilitates the easy reading of multiple messages using a single continuous read operation. This allows the host hardware to use a Direct Memory Access (DMA) controller for the fast reading of messages, as follows:

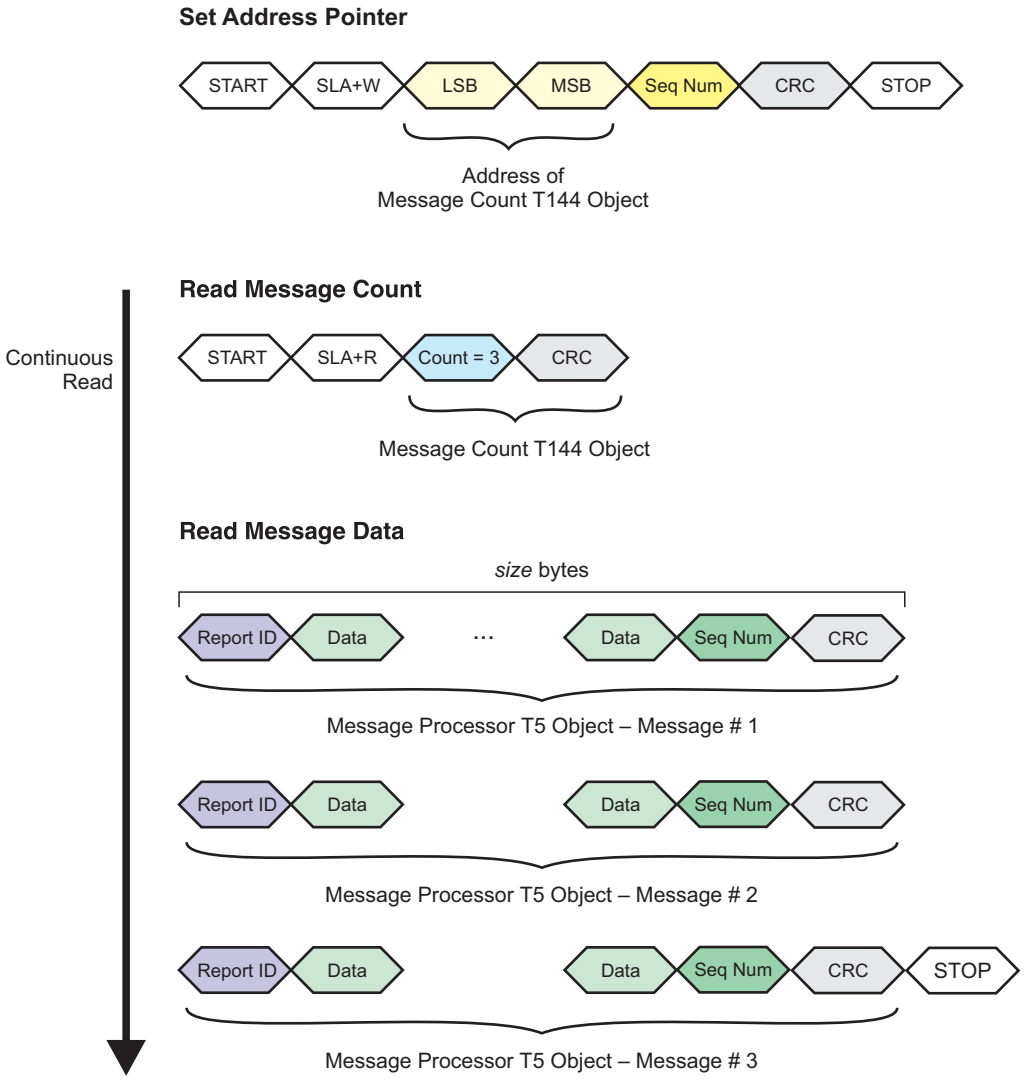
1. The host uses a write operation to set the address pointer to the start of the Message Count T144 object, if necessary. Note that the STOP condition at the end of the read resets the address pointer to its initial location, so it may already be pointing at the Message Count T144 object following a previous message read.
2. The host starts the read operation of the message by sending a START condition.
3. The host reads the Message Count T144 object (two bytes) to retrieve a count of the pending messages, plus the 8-bit CRC.

4. The host calculates the number of bytes to read by multiplying the message count by the size of the Message Processor T5 object. Note that the host should have already read the size of the Message Processor T5 object in its initialization code.

   Note that the size of the Message Processor T5 object as recorded in the Object Table includes the sequence number and checksum bytes.
5. The host reads the calculated number of message bytes. It is important that the host does *not* send a STOP condition during the message reads, as this will terminate the continuous read operation and reset the address pointer. No START and STOP conditions must be sent between the messages.
6. The host sends a STOP condition at the end of the read operation after the last message has been read. The NACK condition immediately before the STOP condition resets the address pointer to the start of the Message Count T144 object.

Figure 7-4 shows an example of using a continuous read operation to read three messages from the device.

FIGURE 7-4: CONTINUOUS READ EXAMPLE



7.4 $\overline{\text{CHG}}$ line

The $\overline{\text{CHG}}$ line is an active-low, open-drain output that is used to alert the host that a new message is available in the Message Processor T5 object. This provides the host with an interrupt-style interface with the potential for fast response times. It reduces the need for wasteful I^2C communications.

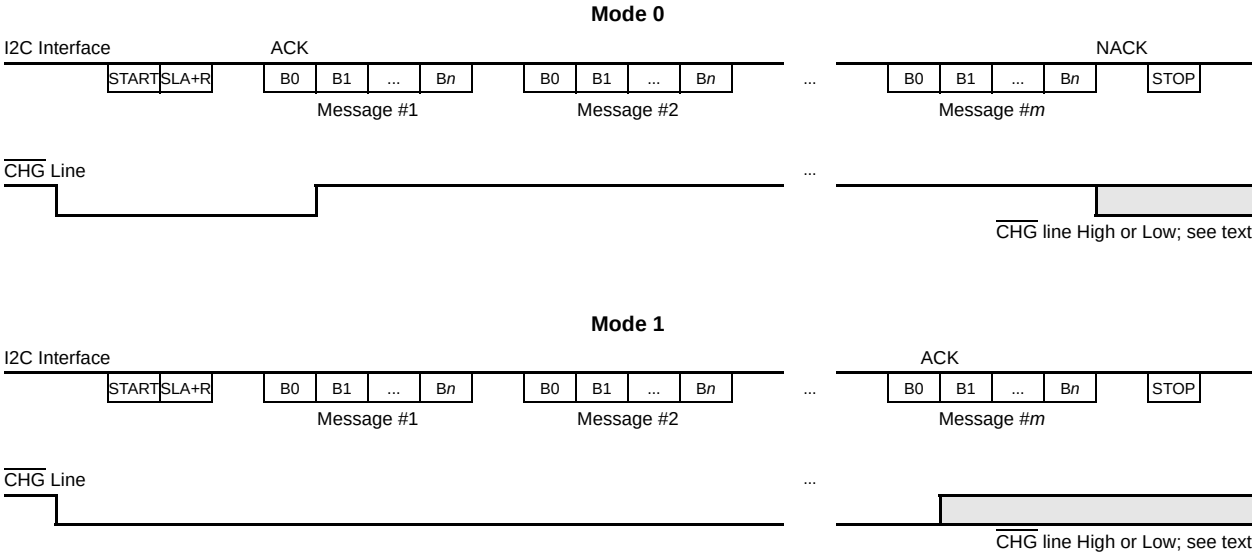
NOTE	The host should always use the $\overline{CHG}$ line as an indication that a message is ready to be read from the Message Processor T5 object; the host should never poll the device for messages.

The $\overline{CHG}$ line should always be configured as an input on the host during normal usage. This is particularly important after power-up or reset (see Section 5.0 “Power-up / Reset Requirements”).

A pull-up resistor is required to VddIO (see Section 2.0 “Schematic”).

The $\overline{CHG}$ line operates in two modes when it is used with I^2C communications, as defined by the Communications Configuration T18 object.

FIGURE 7-5: $\overline{CHG}$ LINE MODES FOR I^2C-COMPATIBLE TRANSFERS



In Mode 0 (edge-triggered operation):

1. The $\overline{CHG}$ line goes low to indicate that a message is present.
2. The $\overline{CHG}$ line goes high when the first byte of the first message (that is, its report ID) has been sent and acknowledged (ACK sent) and the next byte has been prepared in the buffer.
3. The STOP condition at the end of an I^2C transfer causes the $\overline{CHG}$ line to stay high if there are no more messages. Otherwise the $\overline{CHG}$ line goes low to indicate a further message.

Note that Mode 0 also allows the host to continually read messages by simply continuing to read bytes back without issuing a STOP condition. Message reading should end when a report ID of 255 (“invalid message”) is received. Alternatively the host ends the transfer by sending a NACK after receiving the last byte of a message, followed by a STOP condition. If there is another message present, the $\overline{CHG}$ line goes low again, as in step 1. In this mode the state of the $\overline{CHG}$ line does not need to be checked during the I^2C read.

NOTE	If function safety implementation is required (that is, the user’s product is to comply with UL/IEC 60730 Class B), a report ID of 255 is assumed to be an error. A report ID of 255, therefore, should not be used as an indication of the end of message reading.

In Mode 1 (level-triggered operation):

1. The $\overline{CHG}$ line goes low to indicate that a message is present.
2. The $\overline{CHG}$ line remains low while there are further messages to be sent after the current message.
3. The $\overline{CHG}$ line goes high again only once the first byte of the last message (that is, its report ID) has been sent and acknowledged (ACK sent) and the next byte has been prepared in the output buffer.

Mode 1 allows the host to continually read the messages until the $\overline{CHG}$ line goes high, and the state of the $\overline{CHG}$ line determines whether or not the host should continue receiving messages from the device.

NOTE	The state of the $\overline{CHG}$ line should be checked only between messages and not between the bytes of a message. The precise point at which the $\overline{CHG}$ line changes state cannot be predicted and so the state of the $\overline{CHG}$ line cannot be guaranteed between bytes.

The Communications Configuration T18 object can be used to configure the behavior of the $\overline{CHG}$ line. In addition to the $\overline{CHG}$ line operation modes described above, this object allows direct control over the state of the $\overline{CHG}$ line.

7.5 SDA and SCL

The I^2C bus transmits data and clock with SDA and SCL, respectively. These are open-drain. The device can only drive these lines low or leave them open. The termination resistors (Rp) pull the line up to VddIO if no I^2C device is pulling it down.

The termination resistors should be chosen so that the rise times on SDA and SCL meet the I^2C specifications for the interface speed being used, bearing in mind other loads on the bus. For best latency performance, it is recommended that no other devices share the I^2C bus with the maXTouch controller.

7.6 Clock Stretching

The device supports clock stretching in accordance with the I^2C specification. It may also instigate a clock stretch if a communications event happens during a period when the device is busy internally. The maximum clock stretch is 2 ms and typically less than 350 µs.

8.0 PCB DESIGN CONSIDERATIONS

8.1 Introduction

The following sections give the design considerations that should be adhered to when designing a PCB layout for use with the mXT112UD-MAUHA1. Of these, power supply and ground tracking considerations are the most critical.

By observing the following design rules, and with careful preparation for the PCB layout exercise, designers will be assured of a far better chance of success and a correctly functioning product.

8.2 Printed Circuit Board

Microchip recommends the use of a four-layer printed circuit board for mXT112UD-MAUHA1 applications. This, together with careful layout, will ensure that the board meets relevant EMC requirements for both noise radiation and susceptibility, as laid down by the various national and international standards agencies.

8.2.1 PCB CLEANLINESS

Modern no-clean-flux is generally compatible with capacitive sensing circuits.

CAUTION!	If a PCB is reworked to correct soldering faults relating to any device, or to any associated traces or components, be sure that you fully understand the nature of the flux used during the rework process. Leakage currents from hygroscopic ionic residues can stop capacitive sensors from functioning. If you have any doubts, a thorough cleaning after rework may be the only safe option.

8.3 Power Supply

8.3.1 SUPPLY QUALITY

While the device has good Power Supply Rejection Ratio properties, poorly regulated and/or noisy power supplies can significantly reduce performance.

Particular care should be taken of the AVdd supply, as it supplies the sensitive analog stages in the device.

8.3.2 SUPPLY RAILS AND GROUND TRACKING

Power supply and clock distribution are the most critical parts of any board layout. Because of this, it is advisable that these be completed before any other tracking is undertaken. After these, supply decoupling, and analog and high speed digital signals should be addressed. Track widths for all signals, especially power rails should be kept as wide as possible in order to reduce inductance.

The Power and Ground planes themselves can form a useful capacitor. Flood filling for either or both of these supply rails, therefore, should be used where possible. It is important to ensure that there are no floating copper areas remaining on the board: all such areas should be connected to the ground plane. The flood filling should be done on the outside layers of the board.

8.3.3 POWER SUPPLY DECOUPLING

Decoupling capacitors should be fitted as specified in Section 2.2 “Schematic Notes”.

The decoupling capacitors must be placed as close as possible to the pin being decoupled. The traces from these capacitors to the respective device pins should be wide and take a straight route. They should be routed over a ground plane as much as possible. The capacitor ground pins should also be connected directly to a ground plane.

Surface mounting capacitors are preferred over wire-leaded types due to their lower ESR and ESL. It is often possible to fit these decoupling capacitors underneath and on the opposite side of the PCB to the digital ICs. This will provide the shortest tracking, and most effective decoupling possible.

8.3.4 VOLTAGE PUMP

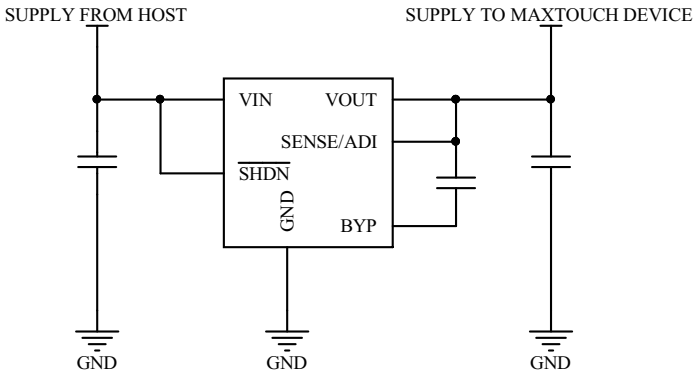
The traces for the voltage pump capacitor between EXTCAP0 and EXTCAP1 (Cd on the schematic in Section 2.0 “Schematic”) should be kept as short and as wide as possible for best pump performance. They should also be routed as parallel and as close as possible to each other in order to reduce emissions, and ideally the traces should be the same length.

8.3.5 VOLTAGE REGULATORS

Each supply rail requires a Low Drop-Out (LDO) voltage regulator, although an LDO can be shared where supply rails share the same voltage level.

Figure 8-1 shows an example circuit for an LDO.

FIGURE 8-1: EXAMPLE LDO CIRCUIT



An LDO regulator should be chosen that provides adequate output capability, low noise, no-load stability, good load regulation and step response. The mXT112UD-MAUHA1 has been qualified for use only with the Microchip LDOs listed in Table 8-1. However, some alternative LDOs with similar specifications are listed in Table 8-2. Microchip has not tested this maXTouch controller with any of these alternative LDOs. Microchip cannot guarantee the functionality or performance of this maXTouch controller with these or any other LDO besides those listed in Table 8-1.

NOTE	Microchip recommends that a minimum of a 1.0 µF ceramic, low ESR capacitor at the input and output of these devices is always used. The datasheet for the device should always be referred to when selecting capacitors and the typical recommended values, types and dielectrics adhered to.

TABLE 8-1: LDO REGULATORS – QUALIFIED FOR USE

Manufacturer	Device	Current Rating (mA)
Microchip Technology Inc.	MCP1824	300
Microchip Technology Inc.	MCP1824S	300
Microchip Technology Inc.	MAQ5300	300
Microchip Technology Inc.	MCP5504	300
Microchip Technology Inc.	MCP1725	500
Microchip Technology Inc.	MIC5514	300
Microchip Technology Inc.	MIC5323	300

TABLE 8-2: LDO REGULATORS – OTHER DEVICES

Manufacturer	Device	Current Rating (mA)
Analog Devices	ADP122/ADP123	300
Diodes Inc.	AP2125	300
Diodes Inc.	AP7335	300
Linear Technology	LT1763CS8-3.3	500
NXP	LD6836	300
Texas Instruments	LP3981	300

8.3.6 SINGLE SUPPLY OPERATION

When designing a PCB for an application using a single LDO, extra care should be taken to ensure short, low inductance traces between the supply and the touch controller supply input pins. Ideally, tracking for the individual supplies should be arranged in a star configuration, with the LDO at the junction of the star. This will ensure that supply current variations or noise in one supply rail will have minimum effect on the other supplies. In applications where a ground plane is not practical, this same star layout should also apply to the power supply ground returns.

Only regulators with a 300 mA or greater rating can be used in a single-supply design.

Refer to the following application note for more information:

- Application Note: MXTAN0208 – *Design Guide for PCB Layouts for maXTouch Touch Controllers*

8.3.7 MULTIPLE VOLTAGE REGULATOR SUPPLY

The AVdd supply stability is critical for the device because this supply interacts directly with the analog front end. If noise problems exist when using a single LDO regulator, Microchip recommends that AVdd is supplied by a regulator that is separate from the digital supply. This reduces the amount of noise injected into the sensitive, low signal level parts of the design.

8.4 Guard Track

Unlike other maXTouch devices, this device does not implement a driven shield. Instead, a guard track (Ground) should be routed between the X and Y tracks. This applies between any self capacitance X/Y lines and mutual capacitance only X/Y lines. It should be fairly wide to avoid X-to-Y coupling in mutual capacitance operation.

The distance between the guard track and the X/Y tracks should ideally be 0.3 mm or greater.

8.5 ESD Ground Routing

To avoid damage due to ESD strikes, the outermost track on the sensor should be an ESD ground. This should completely surround the sensor but with an overlap at the top rather than forming a complete loop.

The ESD ground traces should be connected to a dedicated ground trace in the PCB, and routed such that ESD strike currents do not flow under or close to the touch controller or the connecting wiring between it and the touchscreen array. The ESD ground should be connected in to the main system ground at a star point at the main GND connection to the PCB.

See also:

- MXTAN0208 – *Design guide for PCB Layouts for maXTouch Touch Controllers*

8.6 Analog I/O

In general, tracking for the analog I/O signals from the device should be kept as short as possible. These normally go to a connector which interfaces directly to the touchscreen.

Ensure that adequate ground-planes are used. An analog ground plane should be used in addition to a digital one. Care should be taken to ensure that both ground planes are kept separate and are connected together only at the point of entry for the power to the PCB. This is usually at the input connector.

8.7 Component Placement and Tracking

It is important to orient all devices so that the tracking for important signals (such as power and clocks) are kept as short as possible.

8.7.1 DIGITAL SIGNALS

In general, when tracking digital signals, it is advisable to avoid sharp directional changes on sensitive signal tracks (such as analog I/O) and any clock or crystal tracking.

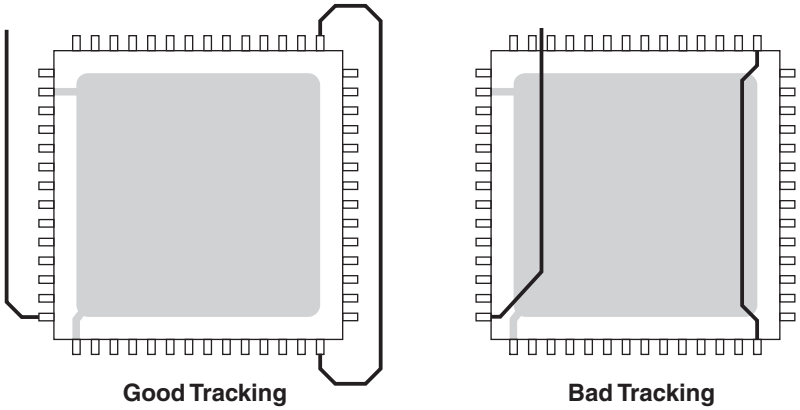
A good ground return path for all signals should be provided, where possible, to ensure that there are no discontinuities.

8.7.2 QFN PACKAGE RESTRICTIONS

The central pad on the underside of the QFN device should be connected to ground. Do not run any tracks underneath the body of the device on the top layer of the PCB, only ground. Figure 8-2 shows examples of good and bad tracking.

FIGURE 8-2: EXAMPLES OF GOOD AND BAD TRACKING

Note: The number of pins and their functions is shown for example purposes only and may not reflect the actual number or function on the device.



8.8 EMC and Other Observations

The following recommendations are not mandatory, but may help in situations where particularly difficult EMC or other problems are present:

- Try to keep as many signals as possible on the inside layers of the board. If suitable ground flood fills are used on the top and bottom layers, these will provide a good level of screening for noisy signals, both into and out of the PCB.
- Ensure that the on-board regulators have sufficient tracking around and underneath the devices to act as a heatsink. This heatsink will normally be connected to the 0 V or ground supply pin. Increasing the width of the copper tracking to any of the device pins will aid in removing heat. There should be no solder mask over the copper track underneath the body of the regulators.
- Ensure that the decoupling capacitors, especially high capacity ceramic type, have the requisite low ESR, ESL and good stability/temperature properties. Refer to the regulator manufacturer’s datasheet for more information.

9.0 GETTING STARTED WITH MXT112UD-MAUHA1

9.1 Establishing Contact

9.1.1 COMMUNICATION WITH THE HOST

The host can use the following interface to communicate with the device:

- I^2C interface (see Section 7.0 “I2C Communications”)

9.1.2 POWER-UP SEQUENCE

The power-up sequence is as follows:

1. On power-up, the $\overline{CHG}$ line goes low to indicate that there is new data to be read from the device. If the $\overline{CHG}$ line does not go low within a suitable timeout (for example, 1 second), there is a problem with the device.
2. Once the $\overline{CHG}$ line goes low, the host should attempt to read the first 7 bytes of memory from location 0x0000 to establish that the device is present and running following power-up. These bytes represent the ID Information portion of the Information Block and should be recorded by the host so it can read the Object Table (see Section 9.2 “Using the Object Protocol”).
3. The device performs a checksum on the configuration settings held in the non-volatile memory. If the checksum does not match a stored copy of the last checksum, then this indicates that the settings have become corrupted. For compliance with UL/IEC 60730 Class B, the host should make the system safe if the read checksum does not match the expected checksum, or if the configuration error bit in the message data from the Command Processor T6 object is set.

Once the device has been initialized, the host must perform the following initialization so that it can communicate with the device:

1. Read the start positions of all the objects in the device from the Object Table and build up a list of these addresses. Note that the number of elements was read by the host at start-up as part of the ID Information bytes.
2. Use the Object Table to calculate the report IDs so that messages from the device can be correctly interpreted.
3. Read any pending messages generated during the start-up process.

Refer to Application Note MXTAN0213, *Interfacing with maXTouch Touchscreen Controllers*, for more information. Refer also to the *mXT336UD-MAUHA1 1.0 Family UL/IEC 60730 Class B Compliance Guide* for more details on the power-up sequence for UL/IEC 60730 Class B compliance.

9.2 Using the Object Protocol

The device has an object-based protocol that is used to communicate with the device. Typical communication includes configuring the device, sending commands to the device, and receiving messages from the device.

9.2.1 CLASSES OF OBJECTS

The mXT112UD-MAUHA1 contains the following classes of objects:

- **Debug objects** – provide a raw data output method for development and testing.
- **General objects** – required for global configuration, transmitting messages and receiving commands.
- **Touch objects** – operate on measured signals from the touch sensor and report touch data.
- **Signal processing objects** – process data from other objects (typically signal filtering operations).
- **Support objects** – provide additional functionality on the device.

9.2.2 OBJECT INSTANCES

TABLE 9-1: OBJECTS ON THE MXT112UD-MAUHA1

Object	Description	Number of Instances	Usage
Debug Objects			
Diagnostic Debug T37	Allows access to diagnostic debug data to aid development.	1	Debug commands only; Read-only object. No configuration or tuning necessary. Not for use in production.

TABLE 9-1: OBJECTS ON THE MXT112UD-MAUHA1 (CONTINUED)

Object	Description	Number of Instances	Usage
General Objects			
Message Processor T5	Handles the transmission of messages. This object holds a message in its memory space for the host to read.	1	No configuration necessary.
Command Processor T6	Performs a command when written to. Commands include reset, calibrate and backup settings.	1	No configuration necessary.
Power Configuration T7	Controls the sleep mode of the device. Power consumption can be lowered by controlling the acquisition frequency and the sleep time between acquisitions.	1	Must be configured before use.
Acquisition Configuration T8	Controls how the device takes each capacitive measurement.	1	Must be configured before use.
Touch Objects			
Multiple Touch Touchscreen T100	Creates a Touchscreen that supports the tracking of more than one touch.	1	Enable and configure as required.
Signal Processing Objects			
Touch Suppression T42	Suppresses false detections caused by unintentional large touches by the user.	1	Enable and configure as required.
Shieldless T56	Allows a sensor to use true single-layer co-planar construction.	1	Enable and configure as required.
Lens Bending T65	Compensates for lens deformation (lens bending) by attempting to eliminate the disturbance signal from the reported deltas.	3	Enable and configure as required.
Noise Suppression T72	Performs various noise reduction techniques during sensor signal acquisition.	1	Enable and configure as required.
Glove Detection T78	Allows for the reporting of glove touches.	1	Enable and configure as required.
Retransmission Compensation T80	Limits the negative effects on touch signals caused by poor device coupling to ground or moisture on the sensor.	1	Enable and configure as required.
Self Capacitance Noise Suppression T108	Suppresses the effects of external noise within the context of self capacitance touch measurements.	1	Enable and configure as required.
Ignore Nodes T141	Defines a set of sensor nodes that are to be excluded from normal processing.	14	Configure as required
Support Objects			
Self Test Control T10	Controls the self-test routines to find faults on the device.	1	Enable and configure as required.
Self Test Pin Faults T11	Specifies the configuration settings for the Pin Fault self tests.	1	Configure as required.
Self Test Signal Limits T12	Specifies the configuration settings for the Signal Limit self tests.	1	Configure as required.
Communications Configuration T18	Configures additional communications behavior for the device.	1	Check and configure as necessary.
GPIO Configuration T19	Allows the host controller to configure and use the general purpose I/O pins on the device.	1	Enable and configure as required.
User Data T38	Provides a data storage area for user data.	1	Configure as required.

TABLE 9-1: OBJECTS ON THE MXT112UD-MAUHA1 (CONTINUED)

Object	Description	Number of Instances	Usage
CTE Configuration T46	Controls the capacitive touch engine for the device.	1	Must be configured.
Timer T61	Provides control of a timer.	4	Enable and configure as required.
Dynamic Configuration Controller T70	Allows rules to be defined that respond to system events.	20	Enable and configure as required.
Dynamic Configuration Container T71	Allows the storage of user configuration on the device that can be selected at runtime based on rules defined in the Dynamic Configuration Controller T70 object.	1	Configure if Dynamic Configuration Controller T70 is in use.
Auxiliary Touch Configuration T104	Allows the setting of self capacitance gain and thresholds for a particular measurement to generate auxiliary touch data for use by other objects.	1	Enable and configure if using self capacitance measurements
Self Capacitance Global Configuration T109	Provides configuration for self capacitance measurements employed on the device.	1	Check and configure as required (if using self capacitance measurements).
Self Capacitance Tuning Parameters T110	Provides configuration space for a generic set of settings for self capacitance measurements.	4	Use under the guidance of Microchip field engineers only.
Self Capacitance Configuration T111	Provides configuration for self capacitance measurements employed on the device.	2	Check and configure as required (if using self capacitance measurements).
Self Capacitance Measurement Configuration T113	Configures self capacitance measurements to generate data for use by other objects.	1	Enable and configure as required.
Message Count T144	Provides a count of pending messages.	1	Read-only object.
Ignore Nodes Controller T145	Specifies how ignored nodes configured in Ignore Nodes T141 are applied to various measurement processes on the device.	1	Configure as required

9.2.3 CONFIGURING AND TUNING THE DEVICE

The objects are designed such that a default value of zero in their fields is a “safe” value that typically disables functionality. The objects must be configured before use and the settings written to the non-volatile memory using the Command Processor T6 object.

Perform the following actions for each object:

1. Enable the object, if the object requires it.
2. Configure the fields in the object, as required.
3. Enable reporting, if the object supports messages, to receive messages from the object.

9.3 Writing to the Device

The following mechanism can be used to write to the device:

- Using an I^2C write operation (see Section 7.2 “Writing To the Device”).

For compliance with UL/IEC 60730 Class B, all writes must include a sequence number and the host should take appropriate action if the device detects an out-of-sequence write. In addition, the host must calculate a CRC on the data sent to the device. Refer to the *mXT336UD-MAUHA1 1.0 Family UL/IEC 60730 Class B Compliance Guide* for full details.

Communication with the device is achieved by writing to the appropriate object:

- To send a command to the device, an appropriate command is written to the Command Processor T6 object.

- To configure the device, a configuration parameter is written to the appropriate object. For example, writing to the Power Configuration T7 configures the power consumption for the device and writing to the Multiple Touch Touchscreen T100 object sets up the touchscreen. Some objects are optional and need to be enabled before use.

IMPORTANT!	When the host issues any command within an object that results in a flash write to the device Non-Volatile Memory (NVM), that object should have its CTRL RPTEN bit set to 1, if it has one. This ensures that a message from the object writing to the NVM is generated at the completion of the process and an assertion of the $\overline{\text{CHG}}$ line is executed. The host must also ensure that the assertion of the $\overline{\text{CHG}}$ line refers to the expected object report ID before asserting the $\overline{\text{RESET}}$ line to perform a reset. Failure to follow this guidance may result in a corruption of device configuration area and the generation of a CFGERR.

9.4 Reading from the Device

Status information is stored in the Message Processor T5 object. This object can be read to receive any status information from the device. Each message includes a sequence number and a CRC for error detection. For compliance with UL/IEC 60730 Class B, the host should monitor the sequence number and take appropriate action if it detects a missing or repeated message, or if a message is received out of sequence. Refer to the *mXT336UD-MAUHA1 1.0 Family UL/IEC 60730 Class B Compliance Guide* for full details.

The following mechanism provides an interrupt-style interface for reading messages in the Message Processor T5 object:

- The $\overline{\text{CHG}}$ line is asserted whenever a new message is available in the Message Processor T5 object (see Section 7.4 “CHG line”). See Section 7.3 “Reading From the Device” for information on the format of the I^2C read operation.

NOTE	The host should always wait to be notified of messages; the host should not poll the device for messages (either by polling the Message Processor T5 object or by polling the $\overline{\text{CHG}}$ line).

10.0 DEBUGGING AND TUNING

10.1 SPI Debug Interface

The SPI Debug Interface is used for tuning and debugging when running the system and allows the development engineer to use Microchip maXTouch Studio to read the real-time raw data. This uses the low-level debug port.

NOTE	The host must not use the Command Processor T6 debug port over the SPI Debug Interface during UL/IEC 60730 Class B operation as use of the SPI Debug Interface is not UL/IEC 60730 Class B compliant.

The SPI Debug Interface consists of the $\overline{\text{DBG\_SS}}$, DBG_CLK, and DBG_DATA lines. These lines should be routed to test points on all designs such that they can be connected to external hardware during system development. These lines should not be connected to power or GND. See Section 2.2.11 “SPI Debug Interface” for more details.

The SPI Debug Interface is enabled by the Command Processor T6 object and by default will be off.

NOTE	When the $\overline{\text{DBG\_SS}}$, DBG_CLK, and DBG_DATA lines are in use for debugging, any alternative function for the pins cannot be used. The touch controller will take care of the pin configuration.

10.2 Object-based Protocol

The device provides a mechanism for obtaining debug data for development and testing purposes by reading data from the Diagnostic Debug T37 object.

NOTE	The Diagnostic Debug T37 object is of most use for simple tuning purposes. When debugging a design, it is preferable to use the SPI Debug Interface, as this will have a much higher bandwidth and can provide real-time data.

10.3 Self Test

The Self Test Control T10, Self Test Pin Faults T11 and Self Test Signal Limits T12 objects run self-test routines in the device to find hardware faults in the device both at power-on/reset and during normal operation. These self-test routines can be configured to check the CPU, clock, memory an power supplies of the devices, as well as CTE operation, pin shorts (X to Y, or X lines to power or GND) and the signal levels.

In addition to one-off hardware tests, the Self Test Control T10 object can also provide continuous monitoring of the health of the device while it is in operation. A periodic Built-In Self Test (BIST) test can be run at a user-specified interval and reports the global pass and specific fail messages (as determined by the device configuration). Reporting is achieved either by standard Self Test Control T10 object protocol messages or by a configurable hardware GPIO pin, configured using the GPIO Configuration T19 object.

IMPORTANT!	For compliance with IEC/UL 60730 Class B safety specification, reporting should be achieved using Self Test Control T10 object protocol messages and not by a hardware GPIO pin.

For a list of the self tests available on the mXT112UD-MAUHA1, see Table 6-1 on page 21

11.0 SPECIFICATIONS

11.1 Absolute Maximum Specifications

Vdd	3.6V
VddIO	3.6V
AVdd	3.6V
Maximum continuous combined pin current, all GPIO*n* pins	40 mA
Voltage forced onto any pin	–0.3 V to (Vdd, VddIO or AVdd) + 0.3 V
Configuration parameters maximum writes	10,000
Maximum junction temperature	125°C

CAUTION! Stresses beyond those listed under *Absolute Maximum Specifications* may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum specification conditions for extended periods may affect device reliability.

11.2 Recommended Operating Conditions

Operating temperature	–40°C to +85°C
Storage temperature	–60°C to +150°C
Vdd	3.3 V
VddIO	1.8 V to 3.3 V
AVdd	3.3 V
XVdd with internal voltage doubler	2 × AVdd
XVdd low voltage operation (without internal voltage doubler)	Connected to AVdd
Temperature slew rate	10°C/min

11.2.1 DC CHARACTERISTICS

11.2.1.1 Analog Voltage Supply – AVdd

Parameter	Min	Typ	Max	Units	Notes
AVdd					
Operating limits	3.0	3.3	3.47	V	
Supply Rise Rate	–	–	0.036	V/µs	For example, for a 3.3 V rail, the voltage should take a minimum of 92 µs to rise

11.2.1.2 Digital Voltage Supply – VddIO, Vdd

Parameter	Min	Typ	Max	Units	Notes
VddIO					
Operating limits – Normal Voltage	2.7	3.3	3.47	V	
Operating limits – Low Voltage	1.71	1.8	1.89	V	
Supply Rise Rate	–	–	0.036	V/µs	For example, for a 3.3 V rail, the voltage should take a minimum of 92 µs to rise
Vdd					
Operating limits	2.7	3.3	3.47	V	
Supply Rise Rate	–	–	0.036	V/µs	For example, for a 3.3 V rail, the voltage should take a minimum of 92 µs to rise
Supply Fall Rate	–	–	0.05	V/µs	For example, for a 3.3 V rail, the voltage should take a minimum of 66 µs to fall

11.2.1.3 XVdd Voltage Supply – XVdd

Parameter	Min	Typ	Max	Units	Notes
XVdd					
Operating limits – voltage doubler enabled	–	2 × AVdd	–	V	
Operating limits – voltage doubler disabled	–	AVdd	–	V	

11.2.2 POWER SUPPLY RIPPLE AND NOISE

Parameter	Min	Typ	Max	Units	Notes
Vdd	–	–	±50	mV	Across frequency range 1 Hz to 1 MHz
AVdd	–	–	±40	mV	Across frequency range 1 Hz to 1 MHz, with Noise Suppression enabled

11.3 Test Configuration

The configuration values listed below were used in the reference unit to validate the interfaces and derive the characterization data provided in the following sections.

TABLE 11-1: TEST CONFIGURATION

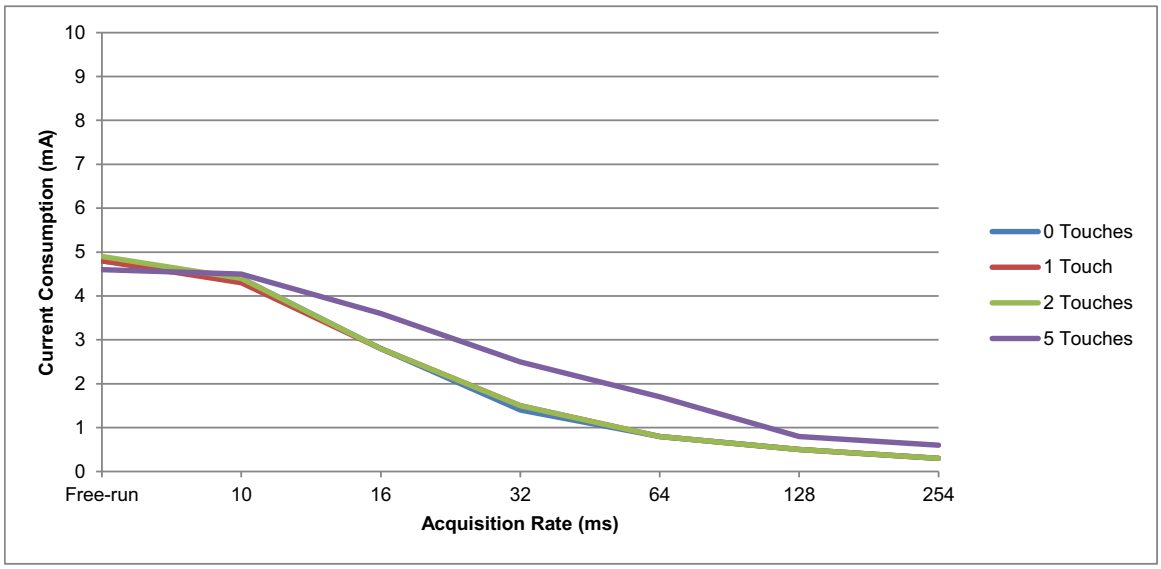
Object/Parameter	Description/Setting (Numbers in Decimal)
Power Configuration T7	
CFG2	0 (Power Monitor Enabled)
Acquisition Configuration T8	
CHRGTIME	40
MEASALLOW	3
Self Test Control T10	Object Enabled
GPIO Configuration T19	Object Enabled
Touch Suppression T42	Object Enabled
CTE Configuration T46	
IDLESYNCSPERX	8
ACTVSYNCSPERX	8
Shieldless T56	Object Enabled
INTTIME	22
Lens Bending T65 Instance 0	Object Instance Enabled
Lens Bending T65 Instance 1	Object Instance Enabled
Lens Bending T65 Instance 2	Object Instance Enabled
Noise Suppression T72	Object Enabled
Glove Detection T78	Object Enabled
Retransmission Compensation T80	Object Enabled
Multiple Touch Touchscreen T100	Object Enabled
XSIZE	14
Auxiliary Touch Configuration T104	Object Enabled
Self Capacitance Noise Suppression T108	Object Enabled
Self Capacitance Configuration T111 Instance 0	
INTTIME	50
IDLESYNCSPERL	24
ACTVSYNCSPERL	24
Self Capacitance Configuration T111 Instance 1	
INTTIME	50
IDLESYNCSPERL	32
ACTVSYNCSPERL	32

11.4 Current Consumption – I²C Interface

NOTE The characterization charts show typical values based on the configuration in Table 11-1. Actual power consumption in the user's application will depend on the circumstances of that particular project and will vary from that shown here. Further tuning will be required to achieve an optimal performance.

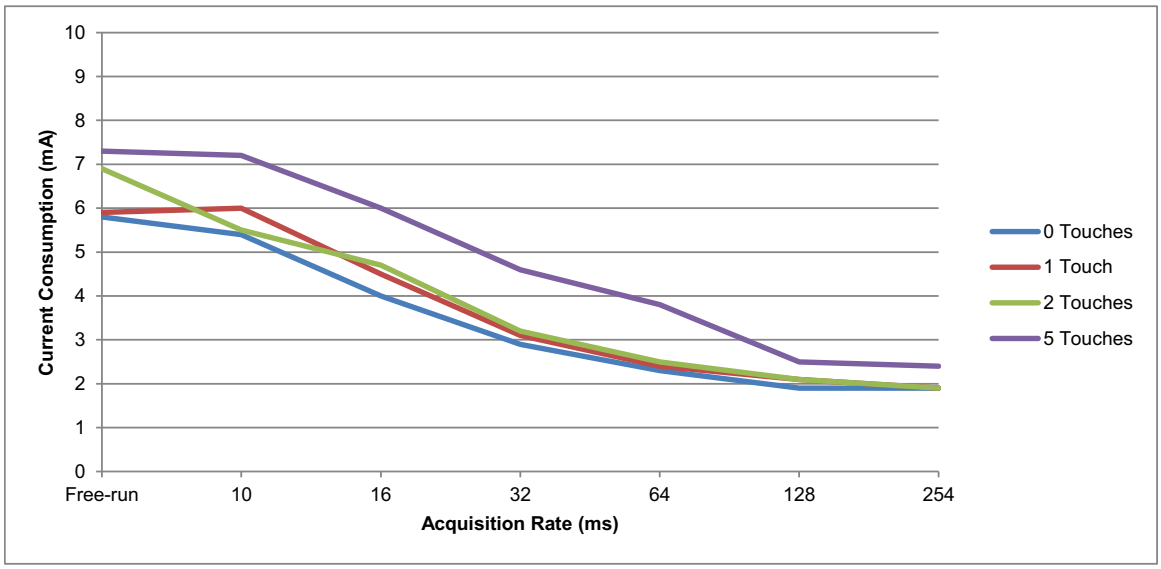
11.4.1 AVDD 3.3V

	Current Consumption (mA)			
Acquisition Rate (ms)	**0 Touches**	**1 Touch**	**2 Touches**	**5 Touches**
Free-run	4.8	4.8	4.9	4.6
10	4.4	4.3	4.4	4.5
16	2.8	2.8	2.8	3.6
32	1.4	1.5	1.5	2.5
64	0.8	0.8	0.8	1.7
128	0.5	0.5	0.5	0.8
254	0.3	0.3	0.3	0.6



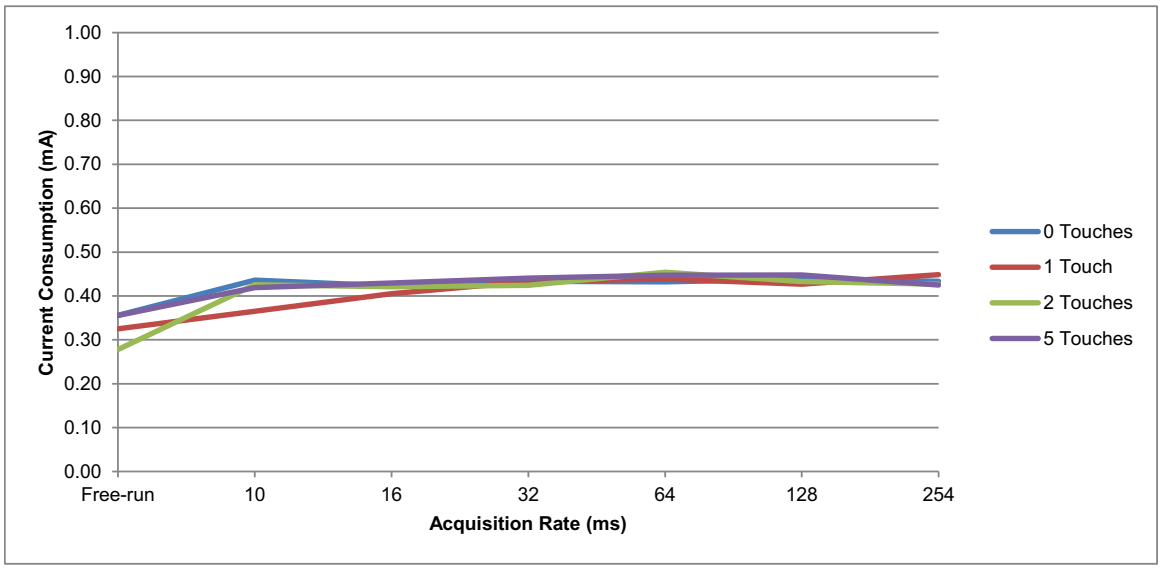
11.4.2 VDD 3.3V

	Current Consumption (mA)			
Acquisition Rate (ms)	**0 Touches**	**1 Touch**	**2 Touches**	**5 Touches**
Free-run	5.8	5.9	6.9	7.3
10	5.4	6	5.5	7.2
16	4	4.5	4.7	6
32	2.9	3.1	3.2	4.6
64	2.3	2.4	2.5	3.8
128	1.9	2.1	2.1	2.5
254	1.9	1.9	1.9	2.4



11.4.3 VDDIO 1.8V

	Current Consumption (mA)			
Acquisition Rate (ms)	**0 Touches**	**1 Touch**	**2 Touches**	**5 Touches**
Free-run	0.36	0.33	0.28	0.36
10	0.44	0.36	0.43	0.42
16	0.42	0.40	0.42	0.43
32	0.43	0.43	0.42	0.44
64	0.43	0.44	0.45	0.45
128	0.44	0.43	0.43	0.45
254	0.43	0.45	0.43	0.42



11.4.4 DEEP SLEEP

T_A = 25°C

	Power Monitoring On		Power Monitoring Off		
Parameter	**Sampling Mode**	**Continuous Mode**		**Units**	**Notes**
Deep Sleep Current	1.2	1.8	1.1	mA	Vdd = 3.3V, AVdd = 3.3V, VddIO = 1.8V
Deep Sleep Power	4.0	5.6	3.6	mW	

11.5 Timing Specifications

NOTE The figures below show typical values based on the test configuration. Actual timings in the user's application will depend on the circumstances of that particular project and will vary from those shown below. Further tuning will be required to achieve an optimal performance.

11.5.1 TOUCH LATENCY

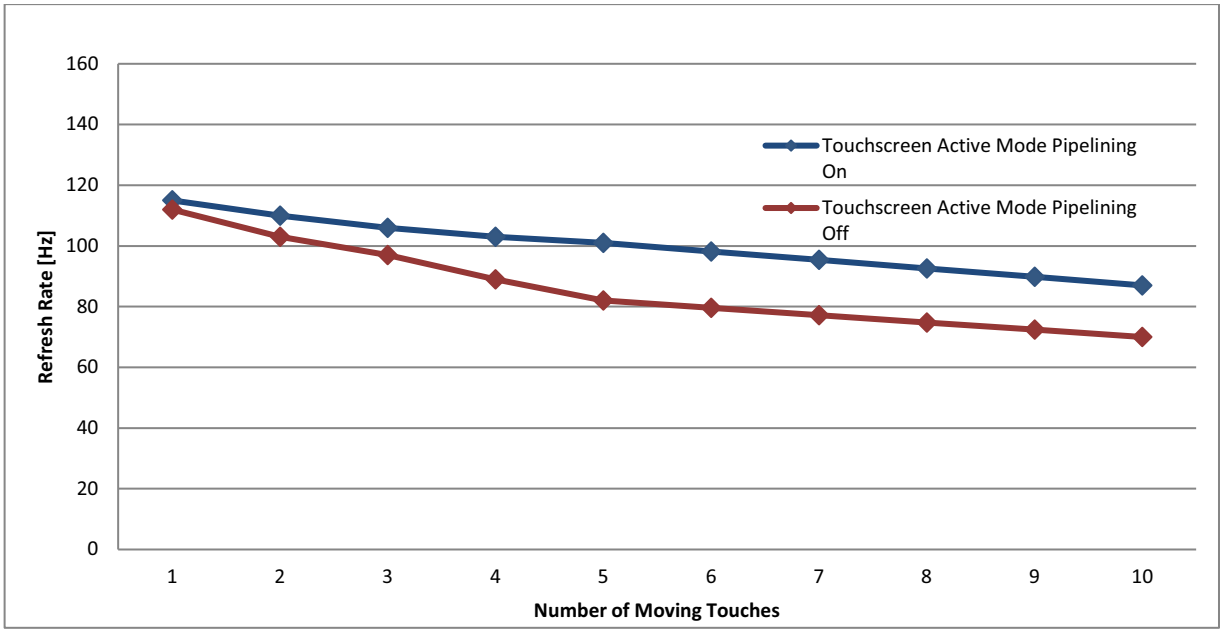
Conditions: XSIZE = 14; CHRGTIME = 40; IDLESYNCSPERX = 8; ACTVSYNCSPERX = 8;
T = ambient temperature; Finger center of screen; Reporting off (except T100)

Idle Primary = Mutual Capacitance; Active Primary = Mutual Capacitance

T100 TCHDIDOWN	Pipelining Off			Pipelining On			Units
	Min	Typ	Max	Min	Typ	Max	
3	26.3	31	40.8	28	32.8	41.2	ms
2	18.6	22.5	32.9	20.6	25	34.1	ms
1	10.8	15.1	24.2	12.9	17.3	26.8	ms

11.5.2 REPORT RATE

Conditions: XSIZE = 14; CHRGTIME = 40; IDLESYNCSPERX = 8; ACTVSYNCSPERX = 8; T = ambient temperature



11.5.3 BURST FREQUENCY TOLERANCE

The burst frequency is directly correlated to the system clock. The burst frequency tolerance depends on the tolerance of the system's oscillator (see Table 11-2).

TABLE 11-2: OSCILLATOR TOLERANCE

Conditions: T= 25°C, 85°C

Min Drift	Nominal	Max Drift	Notes
–5%	40 MHz (calibrated)	+5%	Minimum/Maximum drift over temperature is specified as percentage below/above nominal frequency

11.5.4 RESET TIMINGS

Parameter	POST Enabled (Typ)	POST Disabled (Typ)	Units	Notes
Power on to $\overline{\text{CHG}}$ line low	362	122	ms	Vdd supply for POR VddIO supply for external reset
Hardware reset to $\overline{\text{CHG}}$ line low	362	122	ms	
Software reset to $\overline{\text{CHG}}$ line low	362	122	ms	

Note 1: Any $\overline{\text{CHG}}$ line activity before the power-on or reset period has expired should be ignored by the host. Operation of this signal cannot be guaranteed before the power-on/reset periods have expired.

11.6 Touch Accuracy and Repeatability

Parameter	Min	Typ	Max	Units	Notes
Linearity	–	±0.5	–	mm	Finger diameter 8 mm
Accuracy (across all areas of screen)	–	0.5	–	mm	Finger diameter 8 mm
Repeatability	–	±0.25	–	%	X axis with 12-bit resolution

11.7 Touchscreen Sensor Characteristics

Parameter	Description	Value
Cm	Mutual capacitance	Typical value is between 0.15 pF and 10 pF on a single node.
Cpx	Mutual capacitance load to X	Microchip recommends a maximum load of 300 pF on each X or Y line. (1)
	With Internal Voltage Pump	Maximum recommended load on each X line: (2) Cpx + (*num_Y* × Cm) < 240 pF
	With Internal Voltage Pump and Dual X	Maximum recommended load on each X line: (2) Cpx + (2 × *num_Y* × Cm) < 120 pF
Cpy	Mutual capacitance load to Y	Microchip recommends a maximum load of 300 pF on each X or Y line. (1)
Cpx	Self capacitance load to X	Microchip recommends a maximum load of 130 pF on each X or Y line. (1)
Cpy	Self capacitance load to Y	
ΔCpx	Self capacitance imbalance on X	Nominal value is 14.8 pF. Value increases by 1 pF for every 45 pF reduction in Cpx/Cpy (based on 100 pF load)
ΔCpy	Self capacitance imbalance on Y	

Note 1: Please contact your Microchip representative for advice if you intend to use higher values.

2: *num_Y* = Number of active Y lines defined by Multiple Touch Touchscreen T100.

11.8 Input/Output Characteristics

Parameter	Description	Min	Typ	Max	Units	Notes
Input (All input pins connected to the VddIO power rail)						
Vil	Low input logic level	–0.3	–	0.3 × VddIO	V	VddIO = 1.8 V to Vdd
Vih	High input logic level	0.7 × VddIO	–	VddIO	V	VddIO = 1.8 V to Vdd
Iil	Input leakage current	–	–	1	µA	
$\overline{\text{RESET}}$	Internal pull-up resistor	9	10	16	kΩ	
GPIOs	Internal pull-up/pull-down resistor					

Parameter	Description	Min	Typ	Max	Units	Notes
Input (All input pins connected to the Vdd power rail)						
Vil	Low input logic level	–0.3	–	0.3 × Vdd	V	
Vih	High input logic level	0.7 × Vdd	–	Vdd	V	
Iil	Input leakage current	–	–	1	µA	Pull-up resistors disabled
GPIOs	Internal pull-up/pull-down resistor	9	10	16	kΩ	
Output (All output pins connected to the VddIO power rail)						
Vol	Low output voltage	0	–	0.2 × VddIO	V	VddIO = 1.8 V to Vdd Iol = max 0.4 mA
Voh	High output voltage	0.8 × VddIO	–	VddIO	V	VddIO = 1.8 V to Vdd Ioh = 0.4 mA
Output (All output pins connected to the Vdd power rail)						
Vol	Low output voltage	0	–	0.2 × Vdd	V	Iol = max 0.4 mA
Voh	High output voltage	0.8 × Vdd	–	Vdd	V	Ioh = 0.4 mA

11.9 I²C Specification

Parameter	Value
Address	0x4A
I²C specification (1)	Revision 6.0
Maximum bus speed (SCL) (2)	1 MHz
Standard Mode (3)	100 kHz
Fast Mode (3)	400 kHz
Fast Mode Plus (3)	1 MHz

Note 1: More detailed information on I²C operation is available from www.nxp.com/documents/user_manual/UM10204.pdf.

2: In systems with heavily laden I²C lines, even with minimum pull-up resistor values, bus speed may be limited by capacitive loading to less than the theoretical maximum.

3: The values of pull-up resistors should be chosen to ensure SCL and SDA rise and fall times meet the I²C specification. The value required will depend on the amount of capacitance loading on the lines.

11.10 Thermal Packaging

11.10.1 THERMAL DATA

Parameter	Description	Typ	Unit	Condition	Package
θ_{JA}	Junction to ambient thermal resistance	33.7	°C/W	Still air	56-pin XQFN 6 × 6 × 0.4 mm
θ_{JC}	Junction to case thermal resistance	10.1	°C/W		56-pin XQFN 6 × 6 × 0.4 mm

11.10.2 JUNCTION TEMPERATURE

The maximum junction temperature allowed on this device is 125°C.

The average junction temperature in °C (T_J) for this device can be obtained from the following:

$$T_J = T_A + (P_D \times \theta_{JA})$$

If a cooling device is required, use this equation:

$$T_J = T_A + (P_D \times (\theta_{HEATSINK} + \theta_{JC}))$$

where:

- θ_{JA}= package thermal resistance, Junction to ambient (°C/W) (see Section 11.10.1 “Thermal Data”)
- θ_{JC} = package thermal resistance, Junction to case thermal resistance (°C/W) (see Section 11.10.1 “Thermal Data”)
- $\theta_{HEATSINK}$ = cooling device thermal resistance (°C/W), provided in the cooling device datasheet
- P_D = device power consumption (W)
- T_A is the ambient temperature (°C)

11.11 ESD Information

Parameter	Value	Reference Standard
Human Body Model (HBM)	±2000V	JEDEC JS–001
Charge Device Model (CDM)	±250V	JEDEC JS–001

11.12 Soldering Profile

Profile Feature	Green Package
Average Ramp-up Rate (217°C to Peak)	3°C/s max
Preheat Temperature 175°C ±25°C	150 – 200°C
Time Maintained Above 217°C	60 – 150 s
Time within 5°C of Actual Peak Temperature	30 s
Peak Temperature Range	260°C
Ramp down Rate	6°C/s max
Time 25°C to Peak Temperature	8 minutes max

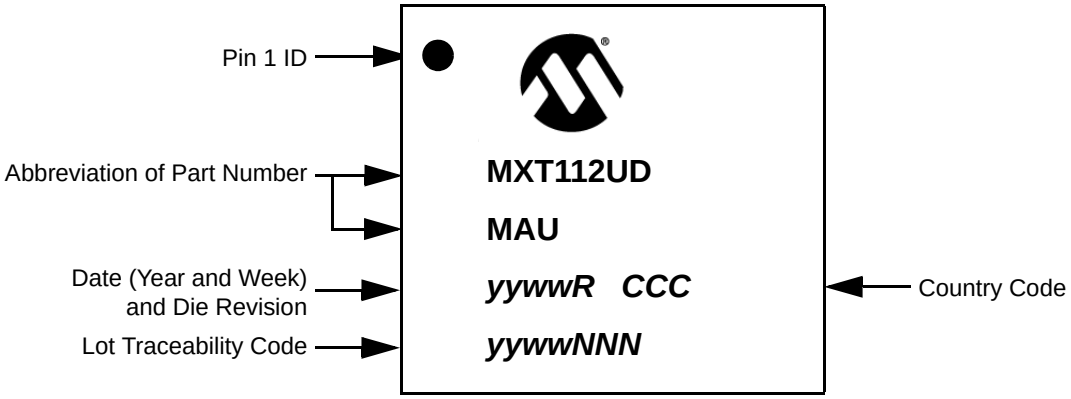
11.13 Moisture Sensitivity Level (MSL)

MSL Rating	Package Type(s)	Peak Body Temperature	Specifications
MSL3	56-pin XQFN	260°C	IPC/JEDEC J-STD-020

12.0 PACKAGING INFORMATION

12.1 Package Marking Information

12.1.1 56-PIN XQFN



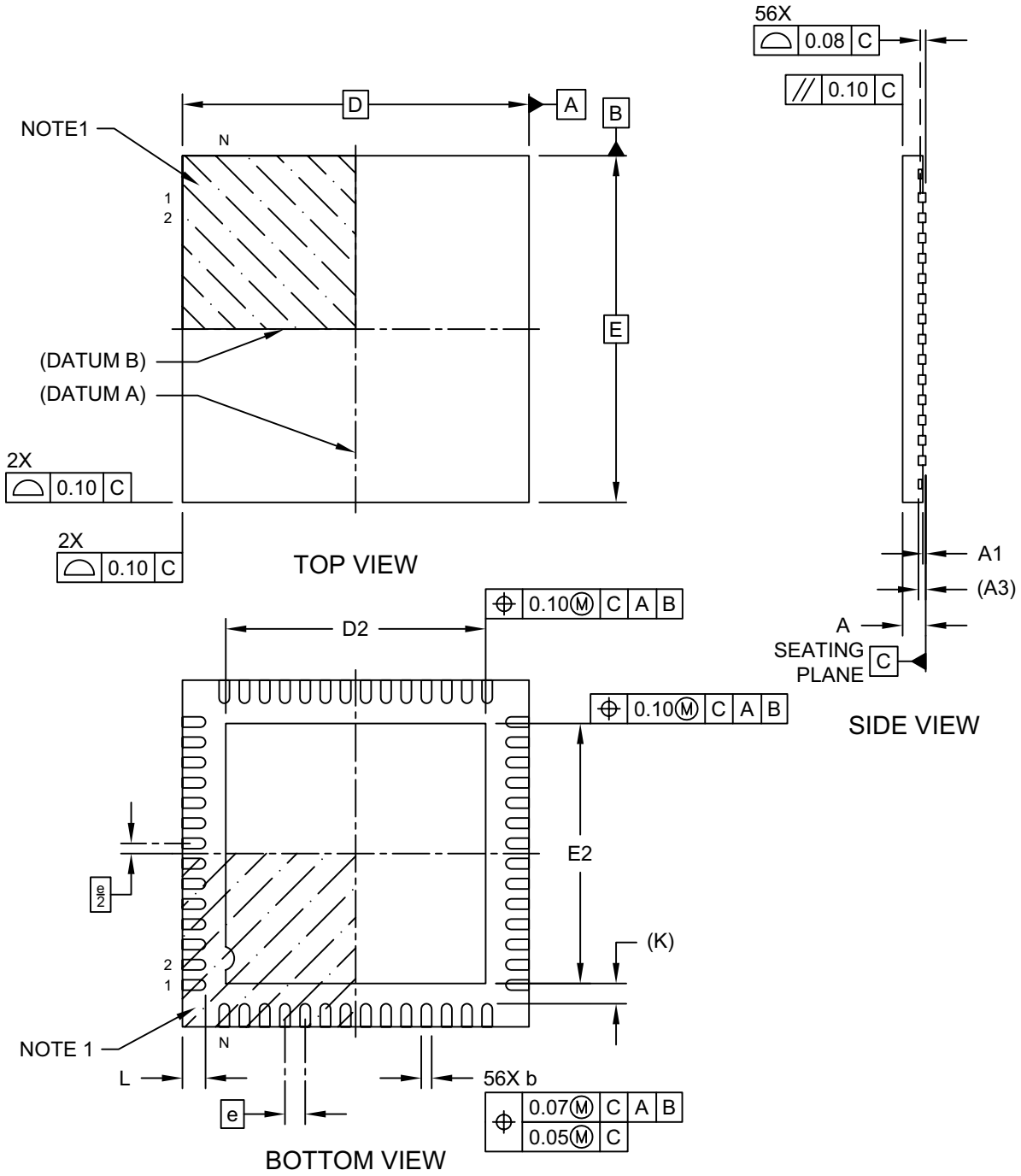
12.1.2 ORDERABLE PART NUMBERS

The product identification system for maXTouch devices is described in "Product Identification System". That section also lists example part numbers for the device.

12.2 Package Details

56-Lead Extremely Thin Quad Flatpack No-Lead Package (TWB) - 6x6x0.4 mm Body [XQFN] Wlth 4.5x4.5 mm Exposed Pad; Atmel Legacy Global Package Code ZIX

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-21448 Rev A Sheet 1 of 2

56-Lead Extremely Thin Quad Flatpack No-Lead Package (TWB) - 6x6x0.4 mm Body [XQFN] Wlth 4.5x4.5 mm Exposed Pad; Atmel Legacy Global Package Code ZIX

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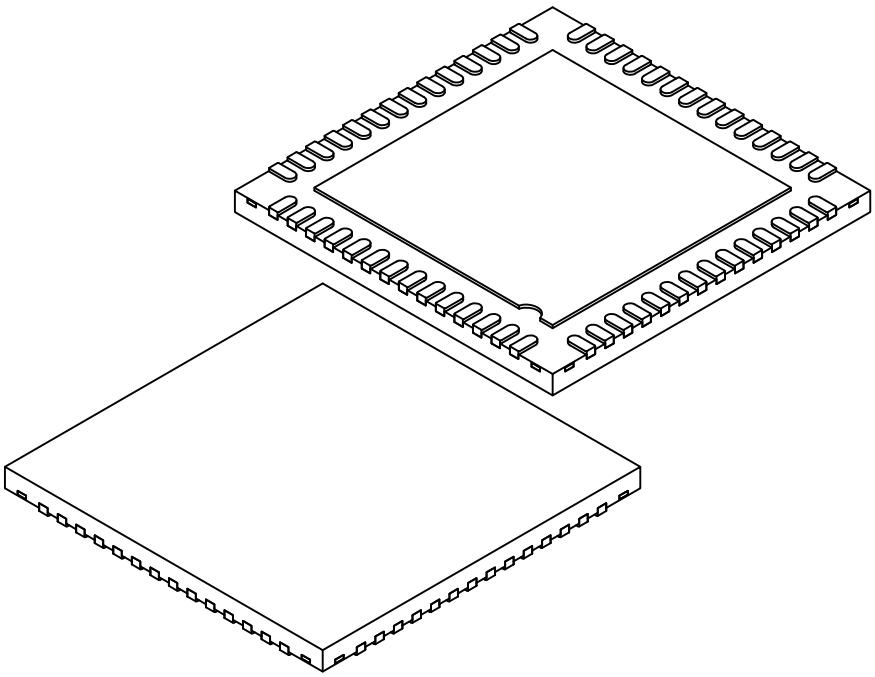


Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		56	
Pitch	e		0.35 BSC	
Overall Height	A	–	–	0.400
Standoff	A1	0.00	–	0.05
Terminal Thickness	A3		0.127 REF	
Overall Length	D		6.00 BSC	
Exposed Pad Length	D2	4.40	4.50	4.60
Overall Width	E		6.00 BSC	
Exposed Pad Width	E2	4.40	4.50	4.60
Terminal Width	b	0.13	0.18	0.23
Terminal Length	L	0.35	0.40	0.45
Terminal-to-Exposed-Pad	K		0.35 REF	

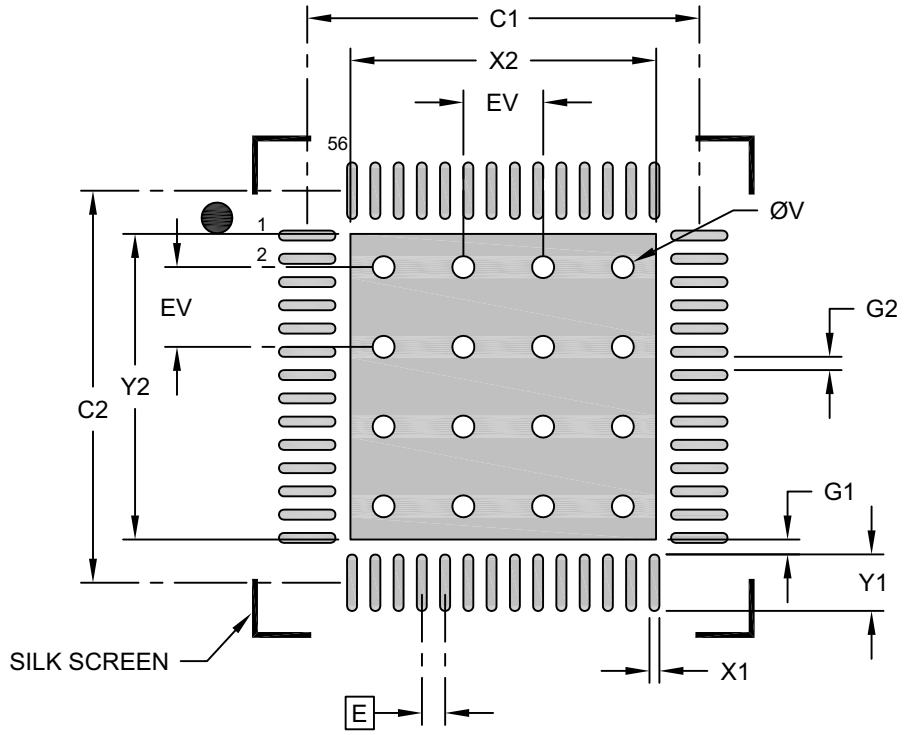
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-21448 Rev A Sheet 2 of 2

56-Lead Extremely Thin Quad Flatpack No-Lead Package (TWB) - 6x6x0.4 mm Body [XQFN] Wlth 4.5x4.5 mm Exposed Pad; Atmel Legacy Global Package Code ZIX

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.35 BSC	
Optional Center Pad Width	X2			4.60
Optional Center Pad Length	Y2			4.60
Contact Pad Spacing	C1		5.90	
Contact Pad Spacing	C2		5.90	
Contact Pad Width (X56)	X1			0.15
Contact Pad Length (X56)	Y1			0.85
Contact Pad to Center Pad (X56)	G1	0.23		
Contact Pad to Contact Pad (X52)	G2	0.20		
Thermal Via Diameter	V		0.33	
Thermal Via Pitch	EV		1.20	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-23448 Rev A

APPENDIX A: ASSOCIATED DOCUMENTS

Microchip maXTouch Documents

The following documents are available by contacting your Microchip representative.

Product Documentation

- *mXT336UD-MAUHA1 1.0 Family UL/IEC 60730 Class B Compliance Guide*

Touchscreen Design and PCB/FPCB Layout Guidelines

- Application Note: QTAN0054 – *Getting Started with maXTouch Touchscreen Designs*
- Application Note: MXTAN0208 – *Design Guide for PCB Layouts for maXTouch Touch Controllers*
- Application Note: QTAN0080 – *Touchscreens Sensor Design Guide*
- Application Note: AN2683 – *Edge Wiring for Self Capacitance maXTouch Touchscreens*

Configuring and Tuning the Device

- Application Note: MXTAN0213 – *Interfacing with maXTouch Touchscreen Controllers*

Tools

- *maXTouch Studio User Guide* (distributed as on-line help with maXTouch Studio)

External Documents

The following documents are not supplied by Microchip. To obtain any of the following documents, please contact the relevant organization.

Standards

- IEC 60730-1, *Automatic electrical controls – Part 1: General requirement*, Edition 5.1, 2015-12
- UL 60730-1, *Automatic Electrical Controls – Part 1: General Requirements*, Edition 5, 2016-08-03

I^2C Interface

- UM10204, *I^2C bus specification and user manual*, Rev. 6 — 4 April 2014
  Available from: www.nxp.com/documents/user_manual/UM10204.pdf

APPENDIX B: REVISION HISTORY

Revision A (October 2020)

Initial edition for firmware revision 1.0.AB – Release

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PRODUCT IDENTIFICATION SYSTEM

The table below gives details on the product identification system for maXTouch devices. See "Orderable Part Numbers" below for example part numbers for the mXT112UD-MAUHA1.

To order or obtain information, for example on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	–XXX	[X]	[X]	[XXX]
Device	Package	Temperature Range	Tape and Reel Option	Pattern

Device:	Base device name		
Package:	A	=	QFP (Plastic Quad Flatpack)
	CC	=	UFBGA (Ultra Thin Fine-pitch Ball Grid Array)
	C2	=	UFBGA (Ultra Thin Fine-pitch Ball Grid Array)
	NH	=	UFBGA (Ultra Thin Fine-pitch Ball Grid Array)
	C4	=	X1FBGA (Extra Thin Fine-pitch Ball Grid Array)
	MA	=	XQFN (Super Thin Quad Flat No Lead Sawn)
	MA5	=	XQFN (Super Thin Quad Flat No Lead Sawn)
Temperature Range:	U	=	–40°C to +85°C (Grade 3)
	T	=	–40°C to +85°C (Grade 3)
	B	=	–40°C to +105°C (Grade 2)
Tape and Reel Option:	*Blank*	=	Standard Packaging (Tube or Tray)
	R	=	Tape and Reel (1)
Pattern:	Extension, QTP, SQTP, Code or Special Requirements (Blank Otherwise)		

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. See "Orderable Part Numbers" below or check with your Microchip Sales Office for package availability with the Tape and Reel option.

Orderable Part Numbers

Orderable Part Number	Firmware Revision	Description
ATMXT112UD-MAUHA1 (Supplied in trays)	1.0.AB	56-pin XQFN 6 × 6 × 0.4 mm, RoHS compliant Industrial grade; not suitable for automotive characterization
ATMXT112UD-MAURHA1 (Supplied in tape and reel)		

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- **General Technical Support** – Frequently Asked Questions (FAQ), technical support requests, online discussion groups, Microchip consultant program member listing
- **Business of Microchip** – Product selector and ordering guides, latest Microchip press releases, listing of seminars and events, listings of Microchip sales offices, distributors and factory representatives

THE MAXTOUCH WEB SITE

Information on Microchip's maXTouch product line can be accessed via the microchip web site at www.microchip.com, This information is also available for direct access via a short-cut at www.maxtouch.com. The maXTouch web pages contain the following information:

- **Product Information** – Product specifications, brochures, datasheets, protocol guides
- **Tools and Software** – Evaluation kits, maXTouch Studio, software libraries for individual maXTouch touch controllers
- **Training and Support** – Generic application notes and training material for the maXTouch product range

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- Technical Support

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