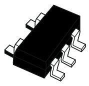
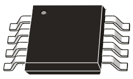
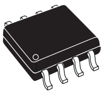
Very high accuracy (20 µV), zero-drift, rail-to-rail output, 3 MHz, 36 V op amp



SOT23-5



MiniSO8



SO8

Maturity status link
TSB181, TSB182

Related products	
TSB611, TSB612	For lower current consumption
TSB621, TSB622	For lower speed
TSB571, TSB572	For rail-to-rail inputs
TSB711, TSB712	For higher speed, precision, and rail-to-rail inputs

Features

- Very low offset voltage: 20 µV max. @ 25 °C
- Rail-to-rail output
- Wide supply voltage: 4 to 36 V
- Gain bandwidth product: 3 MHz
- Slew rate: 2 V/µs
- Low noise: 24 nV/√Hz
- EMI hardened
- High ESD tolerance: 4 kV HBM
- Extended temperature range: -40 °C to 125 °C
- AEC-Q100 qualified

Applications

- Industrial
- Power supplies
- Automotive

Description

The TSB181 and TSB182 are very high precision operational amplifiers ensuring a maximum input offset voltage of 20 µV. They can operate over an extended supply voltage range and feature rail-to-rail output. They offer an excellent speed/current consumption ratio with 3 MHz gain bandwidth product while consuming 650 µA typically per operational amplifier on a large supply voltage range.

The TSB181 and TSB182 operate over a wide temperature range from -40 °C to 125 °C making these devices ideal for industrial and automotive applications with the associated qualification.

Thanks to their small package size, the TSB181 and TSB182 can be used in applications where space on the board is limited. They can thus reduce the overall cost of the PCB.

1 Pin description

Figure 1. **Pin connection TSB181 (top view)**

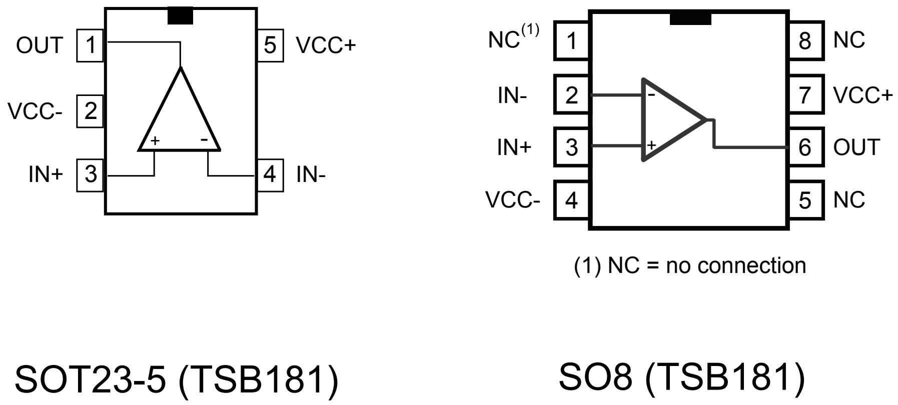
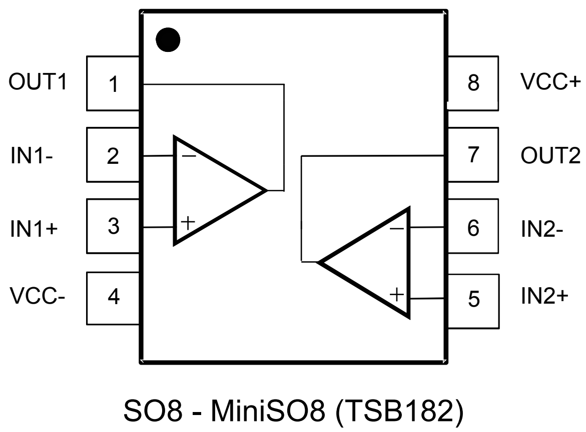


Figure 2. **Pin connections TSB182 (top view)**



2 Absolute maximum ratings and operating conditions

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
Vcc	Supply voltage [1]	40	V
Vid	Differential input voltage [2]	± 0.7	V
Vin	Input voltage	(Vcc-) -0.3 to (Vcc+) +0.3	V
Iin	Input current [3]	10	mA
Tstg	Storage temperature	-65 to 150	°C
Tj	Junction temperature	150	°C
Rth-ja	Thermal resistance junction-to-ambient [4] [5] SO8 MiniSO8 SOT23-5	 125 190 250	°C/W
ESD	Human Body Model (HBM) [6]	4000	V
	Machine Model (MM) [7]	200	
	Charged Device Model (CDM) [8]	1500	

1. *All voltage values, except differential voltage, are with respect to network ground terminal.*
2. *The differential voltage is the difference between inverting and non-inverting terminal voltage.*
3. *Input current must be limited by a resistor in series with the inputs.*
4. *Rth are typical values.*
5. *Short-circuits can cause excessive heating and destructive dissipation.*
6. *According to JEDEC standard JESD22-A114F.*
7. *According to JEDEC standard JESD22-A115A.*
8. *According to ANSI/ESD STM 5.3.1.*

Table 2. Operating conditions

Symbol	Parameter	Value	Unit
Vcc	Supply voltage	4 to 36	V
Vicm	Common mode voltage on input pins	(Vcc-) to (Vcc+) -2	V
T	Operating free-air temperature range	-40 to 125	°C

3 Electrical characteristics

Table 3. Electrical characteristics V_{CC} = 5 V, V_{icm} = V_{CC}/2, R_L = 10 kΩ connected to V_{CC}/2 (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
		DC performance				
V_{IO}	Input offset voltage	V_{icm} = V_{CC}/2				µV
		T = 25 °C	-20		+20	
		Tmin < T < Tmax	-30		+30	
		V_{icm} = 0 V				
		T = 25 °C	-20		+20	
		Tmin < T < Tmax	-30		+30	
$\|\Delta V_{IO}/\Delta T\|$	Input offset voltage drift [1]	Tmin < T < Tmax		30	100	nV/°C
I_{IB}	Input bias current	T = 25 °C			400	pA
		Tmin < T < Tmax			400	
I_{IO}	Input offset current	T = 25 °C			600	
		Tmin < T < Tmax			600	
CMR	Common mode rejection ratio	V_{icm} = 0 to V_{CC} -2 V, V_{out} = V_{CC}/2	105	130		dB
		Tmin < T < Tmax	97			
Avd	Large signal voltage gain	V_{OUT} = 0.5 to (V_{CC} -0.5 V)	105	130		dB
		Tmin < T < Tmax	96			
V_{OL}	Output swing from negative rail	T = 25 °C		30	50	mV
		Tmin < T < Tmax			80	
V_{OH}	Output swing from positive rail	T = 25 °C		20	40	
		Tmin < T < Tmax			60	
I_{OUT}	Isink	V_{OUT} connected to VCC+				mA
		T = 25 °C	20	27		
		Tmin < T < Tmax	10			
	Isource	V_{OUT} connected to VCC-				
		T = 25 °C	20	29		
		Tmin < T < Tmax	10			
I_{CC}	Supply current (per channel)	No load, V_{OUT} = V_{CC}/2		650	850	µA
		Tmin < T < Tmax			900	
		AC performance				
GBP	Gain bandwidth product	R_L = 10 kΩ, C_L = 100 pF	1.8	3		MHz
		Tmin < T < Tmax	1.6			
SR	Slew rate	T = 25 °C	0.85	2		V/µs
		Tmin < T < Tmax	0.75			
Φm	Phase margin	R_L = 10 kΩ, C_L = 100 pF		58		°
Gm	Gain margin			15		dB
En	Equivalent input noise voltage	f = 1 kHz		27		nV/√Hz
		0.1 to 10 Hz		700		nVpp

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
THD+N	Total harmonic distortion + noise	f = 1 kHz, G = 1, V_{OUT} = 1 Vpp		0.005		%
Cs	Channel separation	f = 1 kHz		130		dB
trec	Overload recovery time	G = -10		2		μs
Ts	Settling time	0.1% to final value, G = 1, 1 V step		18		μs
Cload	Capacitive load drive	No sustained oscillation		1		nF

1. *See section Section 5.4.*

Table 4. **Electrical characteristics V_{CC} = 12 V, V_{icm} = V_{CC}/2, R_L = 10 kΩ connected to V_{CC}/2 (unless otherwise specified)**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC performance						
V_{IO}	Input offset voltage	V_{icm} = V_{CC}/2				µV
		T = 25 °C	-20		+20	
		Tmin < T < Tmax	-30		+30	
		V_{icm} = 0 V				
		T = 25 °C	-20		+20	
		Tmin < T < Tmax	-30		+30	
$\|\Delta V_{IO}/\Delta T\|$	Input offset voltage drift [(1)]	Tmin < T < Tmax		25	100	nV/°C
I_{IB}	Input bias current	T = 25 °C			400	pA
		Tmin < T < Tmax			400	
I_{IO}	Input offset current	T = 25 °C			600	
		Tmin < T < Tmax			600	
CMR	Common mode rejection ratio	V_{icm} = 0 to V_{CC} - 2 V, V_{OUT} = V_{CC}/2	116	140		dB
		Tmin < T < Tmax	107			
Avd	Large signal voltage gain	V_{OUT} = 0.5 to (V_{CC} - 0.5 V)	113	135		dB
		Tmin < T < Tmax	106			
V_{OL}	Output swing from negative rail	T = 25 °C		60	90	mV
		Tmin < T < Tmax			120	
V_{OH}	Output swing from positive rail	T = 25 °C		40	70	
		Tmin < T < Tmax			90	
I_{OUT}	Isink	V_{OUT} connected to VCC+				mA
		T = 25 °C	20	26		
		Tmin < T < Tmax	10			
	Isource	V_{OUT} connected to VCC-				
		T = 25 °C	20	29		
		Tmin < T < Tmax	10			
I_{CC}	Supply current (per channel)	No load, V_{OUT} = V_{CC}/2		650	850	µA
		Tmin < T < Tmax			900	
AC performance						
GBP	Gain bandwidth product	R_L = 10 kΩ, C_L = 100 pF	1.8	3		MHz
		Tmin < T < Tmax	1.6			
SR	Slew rate	T = 25 °C	0.8	1.8		V/µs
		Tmin < T < Tmax	0.75			
Φm	Phase margin	R_L = 10 kΩ, C_L = 100 pF		55		°
Gm	Gain margin			12		dB
En	Equivalent input noise voltage	f = 1 kHz		25		nV/√Hz
		0.1 to 10 Hz		650		nVpp
THD+N	Total harmonic distortion + noise	f = 1 kHz, Gain = 1, V_{OUT} = 1 Vpp		0.004		%
Cs	Channel separation	f = 1 kHz		130		dB

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_{rec}	Overload recovery time	G = -10		1		µs
T_s	Settling time	0.1% to final value, G = 1, 10 V step		7		µs
C_{load}	Capacitive load drive	No sustained oscillation		1		nF

1. See section Section 5.4.

Table 5. Electrical characteristics V_{CC} = 36 V, V_{icm} = $V_{CC}/2$, R_L = 10 kΩ connected to $V_{CC}/2$ (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC performance						
V_{IO}	Input offset voltage	V_{icm} = $V_{CC}/2$				µV
		TSB181, T = 25 °C	-25		+25	
		TSB181, Tmin < T < Tmax	-37		+37	
		TSB182, T = 25 °C	-20		+20	
		TSB182, Tmin < T < Tmax	-30		+30	
		Vicm = 0 V				
		TSB181, T = 25 °C	-25		+25	
		TSB181, Tmin < T < Tmax	-37		+37	
		TSB182, T = 25 °C	-20		+20	
		TSB182, Tmin < T < Tmax	-30		+30	
$\|\Delta V_{IO}/\Delta T\|$	Input offset voltage drift (1)	TSB181, Tmin < T < Tmax		20	120	nV/°C
		TSB182, Tmin < T < Tmax		20	100	
I_{IB}	Input bias current	T = 25 °C			500	pA
		Tmin < T < Tmax			500	
I_{IO}	Input offset current	T = 25 °C			800	
		Tmin < T < Tmax			800	
CMR	Common mode rejection ratio	V_{icm} = 0 to V_{CC} -2 V, V_{OUT} = $V_{CC}/2$	127	150		dB
		Tmin < T < Tmax	120			
SVR	Supply voltage rejection ratio	V_{CC} = 4 to 36 V	127	138		dB
		Tmin < T < Tmax	120			
Avd	Large signal voltage gain	V_{OUT} = 0.5 to (V_{CC} -0.5 V)	124	145		dB
		Tmin < T < Tmax	115			
V_{OL}	Output swing from negative rail	T = 25 °C		140	200	mV
		Tmin < T < Tmax			270	
V_{OH}	Output swing from positive rail	T = 25 °C		130	200	
		Tmin < T < Tmax			300	
I_{OUT}	Isink	V_{OUT} connected to VCC+				mA
		T = 25 °C	20	24		
		Tmin < T < Tmax	12			
	Isource	V_{OUT} connected to VCC-				
		T = 25 °C	20	27		
		Tmin < T < Tmax	12			
I_{CC}	Supply current (per channel)	No load, V_{OUT} = $V_{CC}/2$		670	850	µA
		Tmin < T < Tmax			900	
AC performance						
GBP	Gain bandwidth product	R_L = 10 kΩ, C_L = 100 pF	1.8	3		MHz
		Tmin < T < Tmax	1.8			

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
SR	Slew rate	T = 25 °C	0.8	1.7		V/µs
		Tmin < T < Tmax	0.6			
Φm	Phase margin	R_L = 10 kΩ, C_L = 100 pF		54		°
Gm	Gain margin			11		dB
En	Equivalent input noise voltage	f = 1 kHz		24		nV/√Hz
		0.1 to 10 Hz		620		nVpp
THD+N	Total harmonic distortion + noise	f = 1 kHz, G = 1, V_{OUT} = 2 Vpp		0.002		%
C_s	Channel separation	f = 1 kHz		130		dB
t_{rec}	Overload recovery time	G = -10		1		µs
T_s	Settling time	0.1% to final value, G = 1, 10 V step		7		µs
C_{load}	Capacitive load drive	No sustained oscillation		1		nF

1. See section Section 5.4.

4 Typical performance characteristics

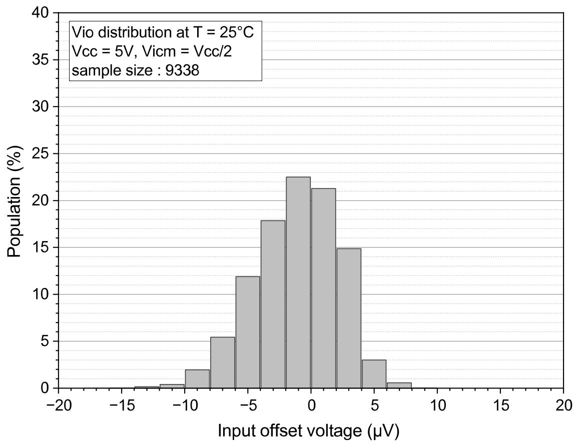


Figure 3. Input offset voltage distribution at V_{CC} = 5 V

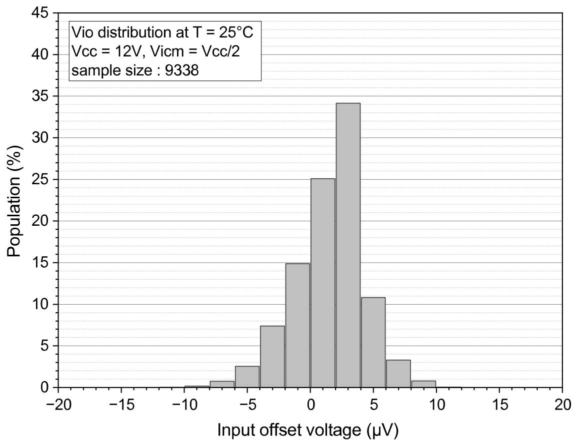


Figure 4. Input offset voltage distribution at V_{CC} = 12 V

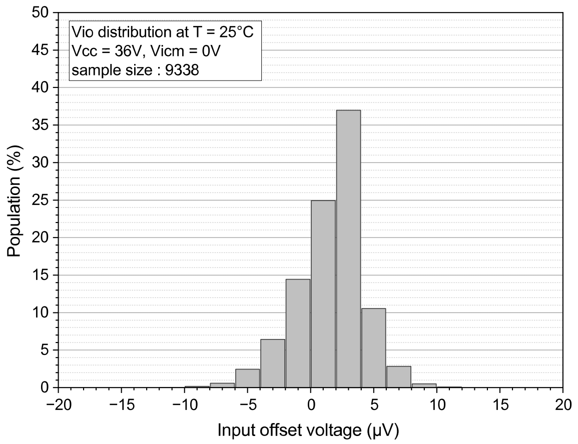


Figure 5. Input offset voltage distribution at V_{CC} = 36 V and V_{icm} = 0 V

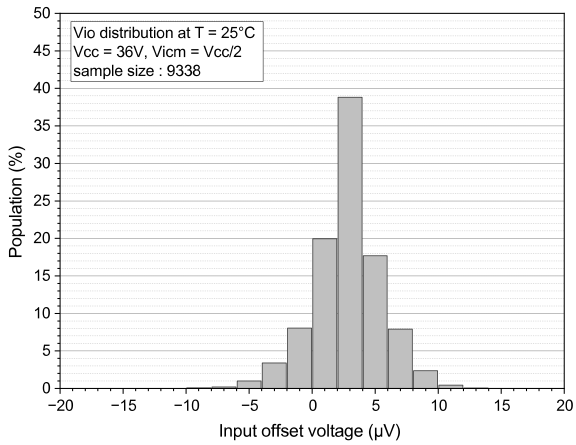


Figure 6. Input offset voltage distribution at V_{CC} = 36 V and V_{icm} = V_{CC}/2

Figure 7. Input offset voltage vs. input common mode voltage at V_{CC} = 5 V

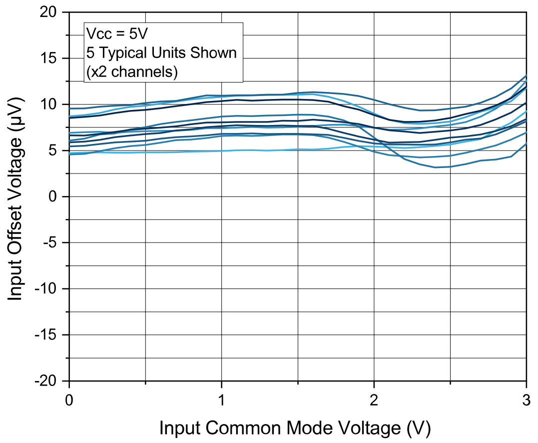


Figure 8. Input offset voltage vs. input common mode voltage at V_{CC} = 12 V

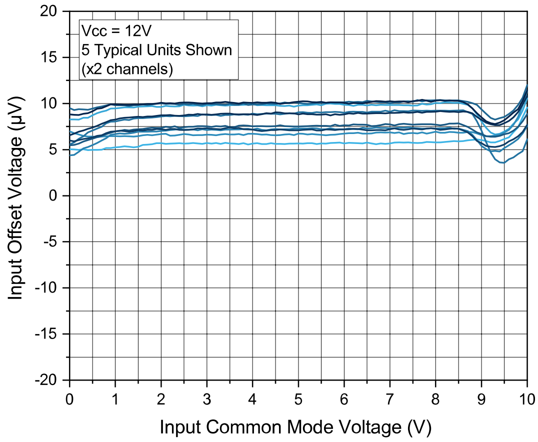


Figure 9. Input offset voltage vs. input common mode voltage at V_{CC} = 36 V

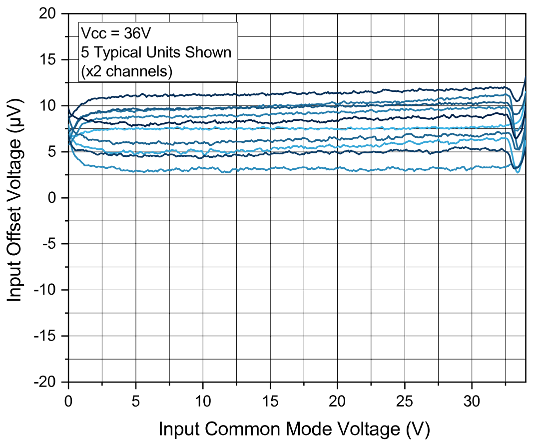


Figure 10. Input offset voltage vs. supply voltage

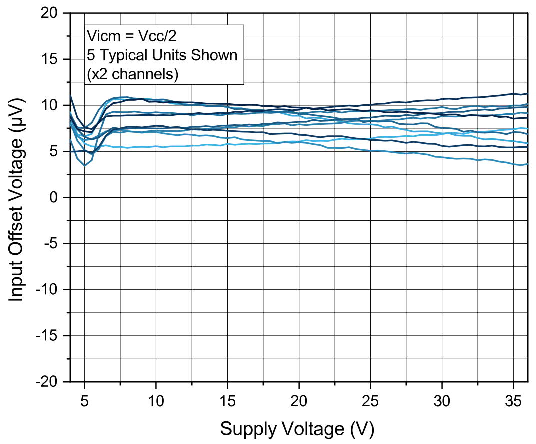


Figure 11. Input offset voltage vs. temperature

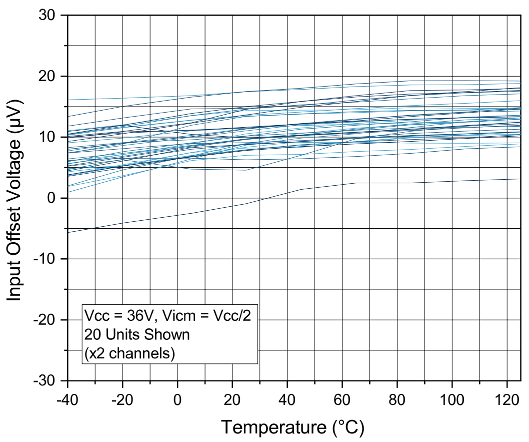
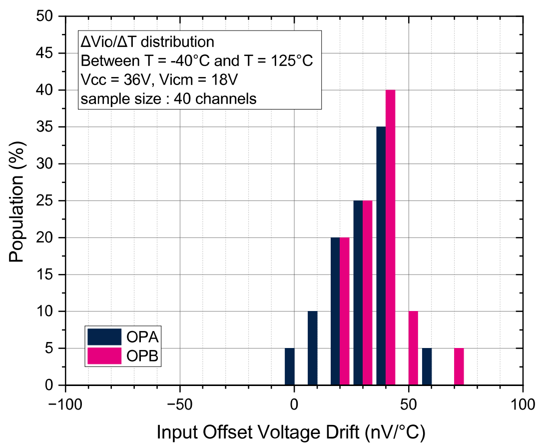


Figure 12. Input offset drift distribution



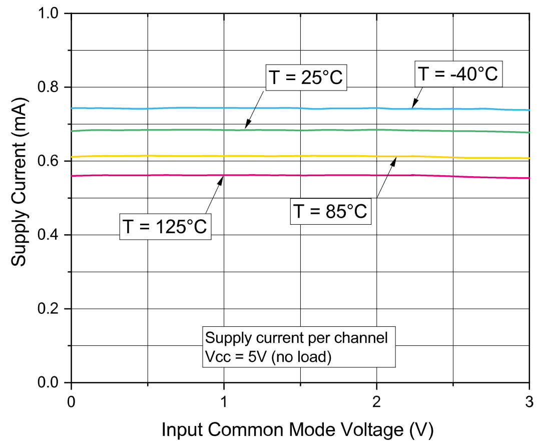


Figure 13. Supply current vs. input common mode voltage at V_{CC} = 5 V

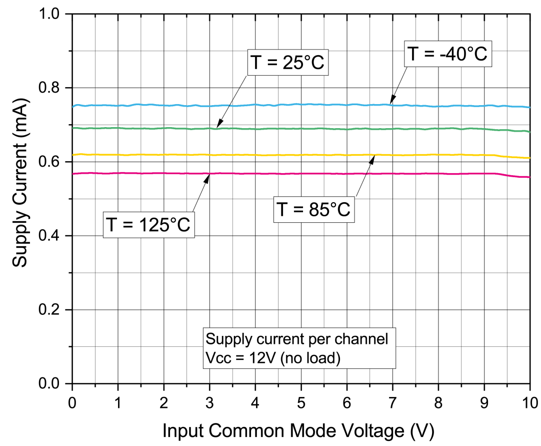


Figure 14. Supply current vs. input common mode voltage at V_{CC} = 12 V

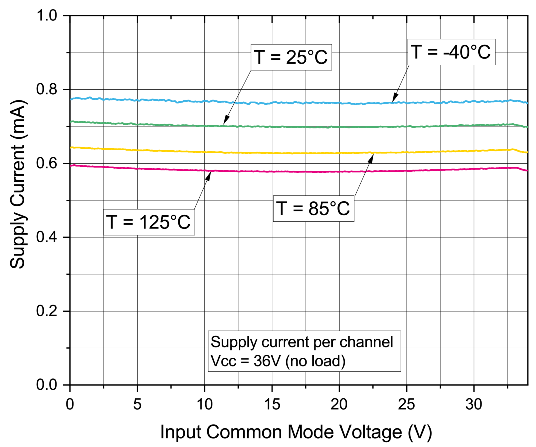


Figure 15. Supply current vs. input common mode voltage at V_{CC} = 36 V

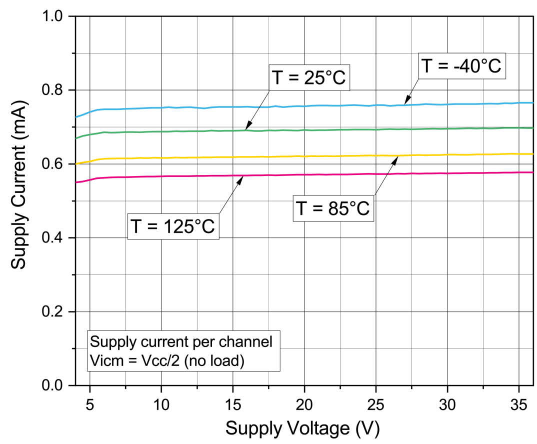


Figure 16. Supply current vs. supply voltage

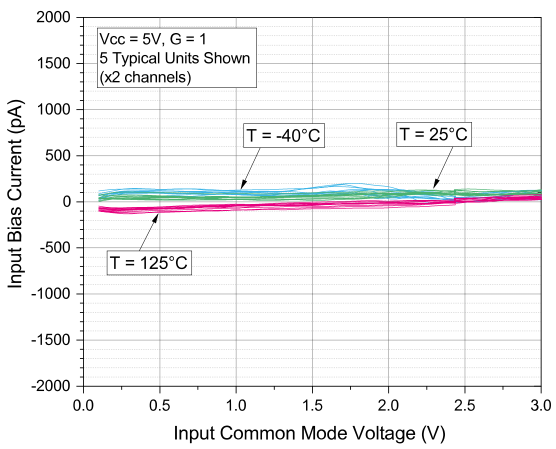


Figure 17. Input bias current vs. input common mode voltage at V_{CC} = 5 V

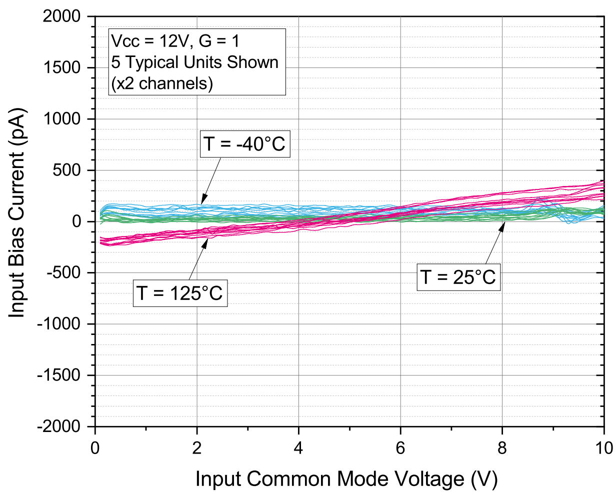


Figure 18. Input bias current vs. input common mode voltage at V_{CC} = 12 V

Figure 19. Input bias current vs. input common mode voltage at V_{CC} = 36 V

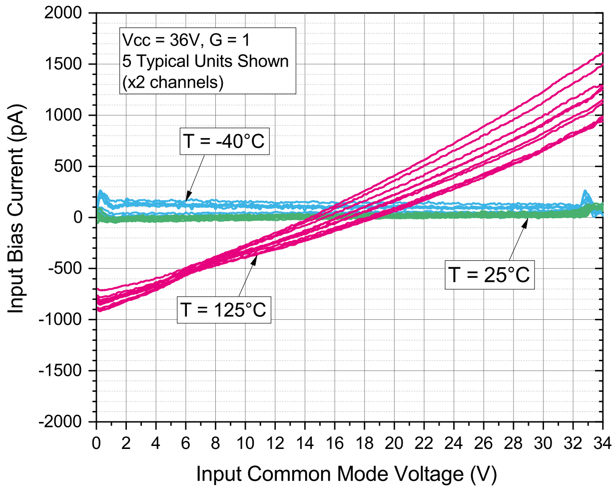


Figure 20. Output current vs. output voltage at V_{CC} = 5 V

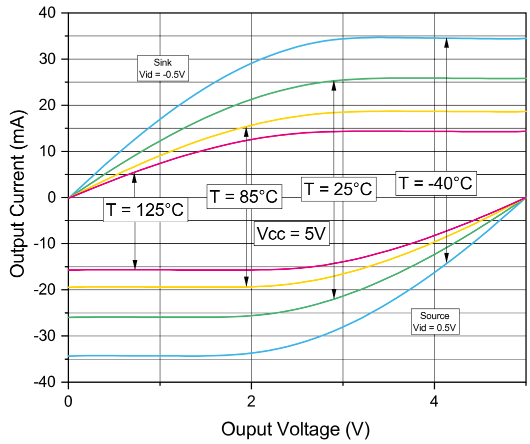


Figure 21. Output current vs. output voltage at V_{CC} = 12 V

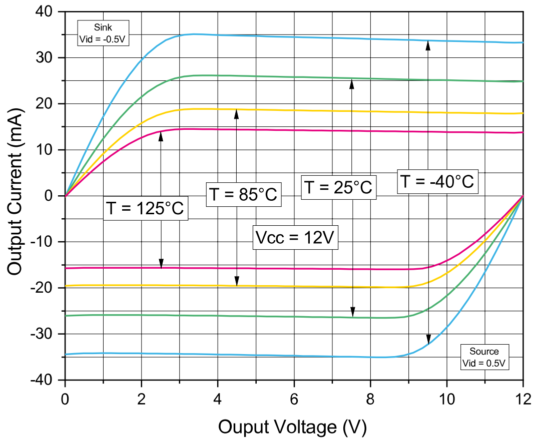


Figure 22. Output current vs. output voltage at V_{CC} = 36 V

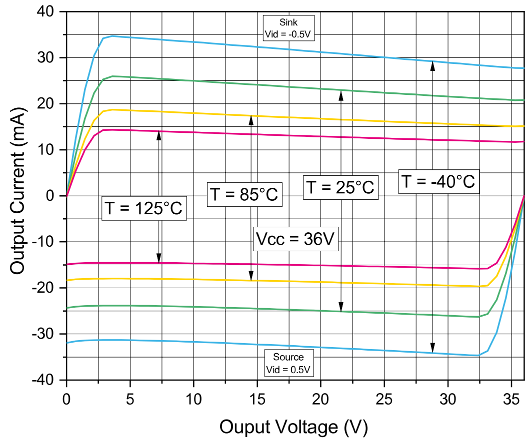


Figure 23. Output linearity at V_{CC} = 36 V

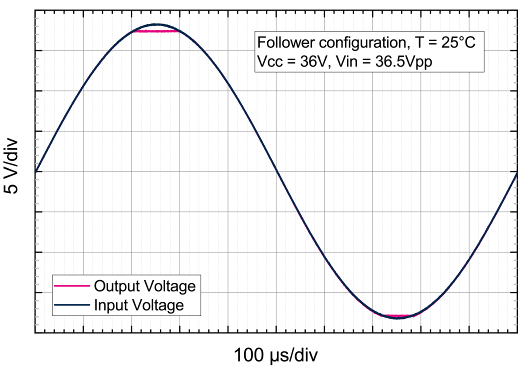


Figure 24. CMRR and PSRR vs. frequency at V_{CC} = 5 V

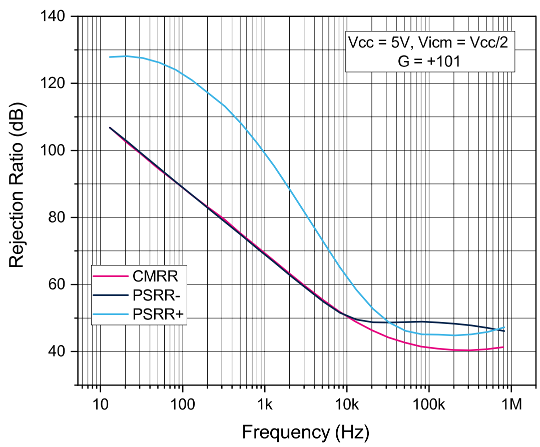


Figure 25. CMRR and PSRR vs. frequency at V_{CC} = 12 V

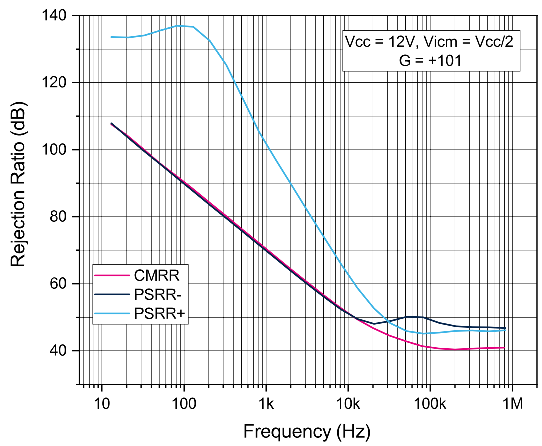


Figure 26. CMRR and PSRR vs. frequency at V_{CC} = 36 V

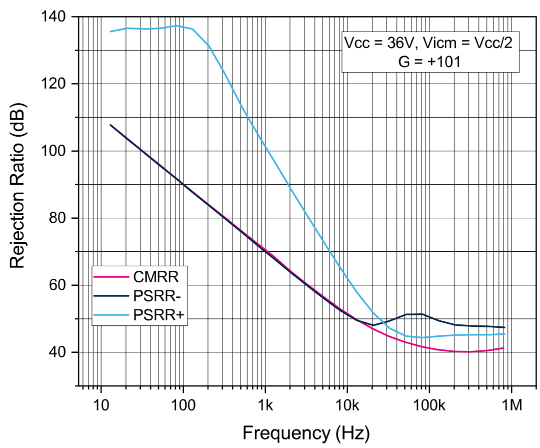


Figure 27. Bode plot at V_{CC} = 5 V

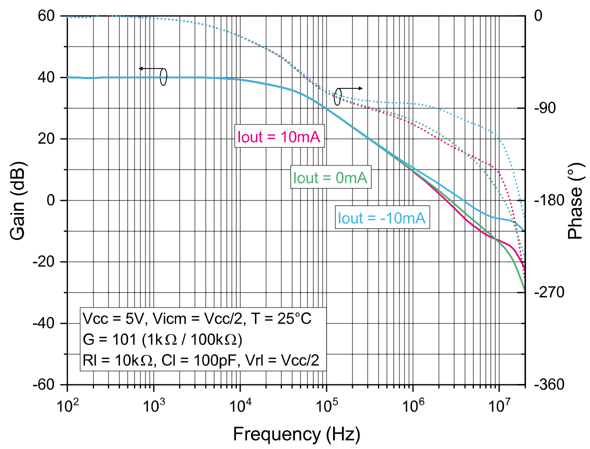


Figure 28. Bode plot at V_{CC} = 36 V

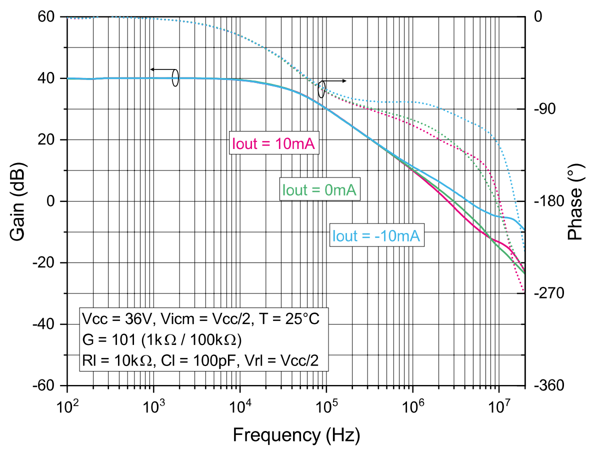


Figure 29. Slew rate vs. input common mode voltage at V_{CC} = 5 V

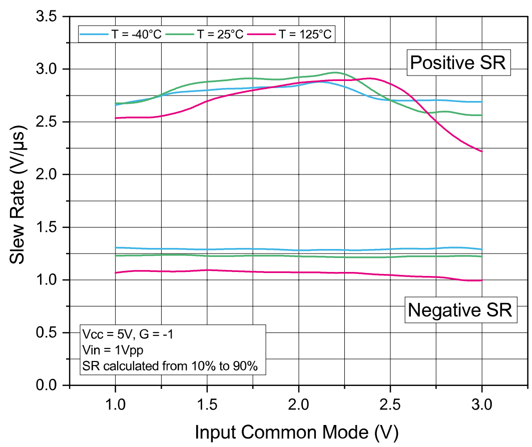


Figure 30. Slew rate vs. input common mode voltage at V_{CC} = 36 V

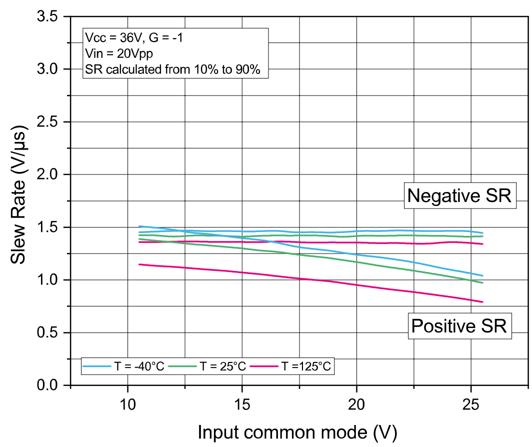


Figure 31. Output voltage vs. input voltage at V_{CC} = 5 V

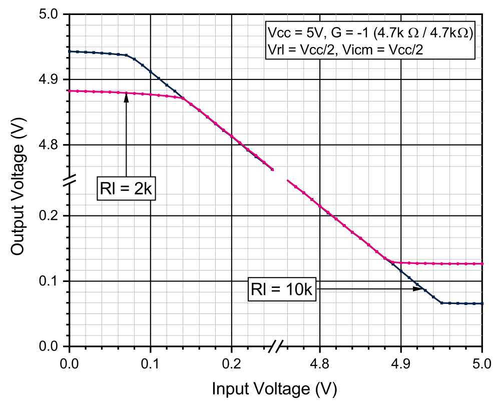


Figure 32. Output voltage vs. input voltage at V_{CC} = 36 V

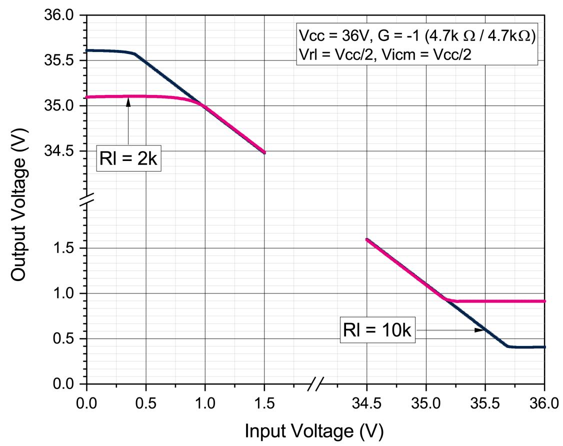


Figure 33. Output drop voltage V_{OH} vs. supply voltage

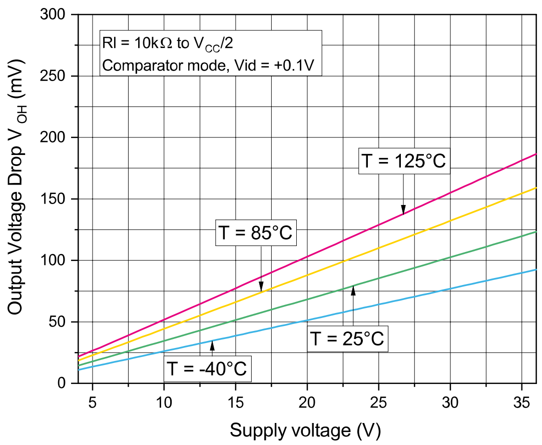


Figure 34. Output drop voltage V_{OL} vs. supply voltage

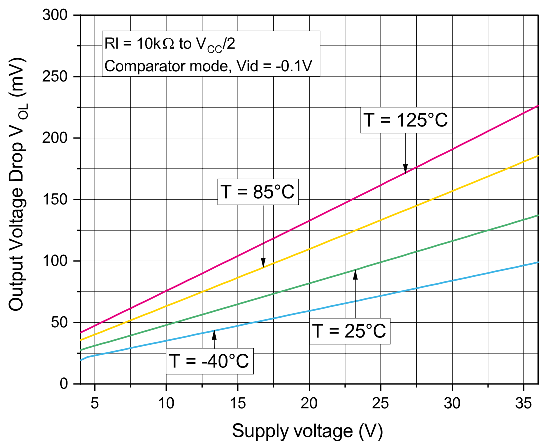


Figure 35. Noise vs. time at V_{CC} = 36 V

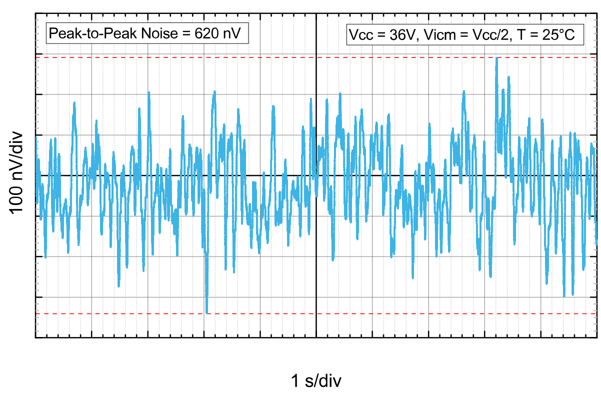
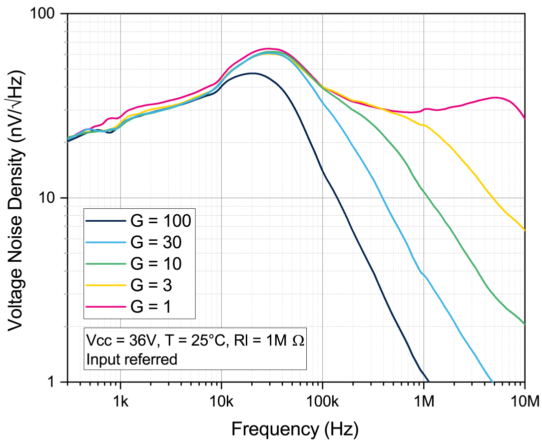


Figure 36. Voltage noise density vs. frequency



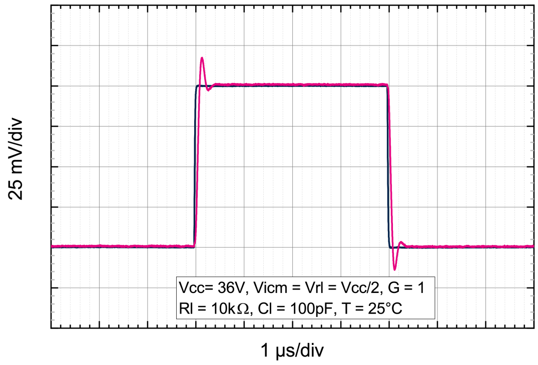


Figure 37. Small signal response at V_{CC} = 36 V

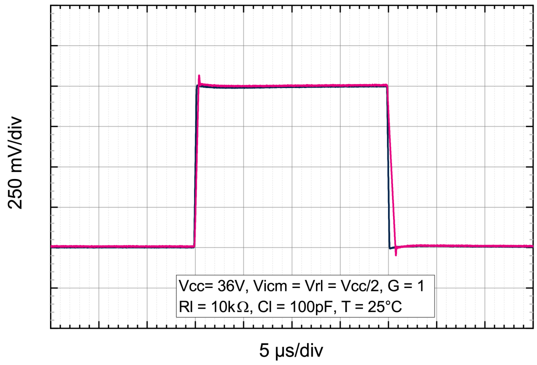


Figure 38. Large signal response at V_{CC} = 36 V

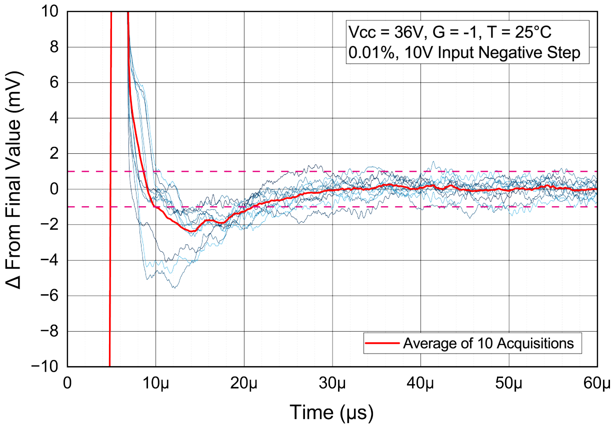


Figure 39. Settling time on negative input step

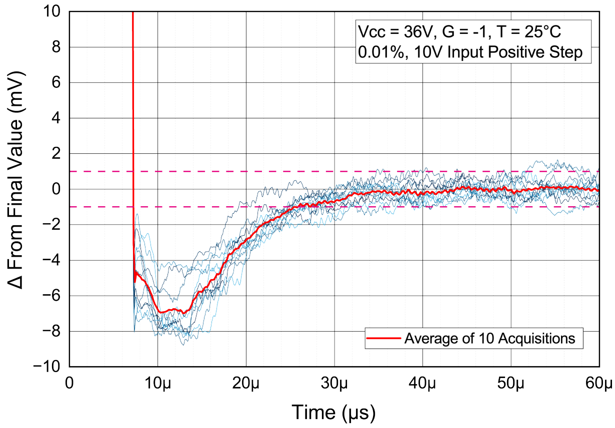


Figure 40. Settling time on positive input step

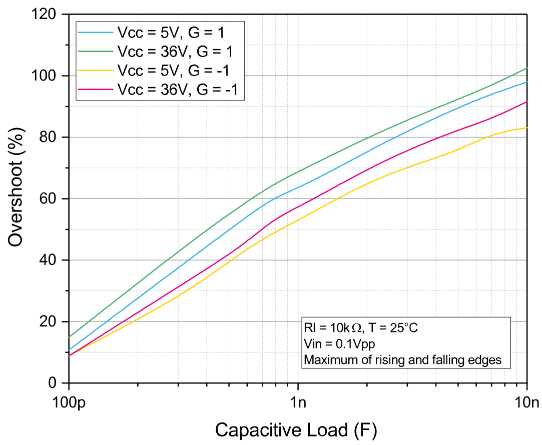


Figure 41. Small step overshoot vs. load capacitance

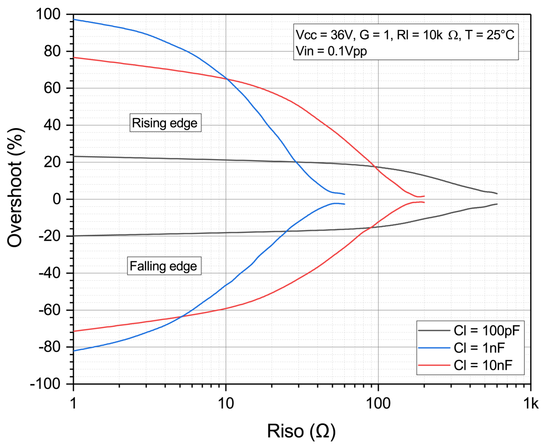


Figure 42. Small step overshoot vs. R_{iso}

Figure 43. Settling time vs. R_{iso}

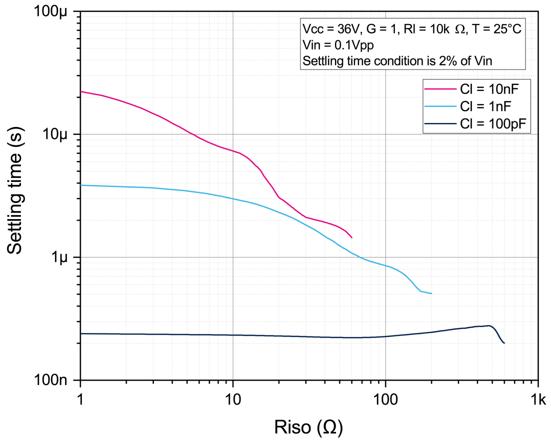


Figure 44. THD vs. frequency

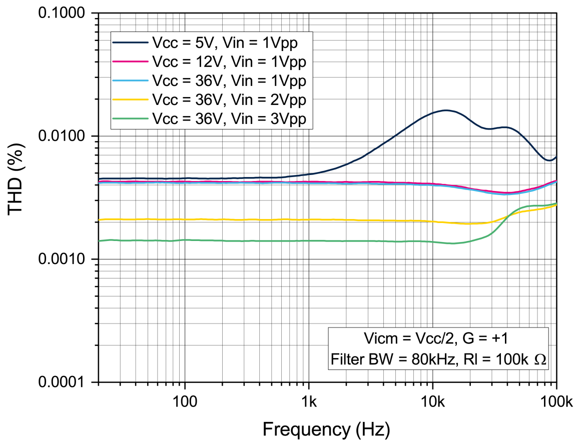


Figure 45. Channel separation vs. frequency

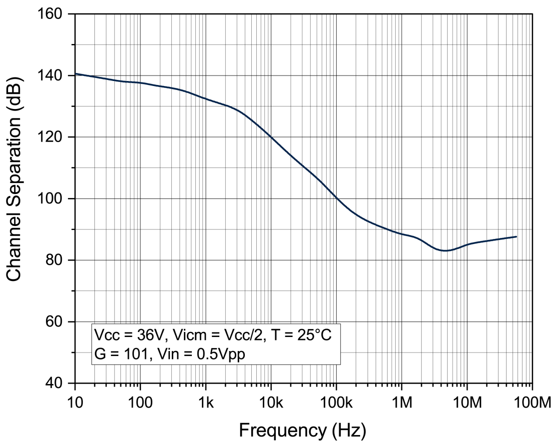


Figure 46. EMI rejection vs. frequency

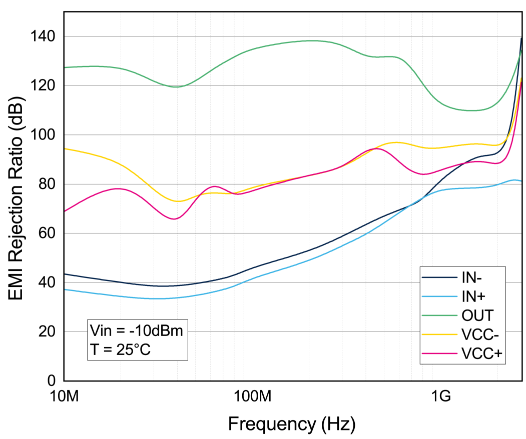


Figure 47. Positive overvoltage recovery

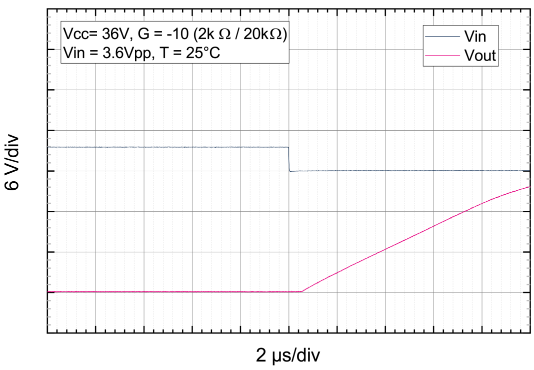


Figure 48. Negative overvoltage recovery

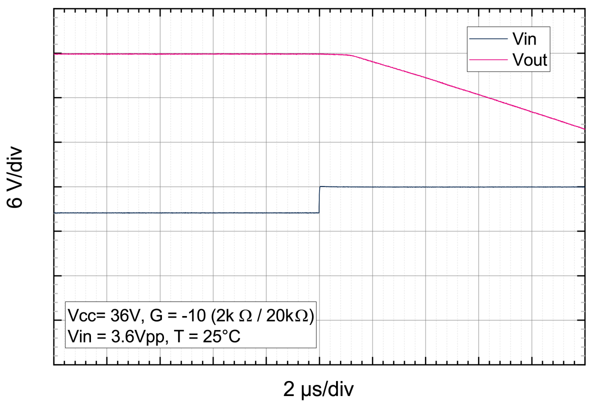
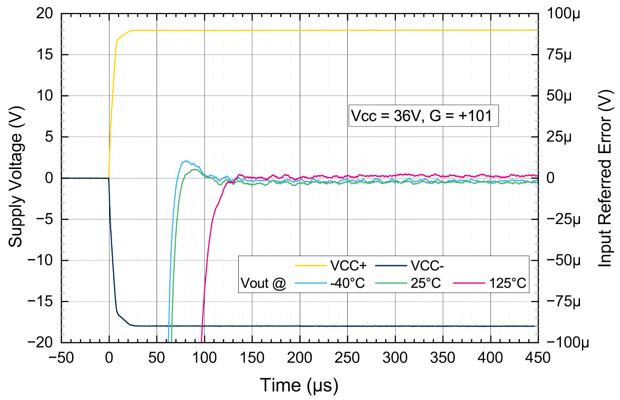


Figure 49. Startup behavior at V_{CC} = 36 V



5 Application information

5.1 Chopper operation theory

The TSB181 and TSB182 are very high precision CMOS devices. They achieve a low offset drift and no 1/f noise thanks to their chopper architecture. Chopper-stabilized amps constantly correct low-frequency errors across the inputs of the amplifier.

5.1.1 Time domain

The basis of the chopper amplifier is realized in two steps. These steps are synchronized thanks to a clock running at 400 kHz.

Figure 50. Block diagram in the time domain (step 1)

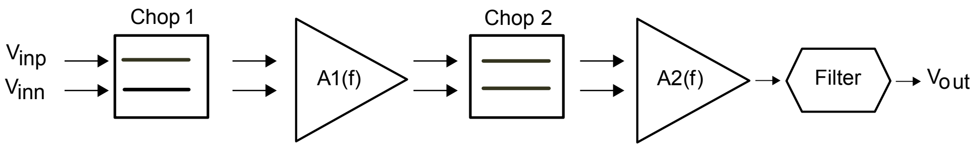


Figure 51. Block diagram in the time domain (step 2)

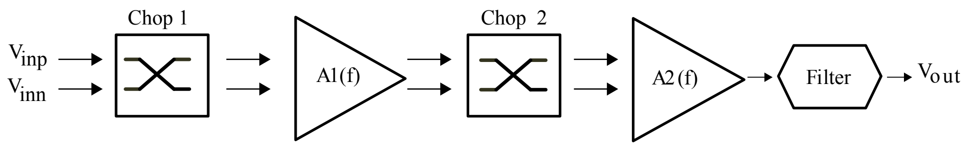


Figure 50 shows step 1, the first clock cycle, where V_{io} is amplified in the normal way.

Figure 51 shows step 2, the second clock cycle, where Chop1 and Chop2 swap paths. At this time, the V_{io} is amplified in a reverse way as compared to step 1.

At the end of these two steps, the average V_{io} is close to zero.

The A2(f) amplifier has a small impact on the V_{io} because the V_{io} is expressed as the input offset and is consequently divided by A1(f).

The averaging of the input offset could only be done by Chop2 stage, but for amplifying the input signal without distorting it, Chop1 stage is needed so that the input signal is always amplified the same way, and not alternatively up and down as per the Vio.

Here is an example of the time representation of a signal going through the system depicted by Figure 50:

Figure 52. Input differential voltage

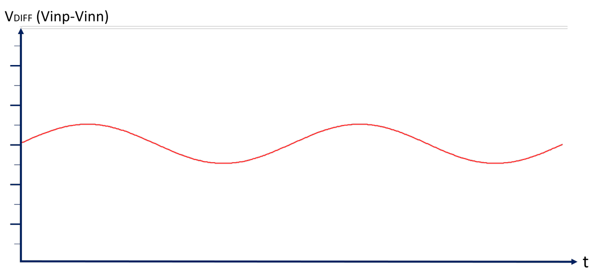


Figure 53. Chopped input diff. voltage

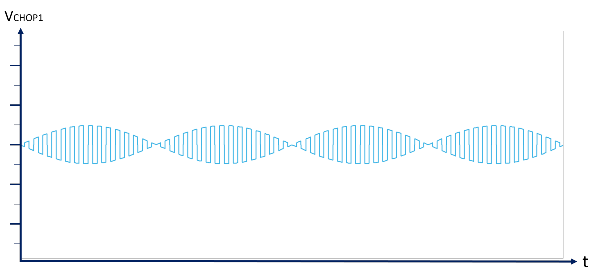


Figure 54. **A1 amplification + intrinsic offset**

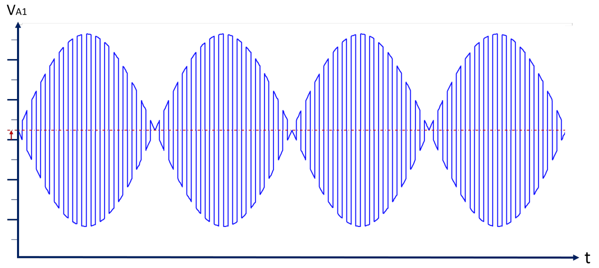
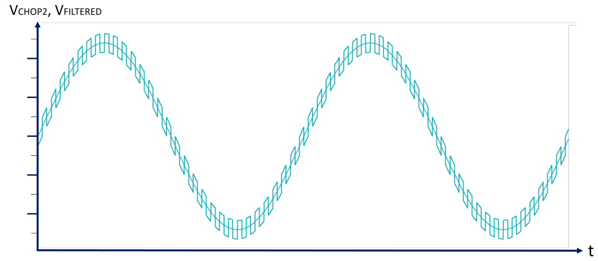


Figure 55. **Unchopped output diff. voltage + filter**



The DC offset and low-frequency noise introduced by A1 are converted to the residual square ripple seen on Figure 55. Due to many non-idealities of the notch filter and some complications in the reconstruction of the signal, the output of the TSB181, TSB182 operational amplifiers can show some of the switching characteristic of the chopping stages, including output ripple and converging steps, especially in some configurations where a fast transient is applied at the input or when driven out of saturation. These non-analog behaviors are drawbacks inherent to the chopper architecture, hence special efforts were made to reduce them as much as possible, such as lowering the output ripple down to the TSB181, TSB182 operational amplifiers' output noise level.

Figure 56. **Normalized cardinal sine**

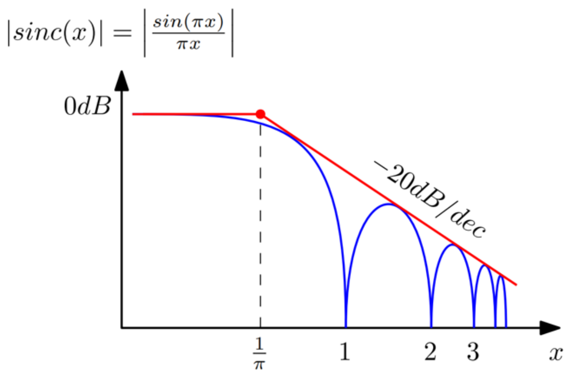
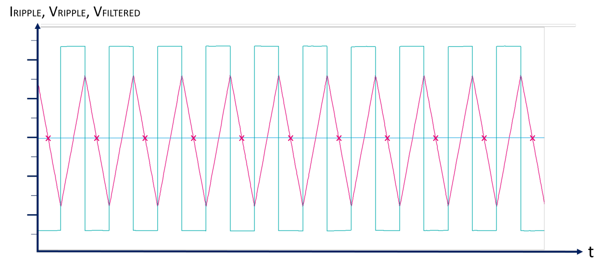


Figure 57. **Output ripple and notch sampler**



The ripple is in fact not at first visible in terms of steps but is more likely a triangular waveform, as the first amplifying stage is driving its output capacitor in current. The ripple is then reduced by a notch filter, a sample-and-hold system taking a picture of the voltage each period of the triangle wave. If tuned wisely, this notch filter can dramatically reduce the output ripple down to a very low level which is acceptable compared to the achieved V_{io} performance. This is made possible thanks to the frequency characteristics of the notch filter, totally rejecting some frequencies (in theory), as shown in Figure 56. The filter is made so that the chopping frequency and its harmonics are canceled out, thus eliminating the ripple, and removing the remaining errors that were at or close to the chopping frequency (1/f noise).

5.1.2 Frequency domain

The frequency domain gives a more accurate vision of the chopper-stabilized amplifier architecture, especially due to the chopping circuits it holds.

Figure 58. Input differential voltage

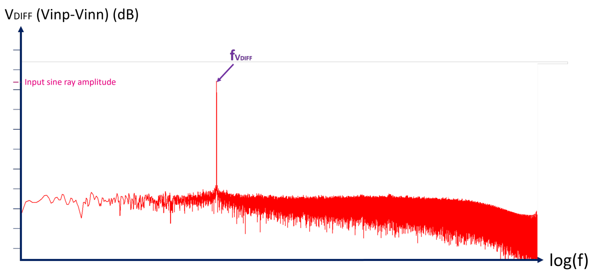


Figure 59. Chopped input diff. voltage

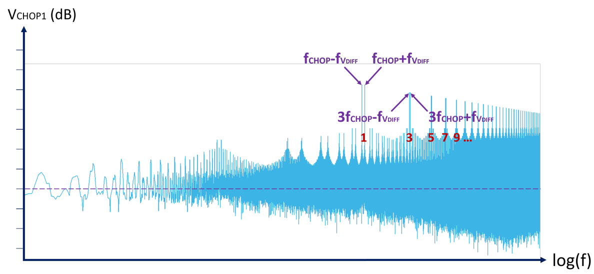


Figure 60. A1 amplification + intrinsic offset

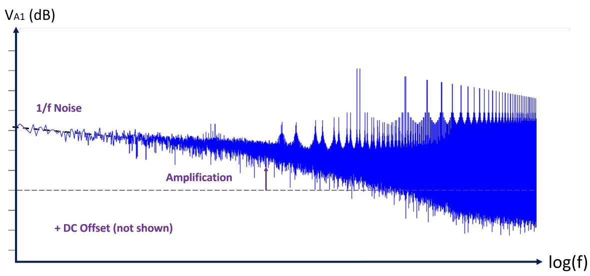
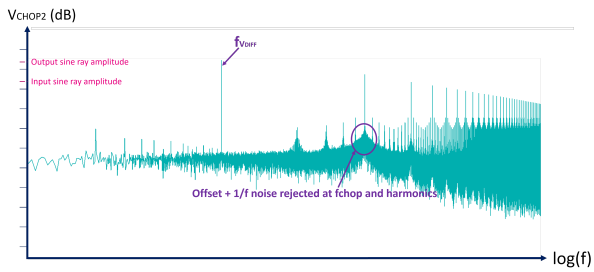


Figure 61. Unchopped output diff. voltage + filter



When chopping the input signal, its frequency gets shifted around the switching frequency of the chop switches (chopping frequency) and all its odd harmonics (frequency signature of a square signal). This enables the signal to be frequency differentiated from the errors introduced by the first amplifying stage A1 (DC offset and flicker noise).

After being amplified, the second chopper stage (Chop 2) demodulates the signal to its original frequency while shifting low frequency errors around the chopping frequency.

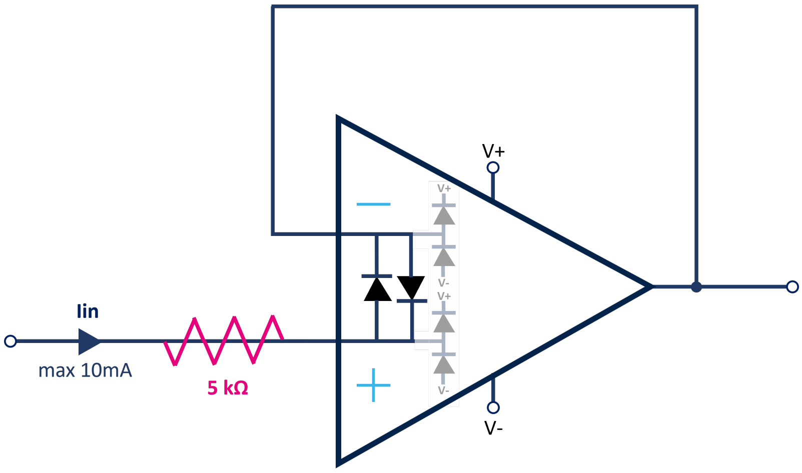
These remaining spikes are then faded out by the notch filter, removing the errors introduced by the amplifying stage.

5.2 ESD protection

Internal ESD diodes are present on every output and input pin of the TSB181, TSB182 ensuring a safe conductive path in case of electrostatic discharge. Should the voltage on the pin exceed the power supply, its ESD diode will become conductive and current will flow through it. This path is designed to resist ESD discharges, however the input pins (IN1-, IN1+, IN2-, IN2+) are not rated to support a continuous (DC) current over 10 mA. In such cases, a limiting resistor must be added to ensure that the input current absolute maximum rating (AMR) is respected.

In addition, anti-parallel diodes have been added for protecting the safe operating area of the input MOS transistors. These diodes shown on Figure 62 limit the differential input voltage to about 0.7 V. Hence, the input current shares a relation with the differential input voltage: at any time, the differential input voltage should be limited to 0.7 V or the input current to 10 mA, whichever comes first.

Figure 62. Differential anti-parallel diodes and ESD diodes



This is particularly needed when using the TSB181, TSB182 in a degraded mode as a comparator, where we recommended putting equal resistors on both inputs, sized for limiting the current below 10 mA.

This can also be needed when driving the TSB181, TSB182 with fast large signals, where the output can't respond instantaneously, creating a differential voltage the time during which the output has not yet reached the input setpoint.

Note that in follower mode, a resistor can be added either on the IN+ pin or in the feedback loop, the difference being that in the feedback loop the resistance will form an RC filter with the input capacitance that can lead to poor stability. We recommend lowering the feedback resistance as much as possible with respect to the maximum 10 mA input current compliance.

Note that differential diodes can also affect the input when short-circuit currents are reached, and the output is not able to maintain the right voltage level.

5.3 EMI filter

Electromagnetic interference (EMI) is a phenomenon where electronic devices create and are affected by electromagnetic fields. In practice, for operational amplifiers, it generally refers to radiated or conducted electromagnetic waves interfering with (for instance, adding to) the signal on one or multiple pins of the operational amplifier and affecting the performances of the operational amplifier (for instance, its input offset voltage). It creates an error on the TSB181, TSB182 output that wouldn't exist without these interferences.

This is a well-known effect, however difficult to tackle as there are many sources of electromagnetic interferences.

That is why TSB181, TSB182 come with built-in EMI filters that help to minimize the output error created by these interferences.

This sensitivity to EMI is measured from 10 MHz to 2.4 GHz and is reported on Figure 46.

For information, TSB181, TSB182 EMI filters are composed of a single RC network present on both input pins, with R = 1 kΩ and C = 1.6 pF. It creates a passive filtering with a cutoff frequency around 100 MHz, optimized for maximizing its impact on EMI rejection, and minimizing its impact on TSB182 stability and noise.

5.4 Input offset voltage drift over temperature

The operational amplifier is one of the main circuits of the signal conditioning chain, and the amplifier input offset is a major contributor to the chain accuracy.

The maximum input voltage drift variation over temperature specified in the electrical characteristics Table 3, Table 4, and Table 5 is defined as the offset variation from -40°C to 125°C.

$$\frac{\Delta V_{io}}{\Delta T} = \left(\frac{V_{io\_-40°C} - V_{io\_125°C}}{-40°C - 125°C}\right) \quad (1)$$

The datasheet maximum value is guaranteed by measurements on a representative sample size ensuring a C_{pk} (process capability index) greater than 1.3.

The value reported in the datasheet is the highest value of the |min| and |max| calculated to get this C_{pk}.

The signal chain accuracy at 25°C can be compensated during production at application level. In this case, the maximum input offset voltage drift over temperature enables the system designer to anticipate the effect of temperature variations. For this purpose can be considered the Table 6 depicting the minimum and maximum values for such drifts computed between T = (Tmin or Tmax) and T = 25°C.

Table 6. Input offset voltage drifts relative to T = 25°C for TSB182

$\frac{\Delta V_{io}}{\Delta T}$	T = -40°C to T = 25°C min / max	T = 25°C to T = 125°C min / max
V_{CC} = 5 V	-70 / 112	-38 / 114
V_{CC} = 12 V	-66 / 142	-47 / 81
V_{CC} = 36 V	-75 / 173	-39 / 89

Table 7. Input offset voltage drifts relative to T = 25 °C for TSB181

|Δ Vio/ΔT|	Package	T = -40°C to T = 25°C min/max	T = 25°C to T = 125 °C min/max
Vcc=5V	SO8	-72 / 106	-18 / 86
	SOT23-5	-74 / 135	-23 / 96
Vcc=12V	SO8	-57 / 118	-23 /65
	SOT23-5	-50 / 152	-31 / 90
Vcc=36V	SO8	-58 / 142	-18 / 68
	SOT23-5	-34 / 188	-14 / 99

The input offset drift values shown in table 7 are computed from the input offset voltage measurements at three temperatures (-40 °C, 25 °C, 125 °C) using the following equation:

$$\frac{\Delta V_{io}}{\Delta T} = \left(\frac{V_{io\_T} - V_{io\_25°C}}{T - 25°C}\right)_{T = -40°C \ or \ 125°C} \quad (2)$$

These measurements were performed on a representative sample size ensuring a C_{pk} (process capability index) greater than 1.3.

5.5 Maximum power dissipation

The usable output load current drive is limited by the maximum power dissipation allowed by the device package. The absolute maximum junction temperature for the TSB181, TSB182 is 150 °C. The junction temperature can be estimated as follows:

$$T_J = P_D \times \theta_{JA} + T_A \quad (3)$$

T_J is the die junction temperature

P_D is the power dissipated in the package

θ_{JA} is the junction to thermal resistance of the package

T_A is the ambient temperature

The power dissipated in the package P_D is the sum of the quiescent power dissipated and the power dissipated by the output stage transistor. It is calculated as follows:

$P_D = (V_{CC} \times I_{CC}) + (V_{CC+} - V_{OUT}) \times I_{OUT}$ when the op amp is sourcing the current.

$P_D = (V_{CC} \times I_{CC}) + (V_{OUT} - V_{CC-}) \times I_{OUT}$ when the op amp is sinking the current.

Do not exceed the 150 °C maximum junction temperature for the device. Exceeding the junction temperature limit can cause degradation in the parametric performance or even destroy the device.

The TSB181, TSB182 short-circuit current is designed in accordance with the bandwidth for sustaining specific capacitive or resistive loads. It is not intended for delivering its maximum output current continuously. There is no other guarantee than respecting the maximum junction temperature of the device.

5.6 Unused channel

When one of the two channels of the TSB182 is not used, it must be properly connected in order to avoid internal oscillations that can negatively impact the signal integrity on the other channel, as well as the current consumption. Two different configurations can be used:

Gain configuration: the channel can be set in gain, the input can be set to any voltage within the V_{icm} operating range.

Buffer configuration: the channel can be set in buffer configuration, with the input set to any voltage within the operating range.

Comparator configuration: the channel can be set to a comparator configuration (without feedback). In this case, positive and negative inputs can be set to any voltage provided that the current on both inputs is limited to 10 mA. The differential voltage will start activating input differential diodes (see ESD protection paragraph in Section 5.2: ESD protection) when reaching a certain threshold (about 0.7 V, can vary in temperature) and must be significantly greater than the input-referred noise (we recommend 100 mV) for ensuring a stable output state.

5.7 PCB layout recommendations

Particular attention must be paid to the layout of the PCB tracks connected to the amplifier, load and power supply. It is good practice to use short and wide PCB traces to minimize voltage drops and parasitic inductance.

To minimize parasitic impedance over the entire surface, a multi-via technique that connects the bottom and top layer ground planes together in many locations is often used.

The copper traces that connect the output pins to the load and supply pins should be as wide as possible to minimize trace resistance.

A ground plane generally helps to reduce EMI, which is why it is generally recommended to use a multilayer PCB and use the ground plane as a shield to protect the internal track. In this case, pay attention to separate the digital from the analog ground and avoid any ground loop.

Place external components as close as possible to the op amp and keep the gain resistances, R_f and R_g, close to the inverting pin to minimize parasitic capacitances.

5.8 Optimized application recommendation

The TSB181, TSB182 is based on a chopper architecture. As the device includes internal switching circuitry, it is strongly recommended to place a 0.1 μF capacitor as close as possible to the supply pins.

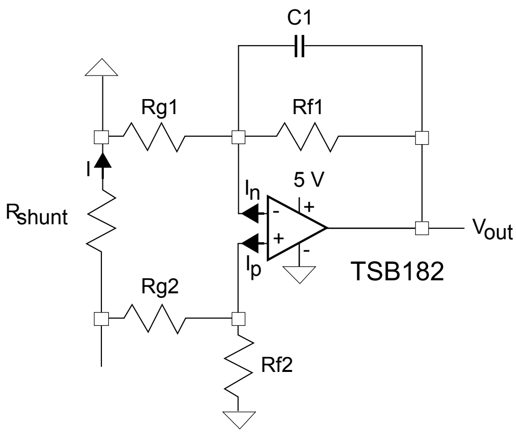
A good decoupling has several advantages for an application. First, it helps to reduce electromagnetic interference. Due to the modulation of the chopper, the decoupling capacitance also helps to reject the small ripple that may appear on the output.

5.9 Basic applications

Low-side current sensing schematic

Power management mechanisms are found in most electronic systems. Current sensing is useful for protecting applications. The low-side current sensing method consists of placing a sense resistor between the load and the circuit ground. The resulting voltage drop is amplified using the TSB182 (see Figure 63).

Figure 63. Low-side current sensing schematic



V_{out} can be expressed as follows:

$$V_{out} = R_{shunt} \times I\left(1 - \frac{R_{g2}}{R_{g2} + R_{f2}}\right)\left(1 + \frac{R_{f1}}{R_{g1}}\right) - V_{io}\left(1 + \frac{R_{f1}}{R_{g1}}\right) \quad (4)$$

Assuming that $R_{f2} = R_{f1} = R_f$ and $R_{g2} = R_{g1} = R_g$, Equation 3 can be simplified as follows:

$$V_{out} = R_{shunt} \times I\left(\frac{R_f}{R_g}\right) - V_{io}\left(1 + \frac{R_f}{R_g}\right) \quad (5)$$

Using the TSB182 operational amplifier for low-side current sensing minimizes the error due to V_{IO} and enables a measurement with better accuracy.

Therefore, for the same accuracy, the shunt resistor can be chosen with a lower value, resulting in lower power dissipation, lower drop in the ground path, and lower cost.

Particular attention must be paid to the matching and precision of R_{g1}, R_{g2}, R_{f1}, and R_{f2}, to maximize the accuracy of the measurement.

The circuit gain must be chosen in line with the minimum operational shunt current and the TSB182 open loop gain above output saturation.

6 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

6.1 SOT23-5 package information

Figure 64. SOT23-5 package outline

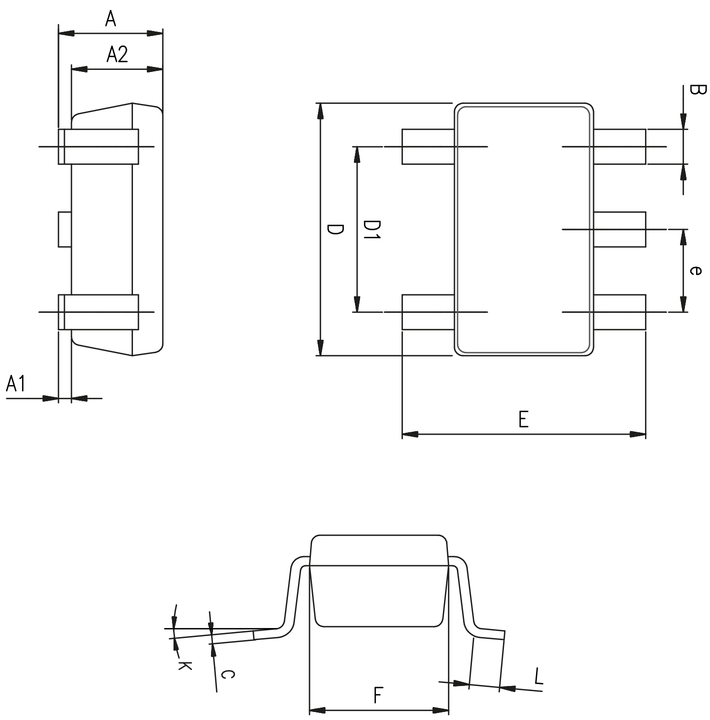


Table 8. SOT23-5 mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.90	1.20	1.45	0.035	0.047	0.057
A1			0.15			0.006
A2	0.90	1.05	1.30	0.035	0.041	0.051
B	0.35	0.40	0.50	0.014	0.016	0.020
C	0.09	0.15	0.20	0.004	0.006	0.008
D	2.80	2.90	3.00	0.110	0.114	0.118
D1		1.90			0.075	
e		0.95			0.037	
E	2.60	2.80	3.00	0.102	0.110	0.118
F	1.50	1.60	1.75	0.059	0.063	0.069
L	0.10	0.35	0.60	0.004	0.014	0.024
K	0 degrees		10 degrees	0 degrees		10 degrees

6.2 SO8 package information

Figure 65. **SO8 package outline**

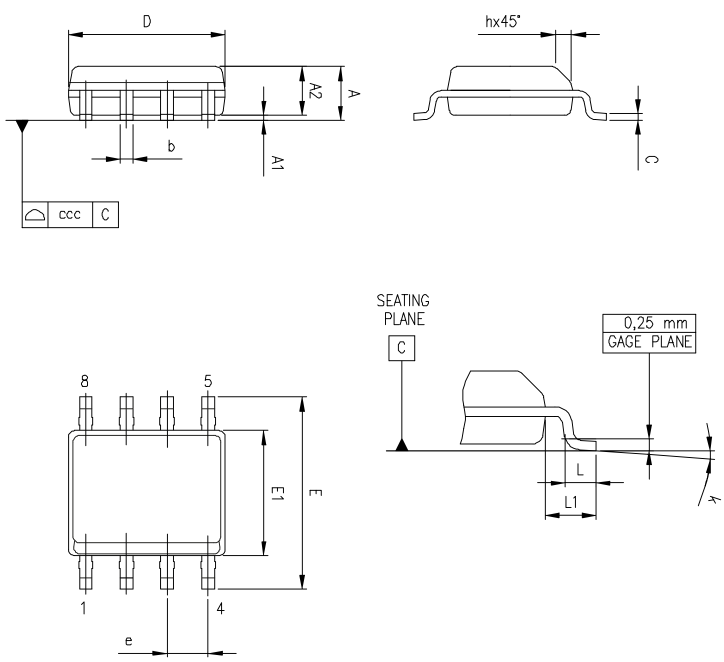


Table 9. **SO-8 mechanical data**

Dim.	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.069
A1	0.1		0.25	0.004		0.01
A2	1.25			0.049		
b	0.28		0.48	0.011		0.019
c	0.17		0.23	0.007		0.01
D	4.8	4.9	5	0.189	0.193	0.197
E	5.8	6	6.2	0.228	0.236	0.244
E1	3.8	3.9	4	0.15	0.154	0.157
e		1.27			0.05	
h	0.25		0.5	0.01		0.02
L	0.4		1.27	0.016		0.05
L1		1.04			0.04	
k	0		8 °	1 °		8 °
ccc			0.1			0.004

6.3 MiniSO8 package information

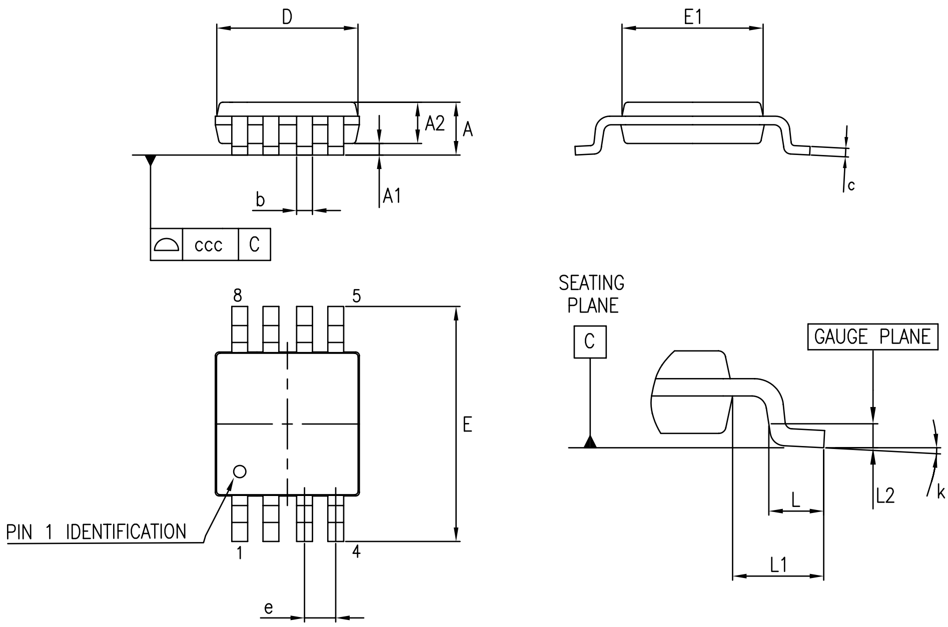


Figure 66. MiniSO8 package outline

Table 10. MiniSO8 mechanical data

Dim.	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.1			0.043
A1	0		0.15	0		0.006
A2	0.75	0.85	0.95	0.03	0.033	0.037
b	0.22		0.4	0.009		0.016
c	0.08		0.23	0.003		0.009
D	2.8	3	3.2	0.11	0.118	0.126
E	4.65	4.9	5.15	0.183	0.193	0.203
E1	2.8	3	3.1	0.11	0.118	0.122
e		0.65			0.026	
L	0.4	0.6	0.8	0.016	0.024	0.031
L1		0.95			0.037	
L2		0.25			0.01	
k	0°		8°	0°		8°
ccc			0.1			0.004

7 Ordering information

Table 11. **Order code**

Order code	Package	Packaging	Marking
TSB181ILT	SOT23-5	Tape & Reel	K243
TSB181IYLT (1)			K244
TSB181IDT	SO8		TSB181I
TSB181IYDT (1)			TSB181IY
TSB182IDT			TSB182I
TSB182IYDT (1)			TSB182IY
TSB182IST	MiniSO8		K238
TSB182IYST (1)			K239

1. *Qualified and characterized according to AEC Q100 and Q003 or equivalent, advanced screening according to AEC Q001 & Q002 or equivalent.*

Revision history

Table 12. Document revision history

Date	Revision	Changes
07-Jul-2023	1	Initial release.
20-Sep-2023	2	Minor text changes.
24-Jan-2024	3	Added $\|\Delta V_{IO}/\Delta T\|$ condition in Table 4, Table 5, Table 6 and new section Section 5: Application information.
12-Mar-2024	4	Minor text changes in Section 5.1.1.
07-Nov-2024	5	Added new TSB181 part number, new package SOT23-5, Figure 1 and Section 6.1: SOT23-5 package information. Updated Section 5.4 and Ordering information.

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