

# FUSB308B

## USB Type-C Port Controller with USB-PD

### Description

The FUSB308B targets system designers looking to implement up to four USB Type-C port controllers (TCPC) with USB-PD capabilities.

This solution provides integrated Type-C Rev 1.3 detection circuitry enabling manual attach/detach detection. Time critical Power Delivery functionality is handled autonomously, offloading the  $\mu$ Processor or Type-C Port Manager (TCPM).

The FUSB308B complies with the USB-PD Interface Specification Rev 1.0 as a TCPC for a standardized interface with TCPM.

### Features

- USB-PD Interface Specification Rev 1.0 Ver. 1.2 Compatible
- USB Type-C Rev 1.3 Compatible
- USB-PD Rev3.0 Ver. 1.2 Compatible
- Sink Transmit
- Extended Data Messages (Chunked)
- Dual-Role Functionality
  - ◆ Manual Type-C Detection
  - ◆ Automatic DRP Toggling
- USB-PD Interface Specification Support
  - ◆ Automatic GoodCRC Packet Response
  - ◆ Automatic Retries of Sending Packet
  - ◆ All SOP\* Types Supported
- 2 VBUS Sources Control
- Integrated 3 W Capable VCONN to CCx Switch
- 10-bit VBUS ADC
- Programmable GPIOs
- 4 Selectable I<sup>2</sup>C Addresses
- Packaging: 16 Pin QFN

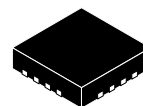
### Applications

- Desktops
- Wall Adapters
- Automotive



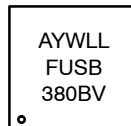
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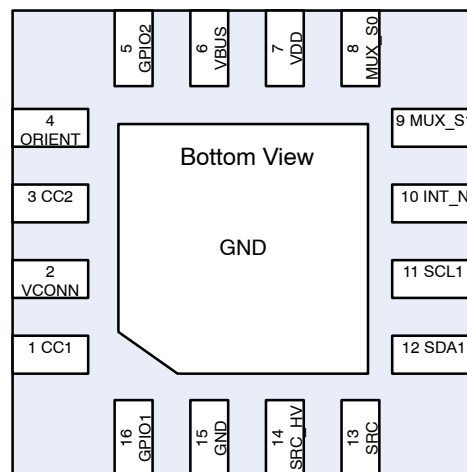
WQFN16 3 x 3, 0.5P  
CASE 510BS

### MARKING DIAGRAM



- A = Assembly Location
- Y = Year
- W = Work Week
- LL = Assembly Lot Code

### PIN ASSIGNMENT



QFN16

### ORDERING INFORMATION

See detailed ordering and shipping information on page 3 of this data sheet.

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Block Diagram

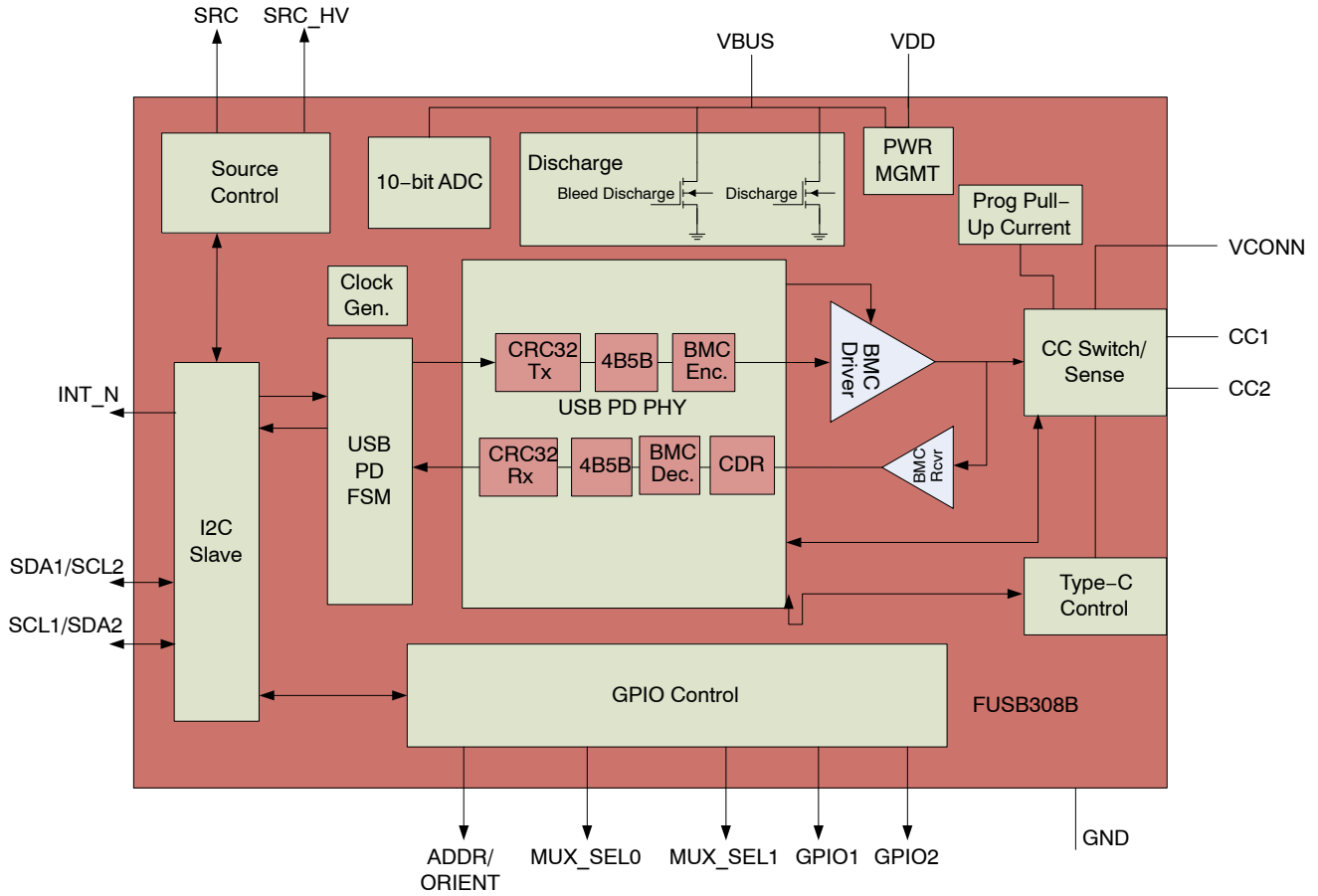


Figure 2. FUSB308B Block Diagram

Pin Configurations

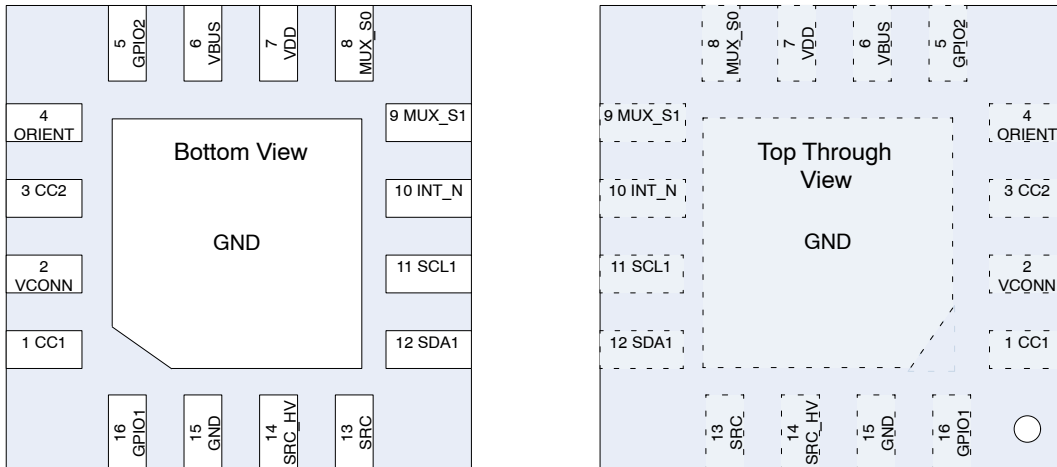


Figure 3. Pin Assignment QFN (FUSB308B)

## Pin Descriptions

Table 2. PIN DESCRIPTION

Name	Type	Description
<b>USB TYPE-C CONNECTOR INTERFACE</b>		
CC1	I/O	Type-C connector Configuration Channel (CC) pins. Initially used to determine when an attach has occurred and what the orientation of the insertion is. Functionality after attach depends on mode of operation detected. Operating as a host: – Sets the allowable charging current for VBUS to be sensed by the attached device
CC2	I/O	– Used to communicate with devices using USB BMC Power Delivery – Used to detect when a detach has occurred Operating as a device: – Indicates what the allowable sink current is from the attached host – Used to communicate with devices using USB BMC Power Delivery
GND	Ground	Ground
VBUS	Power	VBUS supply pin for attach and detach detection when operating as an upstream facing port (Device)
<b>POWER INTERFACE</b>		
VDD	Power	Input supply voltage
GPIO2	3-State CMOS I/O	General Purpose I/O
VCONN	Power Switch	Regulated input to be switched to correct CC pin as VCONN to power USB3.1 fully featured cables, powered accessories or dongles bridging Type C to other video or audio connectors
<b>SIGNAL INTERFACE</b>		
SCL1/SDA2 (Note 1)	Open-Drain I/O	I <sup>2</sup> C serial clock/data signal to be connected to the I <sup>2</sup> C master
SDA1/SCL2 (Note 1)	Open-Drain I/O	I <sup>2</sup> C serial clock/data signal to be connected to the I <sup>2</sup> C master
INT_N	Open-Drain Output	Active LOW open drain interrupt output used to prompt the processor to read the I <sup>2</sup> C register bits
ORIENT/I2C_ADDR (Note 1)	3-State CMOS Output	Selects I <sup>2</sup> C Address on Power up and then becomes a General Purpose CMOS Output
MUX_SEL0	3-State CMOS Output	MUX Selection Output 0
MUX_SEL1	3-State CMOS I/O	MUX Selection Output 1
GPIO1	3-State CMOS I/O	General Purpose I/O
<b>VBUS SOURCE INTERFACE</b>		
SRC_HV	CMOS Output	Controls High Voltage Source Path Load Switch (Active High)
SRC	CMOS Output	Controls external VBUS Source Load Switch on/off. (Active High)

1. A different I2C address is used depending on which SDA and SCL are used and the state of ORIENT/I2C\_ADDR at power up.

**Power Up, Initialization and Reset**

When power is first applied to VDD or VBUS, the FUSB308B goes through its POR sequence to load up all the default values in the register map, read all the fuses so that the trimmed values are available when VDD or VBUS is in its valid range. A software reset can be executed by writing SW\_RES to 1 in RESET Register.

This executes a full reset of the FUSB308B similar to POR where all the I2C registers go to their default state.

When powered down, the FUSB308B will present an Open on both CC lines.

The FUSB308B will present Rp, ROLECTRL= 0x05 when VDD is present

**Programmable GPIOx**

The FUSB308B has two programmable GPIOs. These can be programmed to be Inputs, CMOS Outputs or Open Drain Outputs. To configure them, the TCPM writes to GPIO1\_CFG and GPIO2\_CFG. If the GPIO is configured as an input, its logic value can be read in GPIO\_STAT and ALERT\_VD registers.

**Standard Outputs**

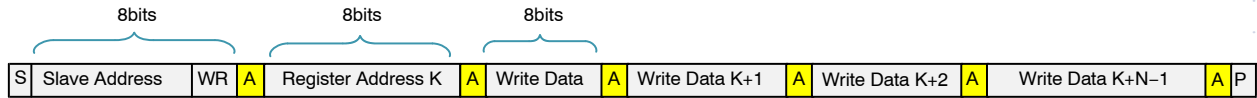
The FUSB308B implements the Orientation and DP Mux Selection Standard Outputs as indicated in STD\_OUT\_CAP register.

To configure the Orientation, and Mux selection, the TPCM writes to STD\_OUT\_CFG.

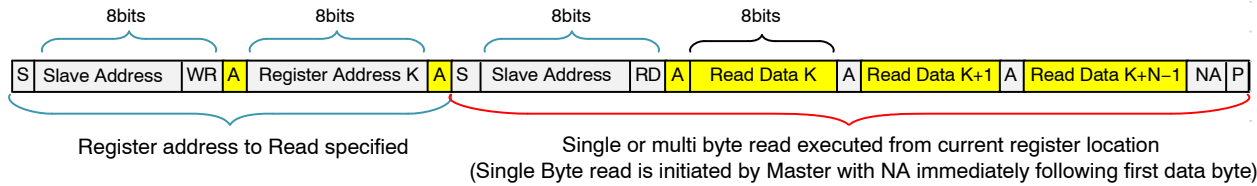
**I<sup>2</sup>C Interface**

The FUSB308B includes a full I<sup>2</sup>C slave controller. The I<sup>2</sup>C slave fully complies with the I<sup>2</sup>C specification version 6 requirements. This block is designed for fast mode plus signals.

Examples of an I<sup>2</sup>C write and read sequence are shown in Figure 4 and Figure 5 respectively.



**Figure 4. I2C Write Example**



NOTE: If Register is not specified Master will begin read from current register. In this case only sequence showing in Red bracket is needed.

	From Master to Slave	<b>S</b>	Start Condition	<b>NA</b>	NOT Acknowledge (SDA High)	<b>RD</b>	Read =1
	From Slave to Master	<b>A</b>	Acknowledge (SDA Low)	<b>WR</b>	Write = 0	<b>P</b>	Stop Condition

**Figure 5. I2C Read Example**

**I<sup>2</sup>C Address Selection**

I<sup>2</sup>C Slave addresses can be changed by configuring the I2C\_ADDR\_GPO input on power up with a pull-up or pull-down resistor and routing the SCL and SDA lines according to Table 3.

**Interrupt Operation**

The INT\_N pin is an active low, open drain output which indicates to the host processor that an interrupt has occurred in the FUSB308B which needs attention. The INT\_N pin is asserted after power-up or device reset RESET.SW\_RES

set to 1b (due to ALERTLI\_PORT\_PWR and PWRSTAT.TCPC\_INIT).

When an interruptible event occurs, INT\_N is driven low and is high-Z again when the processor clears the interrupt by writing a 1 to the corresponding interrupt bit position. Writing a 0 to an interrupt bit has no effect.

A processor firmware has additional control of INT\_N through individual event mask bits which can be set or cleared to enable or disable INT\_N from being driven low when each event occurs.

**Table 3. I<sup>2</sup>C ADDRESSES**

I2C_ADDR	SCLx/SDAx	Slave Address							
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	SCL1/SDA1	1	0	1	0	0	0	0	R/W
1	SCL1/SDA1	1	0	1	0	0	0	1	R/W
0	SCL2/SDA2	1	0	1	0	0	1	0	R/W
1	SCL2/SDA2	1	0	1	0	0	1	1	R/W

## I<sup>2</sup>C Idle Mode

### Entering I<sup>2</sup>C Idle Mode

The FUSB308B does not need to enter I<sup>2</sup>C Idle Mode in order to save power. Entering this mode has no effect on I<sup>2</sup>C function. The FUSB308B can enter idle mode if 0xFF is written to the COMMAND register. Once in Idle mode, the FUSB308B will not set the PWRSTAT.TCPC\_INIT to one.

### Exiting I<sup>2</sup>C Idle Mode

The FUSB308B will exit I<sup>2</sup>C Idle mode when any I<sup>2</sup>C communication is addressed to the slave. The ALERTL.I\_PRT\_PWR interrupt will be set and no PWRSTAT bits will be set.

The device's I<sup>2</sup>C block is always on without power penalties.

### VCONN Control

The FUSB308B integrates a CCx to VCONN switch with programmable OCP capability via the VCONN\_OCP register. If PWRCTRL.VCONN\_PWR is set to 0, the standard VCONN current limit is used (210.5 mA). If PWRCTRL.VCONN\_PWR is set to 1, the programmable VCONN\_OCP is used.

The VCONN switch can be enabled via the PWRCTRL register bits EN\_VCONN and TCPC\_CTRL.ORIENT bits (for CC1/2 selection).

A VCONN valid voltage is monitored and reported on PWRSTAT.VCONN\_VAL. The valid voltage threshold is fixed at 2.4 V.

### Type-C Manual Mode Detection

The CC pull up (Rp) or pull down (Rd) resistors and DRP toggle are setup via the ROLECTRL register. If a TCPM wishes to control Rp/Rd directly, it can write ROLECTRL.DRP = 0b and the desired ROLECTRL bits [3:0] (CC1/CC2).

The FUSB308B can autonomously toggle the Rp/Rd by setting ROLECTRL.DRP = 1b and the starting value of Rp/Rd in ROLECTRL.bits [3:0]. DRP toggling starts by writing to the COMMAND register

If ROLECTRL.DRP = 1b, the only allowed values for CC1/CC2 in ROLECTRL bits [3:0] are Rp/Rp or Rd/Rd.

When ROLECTRL bits 3:0 are set to Open and ROLECTRL.DRP = 0b, the PHY and CC comparators are powered down.

The FUSB308B updates the CCSTAT register on a Connect, Disconnect, a change in ROLECTRL.DRP or a change (tTCPCFilter debounced) on the CC1 or CC2 wire.

The TCPM reads CCSTAT upon detecting an interrupt and seeing the ALERTL.I\_CCSTAT = 1. The FUSB308B indicates the DRP status, the DRP result, and the current CC status in this register.

The FUSB308B will set CCSTAT.LOOK4CON = 0b when it has stopped toggling as a DRP.

The TCPM reads the CCSTAT.LOOK4CON to determine if the FUSB308B is toggling Rp/Rd when operating as a DRP, it then reads CCSTAT.CON\_RES to determine if the FUSB308B is presenting an Rp or Rd and read the CCSTAT.CC1\_STAT and CCSTAT.CC2\_STAT to determine the CC1 and CC2 states.

The FUSB308B debounces the CC lines for tTCPCFilter before reporting the status on CCSTAT. The TCPM must complete the debounce as defined in Type-C Specification.

### BMC Power Delivery

The Type-C connector allows USB Power Delivery (PD) to be communicated over the connected CC pin between two ports. The communication method is the BMC Power Delivery protocol and is used for many different reasons with the Type-C connector. Possible uses are outlined below.

- Negotiating and controlling charging power levels
- Alternative Interfaces such as MHL, Display Port
- Vendor specific interfaces for use with custom docks or accessories
- Role swap for dual-role ports that want to switch who is the host or device
- Communication with USB3.1 full featured cables

The FUSB308B integrates a thin BMC PD client which includes the BMC physical layer and packet buffers which allows packets to be sent and received by the host software through I<sup>2</sup>C accesses.

### Receive State Machine

The TCPM can setup the desired types of messages to be received by the FUSB308B via the RXDETECT register. This register defaults to 0x00 (Receiver disabled) upon power up, reset, Hard Reset transmission and reception, and upon detecting a cable disconnect. A message is not received unless it is first enabled. Figure 6 shows the FUSB308B receive state machine.

Upon a successfully transmitting GoodCRC, the RXSTAT register is updated with the type of message received and the TCPM is alerted via ALERTL.I\_RXSTAT bit (see transition from PRL\_Rx\_Send\_GoodCRC to PRL\_Rx\_Report\_SOP\* in Figure 6). The total number of bytes in the receive buffer RXDATA is stored in RXBYTECNT This number includes the header bytes that are stored in RXHEADL and RXHEADH and the RXSTAT register.

The RXBYTECNT, RXSTAT registers and the internal receive buffer will be cleared after the ALERTL.I\_RXSTAT bit is cleared.

The FUSB308B will automatically transmit a GoodCRC message for valid enabled messages within tTransmit.

A received message is valid when:

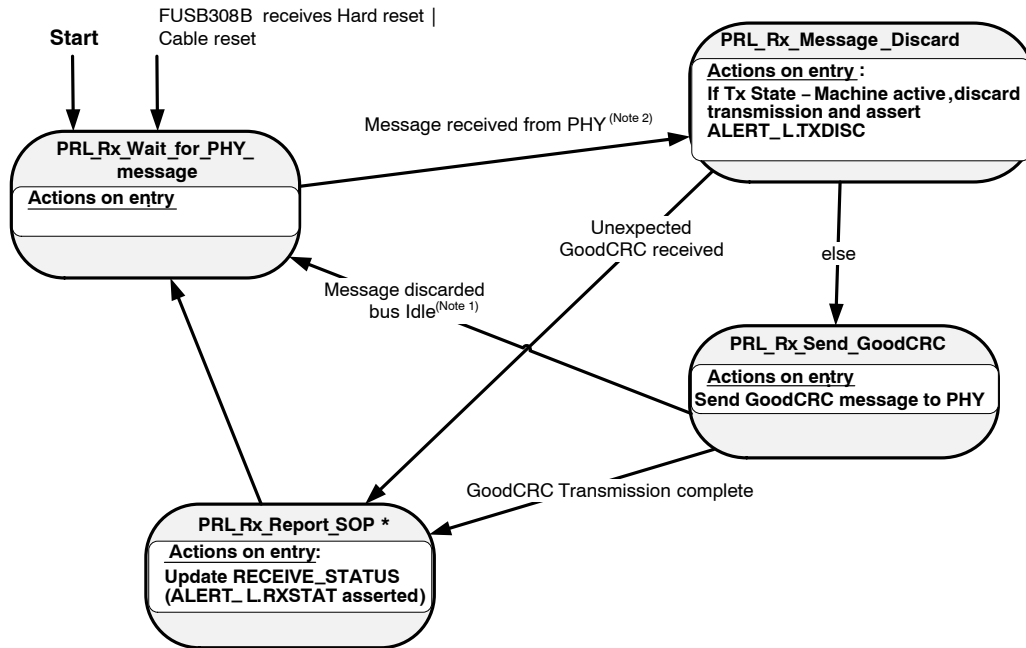
- It is not a GoodCRC message
- The calculated CRC is correct
- The SOP\* type is enabled

The makeup of the GoodCRC message is formed by the received SOP\* type and the contents of MSGHEADR register.

When an expected GoodCRC message or a Hard Reset signaling is received, they will not be replied with a

GoodCRC message (see Note 2 in Figure 6). If a GoodCRC message received was not expected due to the SOP\* type or mismatched Message ID, the receive state machine will not send a GoodCRC message and will transition to PRL\_Rx\_Report SOP\* to inform the TCPM.

If a Hard Reset message is received, the FUSB308B will reset the RXDETECT preventing the reception of future messages until the TCPM re-enables it.



2. This indication is sent by the PHY when a message has been discarded due to CC being busy, and after CC becomes idle again (see USB PD Spec).
3. Messages do not include Hard Reset or Cable Reset signals or expected GoodCRC messages (GoodCRC messages are only expected after the FUSB308B PHY has received the tx message and the FUSB308B Tx state-machine is in the PRL\_Tx\_Wait\_for\_PHY\_response state).

Figure 6. Receive State Machine

### Transmit State Machine

To transmit a message, the TCPM must first write the entire message in the following registers: TXHEADL, TXHEADH, TXBYTECNT and the TXDATA.

The actual transmission starts when the TCPM writes the TRANSMIT register.

The TRANSMIT register is where the message selection is done and it must be written once per transmission.

The TRANSMIT and TXBYTECNT will be reset after executing a successful or failed transmission.

If the TRANSMIT.RETRY\_CNT is set to a number greater than 0, the FUSB308B will automatically retry sending the same message if a GoodCRC is not received

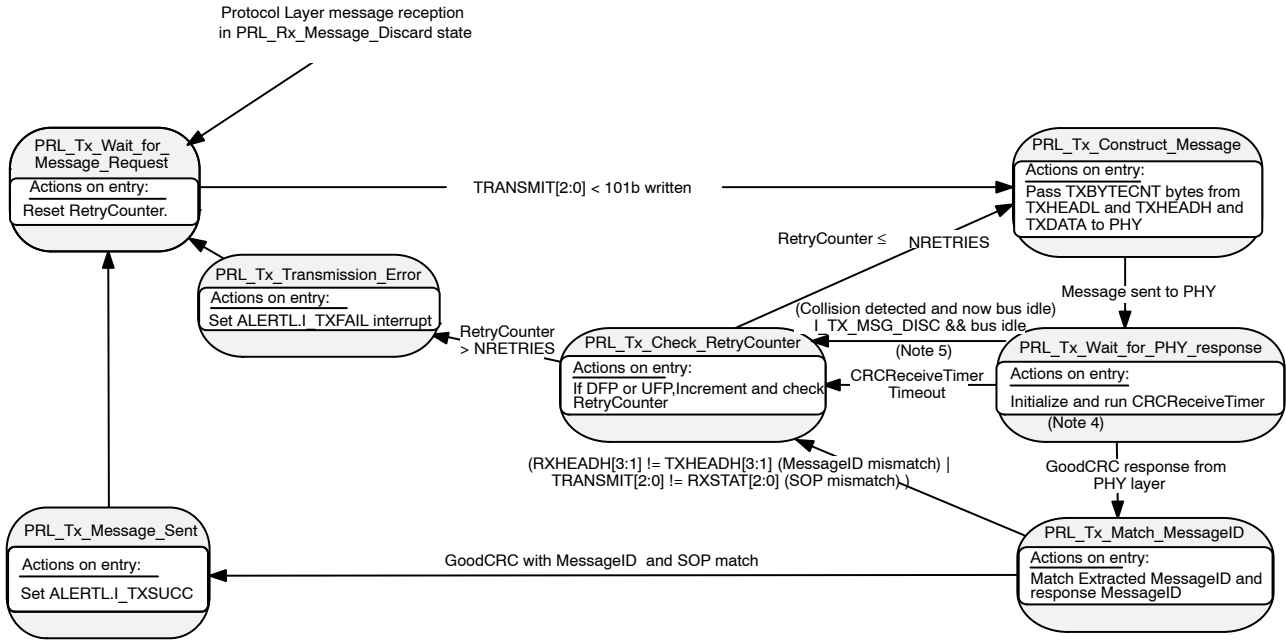
within tCRCReceiveTimer. An automatic retry is not performed when sending Hard-Resets, Cable-Resets, or BIST Carrier Mode 2 signaling.

The TCPM must not write the TRANSMIT register again until ALERTL.I\_TXSUCC, I\_TXFAIL, I\_TX\_DISC have been asserted and cleared.

The TCPM will not write the TRANSMIT register to request a transmission other than a Hard reset until it has cleared all received message alerts. If a TRANSMIT is written when ALERTL.I\_RXSTAT = 1 or ALERTL.I\_RXHRDRST = 1, the transmit request is discarded and ALERTL.I\_TX\_DISC is asserted.



ProtocolTransmit



- The CRCReceiveTimer is only started after the FUSB305 has sent the message. If the message is not sent due to a busy channel then the CRCReceiveTimer will not be started.
- This Indication is sent by the PHY layer when a message has been discarded due to CC being busy, and after CC becomes idle again. The CRCReceiveTimer is not running in this case since no message has been sent.

Figure 7. Transmit State Machine

### Hard Reset/ Cable Reset State Machine

The TCPM will write the TRANSMIT register to initiate the Hard Reset/Cable Reset state machine, see Figure 8. If the FUSB308B is in the middle of a transmission when instructed to send a Hard or Cable reset, it will set the ALERTL.I\_TXDISC bit and send the hard reset signaling as soon as possible. The FUSB308B implements the HardResetCompleteTimer. A Hard Reset or Cable Reset

will be attempted until the HardResetCompleteTimer times out. After a successful transmission or timeout, the FUSB308B will indicate that a Hard Reset or Cable Reset has been sent by asserting both ALERTL.I\_TXSUCC and ALERTL.I\_TXFAIL registers simultaneously. The bits in RXDETECT and RXBYTECNT will be reset to disable PD message passing after a Hard Reset is received or transmitted.

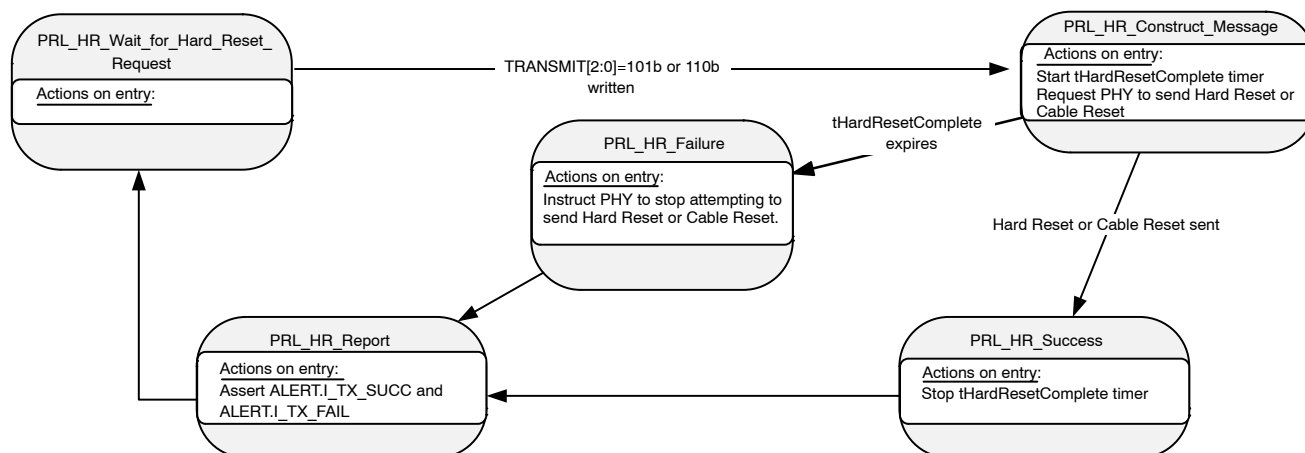


Figure 8. Hard Reset and Cable Reset State Machine

### Automatic GoodCRC Response

Power Delivery packets require a GoodCRC acknowledge packet to be sent for each received packet where the calculated CRC is the correct value. This calculation is done by the FUSB308B.

The FUSB308B will automatically send the GoodCRC control packet in response to alleviate the local processor from responding quickly to the received packet. Once the GoodCRC packet is sent the FUSB308B will trigger the ALERTL.I\_RXSTAT interrupt.

The following sequence of events occur internally within the FUSB308B without processor intervention when it is determined that the receive message has the correct CRC. If the host processor attempts a packet transmission during an Automatic GoodCRC response, the FUSB308B will set the ALERTL.I\_TXDISC bit interrupting the processor. The processor should only transmit a new packet once ALERTL.I\_TXSUCC or ALERTL.I\_TX\_FAIL has been received.

It is assumed that the processor will set the PWRCTRL.ORIENT to specify which channel USB-PD traffic will be transmitted or received.

### BIST Mode

#### Bist Transmit

The FUSB308B will transmit Bist Carrier Mode 2 signaling when directed by the TCPM via TRANSMIT

register. The FUSB308B will exit Bist Mode after tBISTContMode timer expires.

#### Bist Receive

When the FUSB308B is in Bist receive mode via TCPC\_CTRL register, it will acknowledge these packets with a GoodCRC and automatically flush the buffer to allow for thousands of packets to be received without filling the receive buffer. Bist Receive mode will exit on a cable disconnect or a Hard Reset received.

### VBUS Source Control

The FUSB308B has two source path controls (SRC and SRC\_HV). The secondary Source path control will be used to provide higher voltages on VBUS after a PD contract has been established. The primary source path is used for sourcing vsafe5V only.

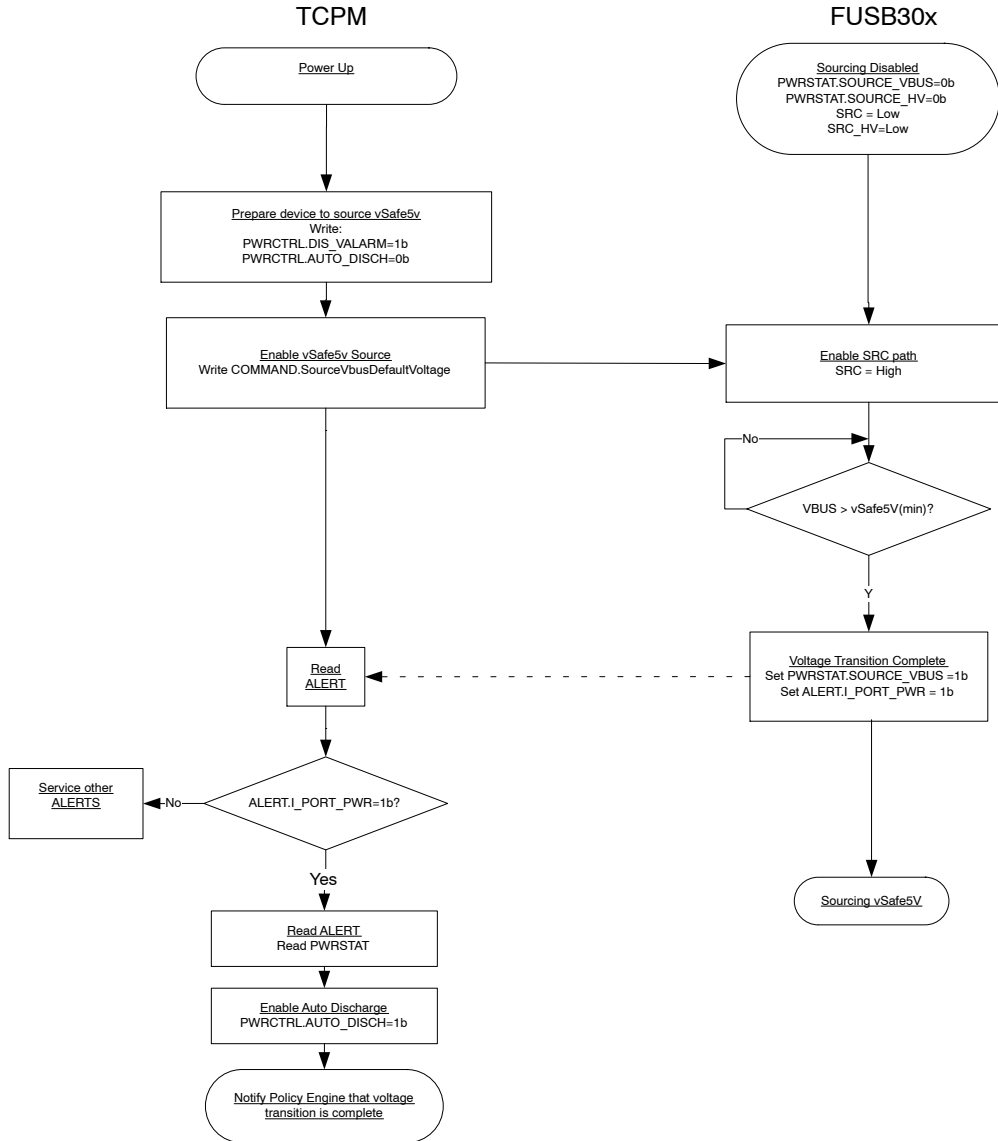
The TCPM will initiate the transition from SRC to SRC\_HV by writing 1000\_1000b to the COMMAND register. The FUSB308B will enable SRC\_HV and then disable the SRC I/O.

When transitioning from a high voltage source to vsafe5V, the TCPM will write 0111\_0111b to the COMMAND register.

**Voltage Transitions**

The FUSB308B has two source control ports: SRC and SRC\_HV. There are two ways to transition between SRC and SRC\_HV as seen in Figure 9 through Figure 12.

Transition to vSafe5v Path on Power up



**Figure 9. Transition to vSafe5V on Power Up**

Transition to HV using SRC\_HV Path

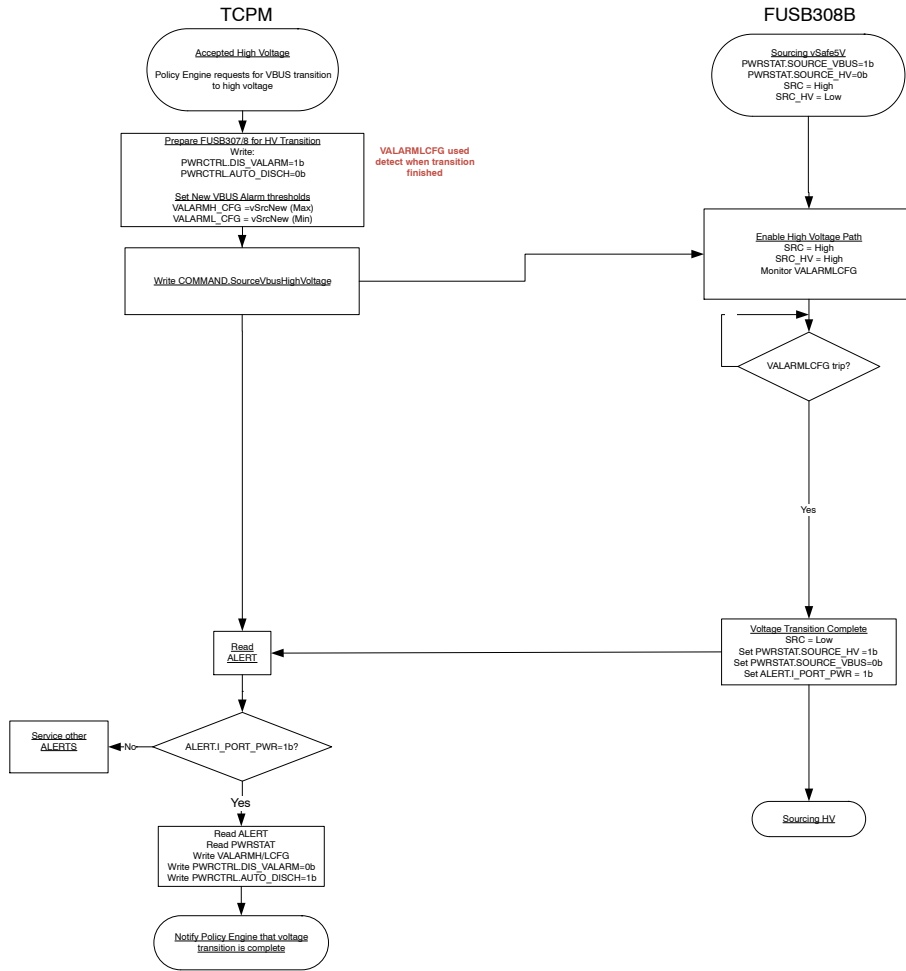


Figure 10. Transition to High Voltage Sourcing using SRC\_HV Controlled Path (FUSB308B)

Transition to vSafe5V using SRC\_HV Path

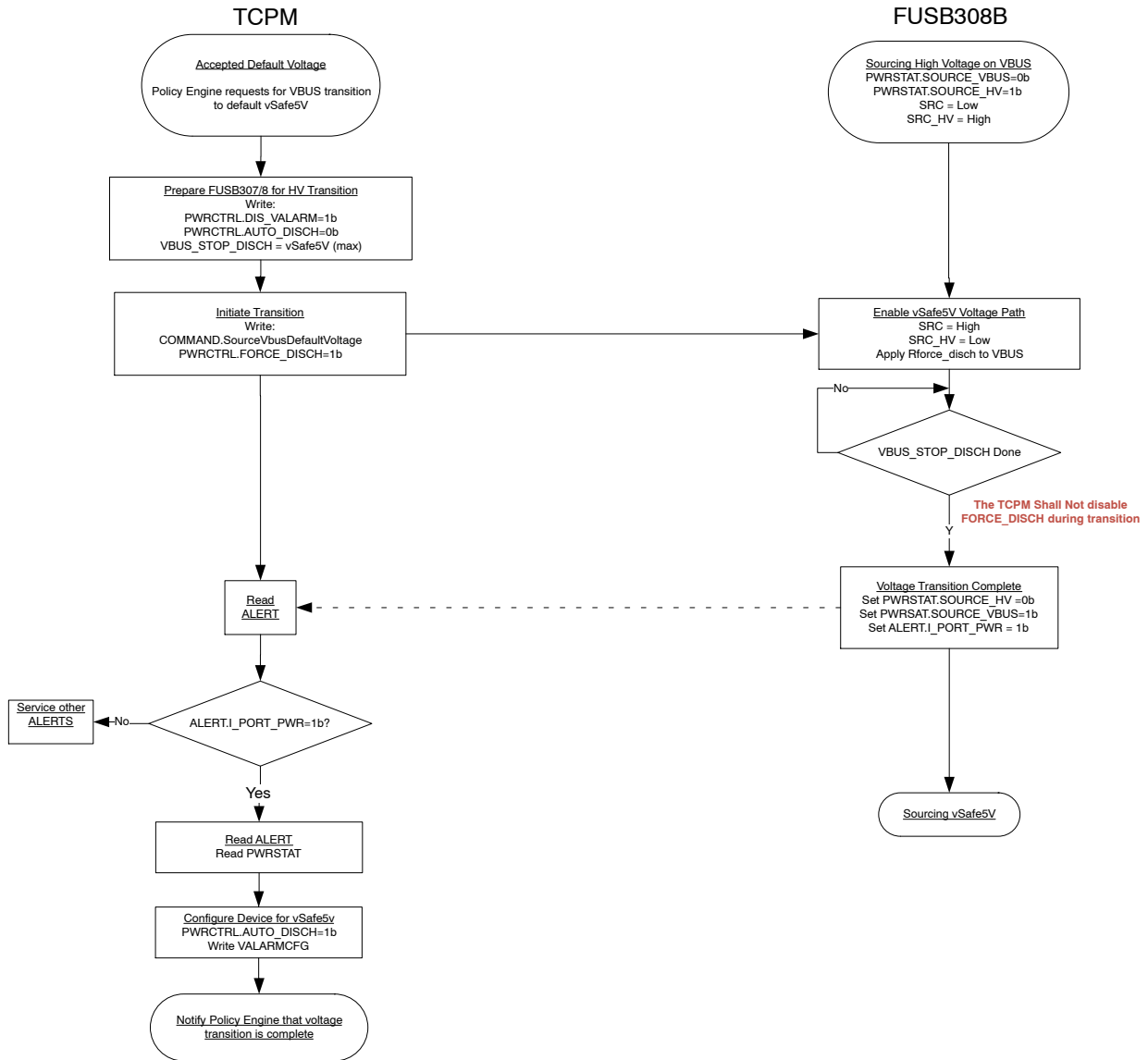


Figure 11. Transition to vSafe5V from SRC\_HV Controlled Path (FUSB308B)

Transition to HV using SRC enabled Path

NOTE: Transitioning from HV on SRC to vSafe5v also on SRC can be done by using Voltage Alarm Low.  
Power supply is responsible for transitioning voltages to meet USB PD spec- no discharge necessary.

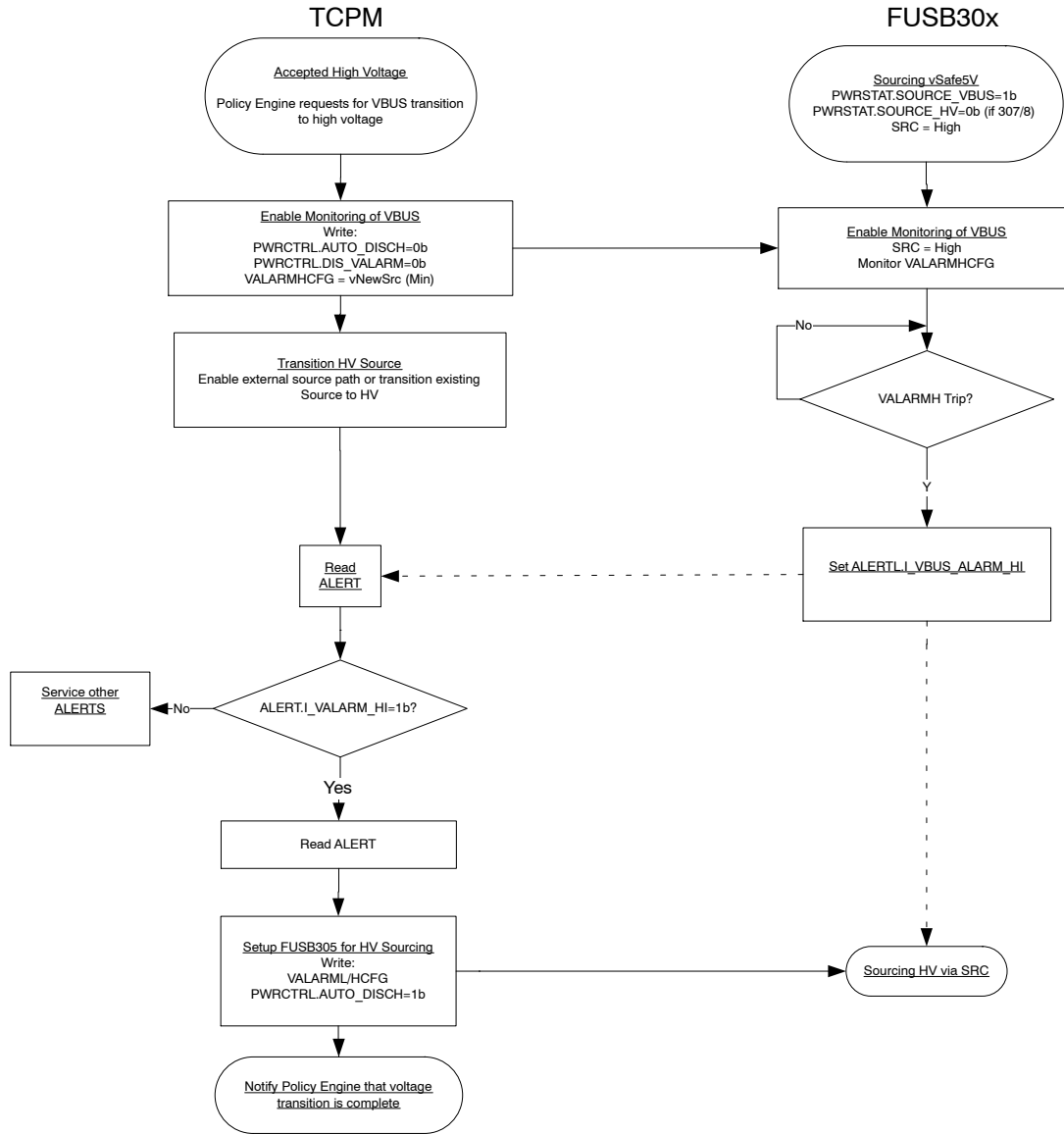


Figure 12. Transition to High Voltage using SRC Controlled Path VBUS

**VBUS Monitoring and Measurement**

The FUSB308B can monitor the presence of VBUS and will report it on PWRSTAT.VBUS\_VAL and interrupt ALERT.I\_PORT\_PWR.

VBUS\_VAL is set according to VBUS thresholds in *vVBUSthr*.

The FUSB308B also supports a more precise voltage measurement via an on-board ADC. The voltage on VBUS is measured at a rate of *tVBUSsample* and it is reported on VBUS\_VOLTAGE\_L/H register. The precision of the measurement is  $\pm 2\%$  with a resolution of 25 mV LSB.

In addition to providing the  $\mu$ Processor an accurate measurement of VBUS, the measurement in VBUS\_VOLTAGE will be used when monitoring various user defined thresholds:

- Voltage alarms in registers VALARMLCFG and VALARMHCFG
- VBUS Disconnect Threshold in registers VBUS\_SNK\_DISC and VBUS\_SNK\_DISC
- VBUS Stop Discharge Threshold in registers VBUS\_STOP\_DISC and VBUS\_STOP\_DISC

The FUSB308B implements Low and High VBUS Voltage Alarms that can be programmable via VALARMLCFG and VALARMHCFG respectively. If the High or the Low thresholds are crossed, the FUSB308B will signal an interrupt on ALERT.I\_VBUS\_ALARM\_HI or ALERT.I\_VBUS\_ALARM\_LO respectively. These alarms can be disabled by writing PWRCTRL.DIS\_VALARM to one.

ALERT.I\_PORT\_PWR is asserted if the bit-wise AND of PWRSTAT and PWRSTAMSK results in any bits that have the value 1.

**VBUS Discharge**

**Manual Discharge**

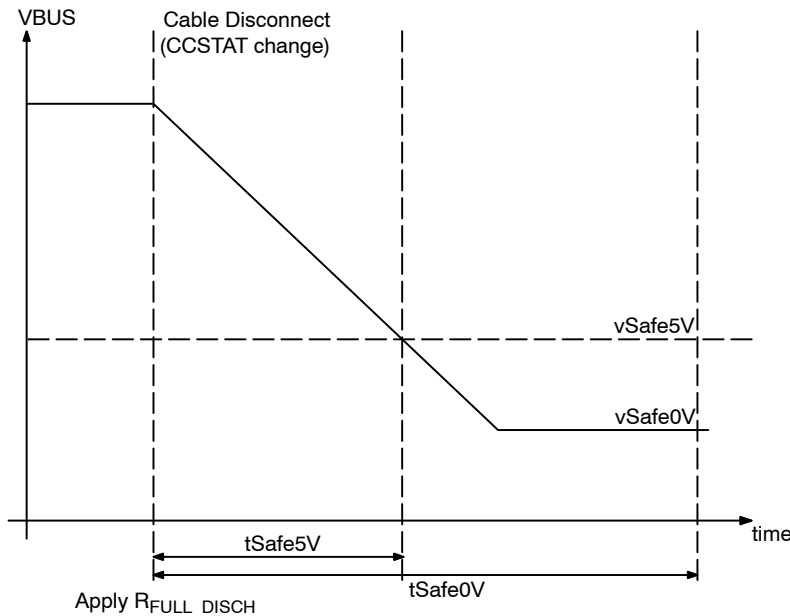
There are two types of manual discharge circuits implemented: A bleed discharge for low current and a force discharge. The bleed discharge can be manually enabled by writing a one to register bit PWRCTRL.EN\_BLEED\_DISCH. When enabled, the bleed discharge provides a low current load on VBUS of 7 KW (max.) via RBLEED. The force discharge is used to quickly discharge VBUS to *vSafe0V* by applying a dynamic load to VBUS via RFULL\_DISCH. The force discharge can be manually enabled by writing a one to register bit PWRCTRL.FORCE\_DISCH. When RFULL\_DISCH is applied, the maximum slew rate allowed for discharging VBUS does not exceed *vSrcSlewNeg* 30 mV/ $\mu$ s as it is specified in the USB-PD spec.

Automatic discharge bit PWRCTRL.AUTO\_DISCH must be disabled before enabling force discharge.

**Automatic Source Discharge after a Disconnect**

Automatic discharge can be enabled by setting PWRCTRL.AUTO\_DISCH register bit. When in Source mode the FUSB308B will fully discharge VBUS to *vSafe5V* (max.) within *tSafe5V* and to *vSafe0V* within *tSafe0V* when a Disconnect occurs. The FUSB308B is in Source mode when the SRC output is asserted.

The FUSB308B in Source mode will detect a Disconnect if the CCSTAT.CCx\_STAT field for the monitored CC pin indicates SRC.Open and enable the FULL Discharge pull-down device. The monitored CC pin is specified by TCPC\_CTRL.ORIENT.



**Figure 13. VBUS Auto Discharge as Source**

### Discharge during a Connection

The discharge functions can be manually activated via the PWRCTRL.FORCE\_DISCH register. The discharge

pull-down is specified by  $R_{FULL\_DISCH}$ . The FUSB308B will automatically disable discharge when VBUS reaches VBUS\_STOP\_DISC threshold.

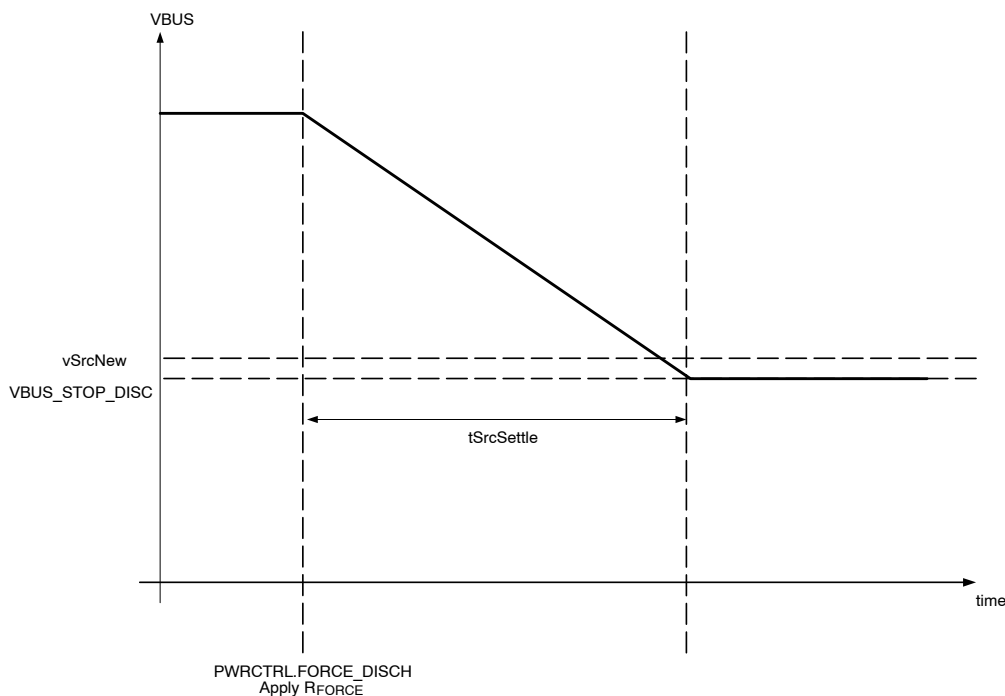


Figure 14. Source Discharge During a Connection

### Watchdog Timer

The watchdog timer functionality is enabled whenever TCPC\_CTRL.EN\_WATCHDOG is set to 1b. The watchdog timer should only be enabled after an attach when the device is in Attached.Src, Attached.Snk or Apply.ROLECONTROL states. The watchdog timer starts when any of the interrupts that are not masked in the Alert register are set or when the INTB pin is asserted. The watchdog timer is cleared on an I2C access by the TCPM

(either read or write). If the INTB pin is still asserted after this I2C access, the watchdog timer will reinitialize and start monitoring again until all of the Alerts are cleared or until the INTB pin is de-asserted.

When the watchdog timer expires, the FUSB308B will immediately disconnect the CC terminations by setting ROLE\_CONTROL bits 3..0 to 1111b, disable all SRC/SRC\_HV or SNK outputs, discharge VBUS to vSafe0V, and set FAULT\_STATUS.I2CInterfaceError.



**USB-PD Rev 3.0 Features****Extended Data Messages**

Extended Data Messages is only supported via Chunking where large messages are broken into 2 or more 26 byte chunks.

**ABSOLUTE MAXIMUM RATINGS**

Symbol	Parameter		Min	Max	Unit
V <sub>DDAMR</sub>	Supply Voltage from VDD		-0.5	6.0	V
V <sub>CC_HDDR</sub> (Note 6)	CC pins when configured as Host, Device or Dual Role Port		-0.5	6.0	V
V <sub>VBUS</sub>	VBUS Supply Voltage		-0.5	28.0	V
T <sub>STORAGE</sub>	Storage Temperature Range		-65	+150	C
T <sub>J</sub>	Maximum Junction Temperature			+150	C
T <sub>L</sub>	Lead Temperature (Soldering, 10 seconds)			+260	C
ESD	Human Body Model, JEDEC JESD22-A114	Connector Pins (VBUS, CCx)	4		kV
		Others	2		kV
	Charged Device Model, JEDEC LESD22-C101	All Pins	1		kV

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

6. As host, device drives CC, VConn.

**RECOMMENDED OPERATING CONDITIONS**

Symbol	Parameter	Min	Typ	Max	Unit
V <sub>VBUS</sub>	VBUS Supply Voltage (Note 7)	4.0	5.0	21.5	V
V <sub>DD</sub>	VDD Supply Voltage	2.8 (Note 8)	3.3	5.5	V
V <sub>CONN</sub>	VCONN Supply Voltage (Note 9)	2.7		5.5	V
I <sub>CONN</sub>	VCONN Supply Current			560	mA
T <sub>A</sub>	Operating Temperature	-40		+85	C
T <sub>A</sub>	Operating Temperature (Note 10)	-40		+105	C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

7. 20 V PD + 5% Tolerance per spec + 0.5 V Load Transition.

8. This is for functional operation only and isn't the lowest limit for all subsequent electrical specifications below. All electrical parameters have a minimum of 3 V operation.

9. For powered accessories Vconn minimum is 2.7 V.

10. Automotive part only, FUSB308BVMPX.

**DC and Transient Characteristics**

Unless otherwise specified: Recommended  $T_A$  and  $T_J$  temperature ranges. All typical values are at  $T_A = 25^\circ\text{C}$  and  $V_{DD} = 3.3\text{ V}$  unless otherwise specified.

**CURRENT CONSUMPTION**

Symbol	Parameter	$T_A = -40\text{ to }+85^\circ\text{C}$ $T_A = -40\text{ to }+105^\circ\text{C (Note 15)}$ $T_J = -40\text{ to }+125^\circ\text{C}$			Unit
		Min	Typ	Max	
I <sub>DISABLE</sub>	Disable Current (ROLECTRL = 0x0F)			10	μA
	Unattached DRP or Source		7	20	μA
	Attached as Source (No PD)		12	22	μA

**BASEBAND PD**

Symbol	Parameter	$T_A = -40\text{ to }+85^\circ\text{C}$ $T_A = -40\text{ to }+105^\circ\text{C (Note 15)}$ $T_J = -40\text{ to }+125^\circ\text{C}$			Unit
		Min	Typ	Max	
UI	Unit Interval	3.03	3.33	3.70	μs

**TRANSMITTER**

zDriver	TX output impedance at 750 kHz with an external 220 pF or equivalent load	33		75	Ω
tEndDriveBMC	Time to cease driving the line after the end of the last bit of the Frame			2	UI
tHoldLowBMC	Time to cease driving the line after the final high-to-low transition	1			μs
tStartDrive	Time before the start of the first bit of the preamble when the transmitter shall start driving the line	-1		1	μs
tBISTContMode	Time a BIST Carrier Mode 2 transmission is performed	30		60	ms
tBUFFER2CC	Time from I2C Stop from writing to TRANSMIT register to first bit of Preamble transmitted			195	μs
t <sub>R</sub>	Rise Time	300			ns
t <sub>F</sub>	Fall Time	300			ns

**RECEIVER**

CReceiver (Note 11)	Receiver capacitance when driver isn't turned on		25		pF
zBmcRx	Receiver Input Impedance	1			MΩ
tCC2BUFFER	Time between last bit of EOP to I_RXSTAT			50	μs
tRxFilter	Rx bandwidth limiting filter (Note 11)	100			ns
nTransitionCount	Transitions count in a time window of 20 μs max	3			Edges
tTransitionWindow	Time window for detecting non-idle	12		20	μs

11. Guaranteed by characterization and/or design. Not production tested.

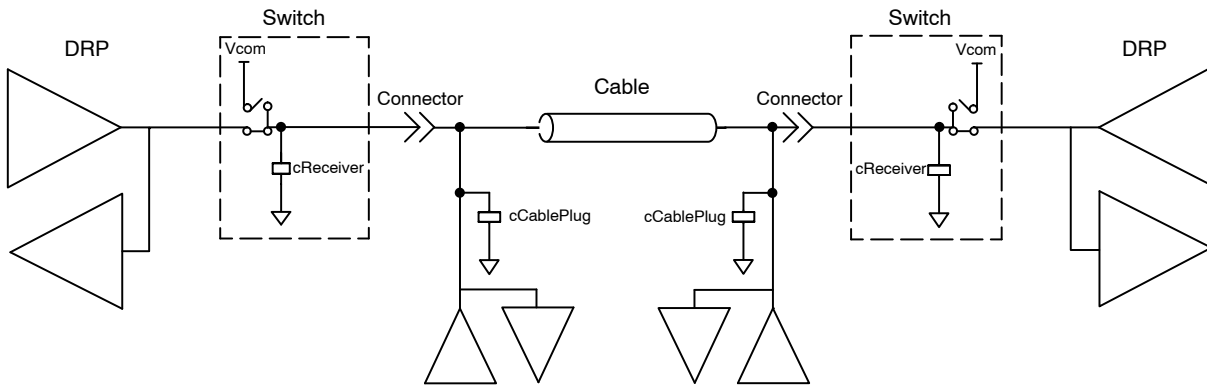


Figure 15. Transmitter Test Load

USB-PD R3.0 SPECIFIC PARAMETERS

Symbol	Parameter	$T_A = -40$ to $+85^\circ\text{C}$ $T_A = -40$ to $+105^\circ\text{C}$ (Note 15) $T_J = -40$ to $+125^\circ\text{C}$			Unit
		Min	Typ	Max	
<b>TRANSMITTER</b>					
rFRSwapTx	Fast Role Swap request transmit driver resistance Measured from $V_{CCx} = 0$ to vFRSwapCableTx			5	$\Omega$
tFRSwapTx	Fast Role Swap request transmit duration	60		120	$\mu\text{s}$
<b>RECEIVER</b>					
tFRSwapRx	Fast Role Swap request detection time	30		50	$\mu\text{s}$
vFRSwapCableTx	Fast Role Swap request voltage detection threshold	490	520	550	mV

TYPE C SPECIFIC PARAMETERS

Symbol	Parameter	$T_A = -40$ to $+85^\circ\text{C}$ $T_A = -40$ to $+105^\circ\text{C}$ (Note 15) $T_J = -40$ to $+125^\circ\text{C}$			Unit
		Min	Typ	Max	
R <sub>SW_CCx</sub>	R <sub>DS(on)</sub> for VCONN to CC1 or VCONN to CC2		0.4	1.0	$\Omega$
I <sub>SW_CCx</sub>	Over Current Protection (OCP) limit at which VCONN switch shuts off over the entire VCONN voltage range VCONN_OCP = 0Fh	600	800	1000	mA
t <sub>SoftStart</sub>	Time taken for the VCONN switch to turn on during which Over-Current Protection is disabled		1.5		ms
I <sub>80_CCx</sub>	DFP 80 $\mu\text{A}$ CC Current (Default) ROLECTRL = 05h	64	80	96	$\mu\text{A}$
I <sub>180_CCx</sub>	DFP 180 $\mu\text{A}$ CC Current (1.5 A) ROLECTRL = 15h	166	180	194	$\mu\text{A}$
I <sub>330_CCx</sub>	DFP 330 $\mu\text{A}$ CC Current (3 A) ROLECTRL = 25h	304	330	356	$\mu\text{A}$
R <sub>DEVICE</sub>	Device pull-down resistance (Note 12)	4.6	5.1	5.6	k $\Omega$
R <sub>a</sub>	Powered Accessory Termination	800		1200	$\Omega$
vRa-SRCdef	R <sub>a</sub> Detection Threshold for CC Pin for Source for Default Current on VBUS	0.15	0.20	0.25	V
vRa-SRC1.5A	R <sub>a</sub> Detection Threshold for CC Pin for Source for 1.5 A Current on VBUS	0.35	0.40	0.45	V
vRa-SRC3A	R <sub>a</sub> Detection Threshold for CC Pin for Source for 3 A Current on VBUS	0.75	0.80	0.85	V

TYPE C SPECIFIC PARAMETERS (continued)

Symbol	Parameter	$T_A = -40$ to $+85^\circ\text{C}$ $T_A = -40$ to $+105^\circ\text{C}$ (Note 15) $T_J = -40$ to $+125^\circ\text{C}$			Unit
		Min	Typ	Max	
vRd-SRCdef	Rd Detection Threshold for Source for Default Current (HOST_CUR1/0 = 01)	1.50	1.60	1.65	V
vRd-SRC1.5A	Rd Detection Threshold for Source for 1.5 A Current (HOST_CUR1/0 = 10)	1.50	1.60	1.65	V
vRd-SRC3A	Rd Detection Threshold for Source for 3 A Current (HOST_CUR1/0 = 11)	2.45	2.60	2.75	V
vRa-SNK	Ra Detection Threshold for CC Pin for Sink	0.15	0.20	0.25	V
vRd-def	Rd Default Current Detection Threshold for Sink	0.61	0.66	0.70	V
vRd-1.5A	Rd 1.5 A Current Detection Threshold for Sink	1.16	1.23	1.31	V
vRd-3.0A	Rd 3 A Current Detection Threshold for Sink	2.04	2.11	2.18	V
zOPEN	CC resistance for disabled state, ROLECTRL = 0Fh	126			k $\Omega$
vVCONNthr	Valid VCONN Voltage Assumes PWRCTRL.EN_VCONN = 1b			2.4	V
tTCPCfilter	Debounce time on CC lines to prevent CCSTAT change in case of minor changes in voltage on CC because of noise	4		500	$\mu\text{s}$
tCCDebounce	Debounce Time for CC Attach Detection	100	150	200	ms
tSetReg	Time between CC status change and I2C registers updated			50	$\mu\text{s}$
tTCPCSampleRate	CC Sample rate for indicating changes on CC lines			1	ms
tDRP	Sum of tToggleSrc and tToggleSnk timers	50		100	ms
tToggleSrc	Time Spent in Apply Rp before transitioning to Apply Rd	DRPTOGGLE = 00	15	30	ms
		DRPTOGGLE = 01	20	40	ms
		DRPTOGGLE = 10	25	50	ms
		DRPTOGGLE = 11	30	60	ms
tToggleSnk	Time Spent in Apply Rd before transitioning to Apply Rp	DRPTOGGLE = 00	35	70	ms
		DRPTOGGLE = 01	30	60	ms
		DRPTOGGLE = 10	25	50	ms
		DRPTOGGLE = 11	20	40	ms

12. RDEVICE minimum and maximum specifications are only guaranteed when power is applied.

VBUS MEASUREMENT CHARACTERISTICS

Symbol	Parameter	$T_A = -40$ to $+85^\circ\text{C}$ $T_A = -40$ to $+105^\circ\text{C}$ (Note 15) $T_J = -40$ to $+125^\circ\text{C}$			Unit
		Min	Typ	Max	
vMDACstepVBUS	VBUS Measure block LSB reported on VBUS_VOLTAGE[9:0] register		25		mV
pMDACVBUS	Accuracy of VBUS Voltage Measurement	$T_A = -40$ to $+85^\circ\text{C}$		$\pm 2$	%
		$T_A = +85$ to $+105^\circ\text{C}$ (Note 12)		$\pm 5$	%
tVBUSsample	Sampling period of VBUS Measurement		3		ms
vVBUSthr	VBUS threshold at which VBUS_VAL interrupt is triggered. Assumes VBUS present detection is enabled	3.5		4.05	V
vVBUShys	Hysteresis on VBUS Comparator		50		mV

**VBUS MEASUREMENT CHARACTERISTICS** (continued)

Symbol	Parameter	T <sub>A</sub> = -40 to +85°C T <sub>A</sub> = -40 to +105°C (Note 15) T <sub>J</sub> = -40 to +125°C			Unit
		Min	Typ	Max	
vSafe0Vthr	Safe Operating Voltage at “Zero Volts” Threshold			0.8	V
vSafe0Vhys	vSafe0V Hysteresis		40		mV
vALARMLSB	LSB of VBUS thresholds for VBUS_SNK_DISCL VBUS_STOP_DISCL VALARMHCFGL VALARMLCFGL		50		mV
pALARM	Accuracy of VBUS thresholds for VBUS_SNK_DISCL VBUS_STOP_DISCL VALARMHCFGL VALARMLCFGL			±5	%

SOURCE AND SINK CONTROL SPECIFICATIONS

Symbol	Parameter		$T_A = -40$ to $+85^\circ\text{C}$ $T_A = -40$ to $+105^\circ\text{C}$ (Note 15) $T_J = -40$ to $+125^\circ\text{C}$			
			Min	Typ	Max	Unit
$R_{BLEED}$	Equivalent Resistance for bleed discharging VBUS	VBUS = 4.0 V to 21.5 V	4		7	$k\Omega$
vSrcSlewNeg	Maximum slew rate allowed when discharging VBUS	VBUS = 4.0 V to 21.5 V			30	mV/ $\mu\text{s}$
tSafe0V	Time to reach vSafe0V max				650	ms
tSafe5V	Time to reach vSafe5V max				275	ms
tSrcSettle	Time to discharge to vSrcNew				275	ms
tAUTO_DISCH_FAIL	Time to declare auto discharge failure to discharge to vSafe0V	Device configured as Source. Measure from CCSTAT change to Open	650			ms
tAUTO_DISCH_FAIL_5V	Time to declare auto discharge failure to discharge to vSafe5V	Device configured as Source. Measure from CCSTAT change to Open	275			ms

OVER-TEMPERATURE SPECIFICATIONS

Symbol	Parameter	Min	Typ	Max	Unit
$T_{SHUT}$	Temp. for VCONN Switch Turn Off		145		$^\circ\text{C}$
$T_{HYS}$	Temp. Hysteresis for VCONN Switch Turn On		10		$^\circ\text{C}$

WATCHDOG TIMER SPECIFICATIONS

Symbol	Parameter	Min	Typ	Max	Unit
$T_{HV}Watchdog$	Time from last I2C transaction or INTB pin assertion to entering ErrorRecovery	1500		2000	ms

IO SPECIFICATIONS

Symbol	Parameter	$V_{DD}$ (V)	Conditions	$T_A = -40$ to $+85^\circ\text{C}$ $T_A = -40$ to $+105^\circ\text{C}$ (Note 15) $T_J = -40$ to $+125^\circ\text{C}$			Unit
				Min	Typ	Max	

HOST INTERFACE PINS(INT\_N, DBG\_N)

$V_{OLINTN}$	Output Low Voltage	3.0 to 5.5	$I_{OL} = 4$ mA			0.4	V
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GPIO, ORIENT AND MUX\_SEL PINS

$V_{IL}$	Low-Level Input Voltage	3.0 to 5.5				0.4	V
$V_{IH}$	High-Level Input Voltage	3.0 to 5.5		1.2			V
$V_{OL}$	Low-Level Output Voltage	3.0 to 5.5	$I_{OL} = 4$ mA			0.4	V
$V_{OH}$	High-Level Output Voltage	3.0 to 5.5	$I_{OH} = -2$ mA	$0.7V_{DD}$			V
$I_{IN}$	Input Leakage	3.0 to 5.5	Input Voltage 0 V to 5.5 V (When GPIO is setup as an input or Tri-Stated output)	-5		5	$\mu\text{A}$
$I_{OFF}$	Off Input Leakage	0	Input Voltage 0 V to 5.5 V	-5		5	$\mu\text{A}$

SRC, SNK AND SRC\_HV

$V_{OL}$	Low-Level Output Voltage	3.0 to 5.5	$I_{OL} = 4$ mA			0.4	V
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IO SPECIFICATIONS (continued)

Symbol	Parameter	V <sub>DD</sub> (V)	Conditions	T <sub>A</sub> = -40 to +85°C T <sub>A</sub> = -40 to +105°C (Note 15) T <sub>J</sub> = -40 to +125°C			Unit
				Min	Typ	Max	

SRC, SNK AND SRC\_HV

V <sub>OH</sub>	High-Level Output Voltage	3.0 to 5.5	I <sub>OH</sub> = -2 mA	0.7V <sub>DD</sub>			V
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I<sup>2</sup>C INTERFACE PINS – STANDARD, FAST OR FAST MODE PLUS SPEED MODE SDA, SCL) (Note 13)

V <sub>DDEXT</sub>	External power supply to which SDA and SCL are pulled up			1.8		3.6	V
V <sub>ILI2C</sub>	Low-Level Input Voltage	3.0 to 5.5				0.4	V
V <sub>IHI2C</sub>	High-Level Input Voltage	3.0 to 5.5		1.2			V
V <sub>HYS</sub>	Hysteresis of Schmitt Trigger Inputs	3.0 to 5.5		0.2			V
I <sub>I2C</sub>	Input Current of SDA and SCL Pins,	3.0 to 5.5	Input Voltage 0.26 V to 2 V	-10		10	μA
I <sub>CC I2C</sub>	VDD current when SDA or SCL is HIGH	3.0 to 5.5	Input Voltage 1.8 V	-10		10	μA
V <sub>OLSDA</sub>	Low-Level Output Voltage at 2 mA Sink Current (Open-Drain)	3.0 to 5.5		0		0.36	V
I <sub>OLSDA</sub>	Low-Level Output Current (Open-Drain)	3.0 to 5.5	V <sub>OLSDA</sub> = 0.4 V	20			mA
C <sub>I</sub> (Note 14)	Capacitance for Each I/O Pin	3.0 to 5.5			5		pF

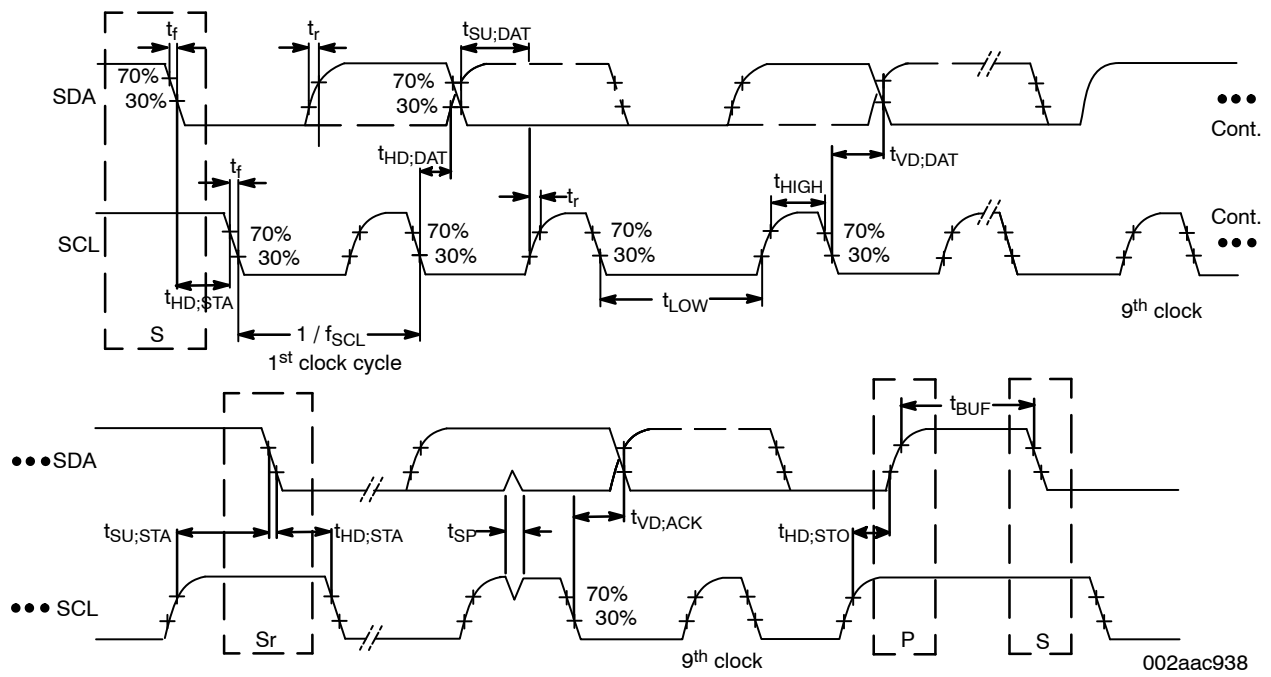
13. I<sup>2</sup>C pull up voltage is required to be between 1.71 V and V<sub>DD</sub>.

FAST MODE PLUS I<sup>2</sup>C SPECIFICATIONS

Symbol	Parameter	Fast Mode Plus		
		Min.	Max.	Unit
f <sub>SCL</sub>	I2C_SCL Clock Frequency	0	1000	kHz
t <sub>HD;STA</sub>	Hold Time (Repeated) START Condition	0.26		μs
t <sub>LOW</sub>	Low Period of I2C_SCL Clock	0.5		μs
t <sub>HIGH</sub>	High Period of I2C_SCL Clock	0.26		μs
t <sub>SU;STA</sub>	Set-up Time for Repeated START Condition	0.26		μs
t <sub>HD;DAT</sub>	Data Hold Time	0		μs
t <sub>SU;DAT</sub>	Data Set-up Time	50		ns
t <sub>r</sub>	Rise Time of I2C_SDA and I2C_SCL Signals (Note 14)	20 × (V <sub>DD</sub> /5.5 V)	120	ns
T <sub>f</sub> (Note 14)	Fall Time of I2C_SDA and I2C_SCL Signals (Note 14)	20 × (V <sub>DD</sub> /5.5 V)	120	ns
t <sub>SU;STO</sub>	Set-up Time for STOP Condition	0.26		μs
t <sub>BUF</sub>	Bus-Free Time between STOP and START Conditions (Note 14)	0.5		μs
t <sub>SP</sub>	Pulse Width of Spikes that Must Be Suppressed by the Input Filter	0	50	ns

14. Guaranteed by characterization. Not production tested.

15. Automotive part only, FUSB308BVMPX.



$V_{IL} = 0.3V_{DD}$   
 $V_{IH} = 0.7V_{DD}$

Figure 16. Definition of Timing for Full-Speed Mode Devices on the I2C Bus



Table 4. REGISTER DEFINITIONS

Address	Register Name	Type	Rst Val	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
00h	VENDIDL	R	79h				Vendor ID Low				
01h	VENDIDH	R	07h				Vendor ID High				
02h	PRODIDL	R	34h				Product ID Low				
03h	PRODIDH	R	01h				Product ID High				
04h	DEVIDL	R	02h				Device ID Low				
05h	DEVIDH	R	02h				Device ID High				
06h	TYPECREVL	R	12h				USB Type-C Revision Low				
07h	TYPECREVH	R	00h				USB Type-C Revision High				
08h	USBPDVER	R	12h				USB PD Version				
09h	USBPDREV	R	20h				USB PD Revision				
0Ah	PDIFREVL	R	12h				USB PD Interface Revision Low (Version)				
0Bh	PDIFREVH	R	10h				USB PD Interface Revision High (Revision)				
10h	ALERTL	R/WC	00h	I_VBUS_ALARM_HI	I_TXSUCC	I_TXDISC	I_TXFAIL	RXHRDRST	I_RXSTAT	I_PORT_PWR	I_CCSTAT
11h	ALERTH	R/WC	00h	I_VD_ALERT	Reserved	Reserved	Reserved	I_VBUS_SNK_DISC	I_RX_FULL	I_FAULT	I_VBUS_ALARM_LO
12h	ALERTMSKL	R/W	FFh	M_VBUS_ALARM_HI	M_TXSUCC	M_TX_DISC	M_TXFAIL	M_RXDRST	M_RXSTAT	M_PORT_PWR	M_CCSTAT
13h	ALERTMSKH	R/W	0Fh	M_VD_ALERT	Reserved	Reserved	Reserved	M_VBUS_SNK_DISC	M_RX_FULL	M_FAULT	M_VBUS_ALARM_LO
14h	PWRSTATMSK	R/W	FFh	M_DEBUG_ACC	M_INIT	M_SRC_HV	M_SRC_VBUS	M_VBUS_VAL_EN	M_VBUS_VAL	M_VCONN_VAL	M_SNKVBUS
15h	FAULTSTATMSK	R/W	B3h	M_ALL_REGS_RESET	Reserved	M_AUTO_DISCH_FAIL	M_FORCE_DISCH_FAIL	Reserved	Reserved	M_VCONN_OCP	M_I2C_ERR
16h..17h	Reserved	R	00h								
18h	STD_OUT_CFG	R/W	40h	TRI_STATE	DEBUG_ACC	Reserved	Reserved	MUX_CTRL		Reserved	ORIENT
19h	TCPC_CTRL	R/W	00h	Reserved	Reserved	EN_WATCHDOG	DEBUG_ACC_CTRL	I2C_CLK_STRETCH		BIST_TMODE	ORIENT
1Ah	ROLECTRL	R/W	0Ah 4Ah	Reserved	DRP	RP_VAL		CC2_TERM		CC1_TERM	

Table 4. REGISTER DEFINITIONS (continued)

Address	Register Name	Type	Rst Val	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
1Bh	FAULTCTRL	R/W	00h	Reserved	Reserved		Reserved	DISCH_TIMER_DIS	Reserved	Reserved	VCONN_OCP_DIS
1Ch	PWRCTRL	R/W	60h	Reserved	VBUS_MON	DIS_VALRM	AUTO_DISCH	EN_BLEED_DISCH	FORCE_DISCH	VCONN_PWR	EN_VCONN
1Dh	CCSTAT	R	00h/20h	Reserved	Reserved	LOOK4CON	CON_RES	CC2_STAT	CC1_STAT		
1Eh	PWRSTAT	R	08h	DEBUG_ACC	TCPC_INIT	SOURCE_HV	SOURCE_VBUS	VBUS_VAL_EN	VBUS_VAL	VCONN_VAL	SNKVBUS
1Fh	FAULTSTAT	R	80h	ALL_REGS_RESET	Reserved	AUTO_DISCH_FAIL	FORCE_DISCH_FAIL	Reserved	Reserved	VCONN_OCP	I2C_ERR
20h..22h	Reserved	R	00h	Reserved							
23h	COMMAND	R	00h	Command							
24h	DEVCAP1L	R	DDh	ROLES_SUPPORT			ROLES_SUPPORT	SWITCH_VCONN	SNK_VBUS	SRC_HV	SRC_VBUS
25h	DEVCAP1H	R	1Eh	Reserved			BLEED_DIS	FORCE_DIS	VBUS_MEAS_ALRM	RP_SUPPORT	
26h	DEVCAP2L	R	D7h	SNK_DISC_DETECT	STOP_DISCH	VBUS_ALRM_LSB		VCONN_POWER_CAP			VCONN_FAULT_CAP
27h	DEVCAP2H	R	01h	Reserved							
28h	STD_IN_CAP	R	00h	Reserved							
29h	STD_OUT_CAP	R	41h	Reserved	DEBUG_ACC	Reserved			MUX_CTRL	Reserved	ORIENT
2Ah..2Dh	Reserved	R	00h	Reserved							
2Eh	MSGHEADR	R/W	02h	Reserved			Cable Plug	Data Role	USB PD Rev		PWR Role
2Fh	RXDETECT	R/W	00h	Reserved	EN_CABLE_RST	EN_HRD_RST	EN_SOP2_DBG	EN_SOP1_DBG	EN_SOP2	EN_SOP1	EN_SOP
30h	RXBYTECNT	R	00h	Received Byte Count							
31h	RXSTAT	R	00h	Reserved							
32h	RXHEADL	R	00h	Received Header Low							
33h	RXHEADH	R	00h	Received Header High							
34h..4Fh	RXDATA	R	00h	Received Data Payload							
50h	TRANSMIT	R/W	00h	Reserved	Retry Counter	Reserved	Reserved	Reserved	Transmit SOP* Message		

Table 4. REGISTER DEFINITIONS (continued)

Address	Register Name	Type	Rst_Val	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
51h	TXBYTECNT	R/W	00h						Transmit Byte Count		
52h	TXHEADL	R/W	00h						Transmit Header Low		
53h	TXHEADH	R/W	00h						Transmit Header High		
54h..6F	TXDATA	R/W	00h						Transmit Payload		
70h	VBUS_VOLTAGE_L	R	00h						VBUS Measurement Output		
71h	VBUS_VOLTAGE_H	R	00h								
72h	VBUS_SNK_DISCL	R/W	A0h						VBUS SINK Disconnected Threshold (See Register Description Table)		
73h	VBUS_SNK_DISCH	R/W	1Ch								
74h	VBUS_STOP_DISCL	R/W	00h						VBUS Discharge Stop Threshold (See Register Description Table)		
75h	VBUS_STOP_DISCH	R/W	00h								
76h	VALARMHCFGL	R/W	00h						Voltage High Trip Point (See Register Description Table)		
77h	VALARMHCFGH	R/W	00h								
78h	VALARMLCFGL	R/W	00h						Voltage Low Trip Point (See Register Description Table)		
79h	VALARMLCFGH	R/W	00h								
7Ah..7Fh	Reserved	R/W	00h						Reserved		
A0h	VCONN_OCP	R/W	0Fh					OCV RANGE	OCP_CUR		
A2h	RESET	R/WC	00h						Reserved		
A4h	GPIO1_CFG	R/W	00h						GPO1_VAL	PD_RST	SW_RST
A5h	GPIO2_CFG	R/W	00h					FR_SWAP_FN	GPO2_VAL	GPI1_EN	GPI2_EN
A6h	GPIO_STAT	R	00h						GPI2_VAL	GPI1_VAL	GPI2_VAL
A7h	DRPTOGGLE	R/W	00h						DRPTOGGLE		
A9h..AFh	Reserved	R	00h						Reserved		
B1h	SRC_FRSWAP	R/W	00h						Reserved		
B2h	SNK_FRSWAP	R/W	00h						Reserved		
B3h	ALERT_VD	R/W	00h	Reserved	I_DISCH_SUCC	I_GPI2	I_GPI1	I_VDD_DTCT	I_OTP	I_SWAP_TX	I_SWAP_RX
B4h	ALERT_VD_MSK	R/W	7Fh	Reserved	M_DISCH_SUCC	M_GPI2	M_GPI1	M_VDD_DTCT	M_OTP	M_SWAP_TX	M_SWAP_RX

**Table 5. VENDIDL**

Address: 00h

Reset Value: 0x79

Type: Read

Bit #	Name	R/W/C	Size (Bits)	Vendor ID Low Description
7:0	VENDIDL	R	8	ON Semiconductor Vendor ID Low: <b>79h</b>

**Table 6. VENDIDH**

Address: 01h

Reset Value: 0x07

Type: Read

Bit #	Name	R/W/C	Size (Bits)	Vendor ID High Description
7:0	VENDIDH	R	8	ON Semiconductor Vendor ID High: 07h

**Table 7. PRODIDL**

Address: 02h

Reset Value: See Below

Type: Read

Bit #	Name	R/W/C	Size (Bits)	Product ID Low Description
7:0	PRODIDL	R	8	Product ID Low, <b>FUSB308B: 34h</b>

**Table 8. PRODIDH**

Address: 03h

Reset Value: 0x01h

Type: Read

Bit #	Name	R/W/C	Size (Bits)	Product ID High Description
7:0	PRODIDH	R	8	Product ID High, <b>All: 1h</b>

**Table 9. DEVIDL**

Address: 04h

Reset Value: 0x02h

Type: Read

Bit #	Name	R/W/C	Size (Bits)	Device ID Low (Version) Description
7:0	REVIDL	R	8	Revision ID Low: <b>01h</b> A_[Revision ID]: 0x01 (e.g. A_revA) B_[Revision ID]: 0x02 (e.g. B_revA) C_[Revision ID]: 0x03 (e.g. C_revA) etc

**Table 10. DEVIDH**

Address: 05h

Reset Value: 0x02h

Type: Read

Bit #	Name	R/W/C	Size (Bits)	Device ID High (Revision) Description
7:0	DEVIDH	R	8	Revision ID High: <b>00h</b> " [Version ID]_revA: 0x00 (e.g. A_revA) [Version ID]_revB: 0x01 (e.g. A_revB) [Version ID]_revC: 0x02 (e.g. A_revC) etc

**Table 11. TYPECREVL**

Address: 06h  
Reset Value: 0x12h  
Type: Read

Bit #	Name	R/W/C	Size (Bits)	Type-C Revision Low Description
7:0	TYPECREVL	R	8	Type-C Revision High: <b>12h</b>

**Table 12. TYPECREVH**

Address: 07h  
Reset Value: 0x00h  
Type: Read

Bit #	Name	R/W/C	Size (Bits)	Type-C Revision High Description
7:0	TYPECREVH	R	8	Type-C Revision High: <b>00h</b>

**Table 13. USBPDVER**

Address: 08h  
Reset Value: 0x12h  
Type: Read

Bit #	Name	R/W/C	Size (Bits)	USB-PD Version Description
7:0	USBPDVER	R	8	USB-PD Version: <b>12h</b>

**Table 14. USBPDREV**

Address: 09h  
Reset Value: 0x20h  
Type: Read

Bit #	Name	R/W/C	Size (Bits)	USB-PD Revision Description
7:0	USBPDREV	R	8	USB-PD Revision: <b>20h</b>

**Table 15. PDIFREVL**

Address: 0Ah  
Reset Value: 0x12h  
Type: Read

Bit #	Name	R/W/C	Size (Bits)	USB-PD Interface Revision Low Description
7:0	PDIFREVL	R	8	USB-PD IF Version: <b>12h</b>

**Table 16. PDIFREVH**

Address: 0Bh  
Reset Value: 0x10h  
Type: Read

Bit #	Name	R/W/C	Size (Bits)	USB-PD Interface Revision High Description
7:0	PDIFREVH	R	8	USB-PD IF Revision: <b>10h</b>

**Table 17. ALERTL**

Address: 10h

Reset Value: 0x00

Type: Read, Write 1 to Clear

Bit #	Name	R/W/C	Size (Bits)	ALERT1 Description
7	I_VBUS_ALARM_HI	R/WC	1	Voltage Alarm Hi <b>0b: Cleared</b> 1b: A high-voltage alarm has occurred
6	I_TXSUCC	R/WC	1	<b>0b: Cleared</b> 1b: Reset or SOP* message transmission successful. GoodCRC response received on SOP* message transmission. Transmit SOP* message buffer registers are empty
5	I_TXDISC	R/WC	1	<b>0b: Cleared</b> 1b: Reset or SOP* message transmission not sent due to incoming receive message. Transmit SOP* message buffer registers are empty
4	I_TXFAIL	R/WC	1	<b>0b: Cleared</b> 1b: SOP* message transmission not successful, no GoodCRC response received on SOP* message transmission. Transmit SOP* message buffer registers are empty.
3	I_RXHRDRST	R/WC	1	Received Hard Reset <b>0b: Cleared</b> 1b: Received Hard Reset message
2	I_RXSTAT	R/WC	1	Receive Status <b>0b: Cleared</b> 1b: RXSTAT changed. RXBYTECNT being 0 does not set this register
1	I_PORT_PWR (Note 16)	R/WC	1	Port Power Status <b>0b: Cleared</b> 1b: Port status changed. Read PWRSTAT register
0	I_CCSTAT	R/WC	1	CC Status <b>0b: Cleared</b> 1b: CC status changed. Read CCSTAT register

16. ALERTL.I\_PORT\_PWR is asserted if the bit-wise AND of PWRSTAT and PWRSTAMSK results in any bits that have the value 1.

**Table 18. ALERTH**

Address: 11h

Reset Value: 0x00

Type: Read, Write 1 to Clear

Bit #	Name	R/W/C	Size (Bits)	ALERT2 Description
7	I_VS_ALERT	RWC	1	Vendor Defined Alert 0b: Cleared 1b: A Vendor Defined Alert occurred. Please read ALERT_VD register
6:4	Reserved	R	3	<b>Reserved: 000b</b>
3	I_VBUS_SNK_DISC	RWC	1	VBUS Sink Disconnect Detected <b>0b: Cleared</b> 1b: A VBUS Sink Disconnect Threshold crossing from High to Low has been detected
2	I_RX_FULL	RWC	1	Rx Buffer Overflow <b>0b: Internal RX Buffer is functioning properly</b> 1b: Internal RX Buffer has overflowed Note: This interrupt indicates overflow of the internal buffer, not the RXDATA space. To clear overflow condition, write to ALERTL.I_RX-STAT Writing a 1 to this register acknowledges the overflow. The actual overflow is cleared by writing to ALERTL.I_RXSTAT
1	I_FAULT (Note 17)	R/WC	1	Fault Alarm <b>0b: Cleared</b> 1b: A Fault alarm has occurred. Read FAULTSTAT register
0	I_VBUS_ALRM_LO	R/WC	1	Voltage Alarm Lo <b>0b: Cleared</b> 1b: A low-voltage alarm has occurred

17. ALERTH.I\_FAULT is asserted if the bit-wise AND of FAULTSTAT and FAULTSTAMSK results in any bits that have the value 1.

**Table 19. ALERTMSKL**

Address: 12h

Reset Value: 0xFF (Resets on POR, SW\_RST and Hard Reset)

Type: Read/Write

Bit #	Name	R/W/C	Size (Bits)	Alert Mask 1 Description
7	M_VBUS_ALRM_HI	R/W	1	0b: Interrupt masked <b>1b: Interrupt unmasked</b>
6	M_TXSUCC	R/W	1	0b: Interrupt masked <b>1b: Interrupt unmasked</b>
5	M_TX_DISC	R/W	1	0b: Interrupt masked <b>1b: Interrupt unmasked</b>
4	M_TXFAIL	R/W	1	0b: Interrupt masked <b>1b: Interrupt unmasked</b>
3	M_RXHRDRST	R/W	1	0b: Interrupt masked <b>1b: Interrupt unmasked</b> <b>Note: Generally this interrupt should not be masked.</b>
2	M_RXSTAT	R/W	1	0b: Interrupt masked <b>1b: Interrupt unmasked</b>
1	M_PORT_PWR	R/W	1	0b: Interrupt masked <b>1b: Interrupt unmasked</b>
0	M_CCSTAT	R/W	1	0b: Interrupt masked <b>1b: Interrupt unmasked</b>

**Table 20. ALERTMSKH**

Address: 13h

Reset Value: 0xFF (Resets on POR, SW\_RST and Hard Reset)

Type: Read/Write

Bit #	Name	R/W/C	Size (Bits)	Alert Mask 2 Description
7	M_VD_ALERT	RW	1	0b: Interrupt masked, <b>1b: Interrupt unmasked</b>
6:4	Reserved	R	3	<b>Reserved: 000b</b>
3	M_VBUS_SNK_DISC	RW	1	0b: Interrupt masked, <b>1b: Interrupt unmasked</b>
2	M_RX_FULL	RW	1	0b: Interrupt masked, <b>1b: Interrupt unmasked</b>
1	M_FAULT	RW	1	0b: Interrupt masked, <b>1b: Interrupt unmasked</b>
0	M_VBUS_ALRM_LO	RW	1	0b: Interrupt masked, <b>1b: Interrupt unmasked</b>

**Table 21. PWRSTATMSK**

Address: 14h

Reset Value: 0xFF (Resets on POR, SW\_RST and Hard Reset)

Type: Read/Write

Bit #	Name	R/W/C	Size (Bits)	Power Status Mask Description
7	M_DEBUG_ACC	RW	1	Debug Accessory Connected Interrupt Mask 0b: Interrupt masked <b>1b: Interrupt unmasked</b>
6	M_INIT	RW	1	TCP Initialization Interrupt Mask 0b: Interrupt masked <b>1b: Interrupt unmasked</b>
5	M_SRC_HV	RW	1	Sourcing High Voltage Interrupt Mask 0b: Interrupt masked <b>1b: Interrupt unmasked</b>
4	M_SRC_VBUS	RW	1	Sourcing VBUS Interrupt Mask 0b: Interrupt masked <b>1b: Interrupt unmasked</b>
3	M_VBUS_VAL_EN	RW	1	VBUS Valid Detection Status Interrupt Mask 0b: Interrupt masked <b>1b: Interrupt unmasked</b>
2	M_VBUS_VAL	RW	1	VBUS Valid Status Interrupt Mask 0b: Interrupt masked <b>1b: Interrupt unmasked</b>
1	M_VCONN_VAL	RW	1	VCONN Present Status Interrupt Mask 0b: Interrupt masked <b>1b: Interrupt unmasked</b>
0	M_SNKVBUS	RW	1	Sinking VBUS Status Interrupt Mask 0b: Interrupt masked <b>1b: Interrupt unmasked</b>



**Table 22. FAULTSTATMSK**

Address: 15h

Reset Value: 0x33 (Resets on POR, SW\_RST and Hard Reset)

Type: Read/Write

Bit #	Name	R/W/C	Size (Bits)	Fault Status Mask Description
7	M_ALL_REGS_RESET	RW	1	All Registers Reset to Default 0b: Interrupt masked <b>1b: Interrupt unmasked</b>
6	Reserved	R	1	<b>Reserved: 0b</b>
5	M_AUTO_DISCH_FAIL	RW	1	Auto Discharge Fail Interrupt Mask 0b: Interrupt masked <b>1b: Interrupt unmasked</b>
4	M_FORCE_DISCH_FAIL	RW	1	Force Discharge Fail Interrupt Mask 0b: Interrupt Masked <b>1b: Interrupt Unmasked</b>
3	Reserved	R	1	<b>Reserved: 0b</b>
2	Reserved	R	1	<b>Reserved: 0b</b>
1	M_VCONN_OCP	RW	1	VCONN OCP Interrupt Mask 0b: Interrupt Masked <b>1b: Interrupt Unmasked</b>
0	M_I2C_ERROR	RW	1	I2C Interface Error Interrupt Mask 0b: Interrupt Masked <b>1b: Interrupt Unmasked</b>

**Table 23. STD\_OUT\_CFG**

Address: 18h

Reset Value: 0x40

Type: Read/Write

Bit #	Name	R/W/C	Size (Bits)	Standard Outputs Configuration
7	TRI_STATE	R/W	1	<b>0b: Standard Output Control</b> 1b: Force all outputs to tri-state
6	Reserved	R/W	1	<b>Reserved: 0b</b>
5	Reserved	R	1	<b>Reserved: 0b</b>
4	Reserved	R	1	<b>Reserved: 0b</b>
3:2	MUX_CTRL	R/W	2	Controls MUX_S0 and MUX_S1 Outputs. <b>00b: MUX_S0 = 0, MUX_S1 = 0. No connection.</b> 01b: MUX_S0 = 1, MUX_S1 = 0. <i>USB3.1 Connected</i> 10b: MUX_S0 = 0, MUX_S1 = 1. <i>DP Alternate Mode – 4 lanes</i> 11b: MUX_S0 = 1, MUX_S1 = 1. <i>USB3.1 + Display Port Lanes 0 &amp; 1</i>
1	Reserved	R	1	<b>Reserved: 0b</b>
0	ORIENT	R/W	1	Controls ORIENT Output <b>0b: Normal (CC1 = A5, CC2 = B5, TX1 = A2/A3, RX1 = B10/B11)</b> 1b: Flipped (CC2 = A5, CC1 = B5, TX1 = B2/B3, RX1 = A10/A11)

**Table 24. TCPC\_CTRL**

Address: 19h

Reset Value: 0x00 (POR, and SW\_RST)

Type: Read/Write

Bit #	Name	R/W/C	Size (Bits)	TCPC Control Register
7:4	Reserved	R	2	<b>Reserved: 00b</b>
5	EN_WATCHDOG	R/W	1	<b>0b: Watchdog Monitoring is disabled (default)</b> 1b: Watchdog Monitoring is enabled
4	Reserved	R/W	1	<b>Reserved: 0b</b>
3:2	I2C_CLK_STRETCH	R	2	<b>00b: I2C clock stretching is disabled. Writing to these register bits will be ignored.</b>
1	BIST_TMODE	R/W	1	BIST Test Data Receive Enable <b>0b: Normal Operation. Incoming messages are stored and passed to host</b> 1b: BIST Test Mode. Receive buffer is cleared immediately after GoodCRC response.
0	ORIENT	R/W	1	Plug Orientation <b>0b: When Vconn is enabled, apply it to the CC2 pin. Monitor the CC1 pin for BMC communications if PD messaging is enabled.</b> 1b: When Vconn is enabled, apply it to the CC1 pin. Monitor the CC2 pin for BMC communications if PD messaging is enabled.

**Table 25. ROLECTRL**

Address: 1Ah

Reset Value (Note 19) 0x0F for FUSB308 without VDD and 0x05 with VDD

Type: Read/Write

Bit #	Name	R/W/C	Size (Bits)	Role Control Description
7	Reserved	R	1	<b>Reserved: 0b</b>
6	DRP (Note 19, 20)	R/W	1	0b: No DRP. Bits B3..0 determine Rp/Rd/Ra settings 1b: DRP
5:4	RP_VAL	R/W	2	00b: Rp default 01b: Rp 1.5 A 10b: Rp 3.0 A 11b: Reserved
3:2	CC2_TERM (Note 21, 22)	R/W	2	00b: Ra 01b: Rp (Use Rp definition in B5..4) 10b: Rd 11b: Open (Disconnect or don't care)
1:0	CC1_TERM (Note 21, 22)	R/W	2	00b: Ra 01b: Rp (Use Rp definition in B5..4) 10b: Rd 11b: Open (Disconnect or don't care)

18. Reset values are loaded on either VBUS or VDD power up.

19. Rp value is defined in B5..4 when performing the DRP toggling as well as when a connection is resolved.

20. The FUSB308B toggles CC1 &amp; CC2 after receiving a.LOOK4CON and until a connection is detected. Upon connection, the FUSB308B resolves to either an Rp or Rd and report the CC1/CC2 State in the CCSTAT register. The FUSB308B will continue to present the resolved Rd or Rp regardless of any changes voltage on the CC wires.

21. When CCx\_TERM bits are set to Open and DRP = 0, the PHY and CC comparators will power down.

22. If DRP = 1,.LOOK4CON starts toggling with the value set in CC1\_TERM/CC2\_TERM. If CC1\_TERM/CC2\_TERM is different than Rp/Rp or Rd/Rd, the COMMAND will be ignored.

**Table 26. FAULTCTRL**

Address: 1Bh

Reset Value: 0x00

Type: Read/Write

Bit #	Name	R/W/C	Size (Bits)	Fault Control Description
7:4	Reserved	R	4	<b>Reserved: 0000b</b>
3	DISCH_TIMER_DIS	R/W	1	Auto and Force VBUS Discharge Timer Enable <b>0b: VBUS Discharge timer is enabled</b> 1b: VBUS Discharge timer is disabled
2	Reserved	R	1	<b>Reserved: 0b</b>
1	Reserved	R	1	<b>Reserved: 0b</b>
0	VCONN_OCP_DIS	R/W	1	VCONN OCP Enable <b>0b: VCONN OCP Enabled</b> 1b: VCONN OCP Disabled

**Table 27. PWRCTRL**

Address: 1Ch

Reset Value: 0x60

Type: Read/Write

Bit #	Name	R/W/C	Size (Bits)	Power Control Description
7	Reserved	R	1	<b>Reserved: 0b</b>
6	DIS_VBUS_MON (Note 23)	R/W	1	Controls <b>VBUS_VOLTAGE_L</b> Monitoring. 0b: VBUS Voltage Monitoring is enabled <b>1b: VBUS Voltage Monitoring is disabled</b>
5	DIS_VALARM	R/W	1	Disables <b>VALARMHCFGL</b> and <b>VALARMLCFGL</b> 0b: Voltage Alarm reporting is enabled <b>1b: Voltage Alarm reporting is disabled</b>
4	AUTO_DISCH (Notes 24, 26)	R/W	1	Auto Discharge on Disconnect 0b: Turn Off Automatically Discharge VBUS based on VBUS Voltage <b>1b: Turn On Automatically Discharge VBUS based on VBUS Voltage</b>
3	EN_BLEED_DISCH (Note 28)	R/W	1	Enable Bleed Discharge <b>0b: Disable bleed discharge of VBUS</b> 1b: Enable bleed discharge of VBUS
2	FORCE_DISCH (Note 25, 27)	R/W	1	Force Discharge <b>0b: Disable forced discharge of VBUS</b> 1b: Enable forced discharge of VBUS
1	VCONN_PWR	R/W	1	VCONN Power Supported <b>Writing this bit has no function. Please use VCONN_OCP to set OCP values</b>
0	EN_VCONN	R/W	1	Enable VCONN 0b: Disable VCONN Source (default) 1b: Enable VCONN Source to CC

23. If VBUS\_MON is disabled, VBUS\_VOLTAGE\_L and VBUS\_VOLTAGE\_H reports all zeroes.

24. Setting this bit in a Source FUSB308B triggers the following actions upon disconnection detection:

1. Disable sourcing power over Vbus
2. VBUS discharge

25. Sourcing power over Vbus shall be disabled before or at same time as starting VBUS discharge.

26. Setting this bit in a Sink FUSB308B triggers the following action upon disconnection detection:

1. VBUS discharge

27. The FUSB308B will automatically disable discharge once the voltage on VBUS is below vSafe0V (max.).

28. Bleed Discharge is a low current discharge to provide a minimum load current if needed.

**Table 28. CCSTAT**

Address: 1Dh

Reset Value: 0x00

Type: Read

Bit #	Name	R/W/C	Size (Bits)	CC Status Description (Note 29)
7:6	Reserved	R	2	<b>Reserved: 00b</b>
5	LOOK4CON	R	1	<b>0b: the FUSB308B is not looking for connection or indicated a potential connection has been found when transitioned from a 1 to 0</b> 1b: the FUSB308B looking for connection
4	CON_RES	R	1	<b>0b: the FUSB308B is presenting Rp</b> 1b: the FUSB308B is presenting Rd This bit is only valid if the FUSB308B was a DRP and has stopped DRP toggling
3:2	CC2_STAT	R	2	If (ROLE_CONTROL.CC2 = Rp) or (CON_RES = 0) <b>00b: SRC.Open (Open, Rp)</b> 01b: SRC.Ra (below maximum vRa) 10b: SRC.Rd (within the vRd range) 11b: reserved If (ROLE_CONTROL.CC2 = Rd) or (CON_RES = 1) 00b: SNK.Open (Below maximum vRa) 01b: SNK.Default (Above minimum vRd-Connect) 10b: SNK.Power1.5 (Above minimum vRd-Connect) Detects Rp 1.5 A 11b: SNK.Power3.0 (Above minimum vRd-Connect) Detects Rp 3.0 A If ROLE_CONTROL.CC2 = Ra, this field is set to 00b If ROLE_CONTROL.CC2 = Open, this field is set to 00b This field always returns 00b if (LOOK4CON = 1) or (PWRCTRL.EN_VCONN = 1 and TPCP_CONTROL.PlugOrientation = 0). Otherwise, the returned value depends upon ROLE_CONTROL.CC2.
1:0	CC1_STAT	R	2	If (ROLE_CONTROL.CC1 = Rp) or (CON_RES = 0) <b>00b: SRC.Open (Open, Rp)</b> 01b: SRC.Ra (below maximum vRa) 10b: SRC.Rd (within the vRd range) 11b: reserved If (ROLE_CONTROL.CC1 = Rd) or CON_RES = 1) 00b: SNK.Open (Below maximum vRa) 01b: SNK.Default (Above minimum vRd-Connect) 10b: SNK.Power1.5 (Above minimum vRd-Connect) Detects Rp-1.5 A 11b: SNK.Power3.0 (Above minimum vRd-Connect) Detects Rp-3.0 A If ROLE_CONTROL.CC1 = Ra, this field is set to 00b If ROLE_CONTROL.CC1 = Open, this field is set to 00b This field always returns 00b if (LOOK4CON = 1) or (PWRCTRL.EN_VCONN = 1 and TPCP_CONTROL.PlugOrientation = 0). Otherwise, the returned value depends upon ROLE_CONTROL.CC1.

29. An event change on this register cause an ALERTL.I\_CCSTAT Interrupt.

**Table 29. PWRSTAT**

Address: 1Eh

Reset Value: 08h

Type: Read

Bit #	Name	R/W/C	Size (Bits)	Power Status Description (Note 30)
7	DEBUG_ACC	R	1	Debug Accessory Attached <b>0b: No Debug Accessory Connected</b> 1b: Debug Accessory Connected Reflects the state of the DEBUG_ACC Output if present
6	TCPC_INIT	R	1	FUSB308B Initialization Status <b>0b: The FUSB308B has completed initialization and all registers are valid</b> 1b: The FUSB308B is still performing internal initialization. Registers 00–0Fh are valid
5	SOURCE_HV	R	1	Sourcing High Voltage. See Transition Flow Charts for details. <b>0b: vsafe5V</b> 1b: High Voltage
4	SOURCE_VBUS	R	1	Sourcing VBUS. Output SRC asserted. 0b: Sourcing VBUS is disabled 1b: Sourcing VBUS is enabled
3	VBUS_VAL_EN	R	1	VBUS_VAL (below) Detection Circuit Status 0b: VBUS_VAL Detection is Disabled 1b: VBUS_VAL Detection is Enabled
2	VBUS_VAL	R	1	VBUS Present <b>0b: Vbus disconnected (below 3.5 V)</b> 1b: VBUS connected (Above 4.0 V)
1	VCONN_VAL	R	1	VCONN Present <b>0b: VCONN is not present or PWRCTRL.EN_VCONN is disabled</b> 1b: This bit is asserted when VCONN is present on CC1 or CC2 Threshold is fixed at 2.4 V
0	SNKVBUS	R	1	Sink VBUS. Output SNK asserted. <b>0b: Sink is disconnected or not supported</b>

30. An event change on this register cause an ALERTL.I\_PWRSTAT Interrupt.

**Table 30. FAULTSTAT**

Address: 1Fh

Reset Value: 0x80

Type: Read/Write 1 to Clear

Bit #	Name	R/W/C	Size (Bits)	Fault Status Interrupt Description (Note 32)
7	ALL_REGS_RESET (Note 31)	R/WC	1	0b: No reset occurred <b>1b: POR or unexpected power reset occurred</b> This bit is asserted when the TCPC resets all registers to their default value. This happens at initial power up or if an unexpected power reset occurs
6	Reserved	R	1	<b>Reserved: 0b</b>
5	AUTO_DISCH_FAIL	R/WC	1	<b>0b: No Discharge Failure</b> 1b: VBUS Discharge Failed Asserts when PWRCTRL.AUTO_DISCH is set and FUSB308B fails to discharge VBUS to vSafe5V (max.) within tSafe5V or vSafe0V(max.) within tSafe0V from disconnection is detected.

**Table 30. FAULTSTAT** (continued)

Address: 1Fh

Reset Value: 0x80

Type: Read/Write 1 to Clear

Bit #	Name	R/W/C	Size (Bits)	Fault Status Interrupt Description (Note 32)
4	FORCE_DISCH_FAIL	R/WC	1	<b>0b: No Discharge Failure</b> 1b: VBUS Discharge Failed Asserts when PWRCTRL.FORCE_DISCH is set and one of the following occurs: If VBUS_STOP_DISCH <= vSafe0V(max.) we fail to discharge VBUS to vSafe0V (max.) within tSafe0V from the time FORCE_DISCH is set. If VBUS_STOP_DISCH > vSafe0V(max.) we fail to discharge VBUS to VBUS_STOP_DISCH within tSrcSettle from the time FORCE_DISCH is set.
3	Reserved	R	1	<b>Reserved: 0b</b>
2	Reserved	R	1	<b>Reserved: 0b</b>
1	VCONN_OCP	R/WC	1	<b>0b: No VCONN Over-Current Detected</b> 1b: Over current on VCONN Latched. See VCONN_ Registers to set VCONN OCP levels.
0	I2C_ERROR	R/WC	1	<b>0b: No Error</b> 1b: I2C Error has occurred Asserts when: or SINK_TRANSMIT has been sent with TRANSMIT_BUFFER empty (TXBYTECNT < 2). COMMAND.DisableVbusDetect is issued while sinking or sourcing VBUS.COMMAND.SinkVbus is issued while sourcing VBUS.COMMAND.SourceVbusDefaultVoltage is issued while sinking VBUS  COMMAND.SourceVbusHighVoltage is issued when device is not already sourcing 5 V, is sinking, or is not capable of sourcing high voltage.  Connect_Invalid State is reached.

31. VBUS\_V\_BIT[9:0] is the measured VBUS voltage divided by VBUS\_SCALE factor.

32. Fault Status are latched and cleared when a 1 is written to the corresponding bit.

33. ALL\_REGS\_RESET do not get set on SW\_RST

**Table 31. COMMAND**

Address: 23h

Reset Value: 0x00

Type: Read/Write (Auto-Clear)

Bit #	Name	R/W/C	Size (Bits)	Register Settings	COMMAND Description
7:0	Command	R/W	8	0001 0001b	<b>Wakel2C</b> (no action is taken other than to wake the I2C interface)
				0010 0010b	<b>DisableVbusDetect.</b> Disable Vbus present detection: PWRSTAT.VBUS_VAL. The FUSB308B will ignore this command and assert the FAULTSTAT.I2C_ERR if it has sourcing or sinking power over Vbus enabled
				0011 0011b	<b>EnableVbusDetect.</b> Enable Vbus present detection
				0100 0100b	<b>DisableSinkVbus.</b> Disable sinking power over Vbus. This COMMAND does not disable PWRSTAT.VBUS_VAL detection
				0101 0101b	<b>SinkVbus.</b> Enable sinking power over Vbus and enable Vbus present detection. The FUSB308B will ignore this command and assert the FAULTSTAT.I2C_ERR if it has sourcing power over Vbus enabled

**Table 31. COMMAND** (continued)

Address: 23h

Reset Value: 0x00

Type: Read/Write (Auto-Clear)

Bit #	Name	R/W/C	Size (Bits)	Register Settings	COMMAND Description
				0110 0110b	<b>DisableSourceVbus.</b> Disable sourcing power over Vbus. This COMMAND does not disable PWRSTAT.VBUS_VAL detection
				0111 0111b	<b>SourceVbusDefaultVoltage.</b> Enable sourcing vSafe5V over Vbus and enable Vbus present detection. Source shall transition to vSafe5V if at a high voltage. The FUSB308B will ignore this command and assert the FAULTSTAT.I2C_ERR if it has sinking power over Vbus enabled
				1000 1000b	<b>SourceVbusHighVoltage.</b> Execute sourcing high voltage over Vbus. FUSB308B will ignore this command and assert the FAULTSTAT.I2C_ERR
				1001 1001b	<b>LOOK4CON.</b> Start DRP Toggling if ROLECTRL.DRP = 1b. If ROLECTRL.CC1/CC2 = 01b start with Rp, if ROLECTRL.CC1/CC2 = 10b start with Rd. If ROLE_CONTROL.CC1/CC2 are not either 01b/01b or 10b/10b, then do not start toggling. The TCPM shall issue . <b>COMMAND.LOK4CON</b> to enable the device to restart Connection Detection in cases where the ROLECTRL contents will not change. An example of this is when a potential connection as a Source occurred but was further debounced by the TCPM to find the Sink disconnected. In this case a Source Only or DRP should go back to its Unattached.Src state. This would result in ROLECTRL staying the same
				1010 1010b	<b>RxOneMore.</b> Configure the receiver to automatically clear the RXDETECT register after sending the next GoodCRC. This is used to shutdown reception of packets at a known point regardless of packet separation or the depth of the receive FIFO in the device
				1100 1100b 1101 1101b 1110 1110b	Reserved. No Action
				1111 1111b	<b>I2CIdle,</b> Enter I2C Idle

**Table 32. DEVCAP1L**

Address: 24h

Reset Value: FUSB308B: DBh

Type: Read

Bit #	Name	R/W/C	Size (Bits)	Device Capabilities 1 L Description
7:5	ROLES_SUPPORT	R	3	Roles Supported: 000b: Type-C Port Manager can configure the Port as Source only or Sink only (not DRP) 001b: Source only 010b: Sink only 011b: Sink with accessory support 100b: DRP Only 101b: Source, Sink, DRP, Adapter/Cable all supported <b>110b: Source, Sink, DRP</b> 110..111b: Not valid
4	SOP_SUPPORT	R	1	0b: All SOP* except SOP'_DBG/SOP''_DBG <b>1b: All SOP* messages are supported</b>

**Table 32. DEVCAP1L** (continued)

Address: 24h

Reset Value: FUSB308B: DBh

Type: Read

Bit #	Name	R/W/C	Size (Bits)	Device Capabilities 1 L Description
3	SWITCH_VCONN	R	1	Supply VCONN: 0b: Not capable of switching VCONN <b>1b: Capable of switching VCONN</b> Support for PWRSTAT.VCONN_VAL and PWRCTRL.EN_VCONN implemented
2	SNK_VBUS	R	1	Sink VBUS: 0b: Not Capable of controlling the sink path to the system load 1b: Capable of controlling the sink path to the system load Support for PWRSTAT.SNKVBUS and COMMAND.SinkVbus implemented
1	SRC_HV	R	1	Source Higher than vSafe5V on VBUS 0b: Not capable of controlling High Voltage Path on VBUS 1b: capable of controlling High Voltage Path on VBUS Support for PWRSTAT.SOURCE_HV and COMMAND.SourceVbusHighVoltage implemented
0	SRC_VBUS	R	1	Source vSafe5V on VBUS 0b: Not of controlling the source path to VBUS <b>1b: Capable of controlling the source path to VBUS</b> Support for PWRSTAT.SOURCE_VBUS, COMMAND.SourceVbusDefaultVoltage, COMMAND.DisableSourceVbus, COMMAND.EnableVbusDetect, and COMMAND.DisableVbusDetect implemented

**Table 33. DEVCAP1H**

Address: 25h

Reset Value: 0x1E

Type: Read

Bit #	Name	R/W/C	Size (Bits)	Device Capabilities 1 H Description
7:5	Reserved	R	3	<b>Reserved : 000b</b>
4	BLEED_DIS	R	1	0b: No Bleed Discharge <b>1b: Bleed Discharge implement</b> Support for PWRCTRL.EN_BLEED_DISCH implemented.
3	FORCE_DIS	R	1	0b: No Force Discharge <b>1b: Force Discharge implement</b> Support for PWRCTRL.FORCE_DISCH, FAULTSTAT.FORCE_DISCH_FAIL, and VBUS_STOP_DISCL implemented
2	VBUS_MEAS_ALRM	R	1	<b>0b: No Vbus voltage measurement or VBUS Alarms</b> <b>1b: Vbus voltage measurement and VBUS Alarms</b> Support for VBUS_VOLTAGE_L, VALARMHCFGL and VALARMLCFGL implemented
1:0	RP_SUPPORT	R	2	Source Power Supported: 00b: Rp default only 01b: Rp 1.5 A and default <b>10b: Rp 3.0A, 1.5 A and default</b> 11b: Reserved



**Table 34. DEVCAP2L**

Address: 26h

Reset Value: 0xD7

Type: Read

Bit #	Name	R/W/C	Size (Bits)	Device Capabilities 2 L Description
7	SNK_DISC_DETECT	R	1	0b: <b>VBUS_SNK_DISCL not implemented</b> 1b: <b>VBUS_SNK_DISCL implemented</b>
6	STOP_DSICH	R	1	0b: <b>VBUS_STOP_DISCL not implemented</b> 1b: <b>VBUS_STOP_DISCL implemented</b>
5:4	VBUS_ALARM_LSB	R	2	VBUS Voltage Alarm LSB Support <b>01b: Voltage Alarm Supports 50 mV LSB</b> Bit 0 of VALARMHCFGL and VALARMLCFGL are ignored
3:1	VCONN_POWER_CAP	R	3	VCONN Power Supported 000b: 1.0 W 001b: 1.5 W 010b: 2.0 W <b>011b: 3 W (at VCONN = 5.5 V)</b> 100b: 4 W 101b: W 110b: 6 W 111b: External
0	VCONN_FAULT_CAP	R	1	VCONN OCP Fault Capable 110b: FUSB308B is not capable of detecting a VCONN fault <b>1b: FUSB308B is capable of detecting a VCONN fault</b>

**Table 35. DEVCAP2H**

Address: 27h

Reset Value: 0x01

Type: Read

Bit #	Name	R/W/C	Size (Bits)	Device Capabilities 2 H Description
7:1	Reserved	R	7	<b>Reserved: 000_0000b</b>
0	Watchdog Timer	R	1	<b>1b: Watchdog Timer Implemented</b>

**Table 36. STD\_OUT\_CAP**

Address: 29h

Reset Value: FUSB308B: 0x05

Type: Read

Bit #	Name	R/W/C	Size (Bits)	Standard Outputs Capabilities Description
7	Reserved	R	1	<b>Reserved: 00b</b>
6	DEBUG_ACC	R	1	0b: Debug Accessory Indicator Not Present 1b: Debug Accessory Indicator Present
5	VBUS_MON	R	1	<b>0b: VBUS Present Monitor Not Present</b>
4	AUDIO_ACC	R	1	<b>0b: Audio Adapter Accessory Indicator Not Present</b>
3	ACTIVE_CABLE	R	1	<b>0b: Active Cable Indicator not Present</b>
2	MUX_CTRL	R	1	0b: Mux Control Not Present <b>1b: Mux Control Present</b>
1	CON_PRESENT	R	1	<b>0b: Connection Present indicator not implemented</b>
0	ORIENT	R	1	<b>1b: Connector Orientation Present</b>

**Table 37. MSGHEADR**

Address: 2Eh

Reset Value: FUSB308B: 0x0B

Type: Read/Write

Bit #	Name	R/W/C	Size (Bits)	Message Header Info Description
7:5	Reserved	R	3	Reserved: 000b
4	CBL_PLUG	R/W	1	Cable Plug <b>0b: Message originated from Source, Sink, or DRP</b> 1b: Message originated from a Cable Plug
3	DATA_ROLE	R/W	1	Data Role <b>0b: SINK</b> 1b: SOURCE
2:1	USBPD_REV	R/W	2	USB-PD Specification Revision 00b: Revision 1.0 <b>01b: Revision 2.0</b> 10b – 11b: Reserved
0	POWER_ROLE	R/W	1	Power Role <b>0b: Sink</b> 1b: Source

**Table 38. RXDETECT**

RXDETECT enables the types of messages and/or signaling to be detected. SOP\* enabling also turns on auto-GoodCRC response. This register is reset when: A Hard Reset is received or sent; after the GoodCRC transmission due to RxOneMore; on a disconnect detection; SW\_RST or POR.

Address: 2Fh

Reset Value: 0x00

Type: Read/Write

Bit #	Name	R/W/C	Size (Bits)	Receive Detect Description (Note 34)
7	Reserved	R	1	<b>Reserved: 0b</b>
6	EN_CABLE_RST	R	1	<b>0b: Do not detect Cable Reset signaling</b>
5	EN_HRD_RST	R/W	1	<b>0b: Do not detect Hard Reset signaling (default)</b> 1b: Detect Hard Reset signaling
4	EN_SOP2_DBG	R/W	1	<b>0b: Do not detect SOP_DBG" message (default)</b> 1b: Detect SOP_DBG" message
3	EN_SOP1_DBG	R/W	1	<b>0b: Do not detect SOP_DBG' message (default)</b> 1b: Detect SOP_DBG' message
2	EN_SOP2	R/W	1	<b>0b: Do not detect SOP" message (default)</b> 1b: Detect SOP" message
1	EN_SOP1	R/W	1	<b>0b: Do not detect SOP' message (default)</b> 1b: Detect SOP' message
0	EN_SOP	R/W	1	<b>0b: Do not detect SOP message (default)</b> 1b: Detect SOP message

34. Writing all 0s to this register disables PD.

**Table 39. RXBYTECNT**

Address: 30h

Reset Value: 0x00

Type: Read

Bit #	Name	R/W/C	Size (Bits)	Received Byte Count Description
7:0	RXBYTECNT	R	8	<b>Number of Bytes Received. This is the number of bytes in RX-DATA plus 3 (RXSTAT and RXHEADL, H)</b>

**Table 40. RXSTAT**

This register indicates the status of the received SOP\* message in RXHEADL, RXHEADH, and RXDATA registers.  
Address: 31h  
Reset Value: 0x00  
Type: Read

Bit #	Name	R/W/C	Size (Bits)	Receive Status Description
7:3	Reserved	R	5	<b>Reserved: 00000b</b>
2:0	RXSOP	R	3	Received SOP <b>000b: Received SOP</b> 001b: Received SOP' 010b: Received SOP'' 011b: Received SOP' DBG 100b: Received SOP'' DBG 110b: Received Cable Reset All others are reserved.

**Table 41. RXHEADL**

Received Header Low byte is stored here. Expected GoodCRC messages are not stored.  
Address: 32h  
Reset Value: 0x00  
Type: Read

Bit #	Name	R/W/C	Size (Bits)	Receive Header Low Description
7:0	RXHEADL	R	8	<b>Rx Header Data Low</b>

**Table 42. RXHEADH**

Received Header High byte is stored here. Expected GoodCRC messages are not stored.  
Address: 33h  
Reset Value: 0x00  
Type: Read

Bit #	Name	R/W/C	Size (Bits)	Receive Header High Description
7:0	RXHEADH	R	8	<b>Rx Header Data High</b>

**Table 43. RXDATA**

Address: 34h–4Fh  
Reset Value: 0x00  
Type: Read

Bit #	Name	R/W/C	Size (Bits)	Receive Payload Description
27:0	RXDATA0..27	R	8	<b>Rx Payload</b>

**Table 44. TRANSMIT**

Writing this register will start a PD transmission. If Cable Reset, Hard Reset or BIST Carrier Mode 2 is written, RETRY\_CNT is ignored and signaling is not retried.  
Address: 50h  
Reset Value: 0x00  
Type: Read/Write

Bit #	Name	R/W/C	Size (Bits)	Transmit Description
7:6	Reserved	R	2	<b>Reserved: 00b</b>
5:4	RETRY_CNT	R/W	2	Retry Counter <b>00b: No message retry is required</b> 01b: Automatically retry message transmission once 10b: Automatically retry message transmission twice 11b: Automatically retry message transmission three times

**Table 44. TRANSMIT** (continued)

Writing this register will start a PD transmission. If Cable Reset, Hard Reset or BIST Carrier Mode 2 is written, RETRY\_CNT is ignored and signaling is not retried.

Address: 50h

Reset Value: 0x00

Type: Read/Write

Bit #	Name	R/W/C	Size (Bits)	Transmit Description
3	Reserved	R	1	Reserved: 0b
2:0	TXSOP	R/W	3	<b>Transmit SOP Message</b> <b>000b: Transmit SOP</b> 001b: Transmit SOP' 010b: Transmit SOP" 011b: Transmit SOP_DBG' 100b: Transmit SOP_DBG" 101b: Transmit Hard Reset 110b: Transmit Cable Reset 111b: Transmit BIST Carrier Mode 2 (Enabled for <i>tBISTContMode</i> )

**Table 45. TXBYTECNT**

Address: 51h

Reset Value: 0x00

Type: Read/Write

Bit #	Name	R/W/C	Size (Bits)	Transmit Byte Count Description
7:0	TXBYTECNT	R/W	8	Number of bytes to be transmitted

**Table 46. TXHEADL**

Address: 52h

Reset Value: 0x00

Type: Read/Write

Bit #	Name	R/W/C	Size (Bits)	Transmit Header Low Description
7:0	TXHEADL	R/W	8	Transmit Header Low

**Table 47. TXHEADH**

Address: 53h

Reset Value: 0x00

Type: Read/Write

Bit #	Name	R/W/C	Size (Bits)	Transmit Header High Description
7:0	TXHEADH	R/W	8	Transmit Header High

**Table 48. TXDATA**

Addresses: 54–6Fh

Reset Value: 0x00

Type: Read/Write

Bit #	Name	R/W/C	Size (Bits)	Transmit Payload Description
27:0	TXDATA0..27	R/W	8	Payload to be transmitted

**Table 49. VBUS\_VOLTAGE\_L**

Address: 70h  
Reset Value: 0x00  
Type: Read

Bit #	Name	R/W/C	Size (Bits)	VBUS Voltage Low Description
Byte 27:0	TX_Data27..0	RW	8	TX Payload

**Table 50. VBUS\_VOLTAGE\_H**

Address: 71h  
Reset Value: 0x00  
Type: Read

Bit #	Name	R/W/C	Size (Bits)	VBUS Voltage High Description (Note 35)
7:4	Reserved	R	4	Reserved: 0000b
3:2	VBUS_SCALE	R	2	00b: VBUS Measurement not scaled 01b: VBUS Measurement divided by 2 10b: VBUS Measurement divided by 4 11b: Reserved
1	VBUS_V_BIT9	R	1	Bit 9 of VBUS Measurement
0	VBUS_V_BIT8	R	1	Bit 8 of VBUS Measurement

35. VBUS\_V\_BIT[9:0] is the measured VBUS voltage divided by VBUS\_SCALE factor.

**Table 51. VBUS\_SNK\_DISCL**

Address: 72h  
Reset Value: 0xA0 (< vSafe5V: 4.0 V)  
Type: Read/Write

Bit #	Name	R/W/C	Size (Bits)	VBUS SINK Disconnect Threshold Low (Note 36)
7:0	VBUS_SNK_DISC	R/W	8	Bits 7:0 of Sink Disconnect threshold

36. Accuracy is set for 50 mV LSB and Bit 0 is ignored.

**Table 52. VBUS\_SNK\_DISCH**

Address: 73h  
Reset Value: 0x00  
Type: Read/Write

Bit #	Name	R/W/C	Size (Bits)	VBUS SINK Disconnect Threshold High
7:2	Reserved	R	6	Reserved: 000000b
1:0	VBUS_SNK_DISC	R/W	2	Bits 9:8 of Sink Disconnect threshold

**Table 53. VBUS\_STOP\_DISCL**

Address: 74h  
Reset Value: 0x1C (< vSafe0V: 700 mV)  
Type: Read/Write

Bit #	Name	R/W/C	Size (Bits)	VBUS Stop Discharge Threshold Low (Note 37)
7:0	VBUS_VTH_LO	R/W	8	Bits 7:0 of Stop Discharge threshold

37. Accuracy is set for 50 mV LSB and Bit 0 is ignored.

**Table 54. VBUS\_STOP\_DISCH**

Address: 75h

Reset Value: 0x00

Type: Read/Write

Bit #	Name	R/W/C	Size (Bits)	VBUS Stop Discharge Threshold High
7:2	Reserved	R	6	Reserved: 000000b
1:0	VBUS_VTH_LO	R/W	2	Bits 9:8 of Stop Discharge threshold

**Table 55. VALARMHCFGL**

Address: 76h

Reset Value: 0x00

Type: Read/Write

Bit #	Name	R/W/C	Size (Bits)	Voltage Alarm High Trip Point Configuration Low Description (Note 38)
7:0	VBUS_VTH_HI	R/W	8	Bits 7:0 of High trip point alarm

38. Accuracy is set for 50 mV LSB and Bit 0 is ignored.

**Table 56. VALARMHCFGH**

Address: 77h

Reset Value: 0x00

Type: Read/Write

Bit #	Name	R/W/C	Size (Bits)	Voltage Alarm High Trip Point Configuration High Description
7:2	Reserved	R	6	Reserved: 000000b
1:0	VBUS_VTH_HI	R/W	2	Bits 9:8 of High trip point alarm

**Table 57. VALARMLCFGL**

Address: 78h

Reset Value: 0x00

Type: Read/Write

Bit #	Name	R/W/C	Size (Bits)	Voltage Alarm Low Trip Point Configuration Low Description (Note 39)
7:0	VBUS_VTH_LO	R/W	8	Bits 7:0 of Low trip point alarm

39. Accuracy is set for 50 mV LSB and Bit 0 is ignored.

**Table 58. VALARMLCFGH**

Address: 79h

Reset Value: 0x00

Type: Read/Write

Bit #	Name	R/W/C	Size (Bits)	Voltage Alarm Low Trip Point Configuration High Description
7:2	Reserved	R	6	Reserved: 000000b
1:0	VBUS_VTH_LO	R/W	2	Bits 9:8 of Low trip point alarm

**Table 59. VCONN\_OCP**

Address: A0h

Reset Value: 0x0F

Type: Read/Write

Bit #	Name	R/W/C	Size (Bits)	VCONN Current Limit Description (Note 40)
7:4		R	4	Reserved: 0b
3	OCP_RANGE	R/W	1	0b: OCP Range between 10 mA – 80 mA (max_range = 80 mA) 1b: OCP Range between 100 mA – 800 mA (max_range = 800 mA)
2:0	OCP_CUR	R/W	3	000b: max_range/8 001b: 2 × max_range/8 010b: 3 × max_range/8 011b: 4 × max_range/8 100b: 5 × max_range/8 101b: 6 × max_range/8 110b: 7 × max_range/8 111b: max_range (see OCP_RANGE definition above)

40. Only used if VCONN\_OCP Register PWRCTRL.EN\_VCONN is set to 1.

**Table 60. RESET**

Address: A2h

Reset Value: 0x00

Type: Read/Write (Self Clearing)

Bit #	Name	R/W/C	Size (Bits)	Reset Description
7:2	Reserved	R	6	Reserved:000000b
1	PD_RST	R/W	1	0b: No Action 1b: Reset PD-PHY and PD-FSMs
0	SW_RST	R/W	1	0b: No Action 1b: Reset all registers to default

**Table 61. GPIO1\_CFG**

Address: A4h

Reset Value: 0x00

Type: Read/Write

Bit #	Name	R/W/C	Size (Bits)	General Purpose I/O 1 Configuration
7:3	Reserved	R	5	Reserved:00000b
2	GPO1_VAL	R/W	1	If GPO1_EN = 1 0b: Set output = 0 1b: Set output = 1 if GPO1_EN = 1
1	GPI1_EN	R/W	1	0b: Input buffer disabled 1b: Input Buffer enabled (Input state can be read in GPIO_STAT Register)
0	GPO1_EN	R/W	1	0b: GPO is High-Z 1b: GPO is enabled

**Table 62. GPIO2\_CFG**

Address: A5h

Reset Value: 0x00

Type: Read/Write

Bit #	Name	R/W/C	Size (Bits)	General Purpose I/O 2 Configuration
7:4	Reserved	R	4	Reserved:0000b
3	Reserved	R/W	1	Reserved: 0b

**Table 62. GPIO2\_CFG** (continued)

Address: A5h

Reset Value: 0x00

Type: Read/Write

Bit #	Name	R/W/C	Size (Bits)	General Purpose I/O 2 Configuration
2	GPO2_VAL	R/W	1	<b>Generic GPIO Function</b> If GPO2_EN=1 & FR_SWAP_FN = 0 0b: Set output = 0 1b: Set output = 1
1	GPI2_EN	R/W	1	<b>Generic GPIO Function</b> If FR_SWAP_FN = 0 0b: Input buffer disabled 1b: Input Buffer enabled (Input state can be read in GPIO_STAT Register)
0	GPO2_EN	R/W	1	<b>0b: GPO is High-Z</b> 1b: GPO is enabled

**Table 63. GPIO\_STAT**

Address: A6h

Reset Value: 0x00

Type: Read

Bit #	Name	R/W/C	Size (Bits)	General Purpose I/O Input Status
7:2	Reserved	R	6	<b>Reserved: 000000b</b>
1	GPI2_VAL	R	1	<b>If GPI2_EN</b> <b>0b: GPIO2 Input is Low</b> 1b: GPIO2 Input is High
0	GPI1_VAL	R	1	<b>If GPI2_EN</b> <b>0b: GPIO1 Input is Low</b> 1b: GPIO1 Input is High

**Table 64. DRPTOGGLE**

Address: A7h

Reset Value: 0x00

Type: Read/Write

Bit #	Name	R/W/C	Size (Bits)	DRP Toggle Timing
7:3	Reserved	R	6	<b>Reserved: 00000b</b>
1:0	DRPTOGGLE	R/W	2	<b>00b: tToggleSrc = 15 ms to 30 ms; tToggleSnk = 35 ms to 70 ms</b> 01b: tToggleSrc = 20 ms to 40 ms; tToggleSnk = 30 ms to 60 ms 10b: tToggleSrc = 25 ms to 50 ms; tToggleSnk = 25 ms to 50 ms 11b: tToggleSrc = 30 ms to 60 ms; tToggleSnk = 20 ms to 40 ms

**Table 65. SRC\_FRSWAP**

Address: B1h

Reset Value: 0x00

Type: Read/Write

Bit #	Name	R/W/C	Size (Bits)	Source Fast Role Swap
7:0	Reserved	R	4	Reserved: 0x00



**Table 66. SNK\_FRSWAP**

Address: B2h

Reset Value: 0x00

Type: Read/Write (Auto-Clear on detect)

Bit #	Name	R/W/C	Size (Bits)	Sink Fast Role Swap
7:0	Reserved	R	8	Reserved:0000000b

**Table 67. ALERT\_VD**

Address: B3h

Reset Value: 0x00

Type: Read/Write 1 to clear

Bit #	Name	R/W/C	Size (Bits)	Vendor Defined Alert
7	Reserved	R	1	Reserved: 0b
6	I_DISCH_SUCC	R/W/C	1	0b: No Interrupt 1b: Auto Discharge or Force Discharge Successful
5	I_GPI2	R/W/C	1	0b: No Interrupt 1b: Input GPI2 change occurred
4	I_GPI1	R/W/C	1	0b: No Interrupt 1b: Input GPI1 change occurred
3	I_VDD_DTCT	R/W/C	1	0b: No Interrupt 1b: VDD detection change occurred (read VD_STAT)
2	I_OTP	R/W/C	1	0b: No Interrupt 1b: OTP condition occurred
1	I_SWAP_TX	R/W/C	1	0b: No Interrupt 1b: Fast role Swap sent due to GPIO input set low
0	I_SWAP_RX	R/W/C	1	0b: No Interrupt 1b: Fast Role Swap request received

**Table 68. ALERT\_VD\_MSK**

Address: B4h

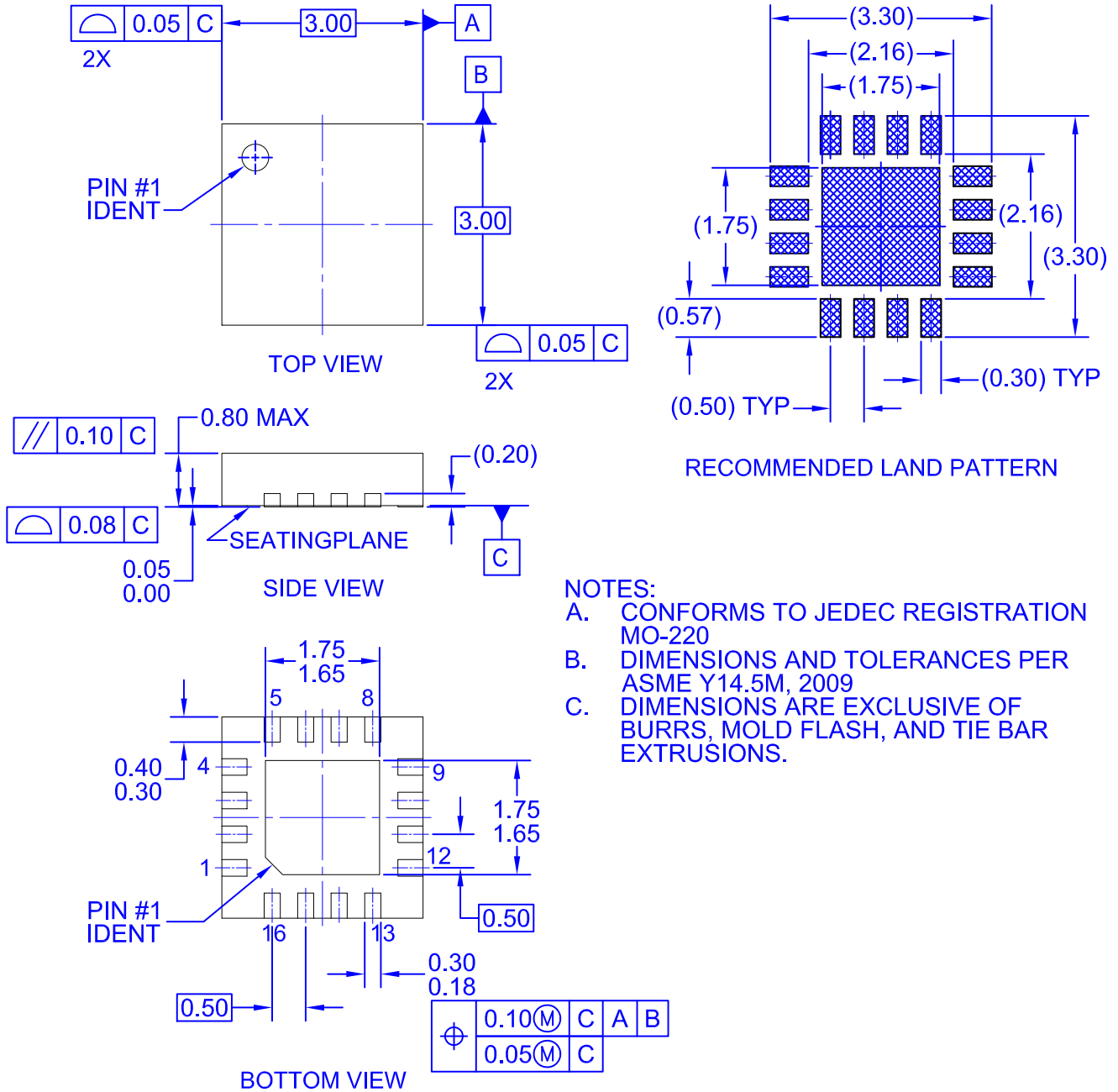
Reset Value: 0x7F


Type: Read/Write

Bit #	Name	R/W/C	Size (Bits)	Vendor Defined Alert Masks
7	Reserved	R	1	Reserved:0b
6	M_DISCH_SUCC	R/W	1	0b: Interrupt masked 1b: Interrupt unmasked
5	M_GPI2	R/W	1	0b: Interrupt masked 1b: Interrupt unmasked
4	M_GPI1	R/W	1	0b: Interrupt masked 1b: Interrupt unmasked
3	M_VDD_DTCT	R/W	1	0b: Interrupt masked 1b: Interrupt unmasked
2	M_OTP	R/W	1	0b: Interrupt masked 1b: Interrupt unmasked
1	Reserved	R/W	1	0b: Interrupt masked 1b: Interrupt unmasked
0	Reserved	R/W	1	0b: Interrupt masked 1b: Interrupt unmasked

PACKAGE DIMENSIONS

WQFN16 3 x 3, 0.5P  
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