

Description

The MCP14H2304 is a high-voltage, high-speed gate driver capable of driving N-channel MOSFETs and IGBTs in a half-bridge configuration. The device's high voltage process enables the MCP14H2304 high-side to switch to 600V in a bootstrap operation.

The MCP14H2304 logic inputs are compatible with standard TTL and CMOS levels (down to 3.3V) to interface easily with controlling devices. The driver outputs feature high pulse current buffers designed for minimum driver cross conduction. MCP14H2304 has an internal deadtime of 100 ns to protect high-voltage MOSFETs against shoot-through.

The MCP14H2304 is offered in an SOIC-8 narrow package and operates over an extended -40°C to $+125^{\circ}\text{C}$ temperature range.

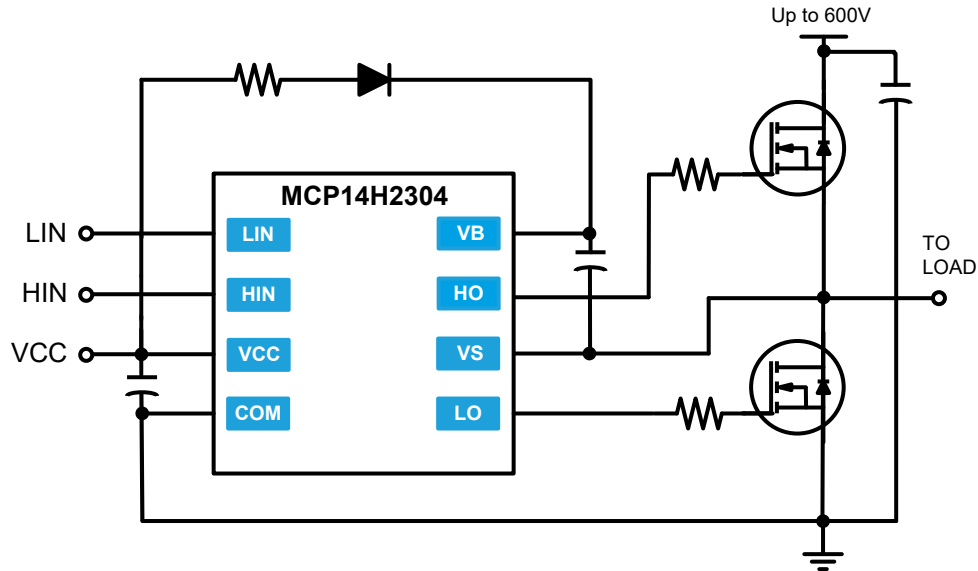
Features

- Drives Two N-channel MOSFETs or IGBTs in a Half-Bridge Configuration
- Floating High-Side Driver in Bootstrap Operation to 600V
- 290 mA Source/600 mA Sink Output Current Capability
- Outputs Tolerant to Negative Transients
- Internal Logic and Deadtime (100 ns) to Protect the MOSFET
- Logic Input (HIN and LIN) 3.3V Capability
- Schmitt Triggered Logic Inputs With Internal Pull Down
- Undervoltage Lockout for High-Side and Low-Side Drivers
- Extended Temperature Range: -40°C to $+125^{\circ}\text{C}$

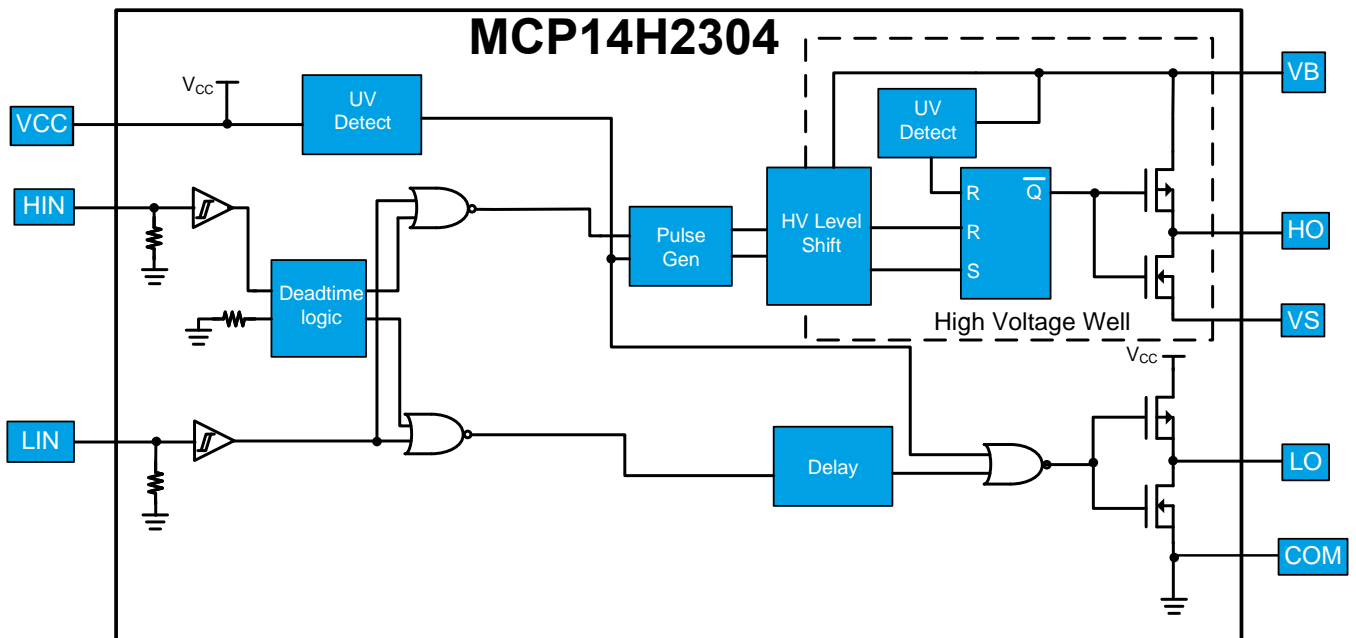
Applications

- Motor Controls
- AC-DC Inverters
- DC-DC Converters
- Class D Power Amplifiers

Typical Application



Block Diagram

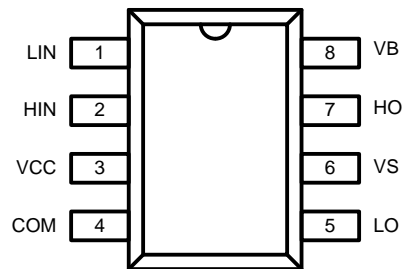


1. Pin Configuration

Pin No.	Pin Name	Pin Description
1	LIN	Logic input for low-side gate driver output, in phase with LO
2	HIN	Logic input for high-side gate driver output, in phase with HO
3	VCC	Low-side and logic fixed supply
4	COM	Low-side and logic return
5	LO	Low-side gate drive output
6	VS	High-side floating supply return
7	HO	High-side gate drive output
8	VB	High-side floating supply

1.1. Package Type

Figure 1-1. SOIC-8 Package (Top View)



2. Electrical Characteristics

2.1. Absolute Maximum Ratings

Parameters	Symbol	Min.	Max.	Unit
High-Side Floating Supply Voltage	V_B	-0.3	624	V
High-Side Floating Supply Offset Voltage	V_S	$V_B - 24$	$V_B + 0.3$	V
High-Side Floating Output Voltage	V_{HO}	$V_S - 0.3$	$V_B + 0.3$	V
Offset Supply Voltage Transient	dV_S/dt	—	50	V/ns
Low-Side and Logic Fixed Supply Voltage	V_{CC}	-0.3	24	V
Low-Side Output Voltage	V_{LO}	-0.3	$V_{CC} + 0.3$	V
Logic Input Voltage (HIN and LIN)	V_{IN}	COM - 0.3	$V_{CC} + 0.3$	V
SOIC-8 Package Power Dissipation at $T_A \leq 25^\circ\text{C}$	P_D	—	0.625	W
SOIC-8 Thermal Resistance (See Note)	θ_{JA}	—	200	$^\circ\text{C}/\text{W}$
Junction Operating Temperature	T_J	—	+150	$^\circ\text{C}$
Lead Temperature (Soldering, 10s)	T_L	—	+300	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55	+150	$^\circ\text{C}$



WARNING

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

Note: When mounted on a standard JEDEC 2-layer FR-4 board.

2.2. Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Unit
High-Side Floating Supply Absolute Voltage	V_B	$V_S + 10$	$V_S + 20$	V
High-Side Floating Supply Offset Voltage	V_S	See Note	600	V
High-Side Floating Output Voltage	V_{HO}	V_S	V_B	V
Low-Side and Logic Fixed Supply Voltage	V_{CC}	10	20	V
Low-Side Output Voltage	V_{LO}	0	V_{CC}	V
Logic Input Voltage	V_{IN}	0	5	V
Ambient Temperature	T_A	-40	125	$^\circ\text{C}$

Logic operational for V_S of -5V to +600V.

2.3. DC Electrical Characteristics

$V_{BIAS} (V_{CC}, V_{BS}) = 15V, T_A = 25^\circ C, \text{ unless otherwise specified.}$						
Parameter (Note 1)	Symbol	Min.	Typ.	Max.	Unit	Conditions
Logic "1" Input Voltage	V_{IH}	2.3	—	—	V	$V_{CC} = 10V \text{ to } 20V$ (Note 2)
Logic "0" Input Voltage	V_{IL}	—	—	0.7	V	$V_{CC} = 10V \text{ to } 20V$ (Note 2)
High Level Output Voltage, $V_{BIAS} - V_O$	V_{OH}	—	0.05	0.2	V	$I_O = 2 \text{ mA}$
Low Level Output Voltage, V_O	V_{OL}	—	0.02	0.1	V	$I_O = 2 \text{ mA}$
Offset Supply Leakage Current	I_{LK}	—	—	50	μA	$V_B = V_S = 600V$
Quiescent V_{BS} Supply Current	I_{BSQ}	20	60	150	μA	$V_{IN} = 0V \text{ or } 5V$
Quiescent V_{CC} Supply Current	I_{CCQ}	50	260	400	μA	$V_{IN} = 0V \text{ or } 5V$
Logic "1" Input Bias Current	I_{IN+}	—	5	40	μA	$V_{IN} = 5V$
Logic "0" Input Bias Current	I_{IN-}	—	1	5	μA	$V_{IN} = 0V$
V_{BS} Supply Undervoltage Positive Going Threshold	V_{BSUV+}	7.7	8.7	9.7	V	
V_{BS} Supply Undervoltage Negative Going Threshold	V_{BSUV-}	7.0	8.0	9.0	V	
V_{CC} Supply Undervoltage Positive Going Threshold	V_{CCUV+}	7.7	8.7	9.7	V	
V_{CC} Supply Undervoltage Negative Going Threshold	V_{CCUV-}	7.0	8.0	9.0	V	
Output High Short Circuit Pulsed Current	I_{O+}	60	290	—	mA	$V_O = 0V, PW \leq 10 \mu s$
Output Low Short Circuit Pulsed Current	I_{O-}	130	600	—	mA	$V_O = 15V, PW \leq 10 \mu s$

Notes:

1. The V_{IN} , V_{TH} , and I_{IN} parameters are referenced to COM and are applicable to the two logic input pins: HIN and LIN. The V_O and I_O parameters are also referenced to COM and are applicable to the respective output pins: HO and LO.
2. For optimal operation, it is recommended that the input pulse (to HIN and LIN) should have an amplitude of 2.3V minimum, with a Pulse Width (PW) of 200 ns, minimum.

2.4. AC Electrical Characteristics

$V_{BIAS} (V_{CC}, V_{BS}) = 15V, C_L = 1000 \text{ pF}, \text{ and } T_A = 25^\circ C, \text{ unless otherwise specified.}$						
Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Turn-on Propagation Delay	t_{ON}	—	95	210	ns	$V_S = 0V$, See Figure 3-2
Turn-off Propagation Delay	t_{OFF}	—	100	210	ns	$V_S = 0V \text{ or } 600V$, See Figure 3-2
Delay Matching, HS and LS Turn On/Off	t_{DM}	—	—	50	ns	See Figure 3-2
Turn-on Rise Time	t_r	—	70	120	ns	
Turn-off Fall Time	t_f	—	35	60	ns	
Deadtime: $t_{DT \text{ LO-HO}}$ and $t_{DT \text{ HO-LO}}$	t_{DT}	80	100	190	ns	See Figure 3-2

3. Timing Waveforms

Figure 3-1. Input/Output Timing Diagram

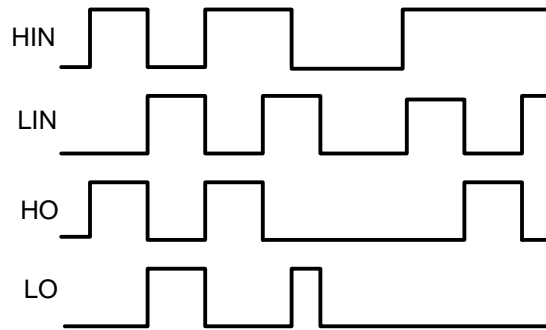
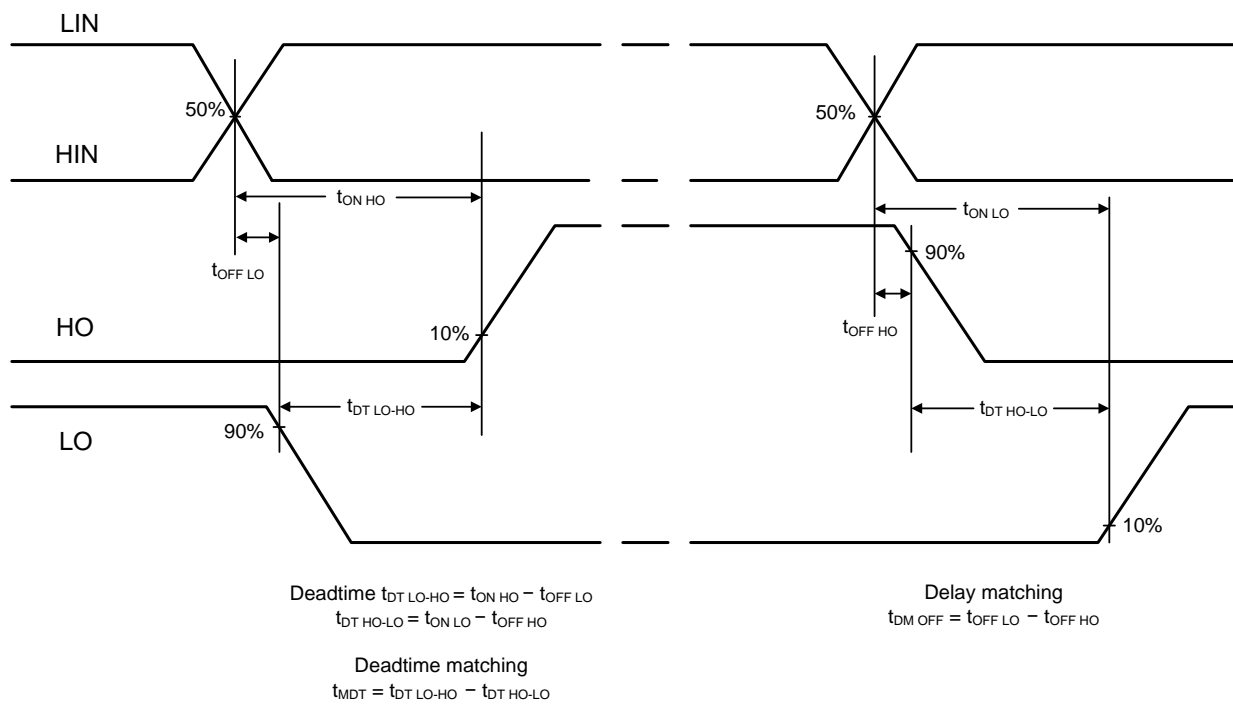


Figure 3-2. Switching Time Waveform Definitions



4. Typical Performance Curves

Figure 4-1. Output Source Current vs. Supply Voltage

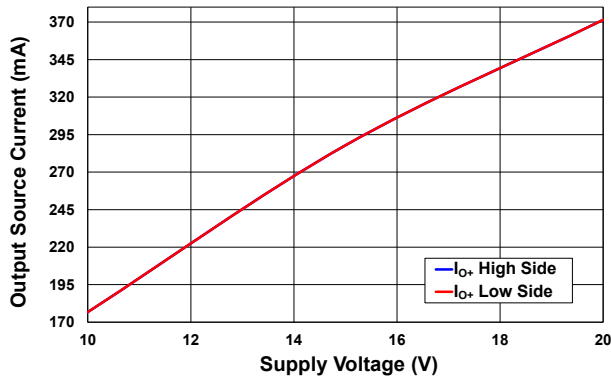


Figure 4-2. Output Source Current vs. Temperature

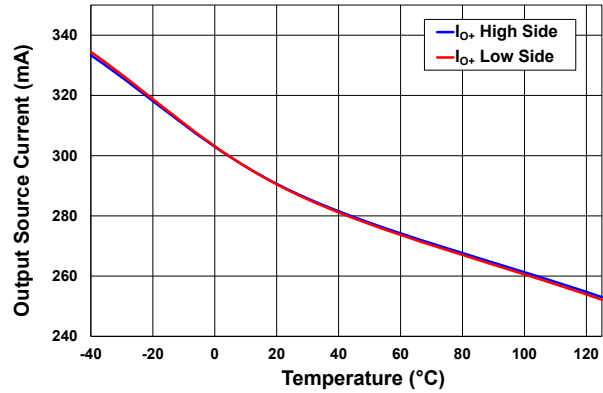


Figure 4-3. Output Sink Current vs. Supply Voltage

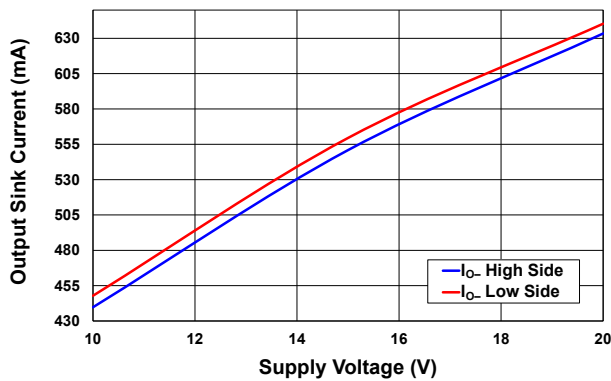


Figure 4-4. Output Sink Current vs. Temperature

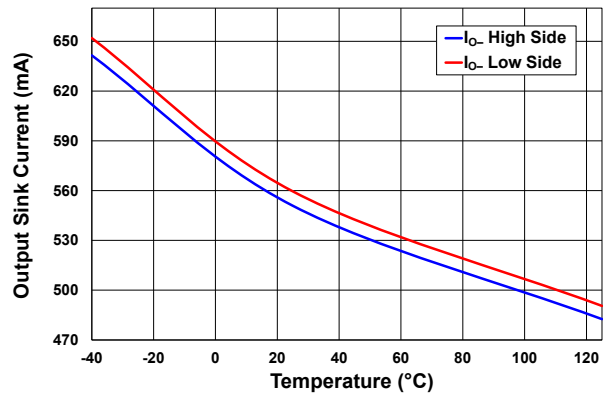


Figure 4-5. Logic 1 Input Voltage vs. Supply Voltage

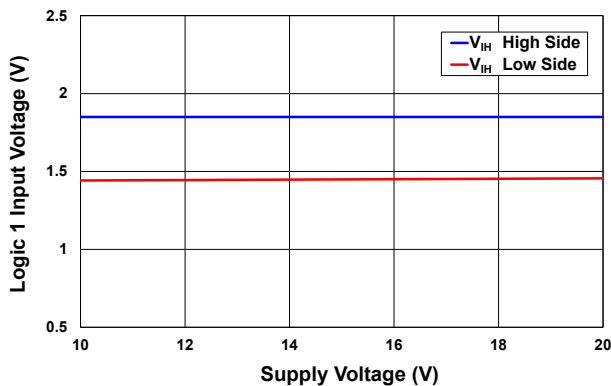


Figure 4-6. Logic 1 Input Voltage vs. Temperature

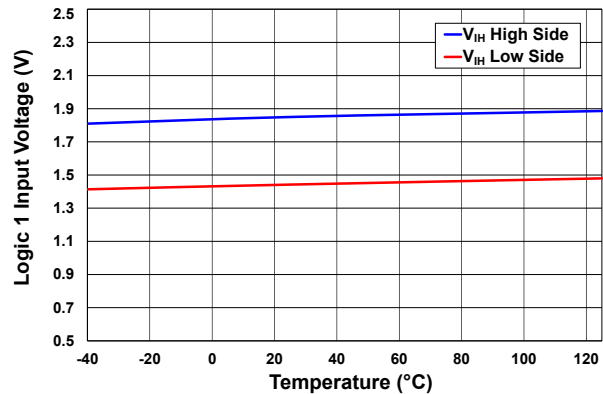


Figure 4-7. Logic 0 Input Voltage vs. Supply Voltage

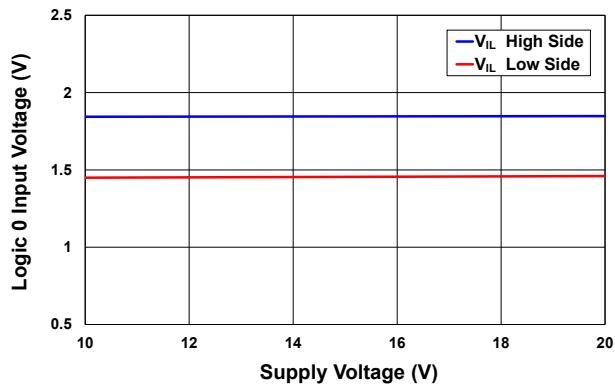


Figure 4-8. Logic 0 Input Voltage vs. Temperature

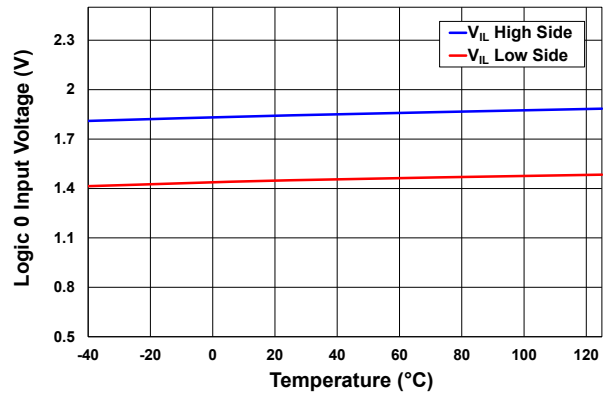


Figure 4-9. Quiescent Current vs. Supply Voltage

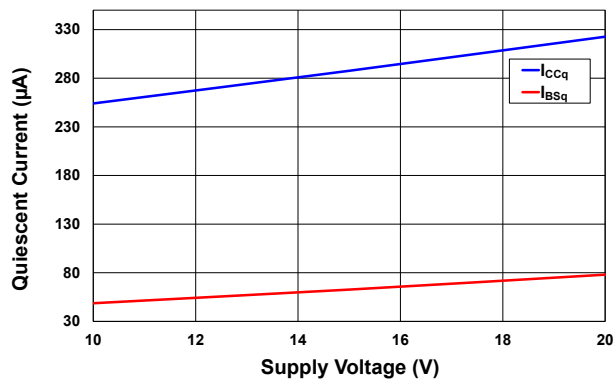


Figure 4-10. Quiescent Current vs. Temperature

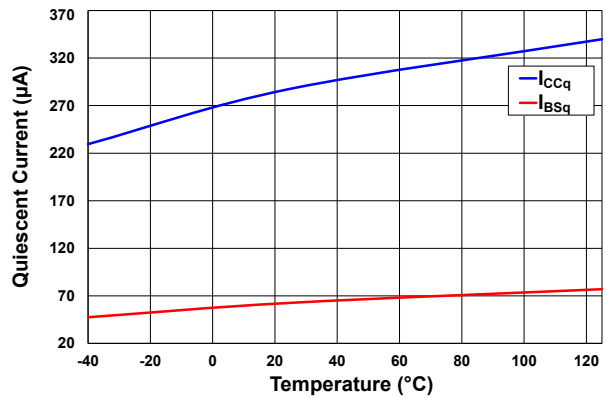


Figure 4-11. Turn-on Propagation Delay vs. Supply Voltage

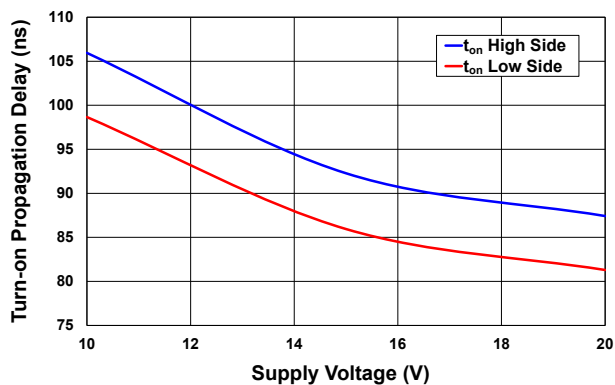


Figure 4-12. Turn-on Propagation Delay vs. Temperature

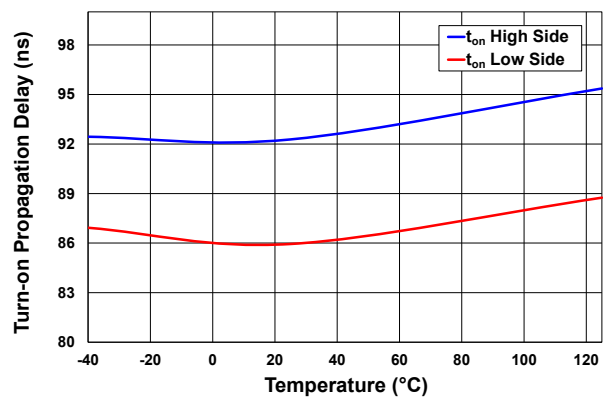


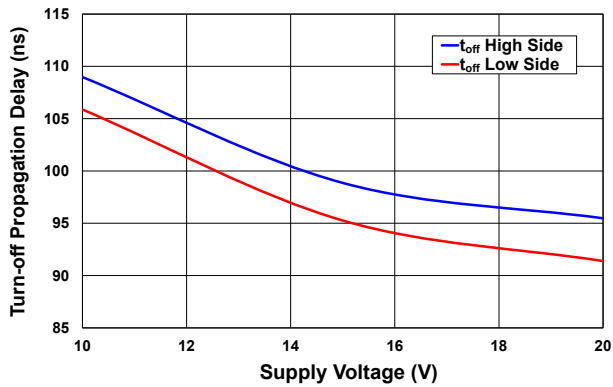
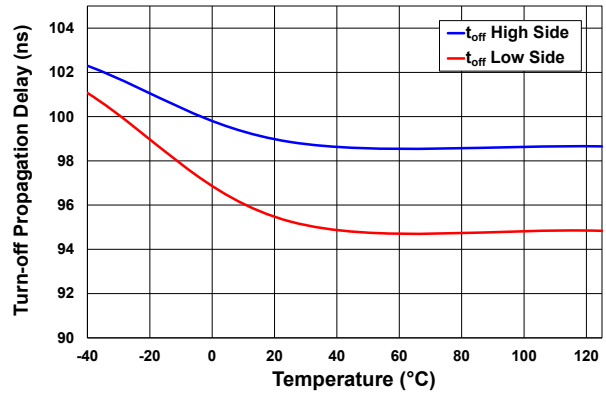
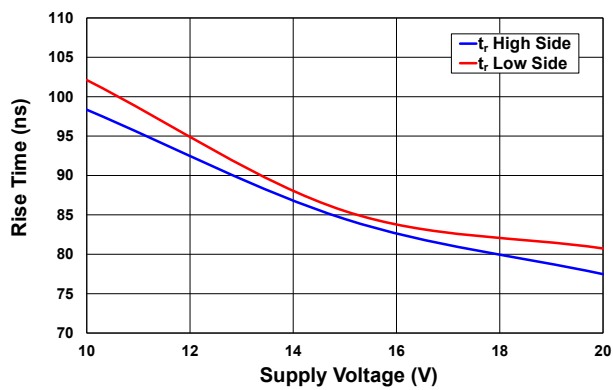
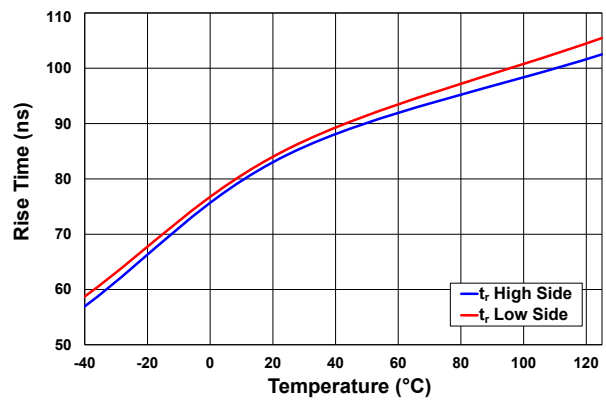
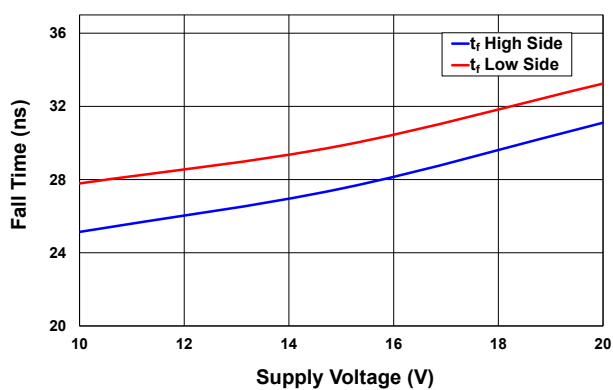
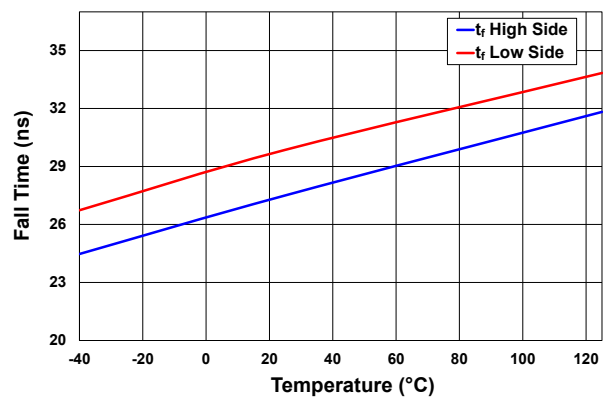
Figure 4-13. Turn-off Propagation Delay vs. Supply Voltage**Figure 4-14.** Turn-off Propagation Delay vs. Temperature**Figure 4-15.** Rise Time vs. Supply Voltage**Figure 4-16.** Rise Time vs. Temperature**Figure 4-17.** Fall Time vs. Supply Voltage**Figure 4-18.** Fall Time vs. Temperature

Figure 4-19. Delay Matching vs. Supply Voltage

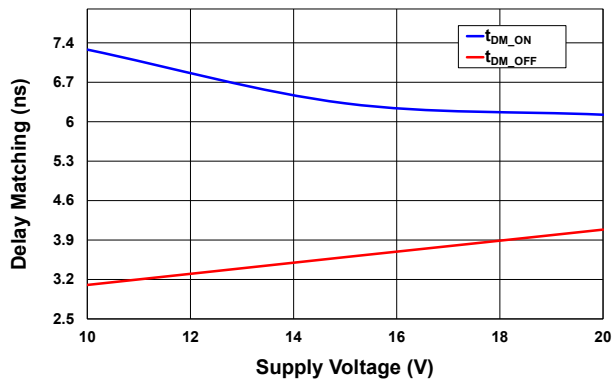


Figure 4-20. Delay Matching vs. Temperature

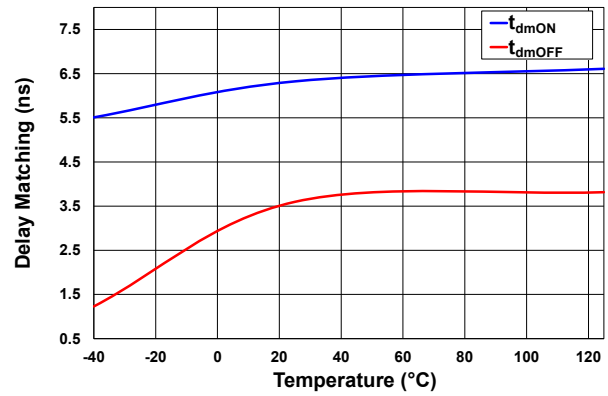


Figure 4-21. Deadtime vs. Supply Voltage

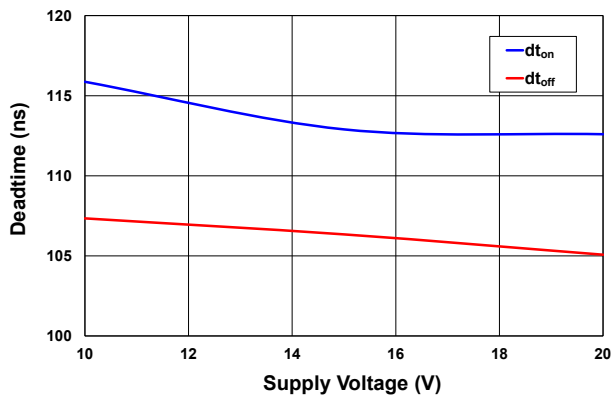


Figure 4-22. Deadtime vs. Temperature

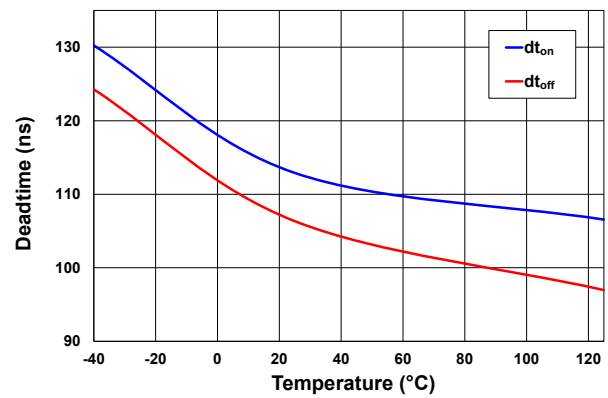


Figure 4-23. VCC UVLO vs. Temperature

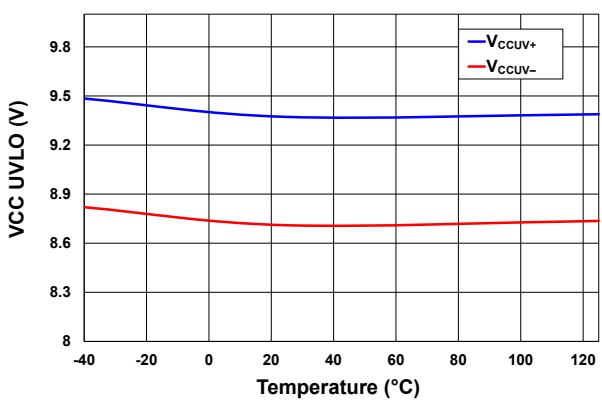
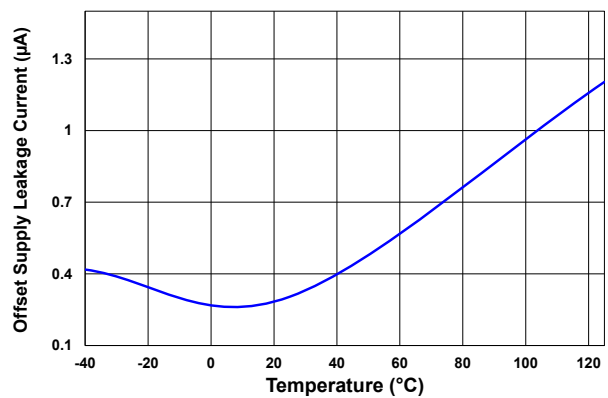


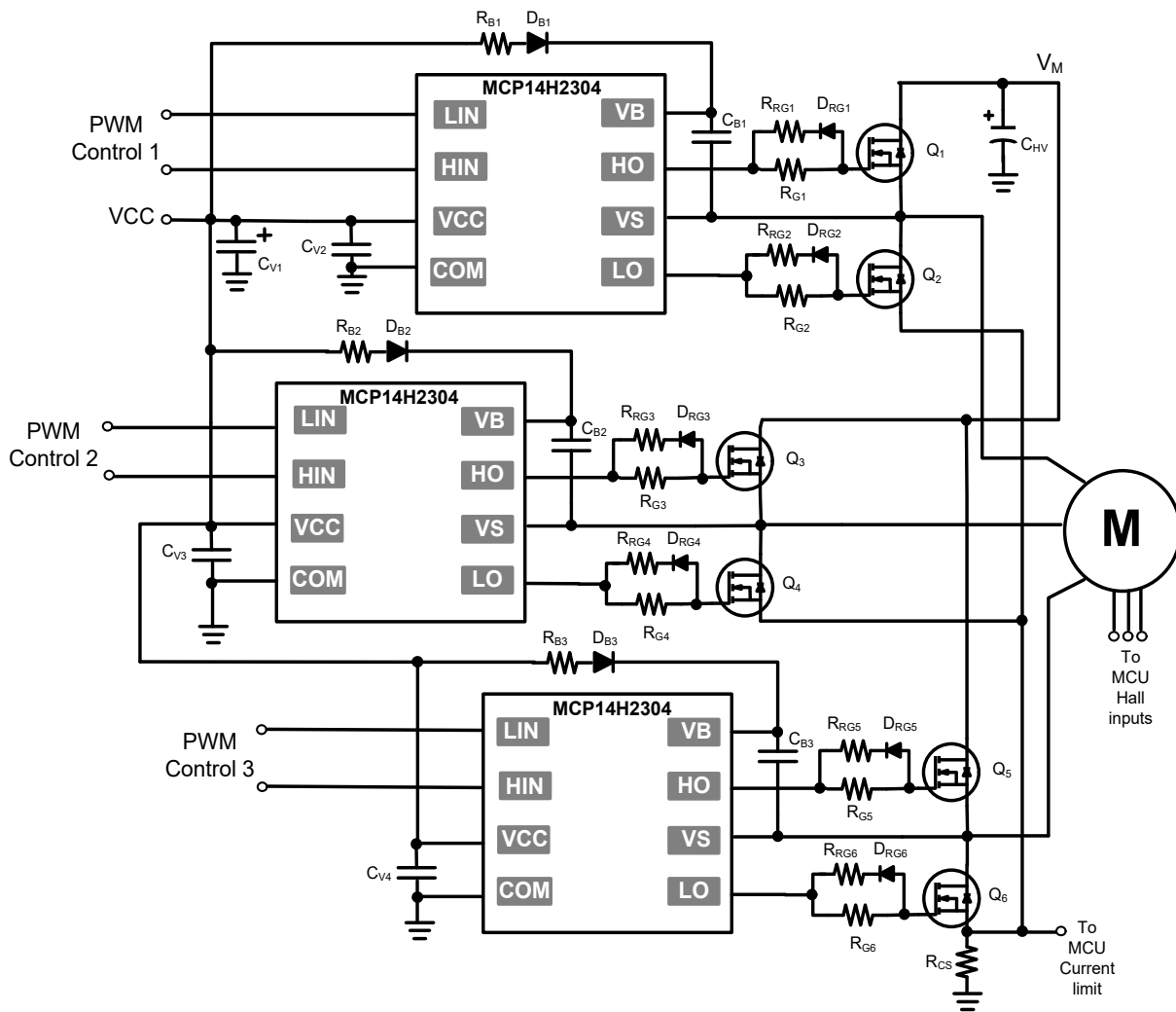
Figure 4-24. Offset Supply Leakage Current vs. Temperature



5. Application Information

The MCP14H2304, halfbridge gate drive is used to optimally and efficiently drive the gate of MOSFETs or IGBTs. Below (Figure 5-1) is an example application using the MCP14H2304 with MOSFETs to make three halfbridge circuits used to drive a three-phase motor. Typically, three-phase motor applications are AC Induction motors, PMSMs, and BLDC motors. The MCP14H2304 is typically used for stepper motor applications. MCP14H2304 can also be used in power supplies. The important parameters of the MCP14H2304 are discussed in this section. The main topics are: bootstrap resistor, diode and capacitor selection, gate driver component selection, decoupling capacitors, and PCB layout suggestions.

Figure 5-1. Three-Phase Motor Drive Application Example Using the MCP14H2304



5.1. Bootstrap Resistor Selection

Considering Figure 5-1, when the low side MOSFET (Q2, Q4, or Q6) turns on, VS pulls to GND and the bootstrap capacitor (C_{B1} , C_{B2} , and C_{B3}) is charged. When the high side MOSFET (Q1, Q3, and Q5) is turned on, VS swings above VCC and the charge on the bootstrap capacitor (C_{Bx}) provides current to drive the IC high side gate driver. The first charge of C_{Bx} from VCC through the bootstrap resistor (R_{B1} , R_{B2} , and R_{B3}) and bootstrap diode (D_{B1} , D_{B2} , and D_{B3}) occurs when power is first applied and

low side turns on the first time. At this time the charge current is the largest as, typically, C_{Bx} is not discharged fully at each cycle during normal operation.

A bootstrap resistor (R_{Bx}) is included in the bootstrap circuit to limit the inrush current that charges C_{Bx} when VS pulls below VCC. This inrush current is largest with the first charge. Limiting inrush current is desirable to limit noise spike on VS and COM, potentially causing shoot-through. The amplitude and length of time of the inrush current is determined mostly by the component value of R_{Bx} and C_{Bx} , as well as the VCC level. The aim in resistor selection for the application is to slow down the inrush current but have limited effect on the RC time constant of charging C_{Bx} .

Typically, values for R_{Bx} are 3Ω to 10Ω , enough to dampen the inrush current but have little effect on the V_{B5} turn ON. Below are some scopeshots illustrating the effect of different R_{Bx} values.

Table 5-1.

Figure 5-2. Bootstrap Inrush Current With $R_{Bx} = 3\Omega$, $C_{Bx} = 2.2\ \mu\text{F}$

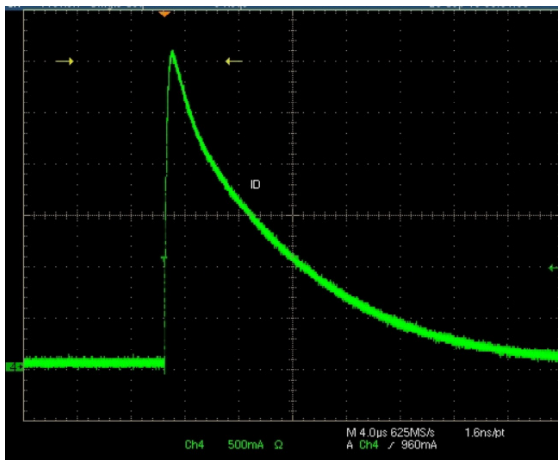


Figure 5-3. Bootstrap Inrush Current With $R_{Bx} = 10\Omega$, $C_{Bx} = 2.2\ \mu\text{F}$

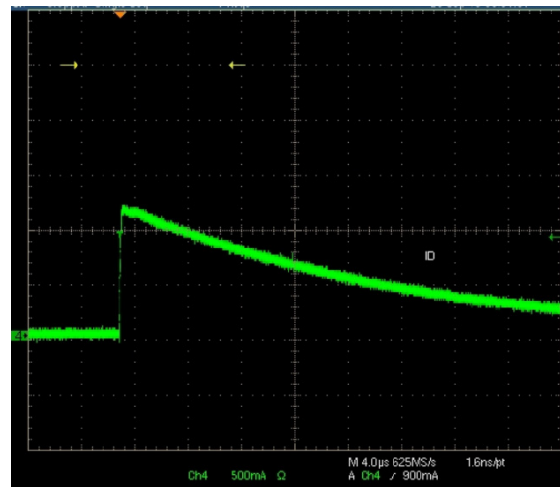


Figure 5-4. V_{B5} Rise Time ($11.8\ \mu\text{s}$) With $C_{Bx} = 2.2\ \mu\text{F}$ and $R_{Bx} = 3\Omega$

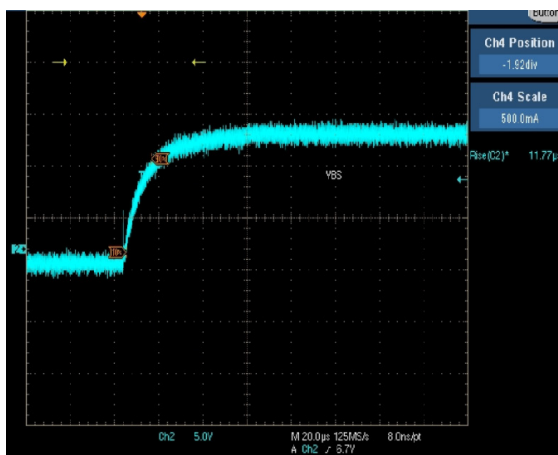
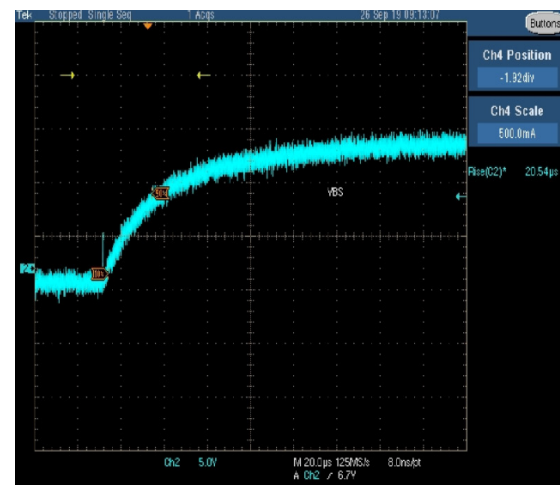


Figure 5-5. V_{B5} Rise Time ($20.5\ \mu\text{s}$) With $C_{Bx} = 2.2\ \mu\text{F}$ and $R_{Bx} = 10\Omega$



5.2. Bootstrap Capacitor Selection

The initial step in determining the value of the bootstrap capacitor is to determine the minimum voltage drop (ΔV_{BS}) that can be guaranteed when the high side device is turned on. In other words, the minimum gate-source voltage (V_{GSmin}) must be greater than the UVLO of the high side circuit, specifically V_{BSUV-} level. Therefore, if V_{GSmin} is the minimum gate-source voltage such that:

$$V_{GSmin} > V_{BSUV-}$$

Then:

$$\Delta V_{BS} = V_{CC} - V_F - V_{GSmin} - V_X$$

Where:

- V_{CC} is the supply voltage to the MCP14H2304
- V_F is the voltage drop across the bootstrap diode (DBS)
- V_X is the voltage drop across the MOSFET

V_X is calculated as the current seen across low side MOSFET multiplied by its $R_{DS(ON)}$ and is simply V_{CE-ON} at the specify output current if an I_{GBT} were used instead.

In addition to the voltage drops across these components, other factors that cause V_{BS} to drop are leakages, charge required to turn on the power devices, and duration of the high-side on time. The total charge (QT) required by the gate driver then equals:

$$QT = QG + QLS + [I_{LKN}] \times t_{HON}$$

Where:

- QG is the gate charge of power device
- QLS is the level shift charge required per cycle
- t_{HON} is the high-side ON time
- I_{LKN} is the sum of all leakages that include:
 - I_{GSS}/I_{GES} : Gate-source leakage of the power device
 - $I_{LK,DB}$: Bootstrap diode leakage
 - $I_{LK,IC}$: Offset supply leakage of HVIC
 - I_{QBS} : Quiescent current for high side supply

QLS is not listed in the datasheet. Depending on the process technology, it could range anywhere from 3-20 nC for 500V to 1200V process respectively. Assuming a value of 10 nC for Microchip's 600V process should be sufficient with added margin.

From the basic equation, then the minimum bootstrap capacitor is calculated as:

$$C_{Bmin} \geq \frac{QT}{\Delta V_{BS}}$$

5.3. Example Using MOSFET

The follow example uses a power MOSFET as the switching device with the following desired parameters:

- Power device = DMNH6021SK3Q
- HVIC gate driver = Microchip's MCP14H2304
- $V_{CC} = 12V$
- $QG = 20 \text{ nC}$
- $I_{GSS} = 100 \text{ nA}$

- $t_{HON} = 10 \mu s$
- $R_{DS(ON)} = 25 \text{ m}\Omega \text{ max, } 125^\circ\text{C}$
- $I_{OUT} = 5A$
- $I_{QBS} = 150 \mu A$
- $I_{LK_IC} = 50 \mu A$
- $QLS = 10 \text{ nC}$
- $V_F = 1.0V$
- $I_{LK_DB} = 100 \mu A$
- $V_{GSmin} = 10V$

From equations above:

$$\Delta V_{BS} = 12V - 1V - 10V - 0.625V = 0.375V$$

$$QT = QG + QLS + [I_{LKN}] \times t_{HON}; \text{ where } I_{LKN} \times t_{HON} = 3nC$$

$$\text{Thus } QT = 20 \text{ nC} + 10 \text{ nC} + 3 \text{ nC} = 33 \text{ nC}$$

$$\text{Therefore } C_{Bmin} = \frac{33 \text{ nC}}{0.375V} = 88 \text{ nF}$$

The bootstrap capacitor calculated in the above problem is the minimal value required to supply the needed charge. It is recommended that a minimal margin of two to three times the calculated value is used. Utilizing values lower than this could result in over charging of the bootstrap capacitor especially during $-VS$ transients. Typically for motor driver applications $C_{BS} = 1 \mu F$ to $10 \mu F$ are used, and for power supplies typically $C_{BS} = 0.1 \mu F$ to $2.2 \mu F$. Also it is recommended to use low ESR ceramic capacitors as close to the VB and VS pin as possible (see [PCB layout suggestions section](#)).

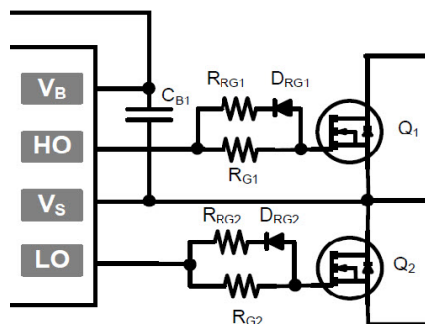
5.4. Bootstrap Diode Selection

The chosen bootstrap diode (D_{BS}) should be rated higher than the maximum rail voltage since the diode must be able to block the full rail voltage and any spikes seen at the VS node. The diode's current rating is simply the product of total charge (QT) required by the HVIC and the switching frequency. An ultrafast recovery diode is recommended to minimize any delay of charging the C_{BS} capacitor. A 1A ultrafast recovery diode is typical for MCP14H2304 applications.

5.5. Gate Resistor Selection

The most crucial time interval of the gate drive is the turn ON and turn OFF of the MOSFET, and the key is performing this function quickly but with minimal noise and ringing to the overall system. Too fast a rise/fall time can cause unnecessary ringing and poor EMI, and too slow a rise/fall time will increase switching losses in the MOSFET.

Figure 5-6. Gate Drive High-side and Low-side Components for the MCP14H2304



Considering the gate driver components for MCP14H2304 in [Figure 5-6](#), with the careful selection of R_{G1} and R_{RG1} , it is possible to selectively control the rise time and fall time of the gate drive to the MOSFET. For turn ON, all current will go from the IC through R_{G1} and charge the MOSFET gate capacitance, hence increasing or decreasing R_{G1} will increase or decrease rise time in the application. With the addition of D_{RG1} , the fall time can be separately controlled as the turn off current flows from the MOSFET gate capacitance, through R_{RG1} and D_{RG1} to the driver in the IC to VS for high side and COM for low side. So increasing or decreasing R_{RG1} will increase or decrease the fall time. Sometimes finer control is not needed and only R_{G1} and R_{G2} is used.

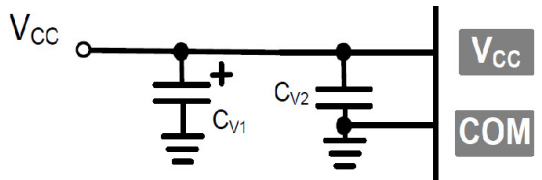
Increasing turn ON and turn OFF has the effect of limiting ringing and noise due to parasitic inductances, hence with a noisy environment, it may be necessary to increase the gate resistors. Gate component selection is a compromise of faster rise time with more ringing, and a poorer EMI but better efficiency, and a slower rise time with better EMI, better noise performance but poorer efficiency. The exact value depends on the parameters of the application and system requirements. Generally, for motors, the switching speed is slower, the deadtime is longer, and the application has more inherent noise, hence higher values are recommended, for example $R_{GX} = 10\Omega - 100\Omega$. For power supplies, the switching speed is faster, deadtimes are shorter for efficiency, and so smaller values are typically used, for example $R_{GX} = 3\Omega \sim 20\Omega$.

To have equal switching times for high-side and low-side, it is recommended that the gate driver components for high-side and low-side are mirrored. For example $R_{RG1} = R_{RG2}$, $D_{RG1} = D_{GR2}$, and $R_{G1} = R_{G2}$.

5.6. Decoupling Capacitors Selection

For optimal operation, VCC decoupling is crucial for all gate driver ICs. With poor decoupling, larger VCC transients will occur at the IC when switching, and for greater and longer VCC drop the IC can go into UVLO.

Figure 5-7. Suggested VCC Decoupling



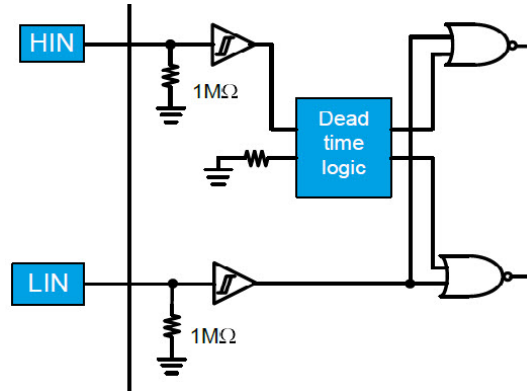
As shown in [Figure 5-7](#), two decoupling capacitors are recommended, C_{V1} and C_{V2} . C_{V1} can be a larger electrolytic, for example 47 μF , 50V, used to dampen low frequency drains on supply. C_{V1} does not need to be right next to the IC. C_{V2} is used to decouple faster edge changes to VCC, and should be a low ESR ceramic capacitor placed close to the VCC pin. This component provides stability when VCC is quickly pulled down with load from the IC. The typical value is 0.1 μF to 1 μF .

For applications with multiple gate driver ICs (for example, BLDC motor drive with three gate drivers, as shown in [Figure 5-1](#)), one larger electrolytic (C_{V1}) can be used and the three ceramic capacitors (C_{V2} , C_{V3} , C_{V4}) should be placed close to the VCC pin (see [Layout section](#)).

5.7. Input Resistors

The MCP14H2304 PWM inputs, HIN and LIN, are very high impedance inputs with a pull down resistor to COM for both the HIN and LIN ([Figure 5-8](#)). The pull down resistor on HIN and LIN has a value of approximately 1.0 M Ω .

Figure 5-8. Input Logic for MCP14H2304



5.8. IC Drive Current and MOSFET/IGBT Gate Charge

Gate driver ICs are defined by their output drive current, its ability to source current to the gate of the MOSFET/IGBT at turn ON and to sink current from the gate of the MOSFET/IGBT at turn OFF. For the MCP14H2304, the drive current is source $I_{O+} = 290$ mA typical, and sink $I_{O-} = 600$ mA, typical.

For a given MOSFET/IGBT, with the known drive current of the MCP14H2304, you can estimate how long it will take to turn on/off the MOSFET/IGBT with the equation:

$$t = \frac{Q_g}{I}$$

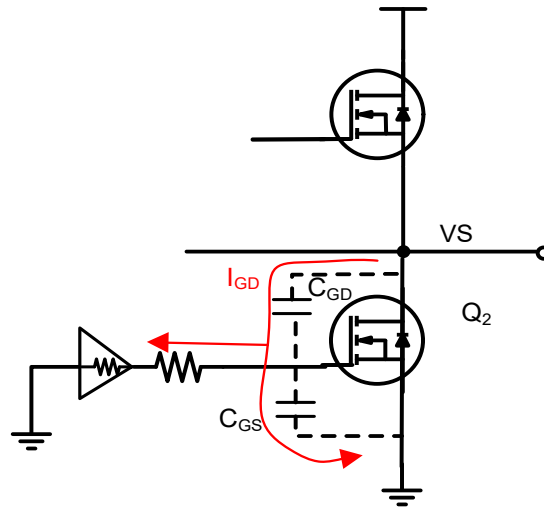
Where:

- Q_g is the total charge of the MOSFET/IGBT as provided by the datasheet
- I is the sink/source capability of the gate driver IC
- t is the calculated rise/fall time with the given charge and drive current

For example with the Diodes' DGTD65T15H2TF, 650V IGBT, $Q_g = 61$ nC; and with the MCP14H2304 $I_{O+} = 290$ nA and $I_{O-} = 600$ mA, the $t_r = 210$ ns and $t_f = 102$ ns. These are estimates, as the total charge given in the datasheet may not be the same conditions in the application. Also, the addition of a gate resistor will increase the t_r and t_f .

5.9. Unexpected Shoot-through with dV_{DS}/dt

Unwanted MOSFET turn-ON, caused by $C_{GD} \times dV_{DS}/dt$ (see Figure 5-9) is often the cause of unexplained shoot through in the halfbridge circuit. Depending on the ratio of the C_{GS}/C_{GD} , when the dV_{DS}/dt across low side MOSFET (Q_2) occurs (i.e when high side MOSFET turns ON), there can be a voltage applied to the gate of the Q_2 MOSFET, turning ON Q_2 , and causing shoot through. In effect, a gate bouncing occurs causing a ringing on the VS line and the power ground.

Figure 5-9. Unexpected Shoot Through With dV_{DS}/dt 

Considering [Figure 5-9](#)

$$I_{GD} = C_{GD} \times dV_{DS}/dt$$

I_{GD} will flow towards the resistive load (and small inductive due to parasitics) of the gate driver and the C_{GS} of the MOSFET. Hence, this unwanted condition may be minimized by looking at the C_{iss}/C_{res} in the MOSFET datasheet (C_{iss}/C_{res} gives an indication of C_{GS}/C_{GD}); having a C_{iss}/C_{res} as large as possible will minimize this phenomenon. Also, an external capacitor can be added to the gate-source of the MOSFET (for example 1 nF), which will increase C_{GS}/C_{GD} .

5.10. Minimum Input Pulse Recommendation

The MCP14H2304 has RC filter on the input lines to be more resilient in noisy environments. With a rising edge at the input to the gate driver, and then after the propagation delay of the IC, delay from gate resistor, and rise time of the MOSFET, the halfbridge will turn ON producing bus voltage at the output. This MOSFET turn ON produces significant system noise. For optimal operation, it is suggested to provide a minimum pulse width at the input to the IC from the MCU to ensure the turn OFF occurs after this event. As a rule of thumb, this minimum pulse should be two times the deadtime for halfbridge drivers. Hence, for the MCP14H2304, the minimum pulse recommended at the logic inputs is 200 ns.

During typical operation, the MCP14H2304 will respond to an input greater than 50 ns (approximate value from the RC input filter response). Hence, for an input pulse greater than approximately 50 ns, the IC will follow the pulse as expected and, for an input pulse shorter than 50 ns, there will be no response from the IC.

5.11. PCB Layout Suggestions

Layout plays a considerable role since unwanted noise coupling, unpredicted glitches and abnormal operation could arise due to poor layout of the associated components. [Figure 5-10](#) shows the schematic with parasitic inductances in the high current path (L_{P1} , L_{P2} , L_{P3} , L_{P4}) which would be caused by inductance in the metal of the trace. Considering [Figure 5-10](#), the length of the tracks in red should be minimized, and the bootstrap capacitor (C_B) and the decoupling capacitor (C_D) should be placed as close to the IC as possible, in addition to using low ESR ceramic capacitors. Finally, the gate resistors (R_{GH} and R_{GL}) and the sense resistor (R_S) should be surface mount devices. These suggestions will reduce the parasitics caused by the PCB traces.

Figure 5-10. Layout Suggestions for MCP14H2304 in a Half-bridge (Lines in Red Should Be as Short as Possible)

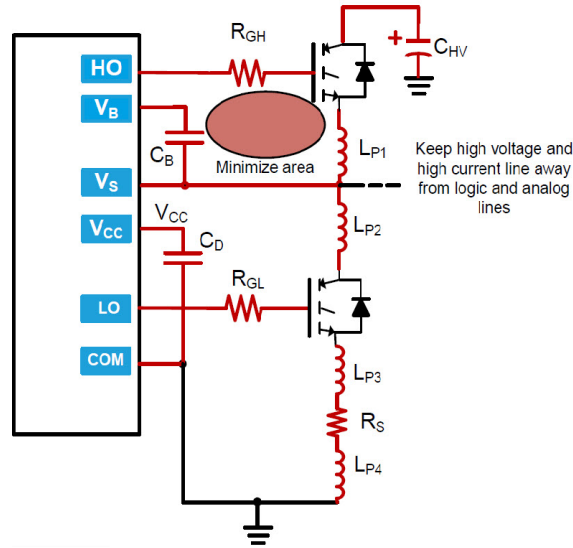


Figure 5-11. Layout Example

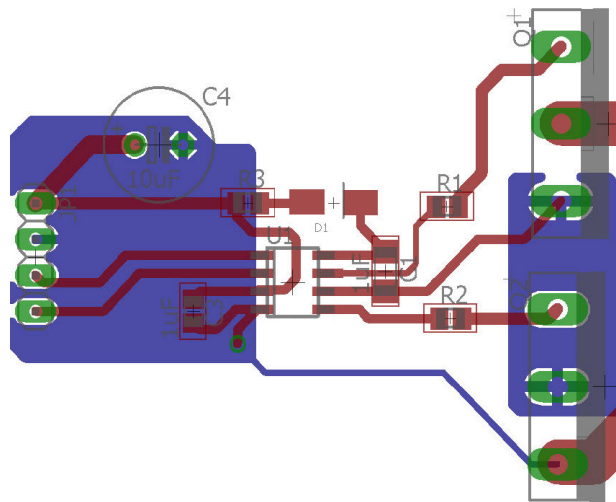
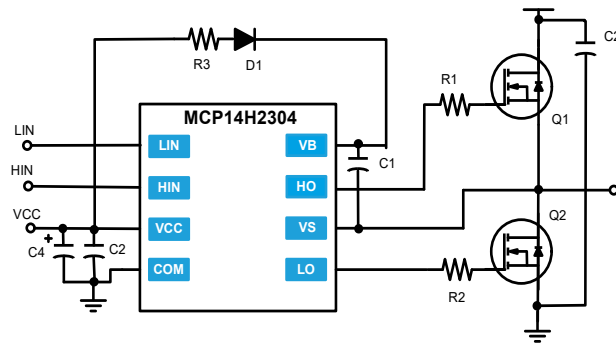
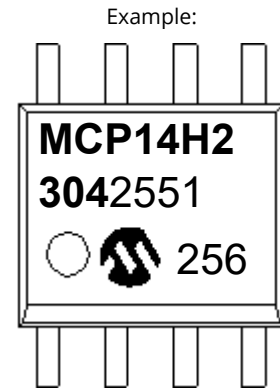
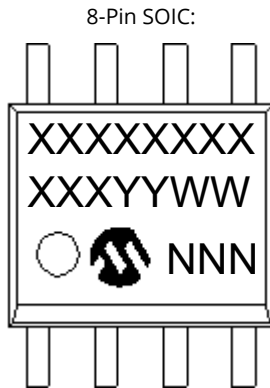


Figure 5-12. Schematic for Layout Example



6. Packaging Information

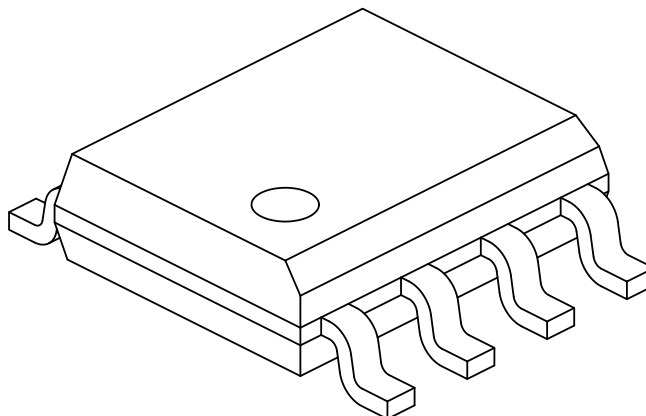
Package Marking Information



Legend:	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
Note:	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or not include the corporate logo.	

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Number of Pins	N	8		
Pitch	e	1.27 BSC		
Overall Height	A	–	–	1.75
Molded Package Thickness	A2	1.25	–	–
Standoff §	A1	0.10	–	0.25
Overall Width	E	6.00 BSC		
Molded Package Width	E1	3.90 BSC		
Overall Length	D	4.90 BSC		
Chamfer (Optional)	h	0.25	–	0.50
Foot Length	L	0.40	–	1.27
Footprint	L1	1.04 REF		
Lead Thickness	c	0.17	–	0.25
Lead Width	b	0.31	–	0.51
Lead Bend Radius	R	0.07	–	–
Lead Bend Radius	R1	0.07	–	–
Foot Angle	θ	0°	–	8°
Mold Draft Angle	θ1	5°	–	15°
Lead Angle	θ2	0°	–	–

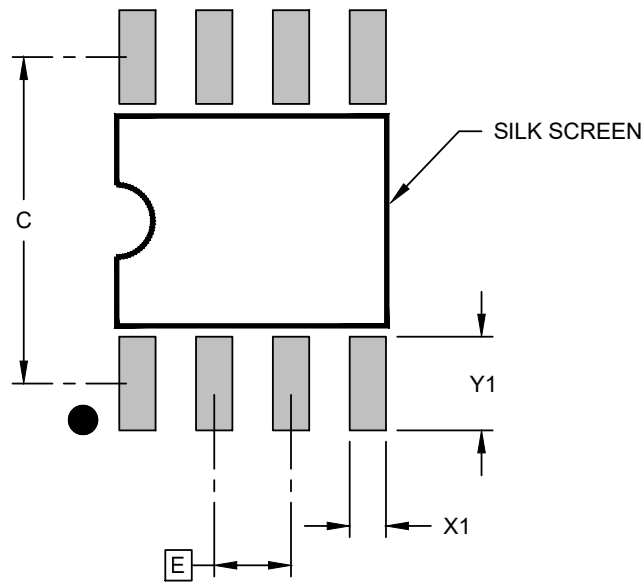
Notes:

1. The Pin 1 visual index feature may vary, but it must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-00057-SN Rev L Sheet 2 of 2

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

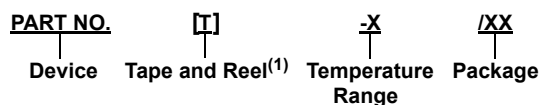
Microchip Technology Drawing C04-02057-SN Rev L

7. Revision History

Doc. Rev.	Date	Section	Comments
A	November 2025		Initial release of this document.

Product Identification System

To order or obtain information, for example, on pricing or delivery, contact Microchip: <https://www.microchip.com/en-us/about/contact-us>.



Device:	MCP14H2304: Half-Bridge Gate Driver	
Tape and Reel Option⁽¹⁾:	Blank	= Tube
	T	= Tape and Reel
Temperature Range:	E	= -40°C to +125°C (Extended)
Package:	SN	= Plastic Small Outline IC, 3.90 mm, SOIC, 8-Pin

Examples:

- MCP14H2304T-E/SN: Half-Bridge Gate Driver, Tape and Reel, Extended temperature range, SOIC-8 package

Note:

1. Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package.

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