

FDG6318PZ

Dual P-Channel, Digital FET

General Description

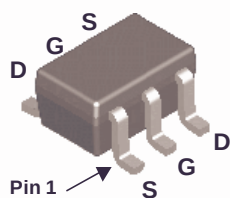
These dual P-Channel logic level enhancement mode MOSFET are produced using Fairchild Semiconductor's especially tailored to minimize on-state resistance. This device has been designed especially for bipolar digital transistors and small signal MOSFETS

Applications

- Battery management

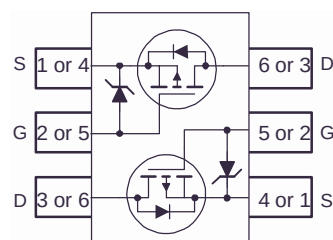
Features

- 0.5A, -20V. $r_{DS(ON)} = 780m\Omega$ (Max) @ $V_{GS} = -4.5V$
 $r_{DS(ON)} = 1200m\Omega$ (Max) @ $V_{GS} = -2.5V$
- Very low level gate drive requirements allowing direct operation in 3V circuits ($V_{GS(TH)} < 1.5V$).
- Gate-Source Zener for ESD ruggedness (>1.4kV Human Body Model).
- Compact industry standard SC-70-6 surface mount package.



SC70-6

The pinouts are symmetrical; pin1 and pin 4 are interchangeable.



MOSFET Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DSS}	Drain to Source Voltage	-20	V
V_{GS}	Gate to Source Voltage	± 12	V
I_D	Drain Current		
	Continuous ($T_C = 25^\circ\text{C}$, $V_{GS} = -4.5V$)	-0.5	A
	Continuous ($T_C = 100^\circ\text{C}$, $V_{GS} = -2.5V$)	-0.3	A
	Pulsed	Figure 4	
P_D	Power dissipation	0.3	W
	Derate above 25°C	2.4	mW/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Temperature	-55 to 150	$^\circ\text{C}$
ESD	Electrostatic Discharge Rating MIL-STD-883D Human Body Model (100pF / 1500 Ω)	1.4	kV

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance Junction to Ambient (Note 1)	415	$^\circ\text{C/W}$
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Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
.68	FDG6318PZ	SC70-6	7"	8 mm	3000

Electrical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

$B_{V_{DSS}}$	Drain to Source Breakdown Voltage	$I_D = -250\mu\text{A}$, $V_{GS} = 0\text{V}$	-20	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{GS} = -16\text{V}$, $V_{GS} = 0\text{V}$	-	-	-3	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 12\text{V}$, $V_{GS} = 0\text{V}$	-	-	± 10	μA

On Characteristics

$V_{GS(TH)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = -250\mu\text{A}$	-0.65	-0.9	-1.5	V
$r_{DS(ON)}$	Drain to Source On Resistance	$I_D = -0.5\text{A}$, $V_{GS} = -4.5\text{V}$	-	580	780	$\text{m}\Omega$
		$I_D = -0.4\text{A}$, $V_{GS} = -2.5\text{V}$	-	910	1200	

Dynamic Characteristics

C _{ISS}	Input Capacitance	V _{DS} = -10V, V _{GS} = 0V, f = 1MHz		-	85.4	-	pF
C _{OSS}	Output Capacitance			-	24.9	-	pF
C _{RSS}	Reverse Transfer Capacitance			-	8.83	-	pF
Q _{g(TOT)}	Total Gate Charge at -4.5V	V _{GS} = 0V to -4.5V	V _{DD} = -10V I _D = -0.5A I _g = 1.0mA	-	1.08	1.62	nC
Q _{g(-2.5)}	Total Gate Charge at -2.5V	V _{GS} = 0V to -2.5V		-	0.67	1.0	nC
Q _{gs}	Gate to Source Gate Charge			-	0.21	-	nC
Q _{gd}	Gate to Drain “Miller” Charge			-	0.33	-	nC

Switching Characteristics ($V_{GS} = -4.5\text{V}$)

t_{ON}	Turn-On Time	$V_{DD} = -10\text{V}$, $I_D = -0.5\text{A}$ $V_{GS} = -4.5\text{V}$, $R_{GS} = 120\Omega$	-	-	35	ns
$t_{d(ON)}$	Turn-On Delay Time		-	10	-	ns
t_r	Rise Time		-	13	-	ns
$t_{d(OFF)}$	Turn-Off Delay Time		-	40	-	ns
t_f	Fall Time		-	24	-	ns
t_{OFF}	Turn-Off Time		-	-	96	ns

Drain-Source Diode Characteristics

V_{SD}	Source to Drain Diode Voltage	$I_{SD} = -0.5\text{A}$	-	-0.9	-1.2	V
t_{rr}	Reverse Recovery Time	$I_{SD} = -0.5\text{A}$, $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	22	ns
Q_{RR}	Reverse Recovered Charge	$I_{SD} = -0.5\text{A}$, $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	16	nC

Notes:

- $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the center drain pad. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by user's board design. $R_{\theta JA} = 415^\circ\text{C/W}$ when mounted on a 1inch^2 copper pad.

Typical Characteristic $T_A = 25^\circ\text{C}$ unless otherwise noted

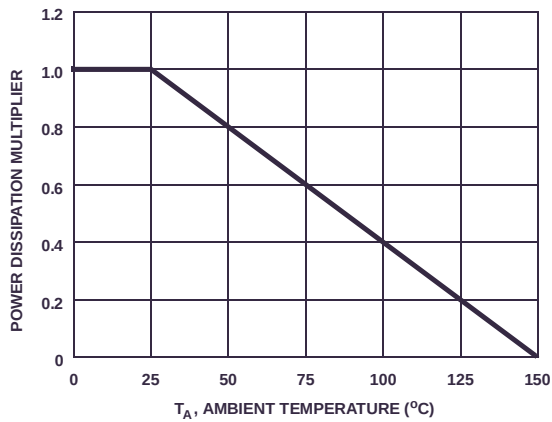


Figure 1. Normalized Power Dissipation vs Ambient Temperature

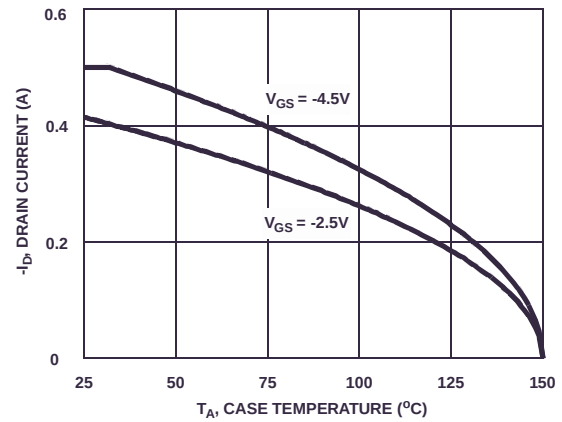


Figure 2. Maximum Continuous Drain Current vs Case Temperature

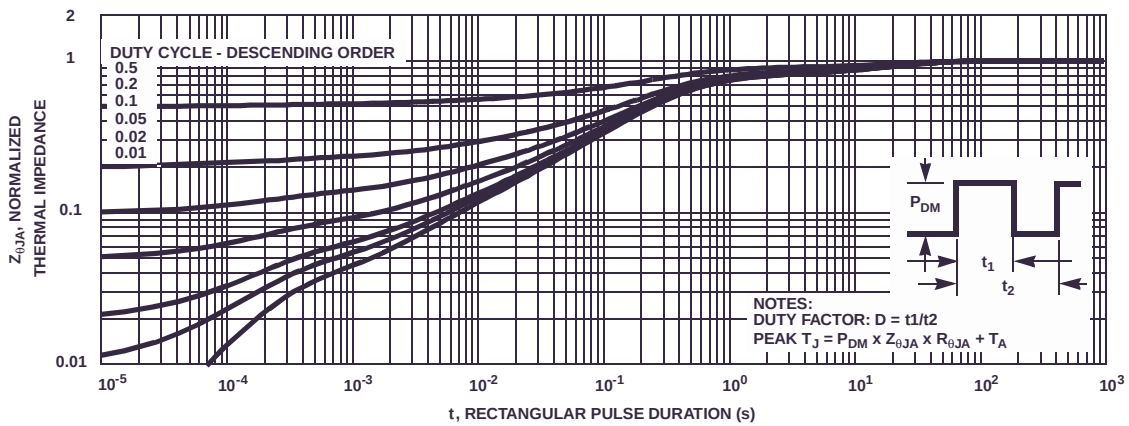


Figure 3. Normalized Maximum Transient Thermal Impedance

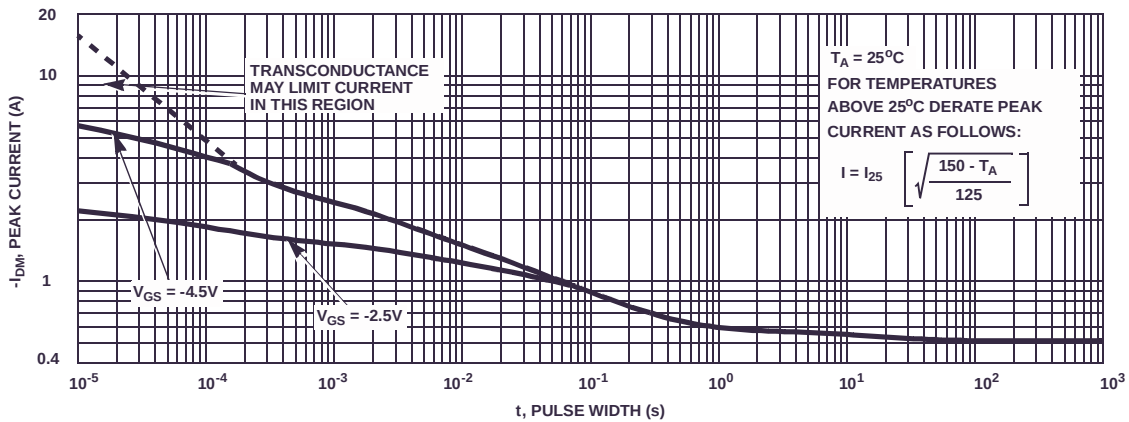


Figure 4. Peak Current Capability

Typical Characteristic (Continued) $T_A = 25^\circ\text{C}$ unless otherwise noted

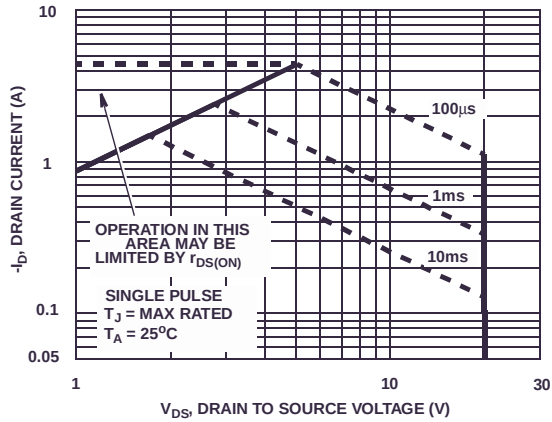


Figure 5. Forward Bias Safe Operating Area

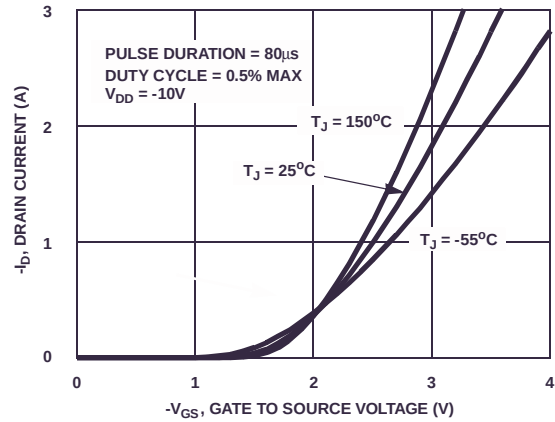


Figure 6. Transfer Characteristics

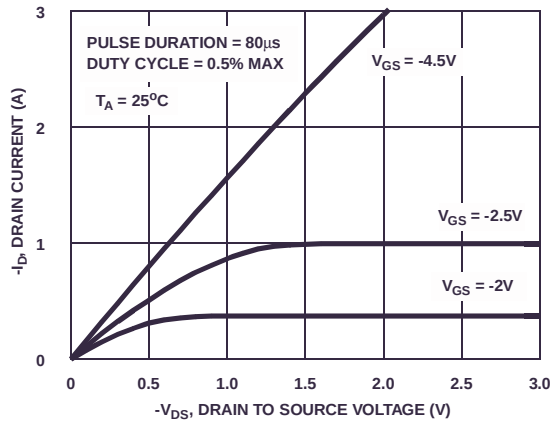


Figure 7. Saturation Characteristics

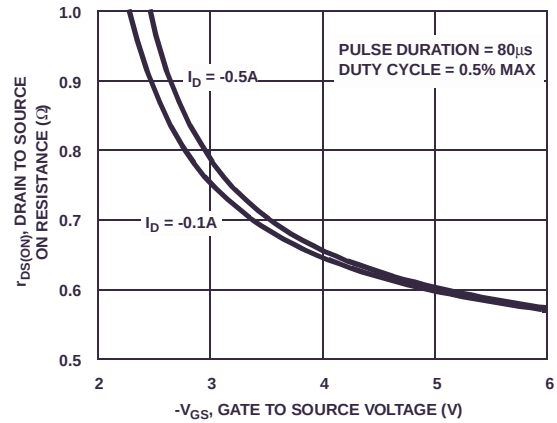


Figure 8. Drain to Source On Resistance vs Gate Voltage and Drain Current

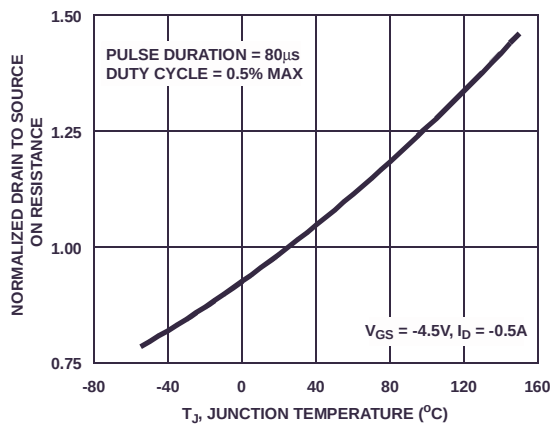


Figure 9. Normalized Drain to Source On Resistance vs Junction Temperature

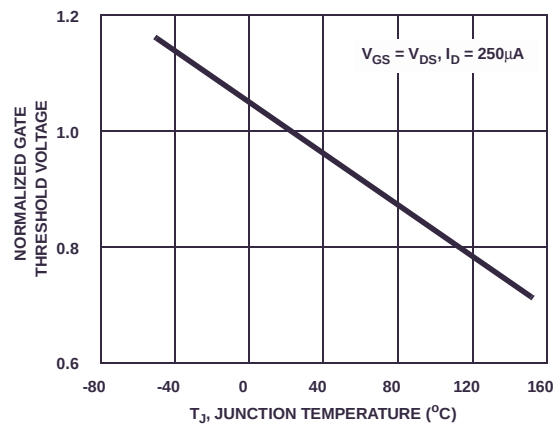


Figure 10. Normalized Gate Threshold Voltage vs Junction Temperature

Typical Characteristic (Continued) $T_A = 25^\circ\text{C}$ unless otherwise noted

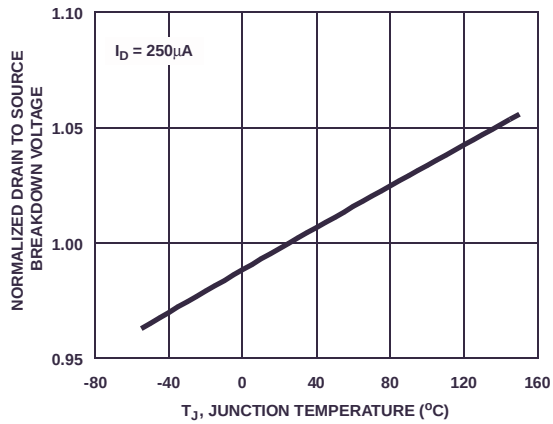


Figure 11. Normalized Drain to Source Breakdown Voltage vs Junction Temperature

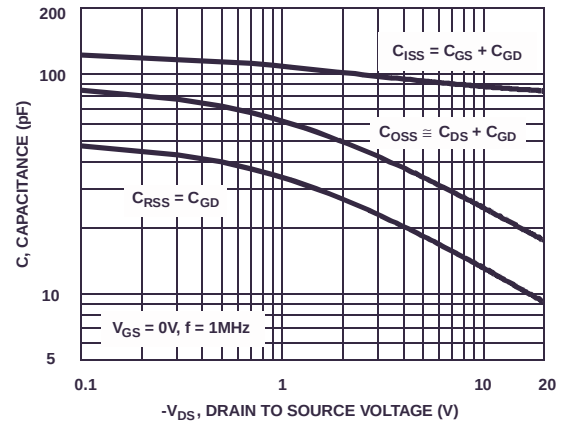


Figure 12. Capacitance vs Drain to Source Voltage

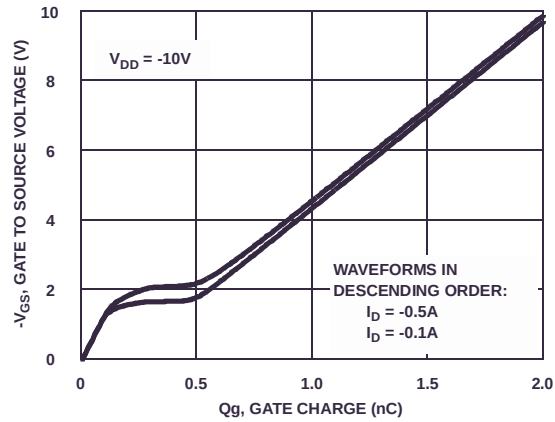


Figure 13. Gate Charge Waveforms for Constant Gate Currents

PSPICE Electrical Model

.SUBCKT FDG6318PZ 2 1 3; rev January 2003

CA 12 8 0.6e-10

CB 15 14 1.1e-10

CIN 6 8 0.75e-10

DBODY 5 7 DBODYMOD

DBREAK 7 11 DBREAKMOD

DPLCAP 10 6 DPLCAPMOD

EBREAK 5 11 17 18 -23.3

EDS 14 8 5 8 1

EGS 13 8 6 8 1

ESG 5 10 8 6 1

EVTHRES 6 21 19 8 1

EVTEMP 6 20 18 22 1

IT 8 17 1

LDRAIN 2 5 1e-9

LGATE 1 9 0.47e-9

LSOURCE 3 7 0.47e-9

MMED 16 6 8 8 MMEDMOD

MSTRO 16 6 8 8 MSTROMOD

MWEAK 16 21 8 8 MWEAKMOD

RBREAK 17 18 RBREAKMOD 1

RDRAIN 50 16 RDRAINMOD 280e-3

RGATE 9 20 12.4

RLDRAIN 2 5 10

RLGATE 1 9 4.7

RLSOURCE 3 7 4.7

RSLC1 5 51 RSLCMOD 1e-6

RSLC2 5 50 1e3

RSOURCE 8 7 RSOURCEMOD 190e-3

RVTHRES 22 8 RVTHRESMOD 1

RVTEMP 18 19 RVTEMPMOD 1

S1A 6 12 13 8 S1AMOD

S1B 13 12 13 8 S1BMOD

S2A 6 15 14 13 S2AMOD

S2B 13 15 14 13 S2BMOD

VBAT 22 19 DC 1

ESLC 51 50 VALUE={ (V(5,51)/ABS(V(5,51))) * (PWR(V(5,51)/(1e-6*20), 2.5)) }

.MODEL DBODYMOD D (IS = 7.7e-11 N=1.277 RS = 1e-3 TRS1 = 2.8e-1 TRS2 = 3e-4 XTI=0 IKF=0.5 CJO = 3.9e-11 TT=33e-9 M = 0.50)

.MODEL DBREAKMOD D (RS = 5.3e-1 TRS1 = 5.5e-3 TRS2 = -9e-5)

.MODEL DPLCAPMOD D (CJO = 0.5e-10 IS = 1e-30 N = 10 M = 0.55)

.MODEL MMEDMOD PMOS (VTO = -1.17 KP = 0.6 IS=1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 12.4)

.MODEL MSTROMOD PMOS (VTO = -1.45 KP = 1.5 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u)

.MODEL MWEAKMOD PMOS (VTO = -0.99 KP = 0.05 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 124 RS = 0.1)

.MODEL RBREAKMOD RES (TC1 = 5.5e-4 TC2 = -1e-7)

.MODEL RDRAINMOD RES (TC1 = 2.8e-3 TC2 = 4.9e-6)

.MODEL RSLCMOD RES (TC1 = 3.7e-3 TC2 = 7.8e-6)

.MODEL RSOURCEMOD RES (TC1 = 3e-3 TC2 = 5.2e-6)

.MODEL RVTHRESMOD RES (TC1 = 9e-4 TC2 = 3e-7)

.MODEL RVTEMPMOD RES (TC1 = -5.5e-4 TC2 = -1e-9)

.MODEL S1AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 0.5 VOFF= 0.2)

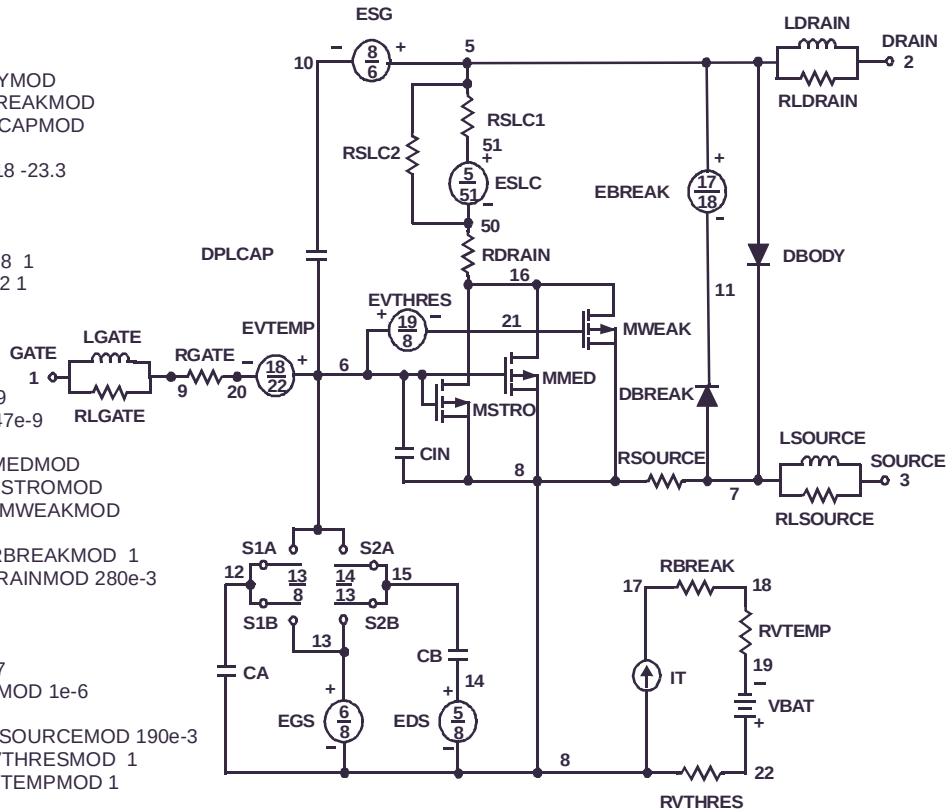
.MODEL S1BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 0.2 VOFF= 0.5)

.MODEL S2AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 0.4 VOFF= -0.1)

.MODEL S2BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -0.1 VOFF= 0.4)

.ENDS

Note: For further discussion of the PSPICE model, consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records, 1991, written by William J. Hepp and C. Frank Wheatley.



SABER Electrical Model

REV January 2003

template fdg6318pz n2,n1,n3

electrical n2,n1,n3

```

{
var i iscl
dp..model dbodymod = (isl = 7.7e-11, nl=1.277, rs = 1e-3, trs1 = 2.8e-1, trs2 = 3e-4, xti=0, cjo = 3.9e-11, ikf=0.5, tt = 33e-9, m = 0.50)
dp..model dbreakmod = (rs = 5.3e-1, trs1 = 5.5e-3, trs2 = -9.0e-5)
dp..model dplcapmod = (cjo = 0.5e-10, isl=10e-30, nl=10, m=0.55)
m..model mmedmod = (type=_p, vto = -1.17, kp=0.6, is=1e-30, tox=1)
m..model mstrongmod = (type=_p, vto = -1.45, kp = 1.5, is = 1e-30, tox = 1)
m..model mweakmod = (type=_p, vto = -0.99, kp = 0.05, is = 1e-30, tox = 1, rs=0.1)
sw_vcsp..model s1amod = (ron = 1e-5, roff = 0.1, von = 0.5, voff = 0.2)
sw_vcsp..model s1bmod = (ron = 1e-5, roff = 0.1, von = 0.2, voff = 0.5)
sw_vcsp..model s2amod = (ron = 1e-5, roff = 0.1, von = 0.4, voff = -0.1)
sw_vcsp..model s2bmod = (ron = 1e-5, roff = 0.1, von = -0.1, voff = 0.4)

```

```

c.ca n12 n8 = 0.6e-10
c.cb n15 n14 = 1.1e-10
c.cin n6 n8 = 0.75e-10

```

```

dp.dbody n5 n7 = model=dbodymod
dp.dbreak n7 n11 = model=dbreakmod
dp.dplcap n10 n6 = model=dplcapmod

```

```

i.it n8 n17 = 1

```

```

l.l drain n2 n5 = 1e-9
l.l gate n1 n9 = 0.47e-9
l.l source n3 n7 = 0.47e-9

```

```

m.mmed n16 n6 n8 n8 = model=mmedmod, l=1u, w=1u
m.mstrong n16 n6 n8 n8 = model=mstrongmod, l=1u, w=1u
m.mweak n16 n21 n8 n8 = model=mweakmod, l=1u, w=1u

```

```

res.rbreak n17 n18 = 1, tc1 = 5.5e-4, tc2 = -1e-7
res.rdrain n50 n16 = 280e-3, tc1 = 2.8e-3, tc2 = 4.9e-6
res.rgate n9 n20 = 12.4
res.rldrain n2 n5 = 10
res.rlgate n1 n9 = 4.7
res.rlsource n3 n7 = 4.7
res.rslc1 n5 n51 = 1e-6, tc1 = 3.7e-3, tc2 = 7.8e-6
res.rslc2 n5 n50 = 1e3
res.rsource n8 n7 = 190e-3, tc1 = 3e-3, tc2 = 5.2e-6
res.rvtemp n18 n19 = 1, tc1 = -5.5e-4, tc2 = -1e-9
res.rvthres n22 n8 = 1, tc1 = 9e-4, tc2 = 3e-7

```

```

spe.ebreak n5 n11 n17 n18 = -23.3
spe.eds n14 n8 n5 n8 = 1
spe.egs n13 n8 n6 n8 = 1
spe.esg n5 n10 n6 n8 = 1
spe.evtemp n20 n6 n18 n22 = 1
spe.evthres n6 n21 n19 n8 = 1

```

```

sw_vcsp.s1a n6 n12 n13 n8 = model=s1amod
sw_vcsp.s1b n13 n12 n13 n8 = model=s1bmod
sw_vcsp.s2a n6 n15 n14 n13 = model=s2amod
sw_vcsp.s2b n13 n15 n14 n13 = model=s2bmod

```

```

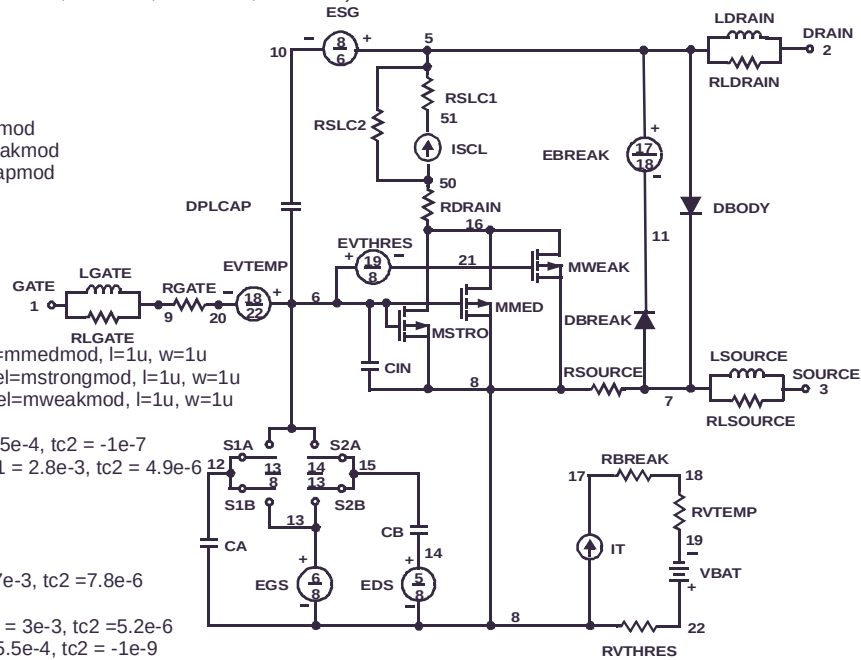
v.vbat n22 n19 = dc=1

```

```

equations {
i (n51->n50) += iscl
iscl: v(n51,n50) = (((v(n5,n51))/(1e-9+abs(v(n5,n51)))))*((abs(v(n5,n51)*1e6/20))** 2.5))
}
}

```



SPICE Thermal Model

REV January 2003
 FDG6318PZ_JA Junction Ambient
 Copper Area= 1sq.in

CTHERM1 Junction c2 0.17e-4
 CTHERM2 c2 c3 2.7e-4
 CTHERM3 c3 c4 5.5e-4
 CTHERM4 c4 c5 1.4e-3
 CTHERM5 c5 c6 2.2e-3
 CTHERM6 c6 c7 2.6e-3
 CTHERM7 c7 c8 6.6e-3
 CTHERM8 c8 Ambient 0.29

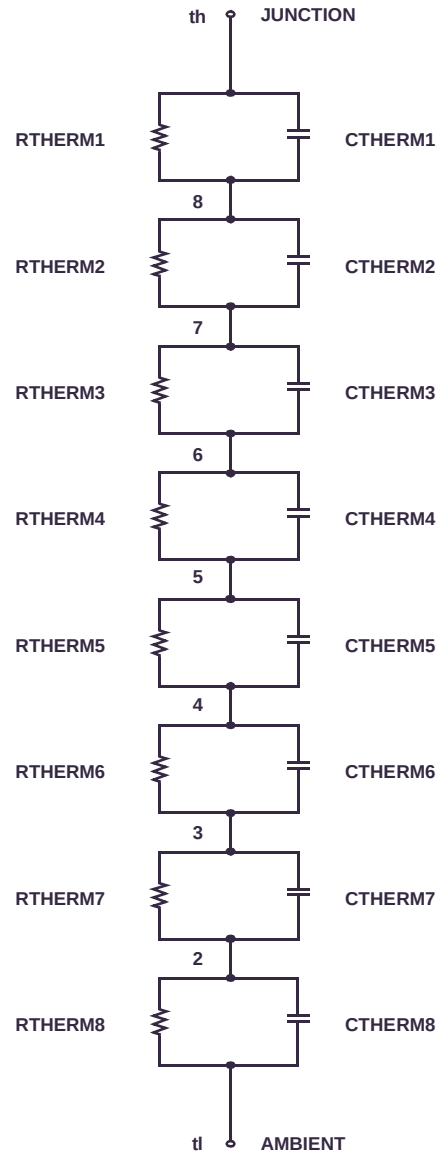
RTHERM1 Junction c2 11.2
 RTHERM2 c2 c3 11.5
 RTHERM3 c3 c4 12.5
 RTHERM4 c4 c5 27
 RTHERM5 c5 c6 81
 RTHERM6 c6 c7 88
 RTHERM7 c7 c8 92
 RTHERM8 c8 Ambient 93

SABER Thermal Model

SABER thermal model FDG6318PZ
 Copper Area= 1sq.in
 template thermal_model th tl
 thermal_c th, tl

```
{
  ctherm.ctherm1 th c2 = 0.17e-4
  ctherm.ctherm2 c2 c3 = 2.7e-4
  ctherm.ctherm3 c3 c4 = 5.5e-4
  ctherm.ctherm4 c4 c5 = 1.4e-3
  ctherm.ctherm5 c5 c6 = 2.2e-3
  ctherm.ctherm6 c6 c7 = 2.6e-3
  ctherm.ctherm7 c7 c8 = 6.6e-3
  ctherm.ctherm8 c8 tl = 0.29
```

```
rtherm.rtherm1 th c2 = 11.2
rtherm.rtherm2 c2 c3 = 11.5
rtherm.rtherm3 c3 c4 = 12.5
rtherm.rtherm4 c4 c5 = 27
rtherm.rtherm5 c5 c6 = 81
rtherm.rtherm6 c6 c7 = 88
rtherm.rtherm7 c7 c8 = 92
rtherm.rtherm8 c8 tl = 93
}
```



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Bottomless™	FAST®	LittleFET™	Power247™	SuperSOT™-3
CoolFET™	FAST _r ™	MicroFET™	PowerTrench®	SuperSOT™-6
CROSSVOLT™	FRFET™	MicroPak™	QFET™	SuperSOT™-8
DOVE™	GlobalOptoisolator™	MICROWIRE™	QS™	SyncFET™
EcoSPARK™	GTO™	MSX™	QT Optoelectronics™	TinyLogic®
E ² CMOS™	HiSeC™	MSXPro™	Quiet Series™	TruTranslation™
EnSigna™	I ² C™	OCX™	RapidConfigure™	UHC™
Across the board. Around the world.™		OCXPro™	RapidConnect™	UltraFET®
The Power Franchise™		OPTOLOGIC®	SILENT SWITCHER®	VCX™
Programmable Active Droop™		OPTOPLANAR™	SMART START™	

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
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