

## N-Channel Power MOSFET

150V, 9A, 65mΩ

### FEATURES

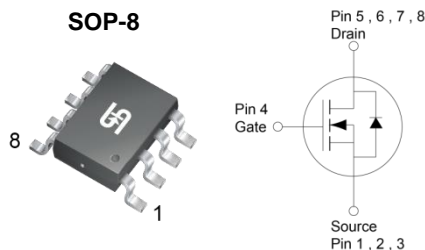
- Low  $R_{DS(ON)}$  to minimize conductive losses
- Low gate charge for fast power switching
- 100% UIS and  $R_g$  tested
- Compliant to RoHS directive 2011/65/EU and in accordance to WEEE 2002/96/EC
- Halogen-free according to IEC 61249-2-21

### KEY PERFORMANCE PARAMETERS

PARAMETER	VALUE	UNIT
$V_{DS}$	150	V
$R_{DS(on)}$ (max)	$V_{GS} = 10V$	65
	$V_{GS} = 6V$	80
$Q_g$	37	nC

### APPLICATIONS

- PoE
- LED Lighting
- Telecom Power



**Note:** MSL 3 (Moisture Sensitivity Level) per J-STD-020

### ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	$V_{DS}$	150	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Continuous Drain Current <sup>(Note 1)</sup>	$I_D$	$T_C = 25^\circ\text{C}$	9
		$T_A = 25^\circ\text{C}$	4
Pulsed Drain Current	$I_{DM}$	36	A
Single Pulse Avalanche Current <sup>(Note 2)</sup>	$I_{AS}$	20	A
Single Pulse Avalanche Energy <sup>(Note 2)</sup>	$E_{AS}$	60	mJ
Total Power Dissipation	$P_D$	$T_C = 25^\circ\text{C}$	12.5
		$T_C = 125^\circ\text{C}$	2.5
Total Power Dissipation	$P_D$	$T_A = 25^\circ\text{C}$	2.2
		$T_A = 125^\circ\text{C}$	0.4
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	- 55 to +150	$^\circ\text{C}$

### THERMAL PERFORMANCE

PARAMETER	SYMBOL	LIMIT	UNIT
Junction to Case Thermal Resistance	$R_{\theta JC}$	10	$^\circ\text{C/W}$
Junction to Ambient Thermal Resistance	$R_{\theta JA}$	57	$^\circ\text{C/W}$

**Thermal Performance Note:**  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistances. The case-thermal reference is defined at the solder mounting surface of the drain pins.  $R_{\theta JA}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.

**ELECTRICAL SPECIFICATIONS** ( $T_A = 25^\circ\text{C}$  unless otherwise noted)

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNIT
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250\mu A$	$BV_{DSS}$	150	--	--	V
Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\mu A$	$V_{GS(TH)}$	2	2.7	4	V
Gate-Source Leakage Current	$V_{GS} = \pm 20V, V_{DS} = 0V$	$I_{GSS}$	--	--	$\pm 100$	nA
Drain-Source Leakage Current	$V_{GS} = 0V, V_{DS} = 150V$	$I_{DSS}$	--	--	1	$\mu A$
	$V_{GS} = 0V, V_{DS} = 150V$ $T_J = 125^\circ\text{C}$		--	--	100	
Drain-Source On-State Resistance (Note 3)	$V_{GS} = 10V, I_D = 4A$	$R_{DS(on)}$	--	51	65	m $\Omega$
	$V_{GS} = 6V, I_D = 4A$		--	59	80	
Forward Transconductance (Note 3)	$V_{DS} = 5V, I_D = 4A$	$g_{fs}$	--	11	--	S
<b>Dynamic</b> (Note 4)						
Total Gate Charge	$V_{GS} = 10V, V_{DS} = 75V,$ $I_D = 4A$	$Q_g$	--	37	--	nC
Total Gate Charge	$V_{GS} = 6V, V_{DS} = 75V,$ $I_D = 4A$	$Q_g$	--	24	--	
Gate-Source Charge		$Q_{gs}$	--	9	--	
Gate-Drain Charge		$Q_{gd}$	--	12	--	
Input Capacitance	$V_{GS} = 0V, V_{DS} = 75V$ $f = 1.0\text{MHz}$	$C_{iss}$	--	1783	--	pF
Output Capacitance		$C_{oss}$	--	94	--	
Reverse Transfer Capacitance		$C_{rss}$	--	18	--	
Gate Resistance	$f = 1.0\text{MHz}, \text{open drain}$	$R_g$	0.4	1.3	2.6	$\Omega$
<b>Switching</b> (Note 4)						
Turn-On Delay Time	$V_{GS} = 10V, V_{DS} = 75V,$ $I_D = 4A, R_G = 2\Omega,$	$t_{d(on)}$	--	7	--	ns
Turn-On Rise Time		$t_r$	--	5	--	
Turn-Off Delay Time		$t_{d(off)}$	--	17	--	
Turn-Off Fall Time		$t_f$	--	11	--	
<b>Source-Drain Diode</b>						
Forward Voltage (Note 3)	$V_{GS} = 0V, I_S = 4A$	$V_{SD}$	--	--	1	V
Reverse Recovery Time	$I_S = 4A,$ $di/dt = 100A/\mu s$	$t_{rr}$	--	50	--	ns
Reverse Recovery Charge		$Q_{rr}$	--	97	--	nC

**Notes:**

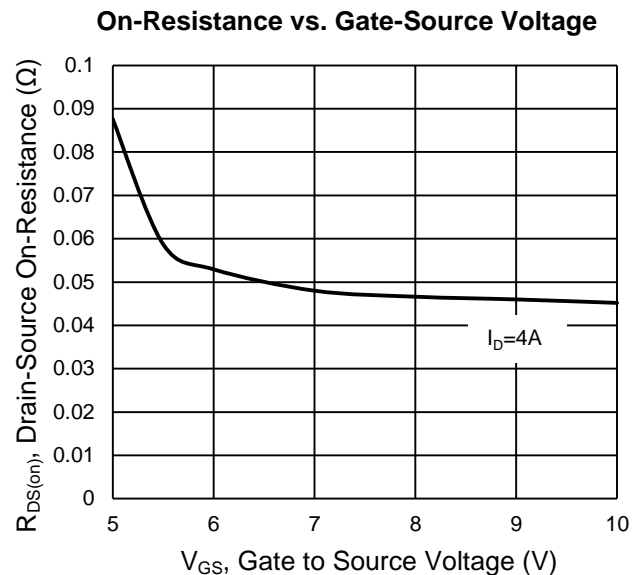
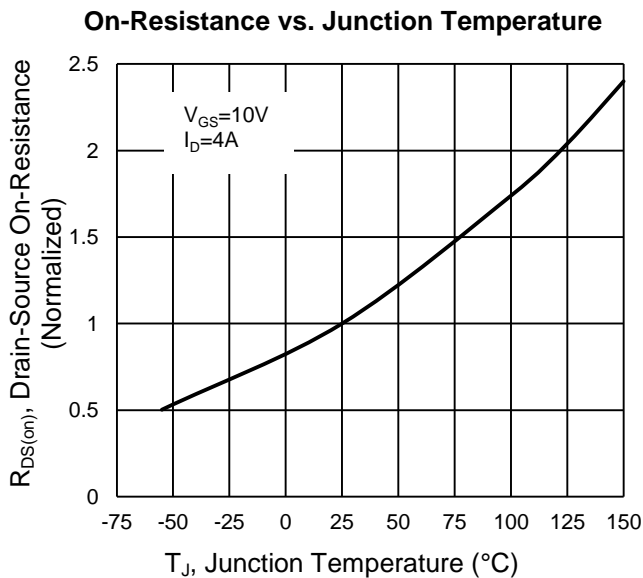
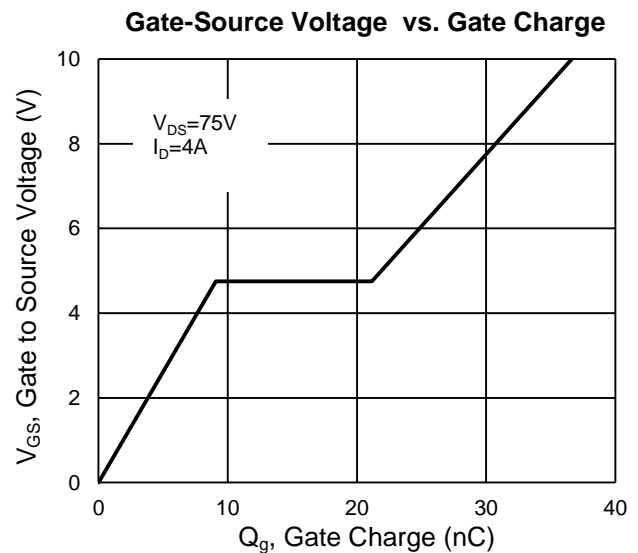
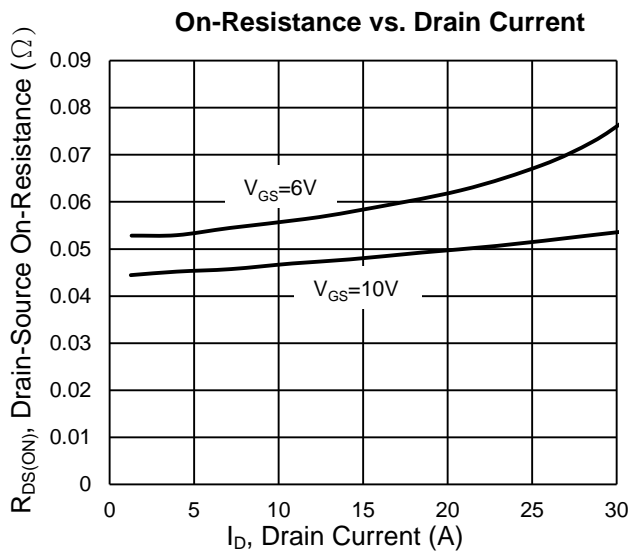
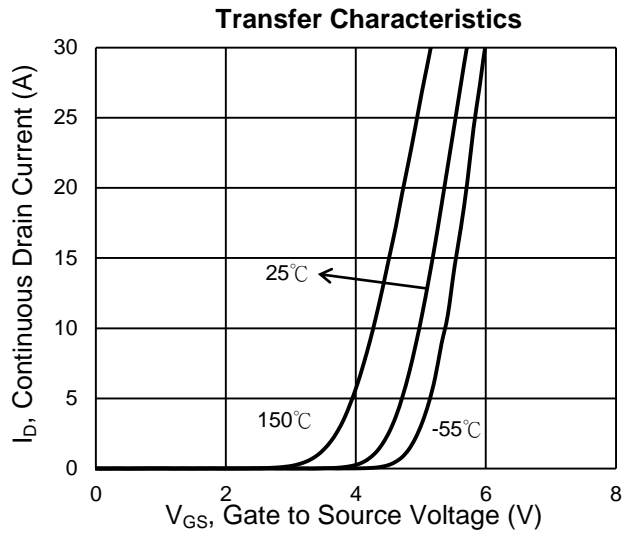
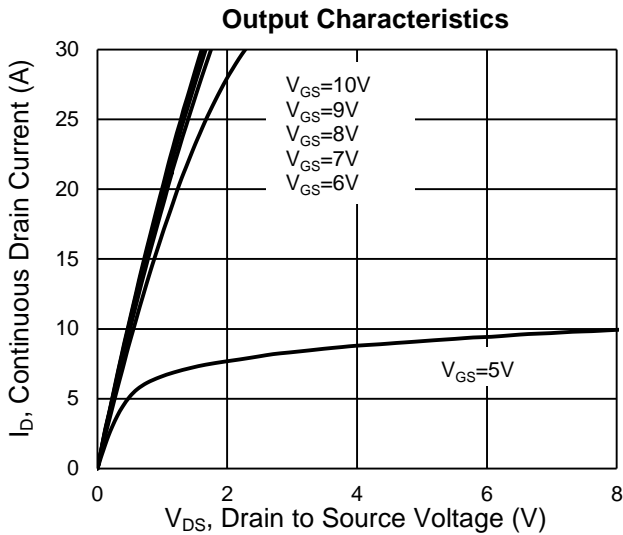
- Silicon limited current only.
- $L = 0.3\text{mH}, V_{GS} = 10V, V_{DD} = 50V, R_G = 25\Omega, I_{AS} = 18A,$  Starting  $T_J = 25^\circ\text{C}$
- Pulse test: Pulse Width  $\leq 300\mu s,$  duty cycle  $\leq 2\%$ .
- Switching time is essentially independent of operating temperature.

**ORDERING INFORMATION**

PART NO.	PACKAGE	PACKING
TSM650N15CS RLG	SOP-8	2,500pcs / 13" Reel

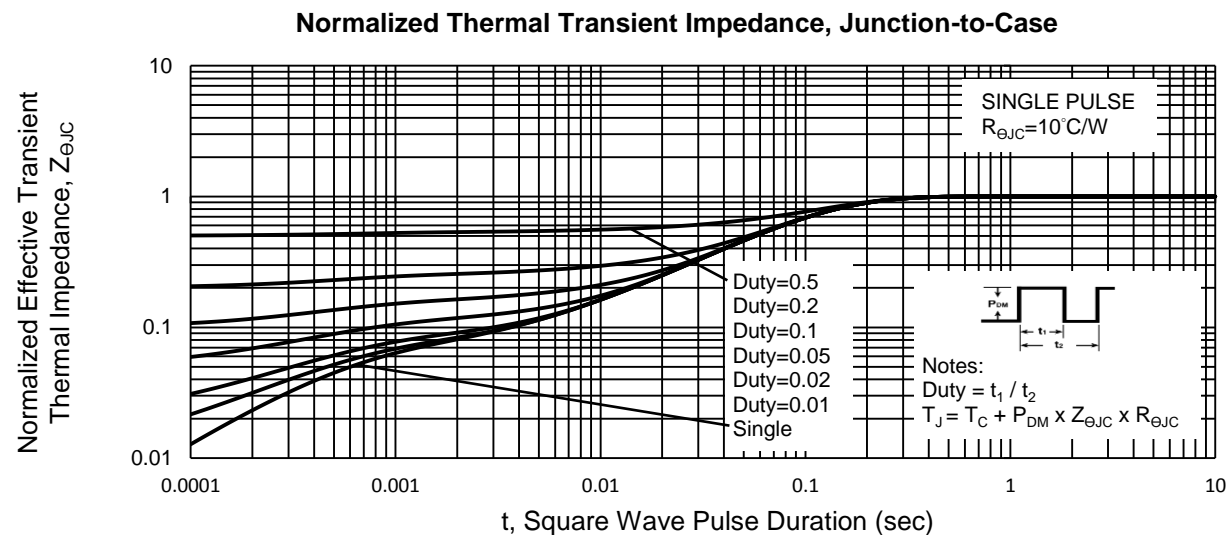
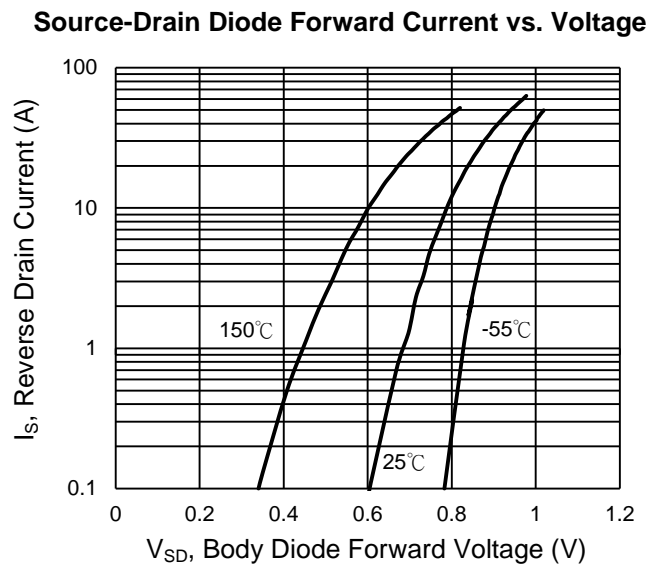
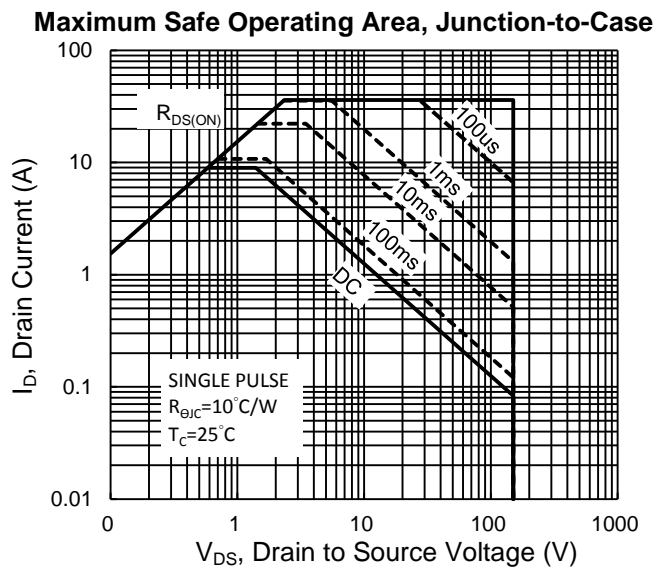
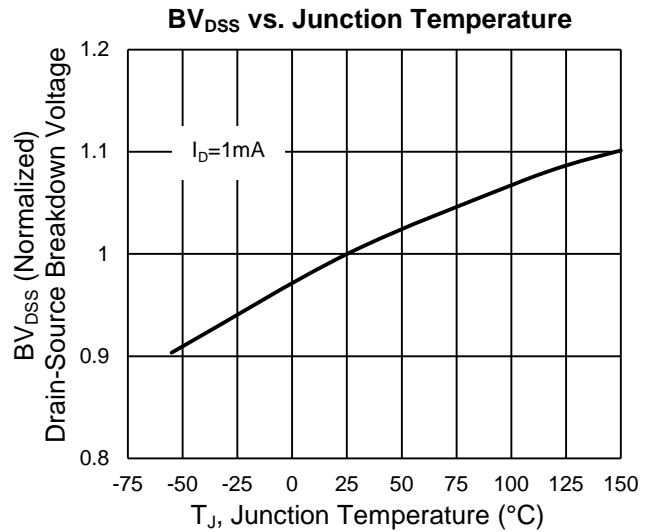
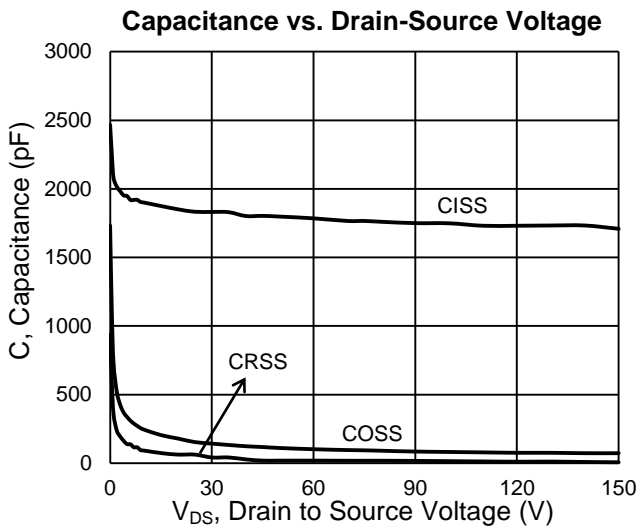
**CHARACTERISTICS CURVES**

( $T_A = 25^\circ\text{C}$  unless otherwise noted)



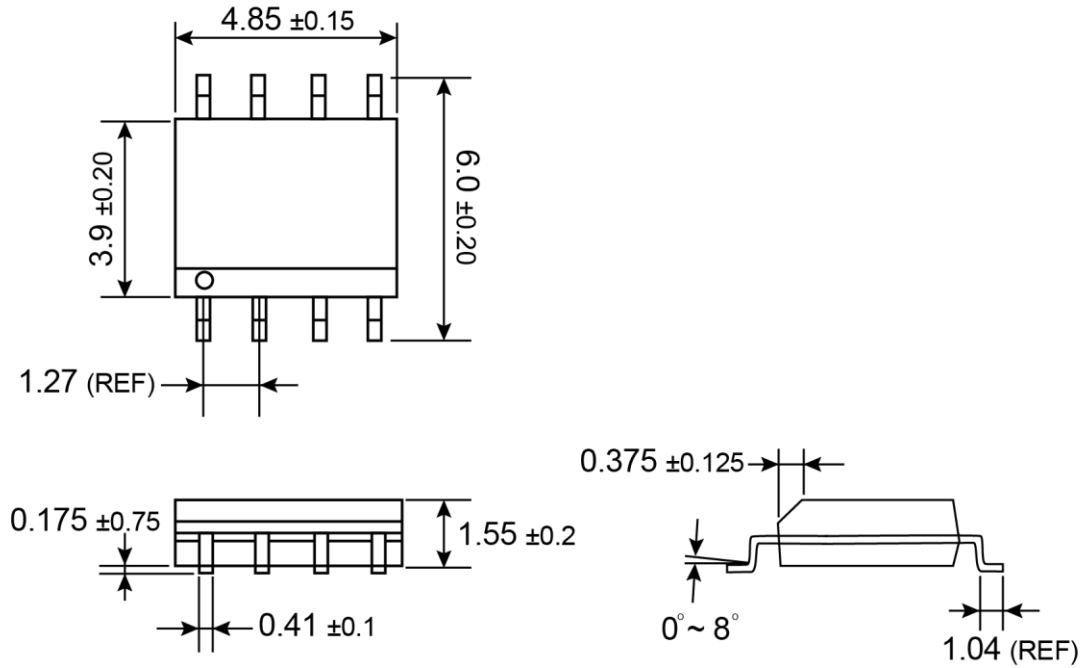
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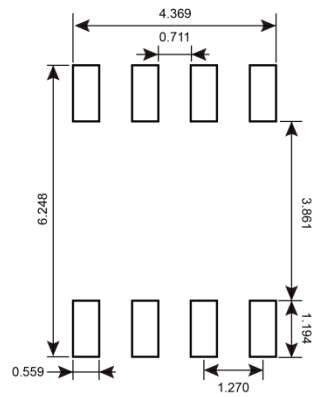


**PACKAGE OUTLINE DIMENSIONS** (Unit: Millimeters)

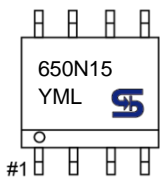
**SOP-8**



**SUGGESTED PAD LAYOUT** (Unit: Millimeters)



**MARKING DIAGRAM**



- Y = Year Code
- M = Month Code
- O =Jan    P =Feb    Q =Mar    R =Apr
- S =May    T =Jun    U =Jul    V =Aug
- W =Sep    X =Oct    Y =Nov    Z =Dec
- L = Lot Code (1~9, A~Z)

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