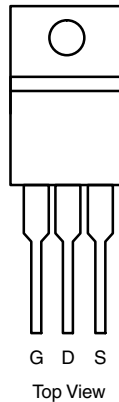


N-Channel 30 V (D-S) MOSFET

PRODUCT SUMMARY

V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)	Q_g (Typ.)
30	0.0051 at $V_{GS} = 10$ V	50 ^d	21.7
	0.0063 at $V_{GS} = 4.5$ V	50 ^d	

TO-220AB

Ordering Information:

SUP50N03-5m1P-GE3 (Lead (Pb)-free and Halogen-free)

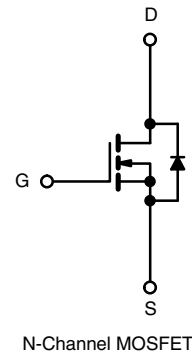
FEATURES

- TrenchFET® Power MOSFET
- 100 % R_g and UIS Tested
- Material categorization:
For definitions of compliance please see www.vishay.com/doc?99912


RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- Power Supply
 - Secondary Synchronous Rectification
- DC/DC Converter



ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current ($T_J = 150$ °C)	I_D	$T_C = 25$ °C 50 ^d	A
		$T_C = 70$ °C 50 ^d	
Pulsed Drain Current	I_{DM}	100	
Avalanche Current	I_{AS}	40	
Single Avalanche Energy ^a	E_{AS}	80	mJ
Maximum Power Dissipation ^a	P_D	$T_C = 25$ °C 59.5 ^b	W
		$T_A = 25$ °C ^c 2.7	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150	°C

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Limit	Unit
Junction-to-Ambient (PCB Mount) ^c	R_{thJA}	46	°C/W
Junction-to-Case (Drain)	R_{thJC}	2.1	

Notes:

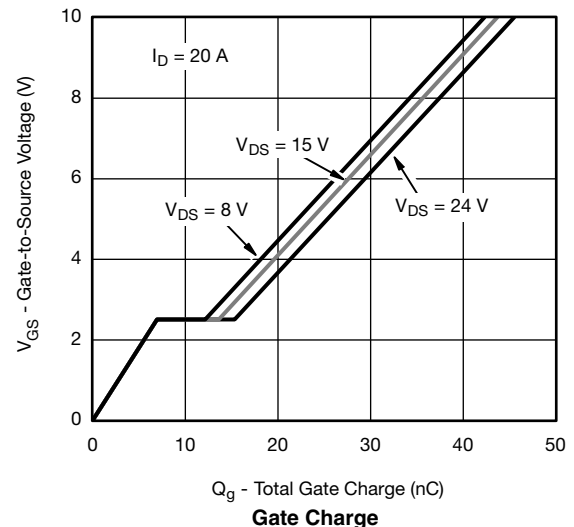
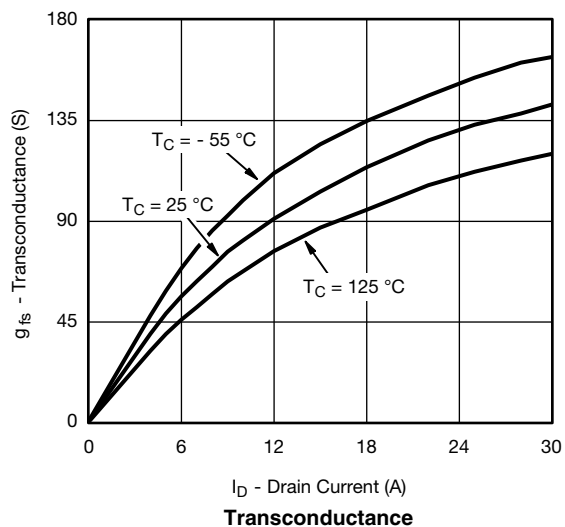
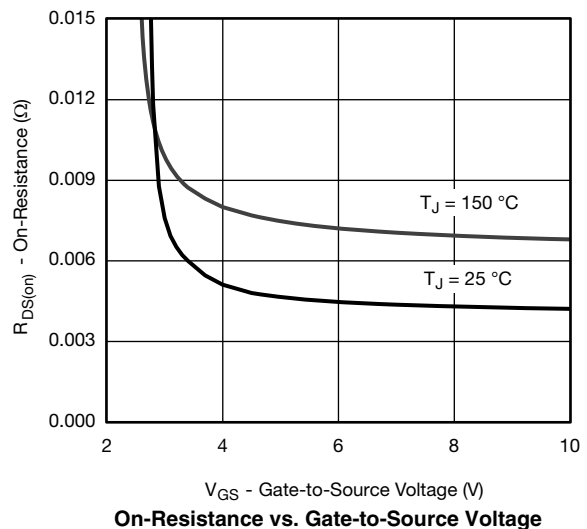
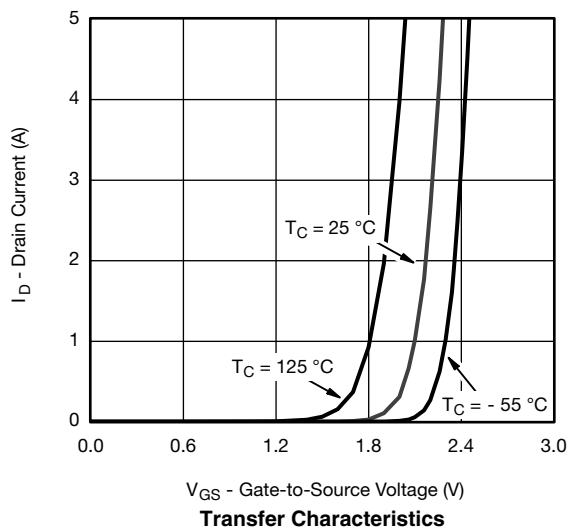
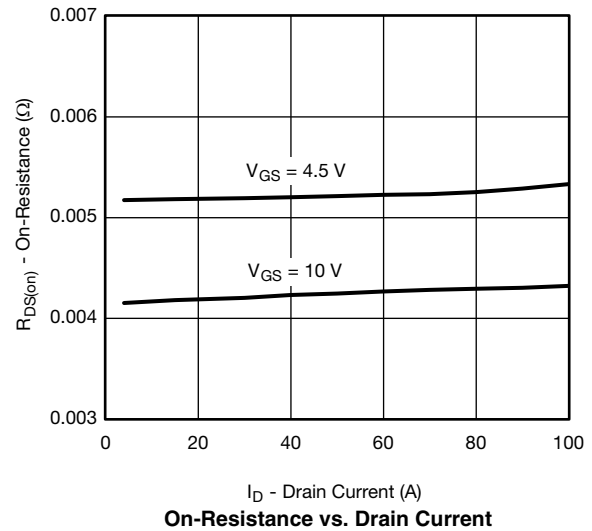
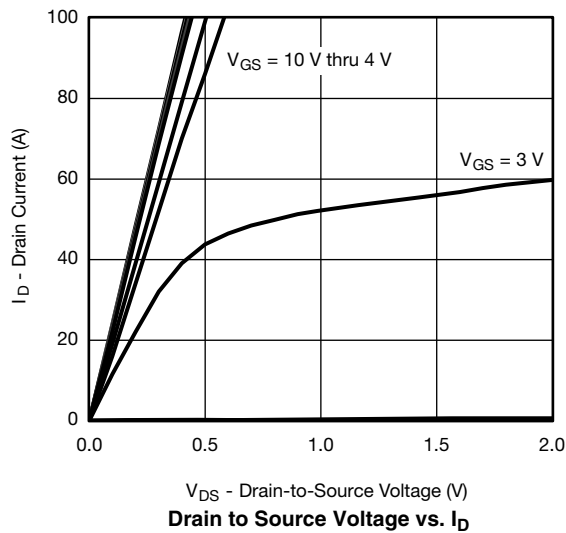
- Duty cycle ≤ 1 %.
- See SOA curve for voltage derating.
- When mounted on 1" square PCB (FR-4 material).
- Package limited.

SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{DS}	V _{DS} = 0 V, I _D = 250 μA	30			V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	1		2.5	
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V			± 250	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 30 V, V _{GS} = 0 V			1	μA
		V _{DS} = 30 V, V _{GS} = 0 V, T _J = 125 °C			50	
		V _{DS} = 30 V, V _{GS} = 0 V, T _J = 150 °C			250	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≥ 10 V, V _{GS} = 10 V	50			A
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = 10 V, I _D = 22 A		0.0042	0.0051	Ω
		V _{GS} = 4.5 V, I _D = 20 A		0.0052	0.0063	
Forward Transconductance ^a	g _{fs}	V _{DS} = 15 V, I _D = 20 A		110		S
Dynamic ^b						
Input Capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = 15 V, f = 1 MHz		2780		pF
Output Capacitance	C _{oss}			641		
Reverse Transfer Capacitance	C _{rss}			260		
Total Gate Charge ^c	Q _g	V _{DS} = 15 V, V _{GS} = 10 V, I _D = 20 A		44	66	nC
		V _{DS} = 15 V, V _{GS} = 4.5 V, I _D = 20 A		21.7	32.6	
Gate-Source Charge ^c	Q _{gs}			7		
Gate-Drain Charge ^c	Q _{gd}			6.7		
Gate Resistance	R _g	f = 1 MHz	0.7	3.5	7	Ω
Turn-On Delay Time ^c	t _{d(on)}	V _{DD} = 15 V, R _L = 1.5 Ω I _D ≅ 10 A, V _{GEN} = 10 V, R _g = 1 Ω		8	16	ns
Rise Time ^c	t _r			9	18	
Turn-Off Delay Time ^c	t _{d(off)}			35	53	
Fall Time ^c	t _f			9	18	
Drain-Source Body Diode Ratings and Characteristics T _C = 25 °C ^b						
Continuous Current	I _S				50	A
Pulsed Current	I _{SM}				100	
Forward Voltage ^a	V _{SD}	I _F = 10 A, V _{GS} = 0 V		0.75	1.5	V
Reverse Recovery Time	t _{rr}	I _F = 10 A, dI/dt = 100 A/μs		34	51	ns
Peak Reverse Recovery Current	I _{RM(REC)}			2	3	A
Reverse Recovery Charge	Q _{rr}			34	51	nC

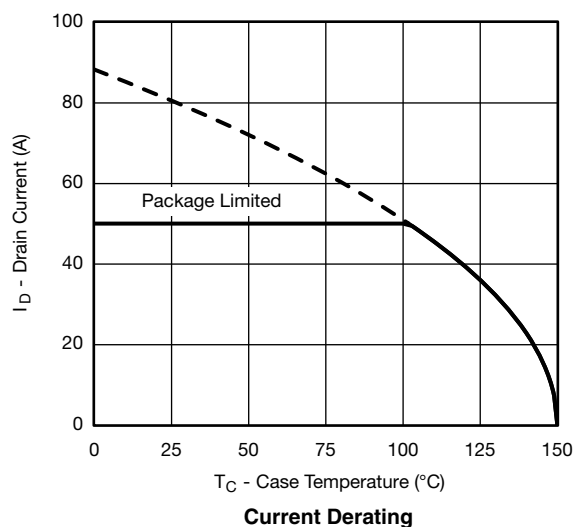
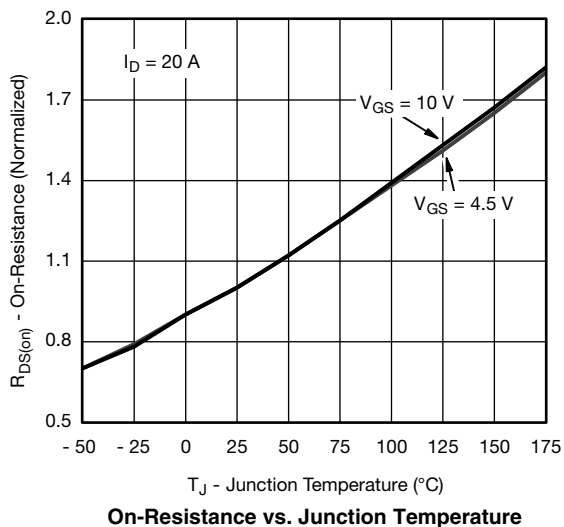
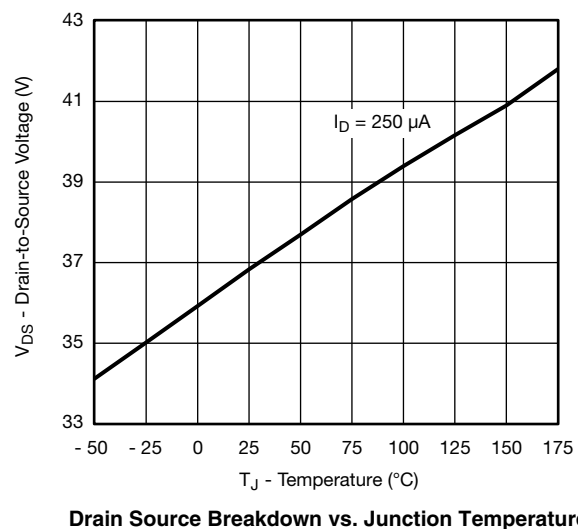
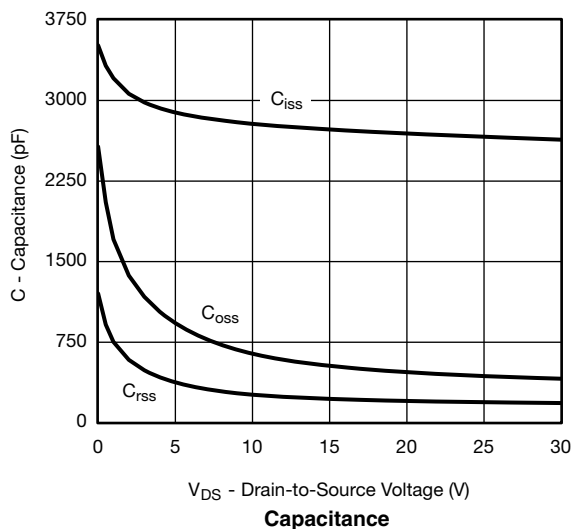
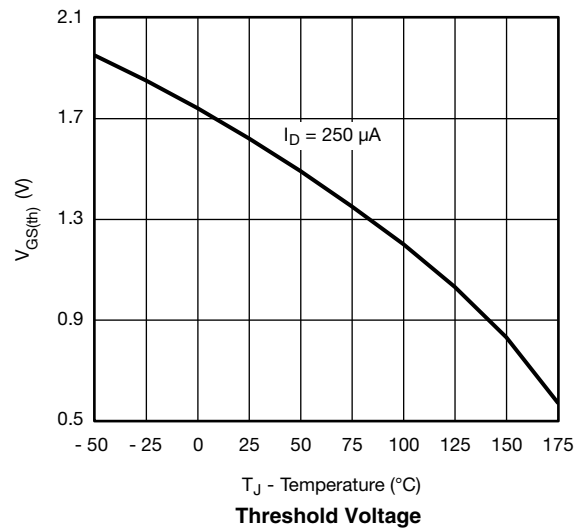
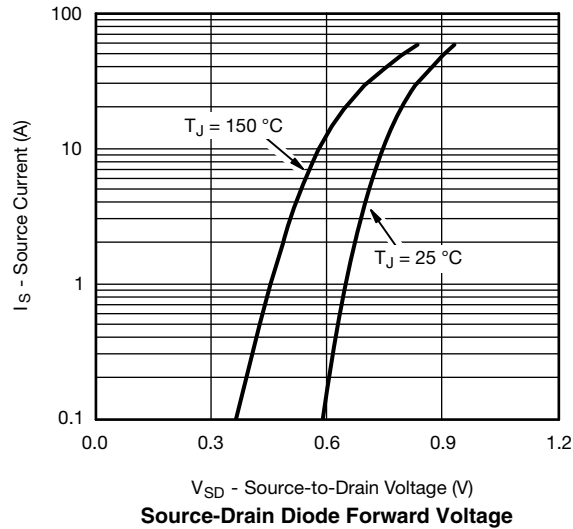
Notes:

- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
b. Guaranteed by design, not subject to production testing.
c. Independent of operating temperature.

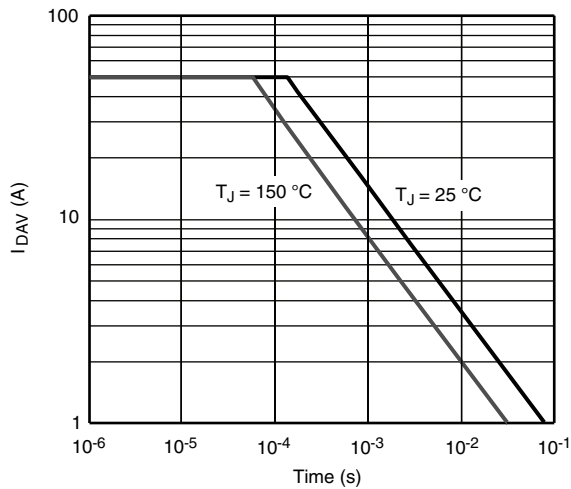
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)


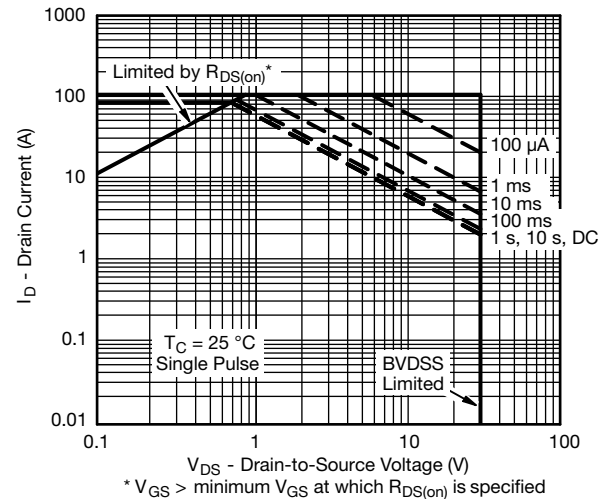
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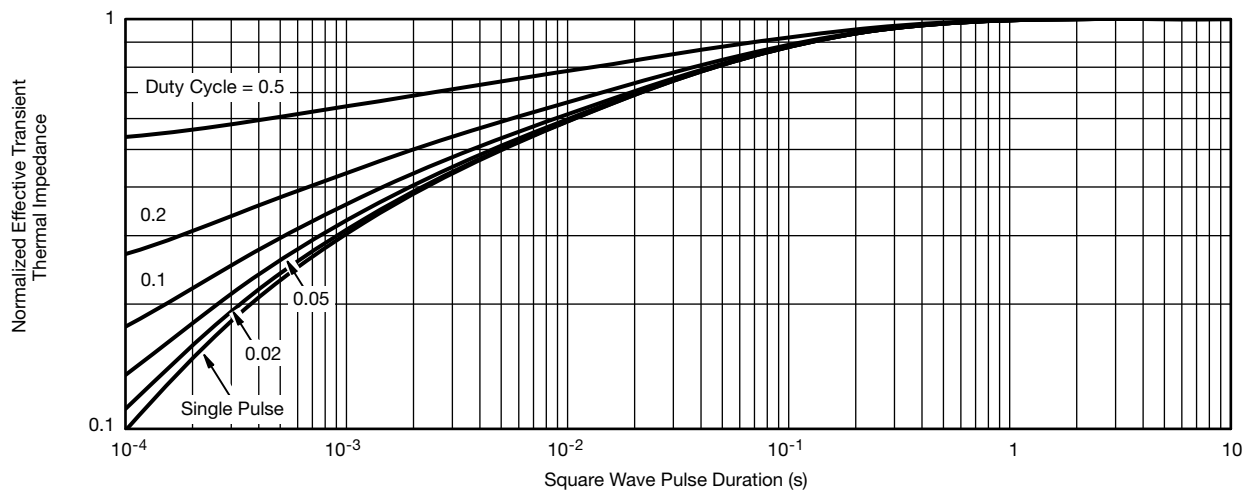


Single Pulse Avalanche Current Capability vs. Time



* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area

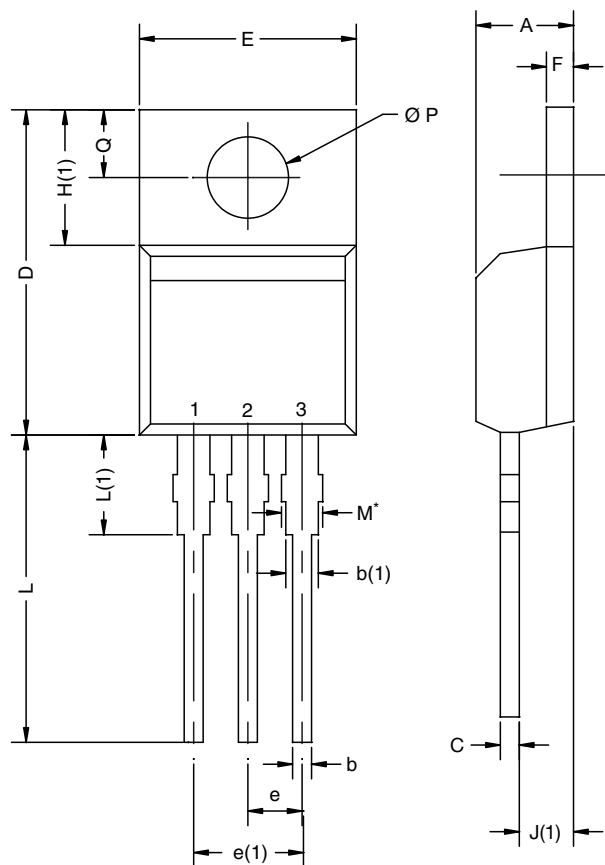


Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?66570.



TO-220AB



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.25	4.65	0.167	0.183
b	0.69	1.01	0.027	0.040
b(1)	1.20	1.73	0.047	0.068
c	0.36	0.61	0.014	0.024
D	14.85	15.49	0.585	0.610
E	10.04	10.51	0.395	0.414
e	2.41	2.67	0.095	0.105
e(1)	4.88	5.28	0.192	0.208
F	1.14	1.40	0.045	0.055
H(1)	6.09	6.48	0.240	0.255
J(1)	2.41	2.92	0.095	0.115
L	13.35	14.02	0.526	0.552
L(1)	3.32	3.82	0.131	0.150
Ø P	3.54	3.94	0.139	0.155
Q	2.60	3.00	0.102	0.118

ECN: T13-0724-Rev. O, 14-Oct-13
DWG: 5471

Note

* M = 1.32 mm to 1.62 mm (dimension including protrusion)
Heatsink hole for HVM



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